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New EMC Design Guidelines for Multilayer Printed Wiring Boards

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Abstract - New board layout design guidelines are presented for multilayer printed wiring boards with surface mount components. These design guidelines differ in many ways from established guidelines that were originally developed for older technology boards.

Summary - Many of the *rules-of-thumb* that have helped circuit board designers to meet electromagnetic compatibility (EMC) requirements in the past are no longer effective. Today's densely populated multi-layer boards are very different from the one or two layer pin-in-hole boards that were the norm ten years ago. VLSI, high-speed logic, programmable components, and surface mount technology have significantly changed electromagnetic compatibility problems and priorities. In many cases, implementing an out-dated EMC design guideline can actually make radiation or susceptibility problems much worse.

This presentation steps through the board layout process while calling attention to good and bad EMC design practices. Each section below describes the layout of a particular type of trace in the order that they should normally be considered.

Return (or ground)

Years ago most crosstalk problems on printed circuit cards were usually due to common impedance coupling. Signal currents dumped into the ground structure by one circuit would raise the potential of the ground and this signal would appear in other circuits that shared the same ground structure. This resulted in the common practice of using one ground plane for digital circuits, another ground plane for analog circuits, and perhaps additional grounds for power or other 'noisy' circuits.

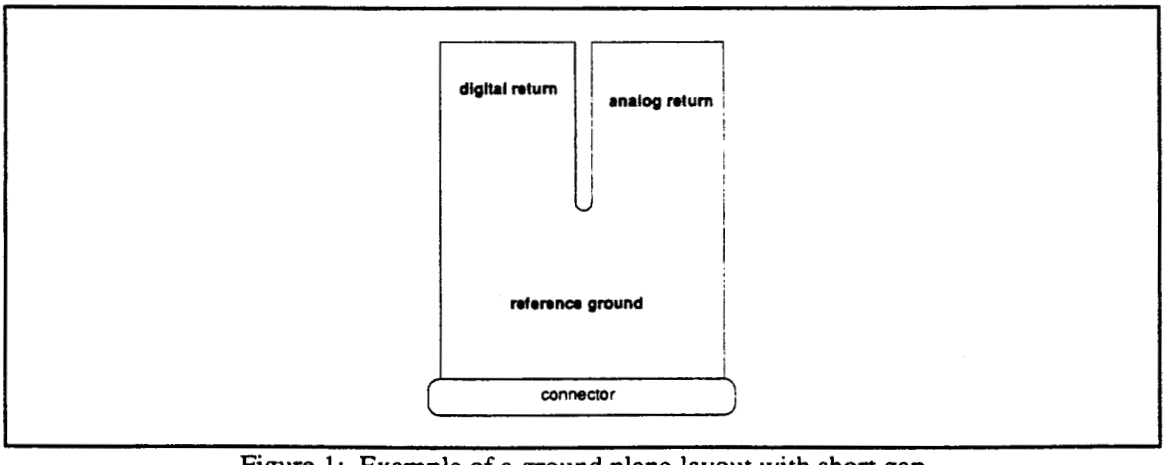

Figure 1: Example of a ground plane layout with short gap

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On today's high-speed multi-layer cards, this is no longer a good practice. Radiated electromagnetic interference and radiated susceptibility have become a significant problem. This problem is much more difficult to deal with when there are different ground planes for different circuits. A better strategy is to have one consistent low-impedance ground for the entire card. It is still possible to place a short narrow gap in the plane to help avoid common impedance crosstalk (see Figure 1), but this gap must be located away from any I/O connectors. A gap must never come between two connectors and care must be taken to ensure that no traces on any other layer cross over the gap.

Power

Cards that use only one voltage should use a power plane that is identical to the return plane. Analog cards that have a matched pair of voltages (e.g. ±12 v) should route these voltages on two layers using identical planes. Cards with both analog and digital circuits should have two power layers. However, rather than assigning one layer to digital power and another to analog, it is much better to keep both analog and digital power on the same layer as illustrated in Figure 2. This approach helps to ensure that components are placed correctly and that there is no overlap of the digital and analog areas. A typical power plane arrangement is illustrated in Figure 3. A/D and D/A converters will straddle the gap between power planes. No trace on any other layer should be routed over a gap between power planes.

I/O traces

Input and output lines are critical because they are attached to the wires that potentially act as the *antenna* to carry electromagnetic energy on or off the card. It is important that all connectors be located toward one side of the card and that all I/O traces are isolated from noisy or susceptible circuits. I/O traces should be routed manually prior to routing any other traces to ensure that they are given the highest priority.

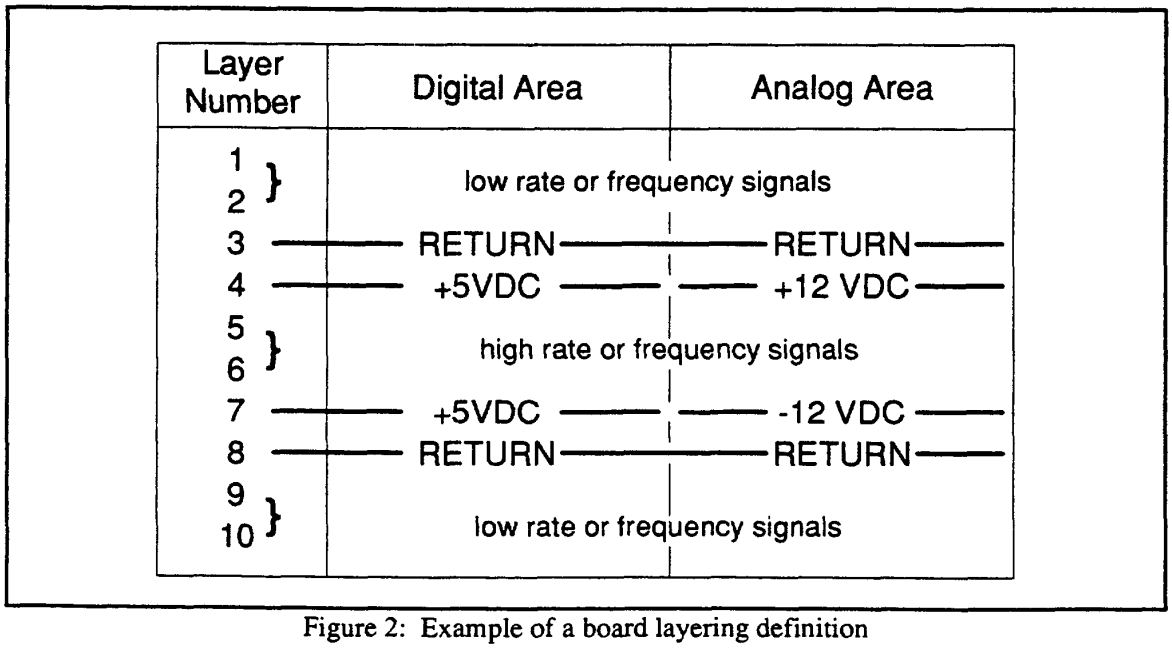

Figure 2: Example of a board layering definition

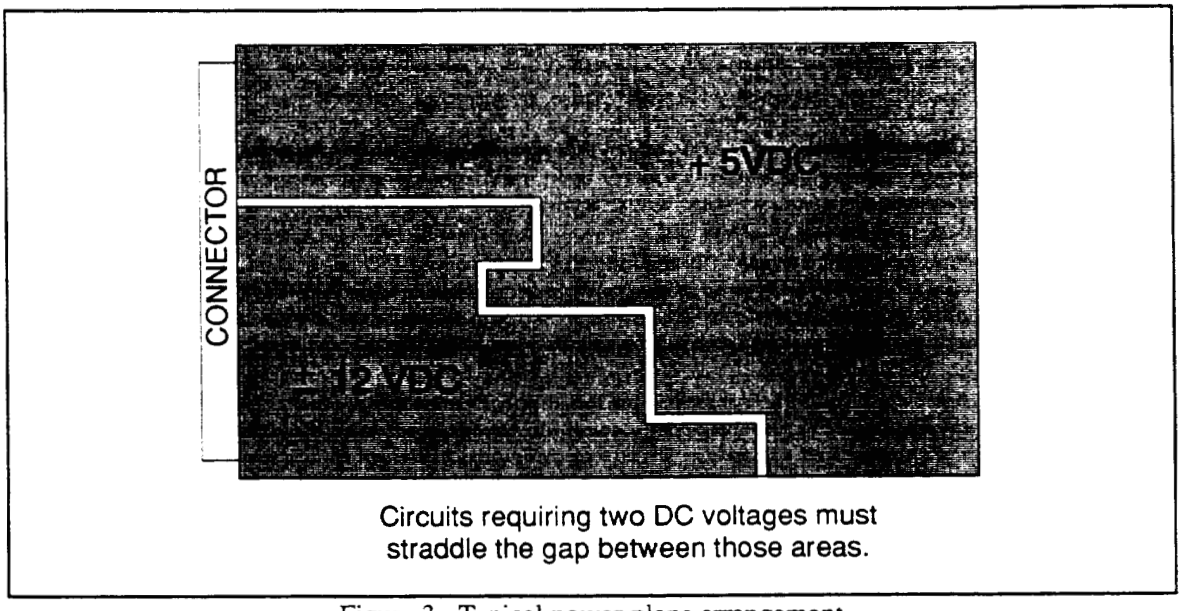

Figure 3: Typical power plane arrangement

Local traces

Very short traces (such as those to a decoupling capacitor) can be routed next to ensure that they stay on a single layer. Old guidelines pertaining to the size and placement of decoupling capacitors must be revised. Newer boards with multiple layers require less decoupling and placement of the capacitors is not as critical as it used to be.

High-Speed traces and Traces for Susceptible Circuits

Critical circuits should be identified and routed manually prior to allowing the autorouter to take over. Contrary to popular belief, it is not usually necessary or desirable to turn corners in 45^{o} increments or even terminate traces in their characteristic impedance. When routing manually, be careful not to make the autorouter's job more difficult by closing off large sections of a layer.

Low-Speed Traces

It is usually best to confine low-speed traces to the outer layers. Routing of low-speed non-susceptible traces is less critical, but balanced signal pairs should still be routed together. The final layout should be thoroughly checked to ensure that the autorouter did not violate any basic EMC design guidelines.