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Reducing Common-Mode Voltage in Three-Phase Sine-Triangle PWM with Interleaved Carriers

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***Abstract*— Interleaving PWM waveforms is a proven method to reduce ripple in dc-dc converters. The present work explores interleaving for three-phase motor drives. Fourier analysis shows that interleaving the carriers in conventional uniform PWM significantly reduces the common-mode voltage. New DSP hardware supports interleaving directly with changes to just two registers at setup time, so no additional computation time is needed during operation. The common-mode voltage reduction ranges from 36% at full modulation to 67% when idling with zero modulation. Third harmonic injection slightly reduces the advantage (to 26% at full modulation). However, the maximum RMS common-mode voltage is still less than 20% of the bus voltage under all conditions. Low-voltage experimental results support the findings.**

I. Introduction

Modern digital signal processors (DSPs), such as a Texas Instruments TMS320F28335, provide new flexibility in pulsewidth modulation (PWM) signal generation. Specifically, different phases of the PWM generator may have its own time base, delayed relative to the others or even at a different frequency. This feature was added to support power topologies such as one of the phase-shift zero-voltage-switching topologies discussed in [1], multi-phase dc-dc converters, or even multiple independent dc-dc converters with different switching frequencies. If motor control is implemented in an FPGA or other programmable device, similar capabilities are possible. The present work will show that interleaving the carriers also provides an advantage in a conventional three-phase motor drive.

Many motor drives use uniformly sampled PWM. All three phases use the same carrier, a triangle wave with frequency f_c. The modulating functions for the three phases, $m_1(t)$, $m_2(t)$, and $m_3(t)$, are sampled at either f_c (symmetric PWM) or $2f_c$ (asymmetric PWM) to determine the duty ratios of each phase. Alternative formulations are based on space vector modulation (SVM) [2]. In SVM, the desired voltage vector is sampled at either f_c or $2f_c$, and then available voltage vectors are chosen to construct the desired voltage vector. There are extra degrees of freedom in the basic formulation of SVM that are used to achieve a variety of goals, including reduced common-mode voltage, in alternative SVM formulations. According to [3], many of these alternatives are impractical, and all of them include some extra computational effort.

Several schemes have been proposed where the PWM frequency is randomized [4, 5] in order to minimize sidebands and harmonics. Such a technique was shown to improve frequency spectrum characteristics of a motor drive at a cost of higher processing overhead. First, the PWM module has to be reconfigured on a cycle-by-cycle basis. Second, the drive control scheme needs to be modified to accommodate the randomness in PWM frequency [4, 5]. Moreover, the theoretical analysis lacks a hard guarantee of signal quality (that is, presence of harmonics in frequency spectrum). In contrast, the proposed scheme has low overhead since the phase shift is set only once using the new ePWM hardware, a mathematical frequency spectrum analysis is presented to guarantee high signal quality, and the motor control algorithm does not need to be modified.

The present work focuses on uniformly sampled sine-triangle PWM, rather than SVM, with interleaved carriers to achieve reduced common-mode voltage. If the carrier waves are interleaved instead of synchronized, the common-mode voltage may be reduced by as much as 67%. This improvement is achieved with a single three-phase inverter, whereas other interleaving techniques [6, 7] require multiple three-phase inverters in parallel. Since the digital hardware is already available, this reduction comes with no extra computational penalty, whereas the SVM variants and random PWM both require significant calculations. The following sections show Fourier analysis and simulations. Two cases are considered, namely, asymmetric uniform PWM with sinusoidal modulation and symmetric uniform PWM with third harmonic injection. Experimental results for a low-voltage inverter agree well with the conclusions.

II. Fourier Analysis of Asymmetric Uniform PWM

The common approach to PWM harmonic analysis is two-dimensional Fourier analysis [8-13]. In conventional Fourier analysis, a periodic function $F(t)$ is decomposed into frequency components by integrating the product of $F(t)$ and complex exponentials. The difficulty with PWM is

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formulating $F(t)$. In two-dimensional Fourier analysis, the two dimensions map time t into the period of the carrier $\left(x = 2\pi f_c t = \omega_c t\right)$ and the period of the modulating function $\left(y = 2\pi f_o t = \omega_o t\right)$. The conventional integral is replaced by a double integral over the two dimensions to find coefficients for a Fourier representation of the general form

$$F(t) = \frac{A_{00}}{2} + \sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\begin{pmatrix} A_{mn}\cos\left(m\omega_c t + n\omega_o t\right) \\ +B_{mn}\sin\left(m\omega_c t + n\omega_o t\right)\end{pmatrix} \tag{1}$$

where A_{mn}, B_{mn} are amplitudes of harmonics m (of the switching frequency) and n (of the modulating frequency). The sine component can be canceled (B_{mn}=0 for all values of m, n) by choosing proper angle references. Also, some special conditions may apply when either m or n equal zero. The advantage of the two-dimensional approach is that $F(t)$ is reduced to a pair of limits of integration, rather than a complicated time-varying square wave.

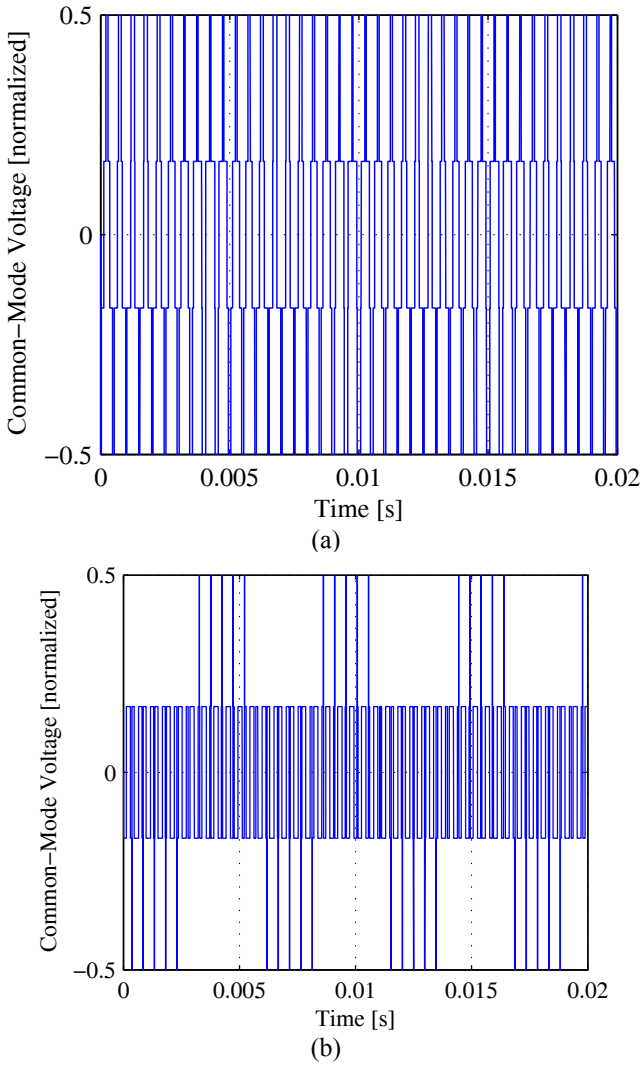

Fig. 1. Simulated common-mode voltage (normalized) for a three-phase inverter, 60 Hz output, 2 kHz switching, modulation depth 0.8: (a) conventional carrier, (b) interleaved carriers.

The present objective is to determine the common-mode voltage $V_0(t)$ when the motor drive three-phase output voltages are $V_1(t)$, $V_2(t)$, and $V_3(t)$. From Kirchhoff's voltage law,

$$V_0 = \frac{1}{3}\left(V_1 + V_2 + V_3\right) \tag{2}$$

Following the notation of [10], each phase voltage is either 0 or V_{dc} at any given time, where V_{dc} is the magnitude of the source. The common-mode voltage V_0 may take four values: 0, $V_{dc}/3$, $2V_{dc}/3$, or V_{dc}. Previous methods to reduce common-mode voltage [3] eliminated the options of 0 and V_{dc}. With interleaved carriers, all four voltages are possible, but a simulation, such as Fig. 1, shows that V_0 is usually either $V_{dc}/3$ or $2V_{dc}/3$. From the simulated result, one would expect that the rms value of V_0 would be much smaller than in a conventional PWM process. The derivation to follow will verify this expectation and quantify the advantage for a given operating point.

The results of [10] for asymmetric uniform PWM with single sine wave modulation can be adapted easily with a coordinate transformation, where x and y are offset by some angle (e.g., $x = \omega_c t + \phi$). Table 1 shows the modulating function (a single-frequency sinusoid) and carrier wave offsets for all three phases. The Fourier representations of V_1-V_3 are

$$\begin{aligned} V_1(t) = \frac{V_{dc}}{2} &+ \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left(A_{mn}\cos\left(m\omega_c t + n\omega_o t\right)\right) \\ &+ \sum_{n=1}^{\infty}\left(A_{0n}\cos\left(n\omega_o t\right)\right) \end{aligned} \tag{3}$$

$$\begin{aligned} V_2(t) = \frac{V_{dc}}{2} &+ \sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\left(A_{mn}\cos\left(\begin{matrix} m\omega_c t + n\omega_o t \\ +\frac{2\pi}{3}(m+n)\end{matrix}\right)\right) \\ &+ \sum_{n=1}^{\infty}\left(A_{0n}\cos\left(n\omega_o t + \frac{2n\pi}{3}\right)\right) \end{aligned} \tag{4}$$

TABLE 1. MODULATING FUNCTIONS AND CARRIERS FOR THE THREE PHASES.

Phase	Carrier Offset (radians on ω_c scale)	Modulating Function
1	0	$M\cos\left(\omega_o t\right)$
2	$+2\pi/3$	$M\cos\left(\omega_o t + 2\pi/3\right)$
3	$-2\pi/3$	$M\cos\left(\omega_o t - 2\pi/3\right)$

$$V_3(t)=\frac{V_{dc}}{2}+\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\left(A_{mn}\cos\left(\begin{matrix}m\omega_c t+n\omega_o t\\ -\frac{2\pi}{3}(m+n)\end{matrix}\right)\right)$$
$$+\sum_{n=1}^{\infty}\left(A_{0n}\cos\left(n\omega_o t-\frac{2n\pi}{3}\right)\right) \quad (5)$$

$$A_{mn}=\frac{2V_{dc}}{q\pi}J_n\left(\frac{\pi}{2}qM\right)\sin\left((m+n)\frac{\pi}{2}\right)$$
$$q=m+n\frac{\omega_0}{\omega_c} \quad (6)$$

All three phases have the same magnitude, but vary in phase. If the carriers are not interleaved, then Eqs. (4)-(5) have phase offsets of only $2n\pi/3$ inside the double summation. The common-mode voltage may be found by substituting (3)-(6) into (2) and simplifying.

$$V_0(t)=\frac{V_{dc}}{2}+\frac{1}{3}\left(\begin{matrix}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left(\begin{matrix}A_{mn}\left(1+2\cos\left(\frac{2\pi}{3}(m+n)\right)\right)\times\\ \cos(m\omega_c t+n\omega_o t)\end{matrix}\right)\\ +\sum_{n=1}^{\infty}\left(\begin{matrix}A_{0n}\left(1+2\cos\left(\frac{2n\pi}{3}\right)\right)\times\\ \cos\left(n\omega_o t+\frac{2n\pi}{3}\right)\end{matrix}\right)\end{matrix}\right) \quad (7)$$

The dc term is an artifact of the way voltages are defined. The second summation is for the case where $m = 0$. From the definition of A_{mn} in (6), $(m+n)$ must be odd for the result to be non-zero. Because of the phase delays, $(m+n)$ must also be a multiple of 3 for the terms in the double summation to be non-zero. By way of contrast, in conventional PWM, n must be a multiple of 3 for the result to be non-zero, regardless of the value of m.

The rms value of the common-mode voltage may be found from the square root of the sum of the squares of the coefficients to the cosine terms. The dc term is discarded, as it is simply an artifact of the voltage definitions. In the following equations, V_{0rms} is the rms value of the common-mode voltage with interleaving and $V_{0nonrms}$ is the rms value of the common-mode voltage without interleaving.

$$V_{0rms}=\sqrt{\left(\begin{matrix}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left(\frac{A_{mn}}{3}\left(1+2\cos\left(\frac{2\pi}{3}(m+n)\right)\right)\right)^2\\ +\sum_{n=1}^{\infty}\left(\frac{A_{0n}}{3}\left(1+2\cos\left(\frac{2n\pi}{3}\right)\right)\right)^2\end{matrix}\right)} \quad (8)$$

$$V_{0nonrms}=\sqrt{\left(\begin{matrix}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left(\frac{A_{mn}}{3}\left(1+2\cos\left(\frac{2n\pi}{3}\right)\right)\right)^2\\ +\sum_{n=1}^{\infty}\left(\frac{A_{0n}}{3}\left(1+2\cos\left(\frac{2n\pi}{3}\right)\right)\right)^2\end{matrix}\right)} \quad (9)$$

Fig. 2 shows the rms common-mode voltage for both conventional PWM and interleaved PWM as modulation depth M varies, with the following parameters: f_o = 60 Hz, f_c = 2 kHz, V_{dc} = 1 (to normalize). With interleaving, the common-mode voltage is relatively constant regardless of modulation depth. When $M = 0$, the common-mode voltages are 0.2297 when interleaved and 0.7016 with conventional modulation, a reduction of 67.26%. When $M = 1$, the common-mode voltages are 0.2299 when interleaved and 0.3596 with conventional modulation, a reduction of 36.07%.

III. Fourier Analysis of Symmetric Uniform PWM with Third Harmonic Injection

The analysis of symmetric uniform PWM with third harmonic injection is significantly more complex than the above analysis of asymmetric uniform PWM with a single sine wave modulating function. Two problems quickly emerge. The modulating function is more complex, leading to four times as many terms in the summation. Also, more harmonics are non-zero due to the sampling algorithm. Closed-form results, while possible, are more difficult to achieve. Fortunately, numerical integration is possible and provides useful results.

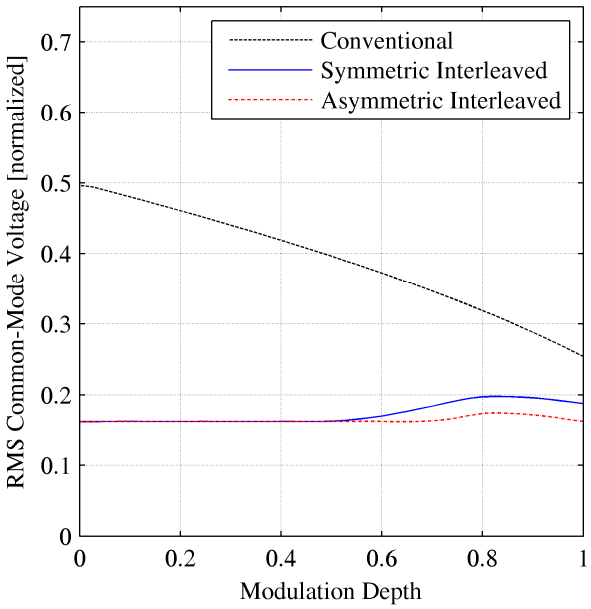

Fig. 2. RMS common-mode voltage as modulation depth varies for both conventional (non-interleaved) PWM and interleaved PWM. Conventional and symmetric interleaved curves include third harmonic injection, whereas the asymmetric interleaved curve does not.

The conventional double Fourier integral that is used to analyze PWM systems is evaluated first over the switching period, and then over the modulating period. The inner integral, evaluated over the switching period, can be performed easily. Unfortunately, terms of the generic form $e^{j\lambda\cos y}$ emerge and must be integrated over y. Closed-form solutions may be obtained from a Bessel function expansion of these terms. In the present work, numerical integration is used instead.

For symmetric uniform PWM with modulating function of the form

$$m(\theta)=\frac{1}{2}(1+M\cos\theta+A\cos 3\theta) \tag{10}$$

the coefficients to the Fourier summations (3)-(5) may be found by numerically evaluating

$$\begin{aligned} A_{mn} &= \mathrm{Re}\left\{\frac{V_{dc}}{2jq\pi^2}\int_{-\pi}^{\pi} e^{jny}\left(e^{jqx_f}-e^{jqx_r}\right)dy\right\} \\ q &= m+n\frac{\omega_o}{\omega_c} \\ x_f &= \frac{\pi}{2}(1+M\cos y+A\cos 3y) \\ x_r &= -\frac{\pi}{2}(1+M\cos y+A\cos 3y) \end{aligned} \tag{11}$$

The result inside the braces should be real. However, due to numerical inaccuracies, there may be an imaginary part that must be discarded. Most applications of this sort use $1/6$ third harmonic injection, that is, $A=-M/6$, to achieve the maximum possible undistorted output.

Once the integration in (11) has been performed numerically, the common-mode voltages given in (8)-(9) for interleaved/non-interleaved PWM may be computed. Fig. 2 also includes a curve for symmetric modulation with interleaving. For the non-interleaved case, the common-mode voltage is affected by neither the sampling method nor the third-harmonic injection. For the interleaved case, there is a slight increase in common-mode voltage at high modulation depths (greater than about 0.5). Still, interleaving the PWM carriers substantially reduces common-mode voltage, by 67.26% at zero modulation depth (as before) and by 26.19% at full modulation.

By comparison, the methods discussed in [3] all have a common-mode voltage magnitude of $1/6$ (normalized), or 0.1667. The common-mode voltage magnitude of interleaved PWM with uniform sampling and third-harmonic injection ranges from 0.2297 to 0.2794. The methods of [3] are computationally intense and, in some cases, impractical. Both approaches achieve the same output voltage range. Given the ease of implementing interleaved uniform PWM, and its substantial improvement over conventional uniform PWM, few applications would require the additional complexity of the methods in [3] to further reduce common-mode voltage.

IV. Simulation Results

The above method is easily implementable on a Texas Instruments TMS320F28335. Digital signal controllers (DSCs, also called digital signal processors or DSPs) in the 2833x family include ePWM peripherals for enhanced pulsewidth modulation. Each channel has its own time base from which two gate waveforms are generated, for the upper and lower IGBT of a leg. Three channels are used for a conventional three-phase inverter, and the channels may be synchronized. One register per channel determines the point in the carrier waveform to which the time base is reset when the synchronization pulse is received. That is, one register per channel determines whether the channels are synchronized or interleaved. This register is separate from the duty ratio and switching period registers, but must be coordinated with the switching period register in order to achieve the proper level of interleaving. Typically, one channel is set as the master and the other two synchronize/interleave from that base.

A simulation was constructed to model the interleaving method. The inverter circuit was modeled with PLECS®[1] version 2.2.1. A deadtime of 2.5 μs and conduction characteristics of an FS100R12KT4G module from Infineon were included. The controller was modeled in Simulink®[2]. For all simulations, the switching frequency was set to 2 kHz and the modulating frequency was set to 60 Hz. Fig. 3 shows the same results as Fig. 2, with simulated results indicated. The simulation follows the same trend, and agrees almost exactly with the predicted performance for conventional modulation. For the interleaved variants, the simulated common-mode voltage is slightly higher than the prediction at high modulation depths. The most likely explanation is that the deadtime interferes with the cancellation effect of the interleaving. Deadtime compensation could be used to achieve the predicted performance. Still, the worst-case

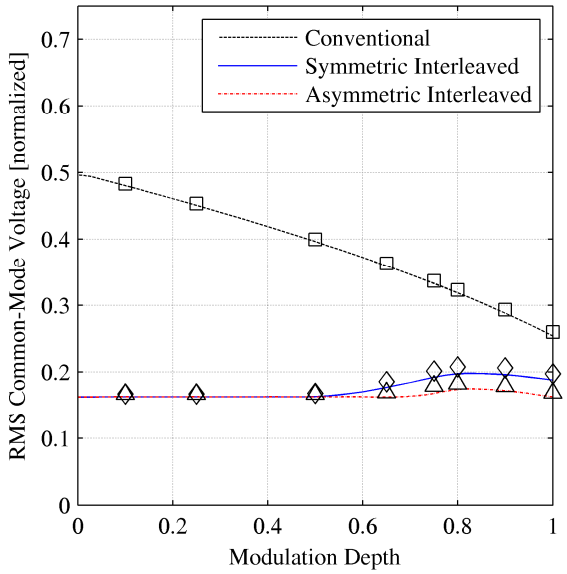

Fig. 3. As in Fig. 2, with simulated results indicated by boxes (conventional), diamonds (symmetric interleaved with third harmonic), and triangles (asymmetric interleaved without third harmonic).

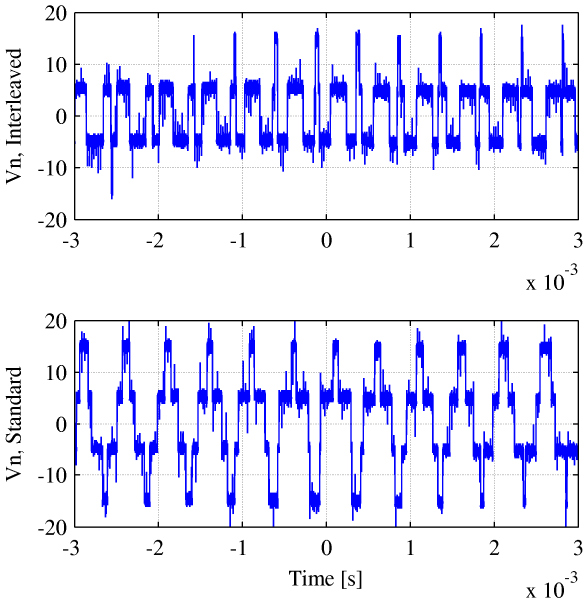

Fig. 4. Example neutral voltage waveforms for interleaved (top) and conventional (bottom) PWM. Modulation frequency was 46.665 Hz with a depth of 0.84.

improvement (at a modulation depth of 1.0 with third-harmonic injection) is 24.14%.

V. Experimental Validation

An inverter was constructed to validate the simulations and calculations. The controller was a TMS320F28335. Switching frequency was fixed at 2 kHz. Linear volts-per-hertz modulation with boost was used, with third-harmonic injection and symmetric uniform sampling. The power stage was based on an Infineon FS100R12KT4G. For these validation experiments, the bus voltage was fixed at 30.3 V and the load motor was a Baldor VM3554T (1½ hp, 4-pole) motor in low-voltage connection. To find the common-mode voltage, all three line-to-negative-bus voltages were probed and averaged. The dc offset was then subtracted to find the ac common-mode voltage applied to the motor.

Fig. 4 shows typical waveforms for the interleaved and standard (non-interleaved) cases. Here the modulation frequency was 46.665 Hz and the modulation depth was 0.84. As in the simulation (Fig. 1), the neutral voltage in the interleaved case is usually at ±1/6 of the bus voltage, with occasional pulses to ±1/2 of the bus voltage. For the non-interleaved case, the neutral voltage is at ±1/2 of the bus voltage for a significant fraction of the time.

Fig. 5 compares the computed results to the experimental results. At high modulation depths, the experimental common-mode voltage is actually slightly less than expected. One possible explanation is that the modulation frequency was lower in the experiment than in the computation. Another possible factor is the lack of stiffness in the bus voltage. Interleaving reduced common-mode voltage by 63.7%, 56.8%, and 39.2% at modulation frequencies of 10 Hz, 30 Hz,

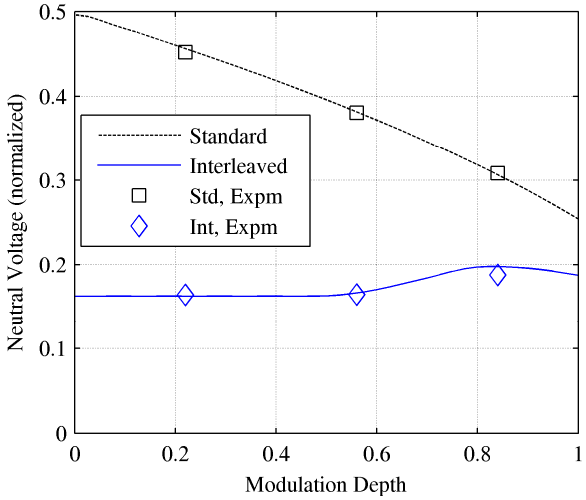

Fig. 5. Comparison of experimental neutral voltage to computed neutral voltage. Symmetric uniformly-sampled PWM with third-harmonic injection was used.

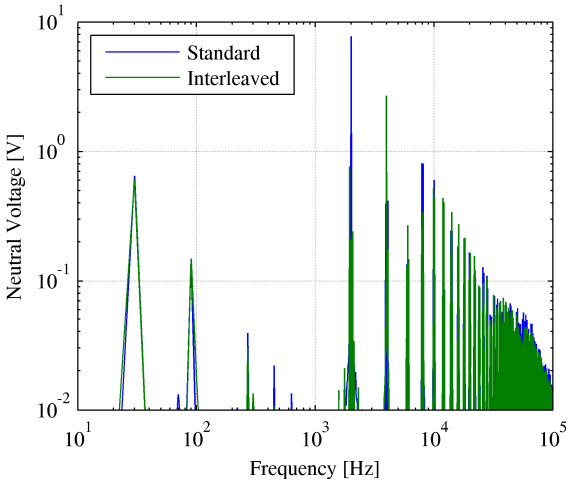

Fig. 6. FFT of neutral voltage for standard (non-interleaved) and interleaved PWM methods. Modulation frequency of 30 Hz, modulation depth of 0.56.

and 46.665 Hz, respectively. The largest common-mode voltage with interleaving was only 5.68 V, or 18.8% of the bus voltage.

Fig. 6 shows fast Fourier transform (FFT) results for the 30 Hz case. In both standard and interleaved PWM, there is some common-mode content at the fundamental and third harmonic of the modulation frequency, possibly due to power supply variations. Subharmonics (between 90 Hz and 1 kHz) are more pronounced in standard PWM. Interleaving nearly eliminates the fundamental of the switching frequency, although the sidebands (switching frequency plus multiples of the modulation frequency) and second harmonic are more pronounced.

VI. Conclusions

A simple method for achieving significantly reduced common-mode voltage in a three-phase inverter was analyzed,

demonstrated through simulations, and validated with an experiment. The method relies on interleaving the carrier waves of the three phases. The advantage of the new method ranges from a low of 26% reduction at full modulation with symmetric uniform PWM and third harmonic injection, to a maximum of 67% reduction at zero modulation depth. No additional computations are needed beyond conventional sine-triangle type uniform PWM. Existing digital hardware in readily available DSCs/DSPs easily implements the interleaving. The improvement varies based on the modulating function and sampling method, but remains substantial regardless. If motor control code is already written for such a DSC with sine-triangle PWM, then the change amounts to two lines of code that change two registers during initialization. Experimental results agree well with the predicted performance and validate the approach.

VII. Acknowledgements

This work was supported by ITW Military GSE and the National Science Foundation I/UCRC on Intelligent Maintenance Systems.

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