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Mehdi Ferdowsi
Missouri University of Science and Technology, ferdowsi@mst.edu

Ali Emadi

Mark Telefus

Curtis Davis

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Pulse Regulation Control Technique for BIFRED Converter

Mehdi Ferdowsi, Ali Emadi

Grainger Power Electronics and Motor Drives Laboratory
Electric Power and Power Electronics Center
Illinois Institute of Technology
Chicago, IL 60616-3793, USA
Phone: +1/(312)567-8940; Fax: +1/(312)567-8976
E-mail: ferdmeh@iit.edu; emadi@iit.edu

Mark Telefus, and Curtis Davis

iWatt Corporation
90 Albright Way
Las Gatos, CA 95032, USA
Phone: +1/(408)374-4200
Fax: +1/(408)341-0455
E-mail: mtelefus@iwatt.com

Abstract—**Pulse Regulation control scheme is presented and applied to BIFRED converter operating in discontinuous conduction mode (DCM). In contrast to the conventional control techniques, the principal idea of Pulse Regulation is to regulate the output voltage using a series of high and low power pulses generated by the current of the input inductor. In this paper, analysis of BIFRED converter operating in DCM is presented. The basic idea of Pulse Regulation as well as the estimation of the output voltage ripple is introduced. Experimental results on a prototype converter are also demonstrated.**

I. INTRODUCTION

It is desirable to have switching power converters, which enjoy profitable features such as wide range of output voltage regulation, small size, low implementation cost, and simple control scheme. It is well proved that it is not simple to achieve these features all at the same time. Boost Integrated Flyback Rectifier/Energy storage DC-DC (BIFRED) converter appears to enjoy most of the desired features at a good extent. It achieves high level of performance by forcing each energy storage element to change its state as independent as possible from the other elements [1].

As its name suggests, BIFRED converter is an integration of boost and flyback converters. Due to its topological complications, achieving line and load regulation in BIFRED converter is not an easy task as in classical topologies such as buck, boost, and flyback converter. Excessive voltage across the energy storage capacitor under variable load condition appears to be the major disadvantage of this topology. To alleviate this problem, different solutions have been suggested in the literature. Authors of [2] represent a variable-frequency control that reduces the voltage stress. Article [3] presents simultaneous phase shift control and duty ratio control to make the output voltage and the voltage across the energy storage capacitor be independently controllable. Authors of [4] and [5] suggest a design in which the flyback part of BIFRED operates in DCM as well as the boost part. In this solution, due to the operation of both stages of BIFRED in DCM, the circuit characteristics, such as voltage transfer ratio, highly become load dependent, therefore it is extremely difficult to provide a wide output voltage regulation range or a fast dynamic response using classical control methods such as pulse width modulation (PWM).

In this paper, Pulse Regulation control technique is proposed to control the output voltage of BIFRED converter. Pulse Regulation is simple and enjoys fast dynamic response [6]. This control scheme regulates the output voltage based on the presence and absence of high-power and low-power pulses. Pulse Regulation is cost effective and robust against the variations of the parameters of the converter.

II. BIFRED CONVERTER

BIFRED converter was initially resulted from integration of a Boost converter, operating in DCM, with a flyback converter, operating in continuous conduction mode (CCM) [1]. Fig. 1 shows the circuit diagram of BIFRED topology. Inserting a diode in front of an isolated SEPIC (Single-Ended Primary Inductance Converter) would result in the same topology [5], [7]. In this converter the input inductor operates independently in the DCM and the energy storage capacitor is in the series path of the energy flow. However, the voltage across the energy storage capacitor has a strong dependency on the output load and it suffers high voltage stress at light loads. Article [5] introduces a new operational mode for this converter, where both the boost and flyback converters operate in DCM. With this new mode of operation, large and load dependent voltage variations of the energy storage capacitor will no longer exits.

Fig. 2 depicts four different operating modes of BIFRED converter operating in DCM-DCM. These operating modes can briefly be described as following:

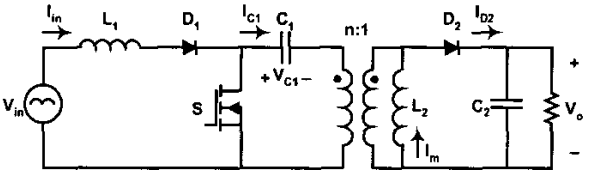

Fig. 1. Circuit diagram of BIFRED converter

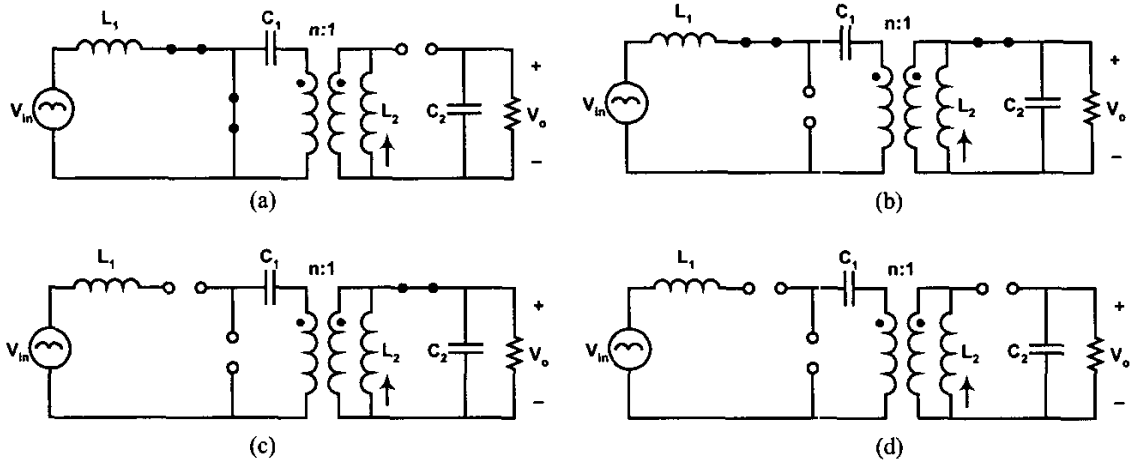

Fig. 2. Four different operational modes of BIFRED converter operating in DCM-DCM: (a) mode I (S: on, D_1: on, D_2: off), (b) mode II (S: off, D_1: on, D_2: on), (c) mode III (S: off, D_1: off, D_2: on), and (d) mode IV (S: off, D_1: off, D_2: off)

Mode I: At the beginning of this mode, switch S is turned on, therefore both switch S and diode D_1 conduct. Input voltage source energizes the input inductor L_1. At the same time, magnetizing inductance of the transformer L_2 receives the energy stored in energy storage capacitor C_1 through switch S. On the secondary side of the transformer, due to the negative voltage appearance across diode D_2, it gets reverse biased and output capacitor C_2 transfers some of its energy to load R.

Mode II: This mode initiates when switch S is turned off. Therefore, the current of the input inductor L_1 flows through the energy storage capacitor C_1 and the primary side of the transformer, delivering its energy to capacitor C_1. Inductor L_1 is completely de-energized at the end of this interval. Secondary diode D_2 is forward biased, which allows the output capacitor to be charged through secondary winding of the transformer.

Mode III: This mode starts when the input current reaches zero. Switch S and diode D_1 do not conduct while secondary diode D_2 conducts. Therefore, output capacitor C_2 receives all of the energy of the magnetizing inductance of the transformer L_2. Throughout this whole interval, the energy state of the input inductor L_1 remains at zero while the energy state of the energy storage capacitor C_1 stays at a constant positive level. This mode ends when the magnetizing inductor L_2 is completely de-energized.

Mode IV: In this mode, switch S and diodes D_1 and D_2 do not conduct while the output capacitor delivers energy to the load. During this interval, the energy state of inductors L_1 and L_2 stay at zero while the energy state of the energy storage capacitor C_1 remains at a constant positive level. This mode finishes when the switch is turned on again.

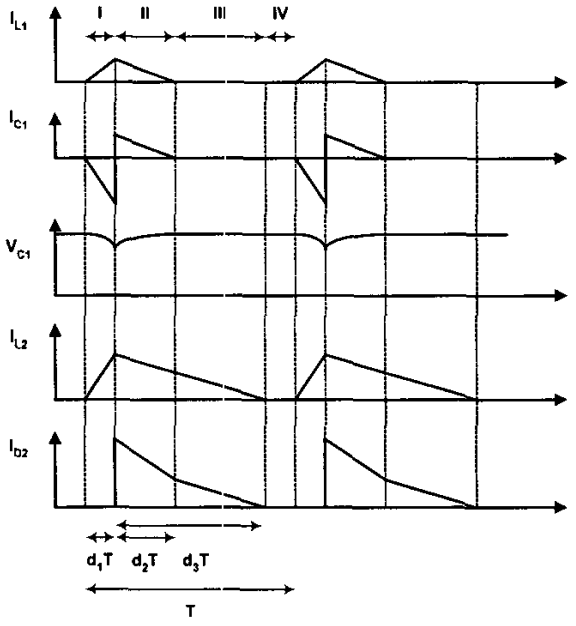

Fig. 3. Typical waveforms of the voltage and current signals of BIFRED converter operating in DCM-DCM

Fig. 3 depicts the typical waveforms of the voltage and current signals of BIFRED converter operating in DCM-DCM, where the current of inductors L_1 and L_2 starts from zero, reaches the maximum level and finally gets back to zero and stays at zero before the switching period ends. As Fig. 3 depicts, the voltage across capacitor C_1 is fairly constant. This voltage will be assumed to be constant in formulation derivation of BIFRED converter in the next

section. Diode D_2 only conducts during modes II and III, hence the current being delivered to capacitor C_2 is discontinuous. The average value of this current will be delivered to the load resistance. As this figure suggests, d_1 is the duty ratio of the conduction period of switch S in mode I, d_2 is the duty ratio of the de-energizing period of input inductor L_1 in mode II, and d_3 is the duty ratio of the conduction period of secondary diode D_2 in modes II and III.

III. FORMULATION DERIVATION OF BIFRED CONVERTER

Current of the input inductor I_{L1} begins the switching period at zero, and increase during the first subinterval with a constant slope, given by the applied input voltage divided by the inductance. The peak inductor current $I_{L1,max}$ is equal to the constant slope, multiplied by the length of the first subinterval:

$$I_{L_1,\max} = \frac{d_1 T V_{in}}{L_1}. \quad (1)$$

Likewise, for the descending current of the input inductor in the second subinterval, by considering the reflected output voltage to the primary side of the transformer and the voltage across the energy storage capacitor C_1, one obtains:

$$I_{L_1,\max} = \frac{d_2 T\left(V_{C_1} + nV_{C_2} - V_{in}\right)}{L_1}. \quad (2)$$

Writing the same equation for inductor L_2, in the first subinterval, yields:

$$I_{L_2,\max} = \frac{d_1 T V_{C_1}}{nL_2}. \quad (3)$$

Furthermore, in the second and third subintervals, based on the descending slope of the magnetizing inductor of the transformer L_2, we can write:

$$I_{L_2,\max} = \frac{d_3 T V_{C_2}}{L_2}. \quad (4)$$

Due to the capacitor charge balance in the equilibrium mode, including the first and the second subintervals, in which the energy storage capacitor conducts, one obtains:

$$\frac{d_1 I_{L_2,\max}}{n} = d_2 I_{L_1,\max}. \quad (5)$$

Likewise for capacitor C_2, based on the average value of the current passing through diode D_2, we obtain:

$$\frac{1}{2} d_3 I_{L_2,\max} + \frac{1}{2} n d_2 I_{L_1,\max} = \frac{V_{C_2}}{R}. \quad (6)$$

Substitution of equations (1), (2), and (3) in (5) to eliminates Vc_1 and d_2 yields:

$$\frac{n d_1^2 T^2 V_{in}^2}{L_1} = nL_2 I_{L_2,\max}^2 + d_1 T I_{L_2,\max}\left(nV_{C_2} - V_{in}\right). \quad (7)$$

Substitution of equations (1), (4), and (5) in (6) to eliminates d_2 and d_3 yields:

$$RL_2 I_{L_2,\max}^2 + Rd_1 T V_{C_2} I_{L_2,\max} = 2TV_{C_2}^2. \quad (8)$$

Solution of (7) and (8) for Vc_2 leads to the quadratic equation of:

$$AV_{C_2}^2 - BV_{C_2} - C = 0 \quad (9)$$

where $A = \frac{2nT}{R}$, $B = \frac{T^2 d_1 V_{in}^2}{L_2}\left(\sqrt{\frac{d_1^2}{4} + \frac{2L_2}{RT}} - \frac{d_1}{2}\right)$, and $C = \frac{n d_1^2 T^2 V_{in}^2}{L_1}$.

Based on the solution of equation (9), we can approximate the input to output voltage transfer ratio of BIFRED converter ($M=Vo/Vin$) as:

$$M = \frac{d_1}{4n}\left(\sqrt{\frac{2RT}{L_2} + \frac{8n^2 RT}{L_1}} + \sqrt{\frac{2RT}{L_2}}\right) \quad (10)$$

The precise value of the voltage transfer ratio (solid line) and its approximation based on equation (10) (dashed line) are sketched in Fig. 4 for different values of the load resistance.

Duty ratios d_2 and d_3, as well as d_1+d_2 as a function of d_1 are depicted in Fig. 5. At the point where d_1+d_2 reaches one, the input inductor will no longer operate in DCM. Furthermore at the point where d_2 and d_3 cross each other, magnetizing inductance of the transformer will no longer operate in DCM. These two points are desired to happen for the same value of d_1. This can be done by choosing the right values for input inductor L_1 and magnetizing inductance L_2. As can be observed from Fig. 5, the converter needs to operate for the duty ratios of d_1 less than the above-mentioned cross points.

We need to note that our calculations in section III are valid if and only if $d_3>d_2$. Therefore, the best design criteria is to designate the values of L_1 and L_2 in a way to make sure that continuous conduction mode of L_1 and L_2 starts at the same point where $d_2=d_3$. In this way, choosing smaller values for d1 guarantees that both of the inductors operate in DCM as well as $d_3>d_2$. Furthermore, magnetizing inductance L_2 nearly operates in critical conduction mode.

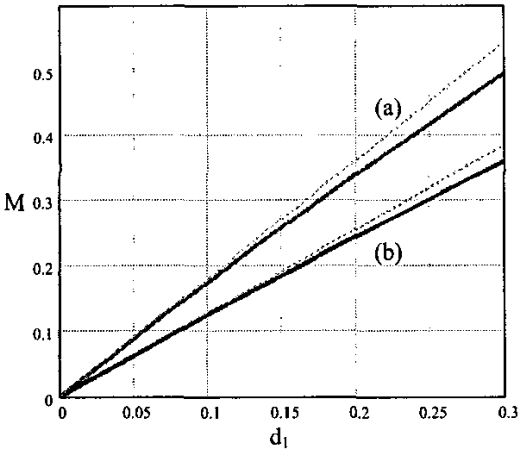

Fig. 4. Precise (solid line) and approximated (dotted line) values of the voltage transfer ratio as a function of d_1; (a) R=20 Ω, and (b) R=10 Ω

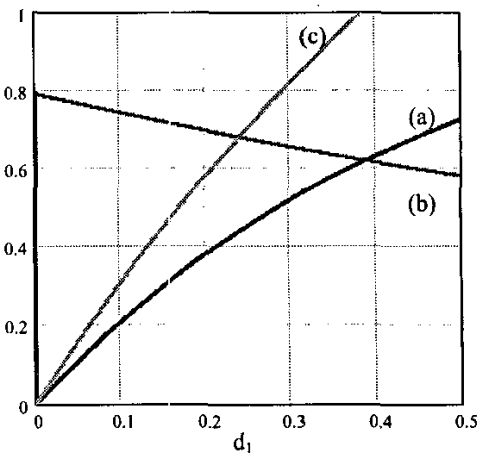

Fig. 5. (a) d_2, (b) d_3, and (c) d_1+d_2 as a function of d1

IV. Pulse Regulation Control Scheme

Pulse Regulation control algorithm achieves output voltage regulation based on generating high and low power pulses, rather than employing PWM control technique. If the output voltage is lower than the desired level, the controller chooses D_H to be the duty ratio and, therefore, high-power pulses are generated sequentially until the desired voltage level is reached. On the other hand, if the output voltage is higher than the desired level, instead of generating high-power pulses, the controller chooses D_L (D_L<D_H) to be the duty ratio and hence, low-power pulses are generated to descend the level of the output voltage. Fig. 6 depicts the block diagram of Pulse Regulation control technique. Due to the longer on time of the switch during a high-power pulse, compared to a low-power pulse, more power will be delivered to the load. The switching frequency is constant and D_H is chosen in a way that the converter operates in DCM but as close as possible to the critical conduction mode. Critical conduction mode occurs when the input voltage is at its maximum level. $k = D_H / D_L$, the ratio between duty cycle of the switch in a high-power cycle D_H and duty cycle of the switch in a low-power cycle D_L, is chosen by making a compromise between the output voltage ripple and the power regulation range from full load to low load.

Fig. 7 depicts the current waveform of the input inductance of BIFRED converter after Pulse Regulation is applied. At the beginning of each switching cycle, based on the difference of the output voltage with the desired voltage level, it will be determined whether a high-power or a low-power cycle needs to be generated. Since the input current ramps linearly with the switch on time, a low-power pulse transfers only $1/k^2$ time as much energy as a high-power pulse.

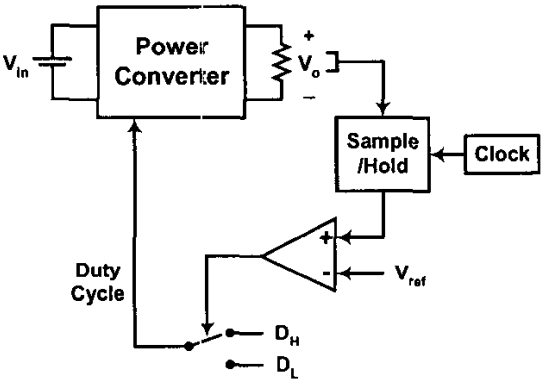

Fig. 6. Block diagram of Pulse Regulation control scheme

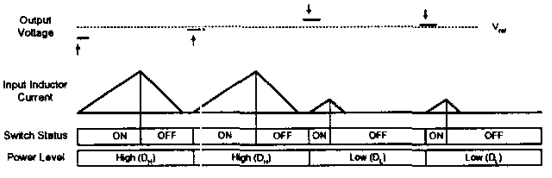

Fig. 7 High and low-power pulse cycles

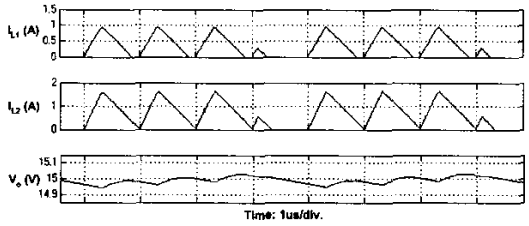

Fig. 8. Simulation results of the Pulse Regulation control of BIFRED converter

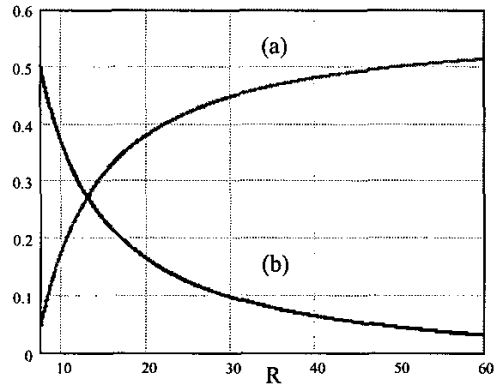

Fig. 9. (a) $\Delta V_{O,HP}$ and (b) $-\Delta V_{O,LP}$ as functions of load resistance

Fig. 8 shows the simulation results of applying Pulse Regulation control method on the input inductor of BIFRED converter with $D_H = 0.3$, $k = 3$, and $V_{ref} = 15$. For this specific value of the output power demand, the control scheme generates three high-power pulses and one low-power pulse in each regulation cycle. As Fig. 8 depicts, both inductors are operating in DCM, yet very close to the critical conduction mode.

We already discussed that the current of the magnetizing inductance needs to reach zero later than the current of the input inductor ($d_3 > d_2$). Because of this fact, employment of Pulse Regulation technique might cause the magnetizing inductor current to be slightly continuous (Fig. 8). The circuit parameters can be designed in a way that d_3 is slightly greater than d_2 over a wide load variations. Therefore, the operation of the magnetizing inductance will be very close to the critical conduction mode.

V. Output Voltage Ripple

Assuming that the output voltage is at its desired level ($V_{C2}=V_{ref}$), we can rewrite equation (7) like:

$$AI_{L_2,max}^2 + BI_{L_2,max} - C = 0, \qquad (11)$$

where $A = nL_2$, $B = d_1 T\left(nV_{ref} - V_{in}\right)$, and $C = -nd_1^2 T^2 V_{in}^2 / L_1$.

Solution of equation (11) for $I_{L2,max}$, having $d_1=D_H$, and using equations (1), (3) and (5) to find $I_{L1,max}$, V_{C1} and d_2 respectively, we can calculate the average value of the current passing through diode D_2:

$$I_{D_{av}} = 0.5 d_3 I_{L_2,\max} + 0.5 n d_2 I_{L_1,\max}. \qquad (12)$$

TABLE I
HIGH AND LOW-POWER PULSE PATTERN PREDICTION IN ONE REGULATION CYCLE

R	$\Delta V_{O,HP}$	$-\Delta V_{O,LP}$	Predicted Pattern
20	0.381	0.164	3*HP - 7*LP
13	0.271	0.274	1*HP - 1*LP
10	0.137	0.408	3*HP - 1*LP

The total changes of the output voltage after applying a high-power pulse can be estimated as:

$$\Delta V_{O,HP} = \left(T/C_2\right)\left(I_{D_{av}} - V_{ref}/R\right). \qquad (13)$$

Likewise, solution of equation (11) for a low-power cycle ($d_1 = D_L = D_H/k$) leads us to the total changes of the output voltage after applying a low-power pulse ($\Delta V_{O,LP}$). $\Delta V_{O,HP}$ and $-\Delta V_{O,LP}$ as a function of load resistance R are sketched in Fig. 9. As we can observe, the control scheme tries to regulate the output voltage by generating the right number of high and low-power pulses in each regulation cycle. We can observe that as the output power increases, $\Delta V_{O,HP}$ decreases; but $-\Delta V_{O,LP}$ increases. This fact implies that at a higher output power level, the control strategy prefers to have more high-power pulses rather than low-power pulses in each regulation cycle and vice versa in light loads. The value of the output load resistance at which the two graphs cross each other is the value of load, which requires one high-power pulse associated with one low-power pulse in each regulation cycle. Considering different values for the load resistance, different patterns of high and low-power cycles can be extracted using Fig. 9. Table I shows some examples of the pattern of high and low-power pulses.

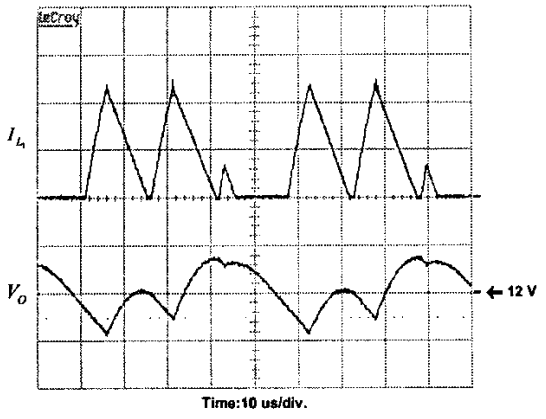

Fig. 10. Measured (a) input current (0.6 A/div) and (b) output voltage ripple (0.1 V/div) for 60% of full load

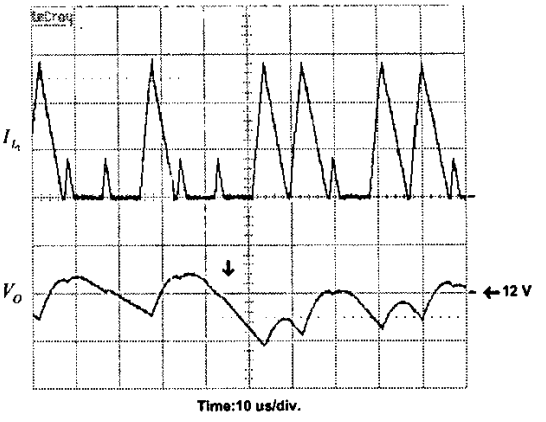

Fig. 11. Measured (a) input current (0.6 A/div) and (b) output voltage ripple (0.1 V/div) for a step load change of 30% to 60% of full load.

According to Table I, for instance, when $R=10$, we have $\Delta V_{O,HP} \approx 1/3 * -\Delta V_{O,LP}$ which predicts for this value of load, in each regulation cycle, the converter generates one low-power pulse associated with each three high-power pulses. Therefore, first we calculate $\Delta V_{O,HP}$ and $-\Delta V_{O,LP}$ (equation (13)) associated with each value of R, then we find two integers as this equation holds.

$$\alpha \cdot \Delta V_{O,HP} = \beta \cdot -\Delta V_{O,LP} \tag{14}$$

where α and β represent the number of high and low-power pulses in each regulation period.

VI. Experimental Results

The experimental results of Pulse Regulation control method applied to BIFRED converter are shown in Figs. 10 and 11. Fig. 10 depicts the input inductor current and the output voltage ripple for the value of load equal to 60% of the full load, whereas Fig. 11 shows the same waveforms for a 30% to 60% step load change. The vertical arrow marks the time instant at which the step change is applied.

VII. Conclusions

BIFRED converter operating in DCM-DCM has the advantage of low voltage level across the energy storage capacitor and, therefore, less voltage stress across the input diode and switch. This converter has found its way into many applications. To address the challenge of designing controllers for this type of converters, this paper has introduced Pulse Regulation control method. This control method has several advantages over the conventional techniques, such as robustness, accuracy, and fast transient response. Simulation as well as experimental results completely match with the theoretical concept.

VIII. References

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