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Grounding of Heatpipe/Heatspreader and Heatsink Structures for EMI Mitigation

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Abstract: EMI problems caused by the presence of heatpipe/heatspreader and heatsink structures in a high-speed design are well known in engineering practice. High-frequency noise can be coupled from IC packages to an electrically conductive heatsink or heatspreader attached to the IC, which then is radiated, or the energy coupled to an enclosure cavity mode. This EMI coupling path was modeled with the finite-difference time-domain (FDTD) method, and a mitigation approach was investigated. Good agreement between measurements and FDTD modeling is demonstrated, indicating FDTD is a suitable tool for analysis and design. Then, several grounding schemes suitable for a heatsink or heatspreader were compared using FDTD modeling. The results indicate that sufficiently connecting the heatspreader or heatsink to the top layer of the PCB, even without further electrically connecting to the PCB ground plane, can result in appreciable EMI reduction. Good electrical connection of the heatsink or heatspreader to the PCB ground plane through an SMT-mount approach can achieve a *10 – 25 dB* reduction for EMI attributable to the proposed coupling path.

INTRODUCTION

Heatsinks and heatpipe/heatspreader structures are widely used in electronic designs for heat dissipation with ICs, ASICs, and CPUs that generate excessive thermal energy. As a metal structure having a significant profile protruding above the printed circuit board (PCB), and significant electrical dimensions at the frequencies of modern high-speed devices, heatsinks can be driven by many structures on the PCB with high-frequency signals or noise on them including ICs, and PCB traces. The driven heatsink or heatpipe/heatspreader in turn can act as a potential radiator of this high frequency noise, exciting an enclosure and resulting in increased radiation through slots and apertures up to several gigahertz.

Other work has studied the EMI due to noise coupled from a high-speed PCB trace in proximity to a heatpipe traversing the PCB [1]. Analysis of EMI problems due to VLSI heatsinks was reported in [2-5] as well. In this study, FDTD modeling was employed to study the EMI from heatspreader or heatsink structures. The noise coupling to the heatsink or heatspreader was modeled by a driven copper patch mimicking noise from a CPU. Good agreement was achieved between measurements and the FDTD modeling for a representative geometry. EMI mitigation by grounding the heatsink or heatspreader was then investigated using FDTD modeling. A method for grounding a heatsink or heatspreader is proposed that can reduce radiation for the EMI coupling path of concern by *10 - 25 dB*. The frequency range considered was *100 MHz – 5 GHz*.

FDTD MODELING OF A HEATPIPE/HEATSPREADER STRUCTURE

Figure 1 shows an experimental setup for studying noise coupled from a driven copper patch to a simplified heatpipe/heatspreader structure. The PCB was standard FR4

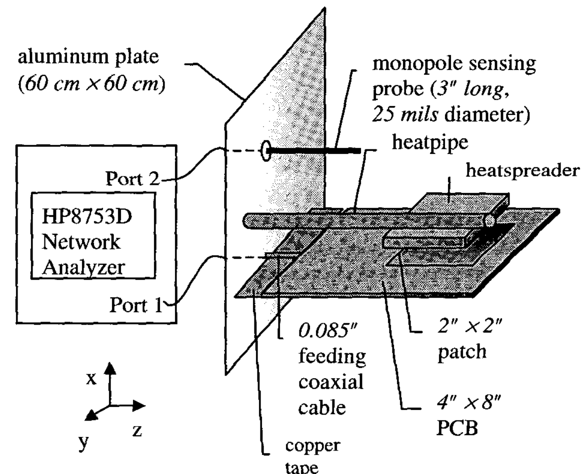

Figure 1. Schematic representation of the experimental heatspreader/heatpipe setup.

material with dimensions of *4″* wide, *8″* long and *60 mils* thick. The bottom layer of the PCB was a copper plane that served as a PCB ground plane. The PCB ground plane was connected, by conductive adhesive copper tape, to a *60 cm × 60 cm* vertical (in the x and y plane) aluminum plate. The aluminum plate was used to mimic an enclosure wall. In addition, the large aluminum plate served to isolate the geometry under investigation from the measurement equipment, and cables.

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On the top layer of the PCB, a *2″ × 2″* copper patch was fed by an *0.085″* semi-rigid coaxial cable, whose outer shield was connected to the PCB ground plane all the way along its length. The center conductor of the feed cable was extended through the bottom of the PCB, and was soldered to the copper patch. The feeding semi-rigid coaxial cable had an SMA connector, which was connected to an SMA female feed thru mounted in the aluminum plate. The feed cable driving the patch on the PCB was then connected to Port 1 of an HP8753D network analyzer. The heatspreader was located and centered directly above the copper patch, and had dimensions of 2″ wide, *2″* long, and *0.36″* thick. The separation between the lower surface of the heatspreader and the patch was approximately *200 mils*. The heatpipe was soldered to the heatspreader along the length of the heatspreader, and then extended across the PCB to make contact with the aluminum plane. The heatpipe diameter was *0.5″*, and the length of the heatpipe spanning from the heatspreader edge nearest to the aluminum plate, to the aluminum plate was approximately *5.7″*. Both the heatspreader and heatpipe were made of copper. The heatpipe was soldered to a large square of copper tape with conductive adhesive backing that was affixed to the aluminum plate in order to have a good electrical contact of the heatpipe to the plate. A *3″* long monopole sensing probe with a *25 mil* diameter was located 2″ above the PCB and centered on the device under test. The monopole sensing probe was connected to Port 2 of the HP8753D network analyzer. $|S_{21}|$ was measured with the network analyzer.

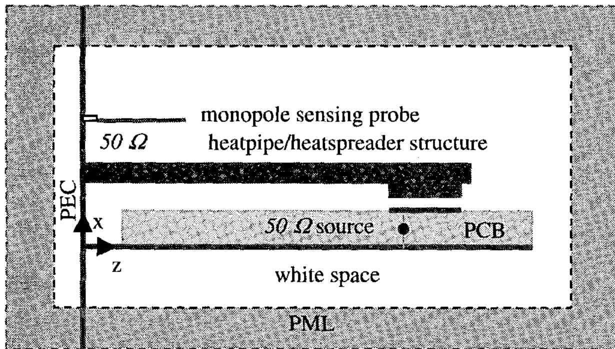


Figure 2. Side view of the geometry used in the FDTD model for coupling from a driven patch to a heatspreader/heatpipe structure.

FDTD modeling was employed to model the experimental configuration shown in Figure 1. An illustration of the FDTD computational domain is shown in Figure 2. A uniform cell size of *60 mils × 50 mils × 100 mils* (x, y, z) was used such that the thickness of the PCB was discretized with one cell. All the metal structures, including the aluminum plate, the PCB ground plane, the copper patch and the heatpipe/heatspreader structure, were modeled as perfect electric conductors (PEC). Perfectly Matched Layers (PML) were employed as a numerical absorbing boundary condition [6]. Since the geometry of the aluminum plate was much larger than the geometry of the test fixture in the experiment, the aluminum plate was approximated as an infinitely large PEC, and was modeled with a PEC surface extended and embedded in the PML, as illustrated in Figure 2. Because a rectangular mesh was used in the FDTD modeling, the cross-section of the cylindrical heatpipe was approximated as a staircased octagon.

Other research has shown that it is necessary to incorporate dispersive, lossy properties in order to capture the behavior of FR-4 in the gigahertz region [7]. A Debye model was used to account for the dispersion characteristics of the dielectric material of the PCB. The Debye equation allows for the calculation of the real and imaginary parts of the complex relative permitivity for dielectric materials as a function of frequency as [8]

$$\varepsilon_r'(\omega) = \varepsilon_{r\infty}' + \frac{\varepsilon_{rs}' - \varepsilon_{r\infty}'}{1 + (\omega\tau_e)^2} \tag{1}$$

$$\varepsilon_r''(\omega) = \frac{(\varepsilon_{rs}' - \varepsilon_{r\infty}')\omega\tau_e}{1 + (\omega\tau_e)^2} \quad , \tag{2}$$

where ε_r' and ε_r'' are the real and imaginary part of the complex relative permittivity, respectively. The permitivities ε_{rs}' and $\varepsilon_{r\infty}'$ are the relative permitivity ε_r' at zero frequency and at infinite frequency, respectively, and τ_e is the relaxation time constant. The FDTD simulation was conducted with $\varepsilon_{rs}' = 4.0$, $\varepsilon_{r\infty}' = 3.7$, and $\tau_e = 4.94\times10^{-11}$. The conductivity of the dielectric material was set to $\sigma = 9.2\times10^{-6}$.

The monopole sensing probe was modeled using a thin-wire subcellular algorithm [9]. A *50 Ω* lumped resistor was introduced between the base of the monopole sensing probe and the aluminum plate to account for the *50 Ω* measurement system, as shown in Figure 2. The lumped resistor was modeled using a subcellular algorithm [10], with the encircling magnetic field components modified in the same fashion as for the thin-wire algorithm to give it specified cross-sectional dimensions. The feeding semi-rigid coaxial cable need not be modeled because its outer shield was connected to the PCB ground plane along its entire length. However, the center conductor of the feeding cable from the PCB ground plane to the copper patch was modeled using a sinusoidally modulated Gaussian voltage source, with a *50 Ω* resistance incorporated into the source cell [11]. As with the thin-wire and resistive loads, the magnetic field components encircling the source cell were modified to give the source cell a specified cross-sectional dimension. The source dimensions used in the FDTD modeling was *20 mils*, the diameter of the extended coaxial cable center conductor feeding the driven patch. The $|S_{21}|$ from the FDTD modeling was calculated as

$$|S_{21}| = 20 \times \log_{10}\left(\frac{V_2}{2V_0}\right) \tag{3}$$

where V_2 is the voltage dropped across the resistor connected to the monopole sensing probe, and V_0 is the voltage generated by the sinusoidally modulated Gaussian source.

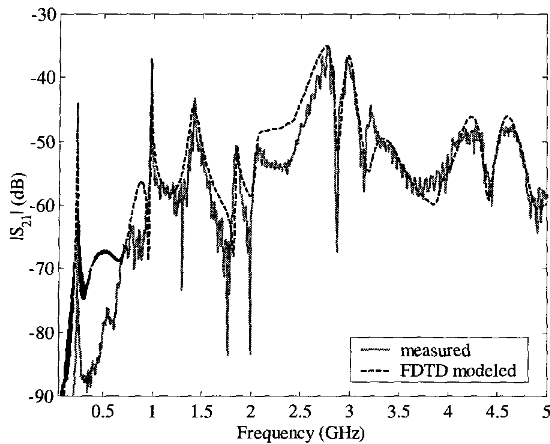


Figure 3. Comparison between the measured $|S_{21}|$ and FDTD results for radiated EMI from the heatpipe/heatspreader structure shown in Figure 1.

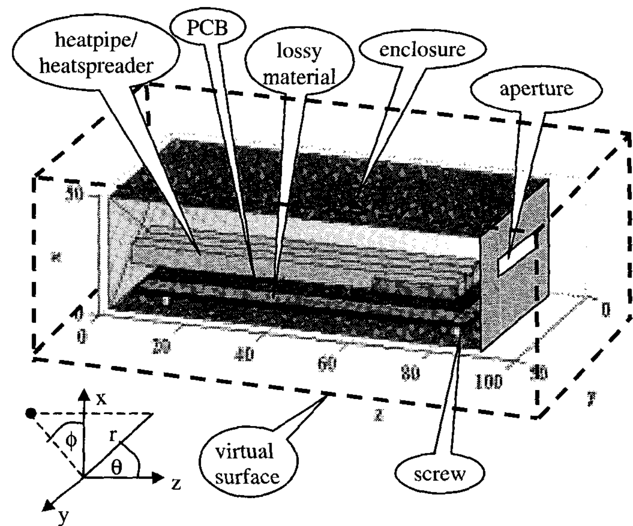


Figure 4. Geometry of the FDTD modeling for studying the heatspreader grounding scheme.

The measured and modeled $|S_{21}|$ are shown in Figure 3. The agreement between the measured and modeled results is in general good. There are significant discrepancies in the magnitude below *1 GHz*, though the resonances at approximately *250MHz*, *500 MHz* and *1 GHz* agree, as well as the approximate *Q's*. Presently, the source of the discrepancy is unknown. Overall, the favorable comparison of the modeling and measurements indicates that FDTD modeling is a suitable tool for analysis, and engineering design for mitigation of EMI problems caused by heatsink or heatspreader structures.

EMI Mitigation through Grounding of the Heatspreader or Heatsink

FDTD modeling then was applied to investigate the influence on EMI of grounding the heatspreader. In this study, a heatspreader/heatpipe geometry was of primary concern, but the mitigation approach through grounding applies equally well to a heatsink structure. The geometry of the device under consideration used in the FDTD modeling is shown in Figure 4.

A modeled heatpipe/heatspreader structure and a PCB were placed in a *2.82″ × 4.5″ × 9″* enclosure, which was modeled as a PEC box. Inside the enclosure, the PCB with a width of *4″* and a length of *8″*, was located *0.36″* above the bottom wall of the enclosure. The modeled PCB had a thickness of *60 mils*, and the dielectric was modeled as a Debye material. The bottom of the PCB was modeled as a PEC plane, and served as the PCB ground plane. This ground plane was connected to the enclosure at its four corners using four PEC boxes to mimic screws connecting a motherboard to a chassis. Connecting the PCB ground to the enclosure at its four corners is not advocated in this research, rather, the four corners were grounded to reflect a common practice in many electronic products.

The heatspreader was positioned *0.24″* above the PCB, and energy was coupled to the heatspreader by a *0.3″ × 0.3″* PEC patch located at the center of the heatspreader. The driven patch was located above the PCB midway between the heatspreader and the PCB. The PEC patch was driven by a sinusoidally modulated Gaussian voltage source with a *50 Ω* impedance. Three strips of lossy material, *0.8″* wide each, were placed around the periphery of the PCB (not including the side where the heatpipe attached to the enclosure) to mimic the losses of components on the PCB [12]. The lossy material was modeled as a dielectric of one FDTD cell thick, with $\varepsilon_r = 1$, and conductivity $\sigma = 0.0227$ *S/cm*. An aperture with dimensions of *0.24″ × 2.5″* was placed on one side wall of the enclosure to allow for radiation. The objective of the geometry was to allow for a comparison between different headspreader grounding schemes, and not to model specific dimensions of the coupling path on the PCB, enclosure, or radiating slots and apertures. The radiated electric field at *3 m* was calculated using an extrapolation with the equivalent electric and magnetic currents on the virtual surface shown in Figure 4 [9]. This far-field extrapolation has been demonstrated to agree well with measurements down to *400 MHz*, though this is well below the typical $\lambda/10$ metric applied for far-field approximations [13]. The source voltage in the results was scaled to *1 V*.

A proposed grounding scheme for the heatspreader is shown in Figure 5. The four edges of heatspreader were extended down toward the PCB and truncated *60 mils* above the PCB. Conducting legs and feet were used to connect the extended blades of the heatspreader to the top layer of the PCB. A practical implementation of this geometry would be a heatspreader or heatsink tapered to a knife edge, which could

be inserted into a PCB SMT mount receptacle made of sheet metal. The heatsink knife-edge would mount into the PCB SMT-mount receptacle in a fashion similar to the knife-edge fitting into finger-stock commonly used in shield room doors. The SMT-mount feet were chosen to be *100 mils* wide and *300 mils* apart from edge to edge so that the feet on the PCB would not severely limit routing flexibility. Five different configurations were studied and compared as detailed below.

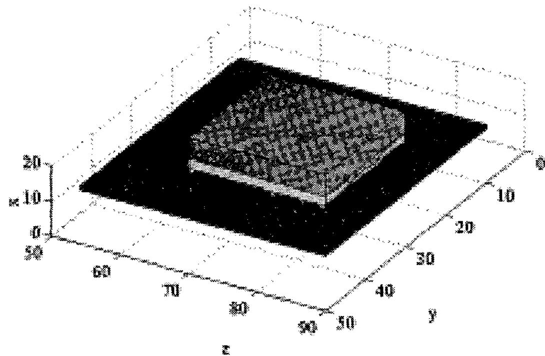
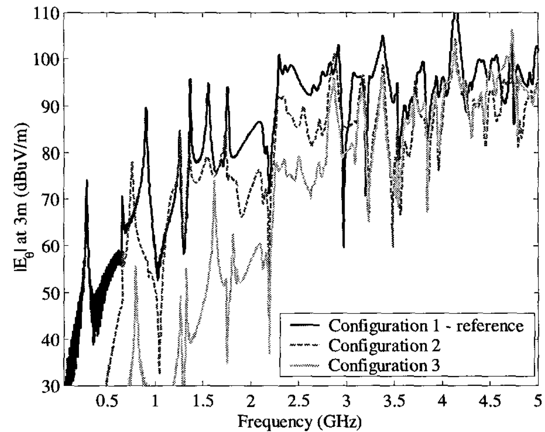


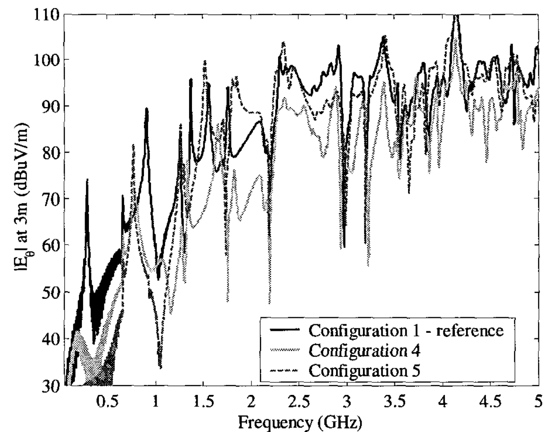
Figure 5. Illustration of the heatspreader grounding showing the extended side blades of the heatspreader and conducting legs and feet.

- Configuration #1 -- No heatspreader grounding scheme was applied. The geometry was exactly the same as shown in Figure 4. This configuration was used as a reference.
- Configuration #2 -- The heatspreader was grounded as shown in Figure 5. Only the four SMT-mount feet at the corners of the heatspreader were connected to the PCB ground plane using *20 mil* diameter vias. The other feet on the PCB were floating. The vias were modeled in the FDTD simulation using the thin-wire algorithm.
- Configuration #3 -- All the feet in Figure 5 were connected to the PCB ground plane with *20 mil* diameter vias.
- Configuration #4 -- No SMT-mount feet in Figure 5 were connected to the PCB ground plane. All the feet were floating.
- Configuration #5 -- All the floating feet and legs in Configuration #2 were removed, except the four SMT-mount feet at the corners. These were connected to the PCB ground plane through *20 mils* vias.

The radiated electric fields from the five configurations are compared in Figure 6 (a) and (b). The curves corresponding to the feet and legs extended from the heatspreader to the top layer of the PCB, including Configurations #2, #3 and #4, are significantly lower than the solid-heavy curve corresponding to the Configuration #1 with no grounding scheme applied. However, when most of the feet and legs were removed and only the feet and legs on the corners remained as in Configuration #5, the strength of the E-field at *3 m* increased back to the original level though there was shifting of resonances. As a result of resonance shifting, the EMI level is actually worse than in the un-grounded case. A result well-known in practice that often prohibits engineers from attempting to ground a heatsink in such a minimal fashion. Comparison of the curves for Configurations #1, #4, and #5 also indicates that the capacitive coupling between the feet, and the PCB ground plane, can play an important role in the EMI reduction.



(a)



(b)

Figure 6. Comparison of FDTD modeled results of radiated EMI from various heatsink grounding schemes.

The curve of Configuration #4, corresponding to all the feet floating, is significantly lower than that of Configuration #1. It indicates that connecting the heatspreader to the top layer of the PCB with a sufficient density, even without a conductive connection to the PCB ground plane, will reduce radiated EMI appreciably. This is a result of capacitive coupling between the feet and PCB ground plane. Here the spacing of the PEC

grounding feet to the PCB ground plane is *60 mils*, though in practice for a multi layer PCB design it would be significantly less, thereby increasing the coupling capacitance of the feet to the PCB ground. Overall, grounding all the feet connections of the heatspreader to the PCB ground plane, as in Configuration # 3, reduced the radiated electric field in excess of *10 - 25 dB* up to *5 GHz*.

CONCLUSION

Good agreement between measured and FDTD modeled results demonstrates that FDTD is a suitable tool for investigating EMI problems due the presence of heatpipe/heatspreader or heatsink structures. FDTD modeling was then used to study an EMI mitigation approach based on a manufacturable SMT grounding design. Several cases of grounding the heatspreader were investigated. The results indicate that connecting the heatspreader to the non-conductive top layer of the PCB, even without further connecting to the PCB ground plane, will reduce the EMI level appreciably, though the greatest EMI reduction is achieved when all connections are grounded.

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