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Fourier Based Three Phase Power Metering System

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Abstract

The increased application of higher frequency nonlinear loads, such as electronic florescent ballasts and higher speed adjustable drives, has resulted in the need to monitor the higher power system harmonics which were largely ignored in earlier power monitors. Addressing this need requires a meter with substantially higher sample rate and greater computational power. This paper describes a zero-blind, three-phase, three-element power meter that samples three voltages and four currents at 256 points per cycle. The instrument relies on the FFT to compute real and reactive power at each harmonic and reports total real, reactive, and distortion power on each phase. The innovative design is based on a multiprocessor chip which incorporates a DSP for acquisition and point metering, a CISC processor for floating point summary data, and a RISC processor for interface to support communications with the host PC. The paper concludes with a system evaluation on highly distorted industrial power system waveforms.

1. Introduction

The greater use of highly distorting loads, such as high-speed adjustable drives and electronic ballasts, has increased the bandwidth of concern in power metering and power quality monitoring. Harmonics often neglected in earlier meters are receiving increased attention resulting in higher sample rates and the need for greater processing power [1].

The Fourier based system provides three-phase, three-element, four-wire metering. It meters the three line-to-neutral voltages and the line and neutral currents at 256 points per cycle. Synchronization to the power system is maintained by a combination of modified zero-crossing and Fourier based approaches.

In addition to reporting the rms and THD of each of the three voltages and four currents monitored, the system also meters the real, reactive, phasor, distortion, and apparent power, as well as the power factor on each phase [3]. In a special mode, called Fourier mode, the Fourier coefficients of the voltages and currents are output to provide spectral data on the input signals along with the time domain data on which they are based.

2. System Architecture

Figure 1 depicts the basic power metering system diagram. PTs, CTs, and analog conditioning circuitry transform the power system voltages and currents to biased signals in the range of 0-5 VDC. Two AD7864-2 quad-channel analog to digital converters, with integral sample and hold circuits, simultaneously acquire the conditioned signals, and provide these to a MC68356 microcontroller system. This microcontroller system provides three processors, a 56002 DSP, 68000 CISC processor, and a RISC communication processor, as well as the on chip complement of timers, interfaces, and support circuitry, from which to develop a powerful metering engine. The system performs all of the metering computations and forwards the metering results to a PC host via a serial link for display.

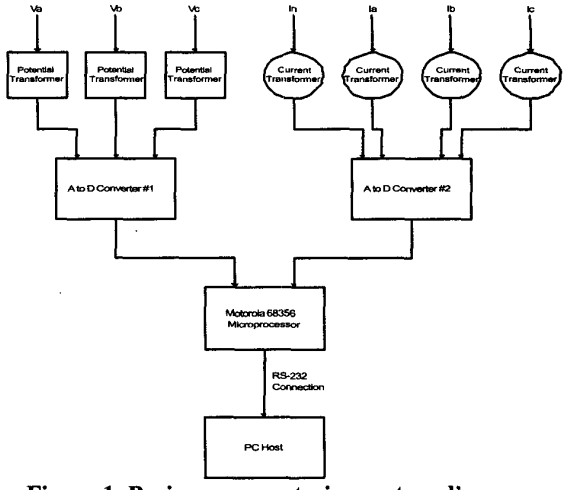

Figure 1. Basic power metering system diagram.

Sampling 60 Hz power system waveforms at 256 points per fundamental cycle requires a sample frequency of 15.36 KHz, providing an intersample interval of

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65.1 μs; therefore each of the twin AD7864-2 quad-channel 12-bit analog to digital converters, with four channel conversion times of 7 μs, have more than adequate time to perform their conversions. Each of the converters is strobed simultaneously so that all voltage and current acquisitions occur in coincidence, thus preserving the relative phase information between channels. Each of the converters is provided with a 12-bit parallel interface. Since the on-chip 56002DSP has a 24-bit wide data memory, the two converter outputs can be accessed with a single 24-bit read. Since one converter monitors the line to neutral voltages and the other the phase and neutral currents, a single read will capture a VI metering element point pair. The sample timing is provided by the conversion start signal ($\overline{CONVST}$) which originates from the integrated multiprotocol processor (IMP) portion of the 68356 microprocessor, triggered by a periodic interrupt timer which is programmed to interrupt every 65.1 μs. On the rising edge of $\overline{CONVST}$, the $\overline{BUSY}$ signal goes high and all selected channels of the two converters are simultaneously sampled; then these analog signals are converted to digital signals. When all four channels of the second converter have been converted, $\overline{BUSY}$ goes low, which is used to trigger an interrupt on the DSP. This interrupt then causes four successive reads to address y:$FFFF, where the converters are memory mapped as a peripheral device. Figure 2 details the A to D converter interface. Each one of these reads is a 24-bit read with the high 12 bits from the first converter and the low 12 bits from the second converter. The first read acquires the phase A voltage and the neutral current, the second read acquires the phase B voltage and phase A current, the third read acquires the phase C voltage and phase B current, and the fourth rereads the phase A voltage and acquires the phase C current. Once these four reads have been completed, the DSP separates the voltage and current data and stores these values into their respective data arrays in memory, before returning from the interrupt.

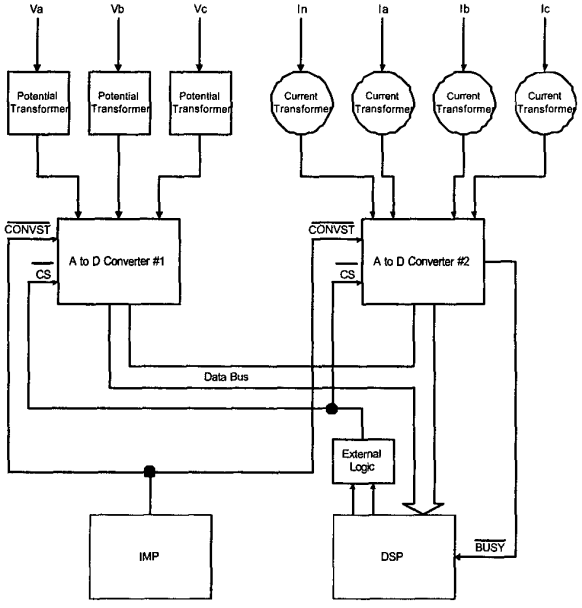

Figure 2. A to D converter diagram.

2.1. Motorola 68356 microprocessor

The 68356 microprocessor is actually two microprocessors integrated into one chip. The 68356 consists of a 56002 DSP and a 68302 IMP. The 68302 can be further broken down into a 68000 CISC core processor and a RISC communication processor. Figure 3 shows the data flow through the system's main components.

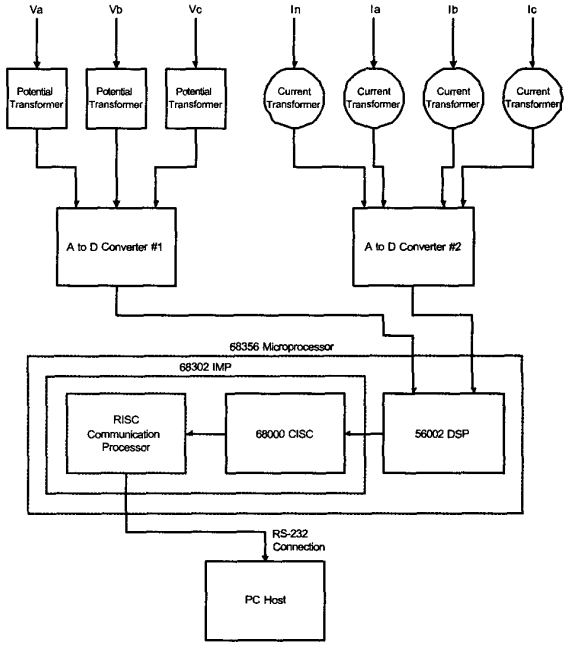

Figure 3. Expanded power metering system diagram.

2.1.1. 56002 DSP

As mentioned before, the DSP reads the digital voltage and current data from the A to D converters and stores these values into their respective data arrays in memory. Once the data for a full power cycle (256 points) for each of the three phase voltages, each of the three phase currents, and the neutral current has been collected, the DSP performs a FFT on each of these seven sets of point data in order to calculate their respective Fourier coefficients [2, 4]. Once these coefficients have been calculated, they are used by the DSP to either calculate power sums which will be used in the power calculations (normal mode), or they are added to a running sum of

Fourier coefficients to be output (Fourier mode). If the DSP is in normal mode the phase powers are averaged over 128 cycles and these results are then written to the IMP, to be used in the power calculations. Otherwise, the Fourier coefficient sums are written to the IMP where they are averaged and scaled before being output to the host PC. Figure 4 depicts the program flow for the DSP.

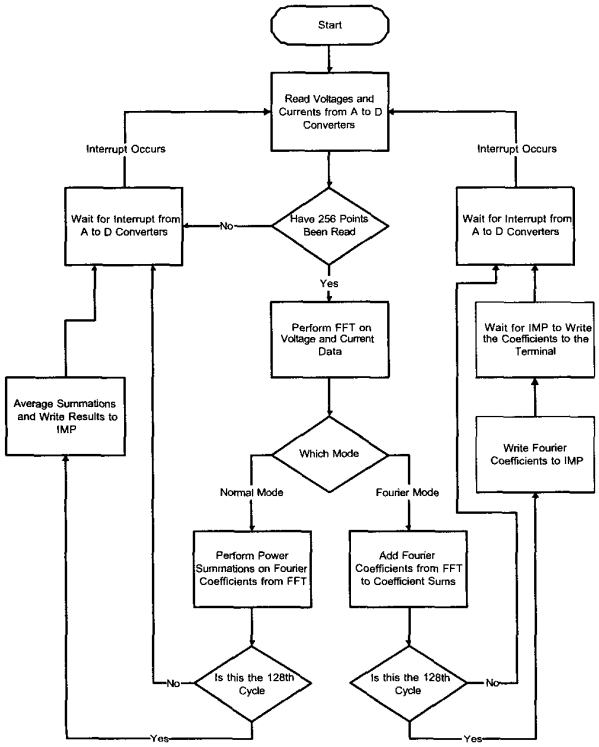

Figure 4. DSP program flow diagram.

ASCII data to be sent via an RS-232 connection to the host PC, where it can be viewed. The first set of calculations is always displayed; and any subsequent set of calculations may be displayed by pressing any of the terminal keys except Esc. Pressing the Esc key switches the power meter into Fourier mode, in which case the Fourier coefficients for each of the seven input signals are output to the terminal screen. After the Fourier coefficients are output, the power meter is automatically switched back to normal mode and the next set of results is displayed. Figure 5 depicts the program flow for the IMP.

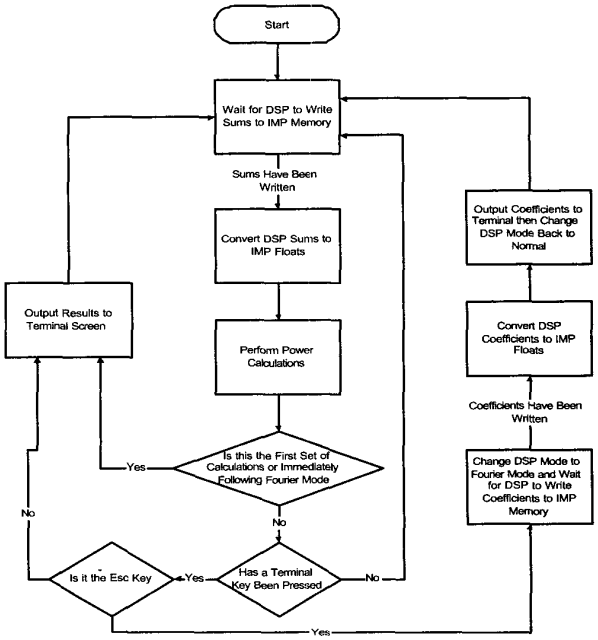

Figure 5. IMP program flow diagram.

2.2.2. 68302 IMP

During normal mode, once the power sums have been calculated and averaged together for 128 cycles by the DSP, they are then written to the IMP. The IMP must first convert the DSP fixed point fractional numbers to IMP floating point numbers (see section 3.2), before performing the power calculations and outputting the results to the host PC. During Fourier mode, once the Fourier coefficients have been summed for 128 cycles by the DSP, they are then written to the IMP, which must convert the DSP fixed point fractional numbers to IMP floating point numbers and scale these coefficients before outputting them to the host PC.

In normal mode, once the power calculations are completed, they are written as formatted ASCII strings into IMP memory and the IMP checks to see if the results are to be displayed. If they are to be displayed, the RISC communication processor is triggered, which causes this

3. Theoretical Basis

The basis for this power metering system is the Fast Fourier Transform. The FFT algorithm used is a radix 2 decimation in frequency (DIF) real FFT. This algorithm is radix 2 because the number of input points must be a multiple of 2 (i.e. $256 = 2^8$). The algorithm is DIF because of the basic butterfly computation used, which performs the additions and subtractions before multiplication by the twiddle factor, W. Figure 6 depicts the basic DIF butterfly computation.

The FFT algorithm used is based on the Cooley-Tukey approach, which groups the butterfly computations according to their W value, in order to cut down on the number of computations. A real FFT was chosen, opposed to a complex FFT, because there is no imaginary part to any of the input sequence, therefore making it feasible to use a real FFT, which greatly reduces the number of required computations. A complex FFT of length N would

require $(N/2)*\log_2(N)$ complex multiplies and $(N/2)*\log_2(N)$ complex adds, while a real FFT of the same length only requires $N/2 + (N/4)*\log_2(N/2)$ complex multiplies and $(N/4)*\log_2(N/2)$ complex adds, thus reducing the time for a real FFT to approximately half of the time for the same sized complex FFT.

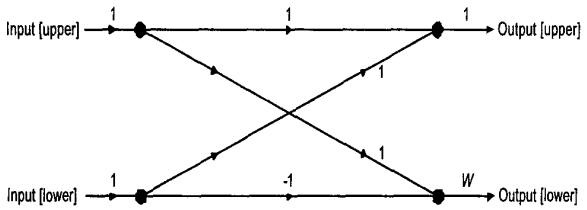

Figure 6. Decimation in frequency butterfly.

The real FFT algorithm requires that the input sequence of length N be split into two arrays of length N/2, the even and odd elements of the original sequence. The real FFT algorithm then performs a complex FFT of length N/2 using the even elements as the real part of the input sequence and the odd elements as the imaginary part of the input sequence. The results of the complex FFT are then combined using a trigonometric recombination procedure to produce the bit reversed Fourier coefficients of the original sequence. Finally the bit reversed coefficients are rewritten in normal order using the special bit reversed addressing mode of the DSP. These coefficients are now ready to be used to calculate the sums that will be used in the power calculations during normal mode, or they can be added to the running sum of Fourier coefficients to be output during Fourier mode.

3.1. Derivation of power sums

Given that the input sequence to the FFT algorithm is comprised only of real numbers, the output coefficient sequence will only be half the length of the input sequence; so the upper boundary on the sums is N/2. There was also a DC offset added to the original waveforms when they were transformed to be between 0 and 5 volts; therefore this DC offset must not be added into the following calculations, causing the lower bound of the sums to be 1 instead of 0.

The following are the sums used in the RMS and THD equations for voltage and current:

(1) $X_n = R_n + j\, I_n$

(2) $X^2\text{rms\_sum} = \sum_{n=1}^{N/2} R_n^2 + I_n^2$

(3) $X^2\text{fundamental} = R_1^2 + I_1^2$

The following is the derivation of the sums used to calculate all of the power quantities:

(4) $V_n = A_n + j\, B_n$

(5) $I_n = C_n + j\, D_n$

(6) $S = V\, I^* = P + j\, Q$

Combining equations 4, 5, and 6 yields the following two equations:

(7) $P\_sum = \sum_{n=1}^{N/2} A_n * C_n + B_n * D_n$

(8) $Q\_sum = \sum_{n=1}^{N/2} B_n * C_n - A_n * D_n$

3.2. DSP to IMP conversion

For normal mode the DSP numbers are 56 bit fixed point fractional numbers with an epsilon ($\mathcal{E}$) of 2^{-23}, while the IMP floating point numbers are 32 bit numbers following the IEEE floating point standard. Since the IMP data bus is only 16 bits, the DSP numbers must be written to the IMP in 16 bit pieces. The first word of the IMP is written with the highest 16 bits of the DSP number, then the second word is written with the next 16 bits of the DSP number. The third IMP word is always written with an upper byte of 0 and a lower byte containing the next 8 bits of the DSP number; and the final IMP word is written with the remaining 16 bits of the DSP number. Now that the DSP number has been written to the IMP's memory, it is ready to be converted to an IMP float.

The DSP number now occupies four consecutive words (16 bits each) of IMP memory. In order to perform the conversion, these four words are cast as two unsigned long integers (32 bits each): DSP_number_high, which is the higher order portion, and DSP_number_low, which is the lower order portion. Since some of these DSP numbers can be negative (the reactive powers), this condition must be tested for and one of two different methods of conversion must be chosen based on this test. The test is performed by comparing DSP_number_high to 2^{31} (80000000h) in order to see if the most significant bit is set. This bit corresponds to the most significant bit of the original DSP number, the sign bit; so if this bit is set, the DSP number is negative, otherwise it is positive. Once the sign of the DSP number is known, one of the following methods of conversion can be used.

The following is the conversion for a positive number during normal mode: IMP_number = DSP_number_high $* \mathcal{E}$ + DSP_number_low $* \mathcal{E} * 2^{-24}$

The following is the conversion for a negative number during normal mode: IMP_number =

$-((2^{32} - \text{DSP\_number\_high} - 1) * \mathcal{E}$

$+ (2^{24} - \text{DSP\_number\_low} - 1) * \mathcal{E} * 2^{-24})$

For both conversions, the higher portion of the DSP number is multiplied by $\mathcal{E}$ since this is the basic unit of increment for a 24-bit DSP number. The lower portion of

the DSP number is multiplied by $\varepsilon * 2^{24}$ because the lower 24 bits of a 52-bit DSP number are the low order expansion bits, used to give the DSP number more accuracy; so this portion must be given less weight when added to the higher portion of the DSP number in order to obtain the IMP number. For the negative conversion, the DSP number is stored in two's compliment form; so a two's compliment subtraction must be performed in order to convert the two's compliment number into a straight binary number before the above mentioned multiplications. Also for the negative conversion, all of the calculations are performed using positive numbers; so the final result must be negated before being written as an IMP float. Figure 7 details the DSP to IMP conversion during normal mode.

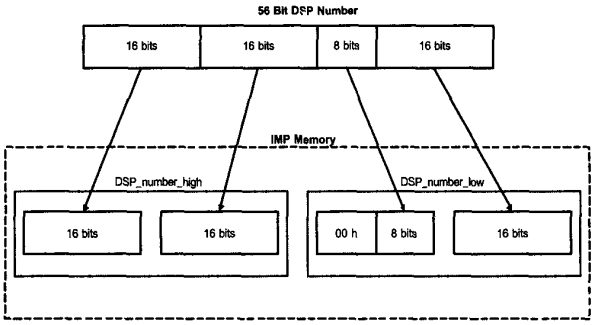

Figure 7. DSP to IMP conversion during normal mode.

Positive Example

DSP number = 3.52 = 01C28F5C28F5C2 h
DSP_number_high = 01C28F5C h
DSP_number_low = 0028F5C2 h
IMP_number = 01C28F5C h * 2^{-23} + 0028F5C2 h * 2^{-23} * 2^{-24} = 3.52

Negative Example

DSP number = -0.834 = FF953F7CED9168 h
DSP_number_high = FF953F7C h
DSP_number_low = 00ED9168 h
IMP_number = -((2^{32} - FF953F7C h - 1) * 2^{-23} + (2^{24} - 00ED9168 h - 1) * 2^{-23} * 2^{-24}) = -0.834

For Fourier mode the DSP numbers are only 32-bit fixed point fractional numbers, since the lower 24 expansion bits are not used. These numbers are transferred to the IMP in two 16-bit writes and only occupy 32 bits, or one unsigned long integer in IMP memory. The conversion for these coefficients is the same as for the higher portion of the before mentioned conversion.

The following is the conversion for a positive number during Fourier mode: IMP_number = DSP_number * ε

The following is the conversion for a negative number during Fourier mode: IMP_number = -((2^{32} - DSP_number - 1) * ε)

3.3. Power Calculations

Once the DSP sums have been converted to IMP floats in normal mode, they are then ready to be used in the power calculations. Since the original voltage and current signals were scaled down by the potential transformers and current transformers, respectively, the resulting power calculations must be scaled up before being displayed to account for the initial down scaling. Fortunately this is easy to do, and only requires multiplication by a constant called the gain factor (GF). Since both the voltage and current were scaled down by different factors, there are two GFs, one for voltage (GF_v) and one for current (GF_i).

The following are the equations for the GFs, where $Vrms_{max}$ is the maximum rating of the potential transformers, $Irms_{max}$ is the maximum rating of the current transformers, Sum_fac is the constant pulled outside of the summations, FFT_fac is due to the 256 point FFT, and n is the number of bits in the A to D converter:

(9) $GF_v = Vrms_{max} * 2 * \sqrt{2} / FFT\_fac / Sum\_fac / 2^n / \varepsilon$
$= 180 * 2 * \sqrt{2} / 128 / \sqrt{2} / 2^{12} / 2^{-23} = 5760$

(10) $GF_i = Irms_{max} * 2 * \sqrt{2} / FFT\_fac / Sum\_fac / 2^n / \varepsilon$
$= 7.4 * 2 * \sqrt{2} / 128 / \sqrt{2} / 2^{12} / 2^{-23} = 236.8$

The following are the calculations for RMS and THD (See equations 2 and 3 for reference):

(11) $Xrms = \sqrt{\ } X^2rms\_sum * GF_x$

(12) $\%THD_x = \sqrt{\ } (X^2rms\_sum - X^2fundamental) / \sqrt{\ } X^2fundamental * 100$

The following is the derivation of the power calculations (See equations 7 and 8 for reference):

(13) Real Power = P = P_sum * GF_v * GF_i
(14) Reactive Power = Q = Q_sum * GF_v * GF_i
(15) Apparent Power = U = Vrms * Irms
(16) Phasor Power = S = $\sqrt{\ } (P^2 + Q^2)$
(17) Distortion Power = D = $\sqrt{\ } (U^2 - S^2)$
(18) Power Factor = PF = P / U

3.4. Fourier Coefficient Calculations

Once the Fourier coefficient sums have been converted to IMP floats in Fourier mode, they must first be divided by 128 to average them over 128 cycles, before they are properly scaled. To cut down on the number of floating point multiplications, the DSP to IMP conversion is combined with the averaging over 128 cycles and the scaling in the actual program.

The following are the scale factors (SF) for the Fourier coefficients:

(19) $SF_v = Vrms_{max} * 2 * \sqrt{2} / 2^n / \mathcal{E}$

$= 180 * 2 * \sqrt{2} / 2^{12} / 2^{-23} = 1042671.37527$

(20) $SF_i = Irms_{max} * 2 * \sqrt{2} / 2^n / \mathcal{E}$

$= 7.4 * 2 * \sqrt{2} / 2^{12} / 2^{-23} = 42865.37876$

4. Experimental Results

The system was first tested with a phase controlled tungsten load consisting of a 40-watt lamp connected to a dimmer switch. With the light bulb turned completely on, the meter read approximately 40 W real power, 0 Var reactive power, and 1.0 power factor. As the bulb was dimmed, the real power decreased, the reactive and distortion powers increased, and the power factor decreased; all of which are to be expected when dimming a light bulb.

Next, a nonlinear load (industrial drill) was used in testing the system. Figure 8 and Figure 9 show the voltage and current waveforms, respectively, for this test load.

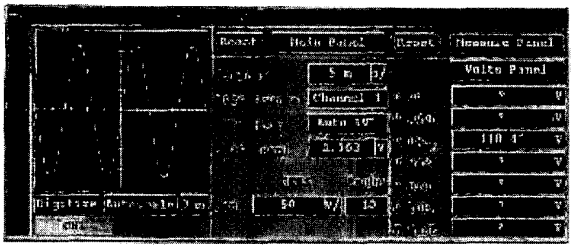

Figure 8. Voltage waveform for the industrial drill.

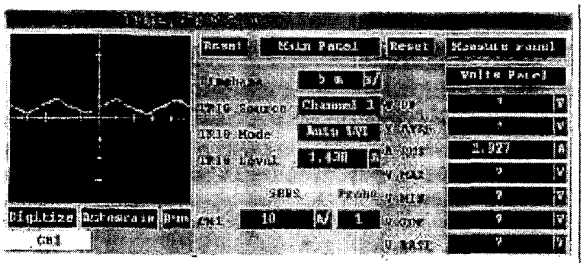

Figure 9. Current waveform for the industrial drill.

Since the drill uses only one phase, the single phase voltage was connected to all three of the phase voltages of the power meter; and the single phase current was connected to all three of the phase currents and to the neutral current of the power meter. Therefore all three phases should get approximately the same readings.

Figure 10 shows the meter output, during normal mode, for the industrial drill. As expected, the measurements for all three phases are approximately the same. Since this is a nonlinear load the distortion power is significant, as the harmonic distortion for the current is about 18%.

IaRMS	=	2.1629 A	VaRMS	=	120.8234 V
IbRMS	=	2.1556 A	VbRMS	=	120.6043 V
IcRMS	=	2.1677 A	VcRMS	=	120.4683 V
InRMS	=	2.1570 A			
IaTHD	=	17.9211 %	VaTHD	=	5.6506 %
IbTHD	=	17.9718 %	VbTHD	=	5.7492 %
IcTHD	=	18.1288 %	VcTHD	=	5.7354 %
InTHD	=	17.9305 %			
Ua	=	261.3326 VA	Sa	=	257.7995 VA
Ub	=	259.9695 VA	Sb	=	256.4421 VA
Uc	=	261.1385 VA	Sc	=	257.6011 VA
Pa	=	249.5029 W	Qa	=	64.8756 Var
Pb	=	248.0834 W	Qb	=	64.9399 Var
Pc	=	249.2341 W	Qc	=	65.1207 Var
Da	=	42.8272 VA	PFa	=	0.9547
Db	=	42.6799 VA	PFb	=	0.9543
Dc	=	42.8365 VA	PFc	=	0.9544

Figure 10. Normal mode sample output data.

5. Conclusions

The DSP, CISC, and RISC processors each contribute to the performance of the 256 point per cycle, three-phase Fourier based power meter. The limiting factor to increasing the sampling rate in this application is the fixed point CISC processor, which required 128 power system cycles per update.

Averaging the power summations over 128 cycles lessons the effectiveness of measuring brief electromagnetic phenomenon. The solution to this problem would be to replace the 68000 portion of the IMP with a microprocessor containing a floating-point coprocessor. This would allow the power calculations to be performed every power cycle, and would alleviate the negative effects that averaging induces on the resulting power measurements.

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