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Analysis of Chip-level EMI using Near-Field Magnetic Scanning

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Abstract— Integrated circuits (ICs) are often a significant source of radiated energy from electronic systems. Well designed ICs maintain good control of the currents that they generate. However, poorly designed ICs can drive high-frequency noise currents onto nominally low-frequency input and output pins. These currents can excite unintentional radiating structures on the printed circuit board resulting in radiated emissions that are difficult or expensive to control. This paper discusses the use of magnetic near-field scanning techniques to measure the current distribution in IC packages. This technique is applied to common ICs including a clock driver, a memory module and a field programmable gate array (FPGA). Results show that near-field magnetic scanning is an effective tool for investigating chip-level EMI problems.

Keywords-IC; VLSI; EMI; Near-field Magnetic Scanning

I. INTRODUCTION

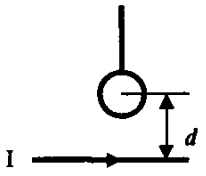
As ICs continue to grow in size and power consumption, they play a more important role in determining the electromagnetic compatibility of the electronic systems in which they are used. In general, IC structures and packages are electrically small and do not radiate energy efficiently by themselves. The RF currents generated by ICs usually have to drive a bigger structure on or attached to the printed circuit board to radiate significantly. However, noise coupled from ICs to resonant structures on or near the board is a common problem in high-speed digital systems. Noise can be coupled via electric or magnetic fields from the IC or it can be conductively coupled directly to the board through signal or power pins.

Well designed ICs are much less likely to produce unwanted noise than poorly designed ICs. However, it can be difficult to determine the difference between a good design and a bad design using traditional methods of characterizing integrated circuit devices.

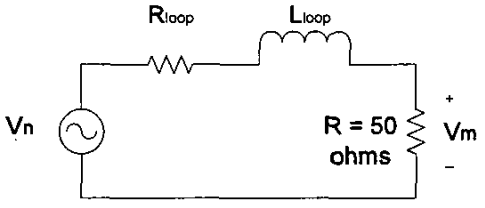
This paper discusses the application of near-field magnetic scanning techniques to determine the common-mode current distribution on IC pins and inside the package. A few sample devices are evaluated to demonstrate how magnetic field scans can be an effective tool for identifying EMI problems attributable to poor IC designs.

II. MEASUREMENT TECHNIQUE

The magnetic field (H-field) near a current source is proportional to the magnitude of the current; thus the current direction and magnitude can often be determined by measuring the H-field near the current. The H-field can be measured using a small loop probe and an appropriate instrument, such as an oscilloscope or spectrum analyzer [1, 2, 3]. Fig. 1 illustrates the magnetic field loop probe and its equivalent circuit model.



(a) Measurement probe position



(b) Circuit model

Fig. 1. Probe position and circuit model.

In Fig. 1(a), a small loop is located above the current source to measure the H-field generated by the current. The distance between the center point of the loop and the current source is *d*. In Fig. 1(b), V_n is the voltage induced in the loop by the H-field, R_{loop} is the resistance of the loop (which is usually negligible), L_{loop} is the inductance of the loop, the 50-ohm resistor represents the input impedance of the instrument, and V_m is the voltage measured by the instrument. If the presence of the probe does not significantly disturb the field, the H-field generated by a thin-wire current source is given by:

$$H \approx \frac{I}{2\pi d} \quad (1)$$

And the voltage induced in the loop, V_n, is approximately:

$$V_n \approx \omega\mu HA \approx \frac{\omega\mu AI}{2\pi d} \quad (2)$$

where, A is the area of the loop and ω is the angular frequency of the current. As long as the reactance of the loop inductance is much smaller than 50 ohms, the measured voltage, V_m, is equal to V_n, which is proportional to the source current, I. For example, a loop with a diameter of 1 mm made of wire with a diameter of 0.25 mm has an inductance of about 1 nH. The inductive reactance of the loop is small relative to the 50-ohm resistance of the measurement equipment and can be neglected at frequencies up to 1 GHz with an error less than 1%. Smaller loops have higher spatial resolution. However, the loop must be large enough to provide an adequate signal-to-noise ratio. Generally speaking, the small probes used for IC package scanning do not disturb the magnetic fields enough to alter the measurement [4]. It is possible, however, to compensate for the probe-induced disturbance if higher accuracy is desired [5]. In the work presented here, a small probe with a loop diameter of about 1.2 mm and a wire diameter of 0.25 mm is used.

In our experiments, the H-field over an IC device was measured by scanning the surface of the device using an automated field scanner. The scanner measures the real-time signal using an appropriate instrument. Measured data is simultaneously downloaded and saved in the computer that controls the scanner. The data is saved in a matrix format where each element of the matrix corresponds to a location over the IC device being measured. The H-field at different locations can be measured simultaneously using several loop probes if the correlation between the current at different locations is of interest.

III. Experimental Results

The current distributions of several chips with different functionalities were measured using the near-field magnetic scanner described in the previous section. The purpose of these measurements was to identify current distributions that were an indication of radiated EMI problems. Fig. 2 shows a photo of typical measurement setup.

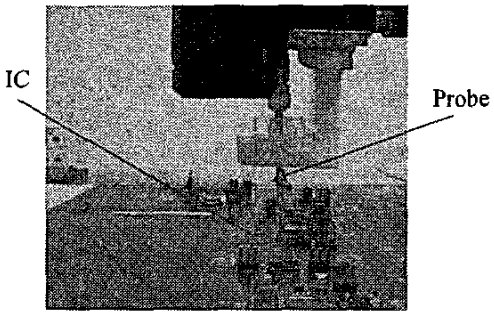


Fig. 2. Measurement setup.

The automated field scanner was connected to an HP 8563E spectrum analyzer and used to measure the near-magnetic field over various ICs in the frequency domain. The height of the probe over the chip was kept unchanged while the probe was scanned in a horizontal plane parallel to the chip package surface. Height was typically less than 1 mm. The magnetic field components were measured in two orthogonal directions by orienting the loop probe in two orthogonal polarizations at each measurement point. The total field was calculated as the root mean square of the two field components. Color was used to represent the relative magnitude of the field on a two-dimensional map of the IC package under evaluation.

We measured the current distribution of several ICs with different functionalities including several clock generators, memory devices, and an FPGA. The measurement results are summarized below.

A. Clock generator

One of the devices evaluated was a clock generator for personal computer motherboards. This IC has 56 pins and can generate many different clock signals simultaneously including,

- differential current-mode clock pairs
- 66.67 MHz 3.3 V CK66 clock outputs
- 33.3 MHz 3.3 V PCI clock outputs
- 3.3 V memory reference clock outputs
- 48 MHz 3.3 V CK48 clock outputs
- buffered copies of the crystal reference.

Fig. 3 shows the shows the magnetic field scan just above the surface of the clock generator IC. The figure shows that this IC generates a relatively strong common-mode current that flows from the upper left corner of the package to the lower right corner. This current is drawn from the power/ground plane pair on the print circuit board. Although the plane pair is solid beneath the clock driver package, and although there are many V_{SS} and V_{DD} pins on both sides of this device, most of the current flows between one particular V_{SS} pin and one particular V_{DD} pin on opposite sides of the package. The magnetic flux generated by this current loop is capable of driving common-mode currents onto cables and/or enclosures attached to the plane pair [6].

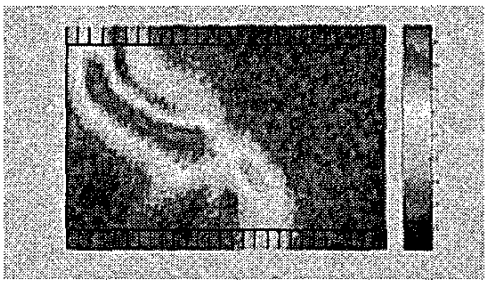


Fig. 3. H-field scan above the surface of a clock driver

Various attempts to reduce this current were unsuccessful until the V_{DD} pin on the upper left corner of the package was disconnected. Fig. 4 shows the magnetic scan obtained with the disconnected pin. The common mode current now flows across the chip from the lower left corner of the package to the lower right. Disconnecting the V_{DD} pin had no other obvious effect on the chip's operation.

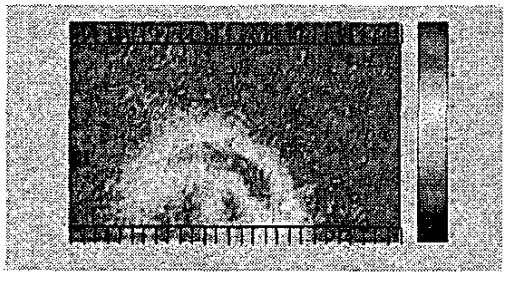


Fig. 4. Magnetic scan when VDD pin on the upper left corner was disconnected.

Normally, we would expect the currents supplying a particular clock to be drawn from the nearest V_{SS}/V_{DD} pin pair. It is not clear why this device behaves this way because we have no detailed information about its design. This behavior was observed in other samples of the same clock driver, but was not observed in other clock drivers. This common mode current could present significant EMI challenges for any product that uses this device. The results suggest that improvements in the VLSI layout should be made to reduce the potential costs of suppressing EMI problems at the system level.

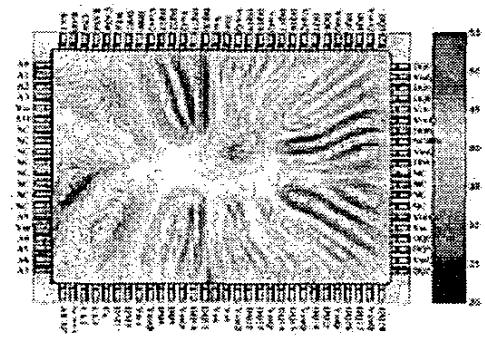
B. *Memory chip*

Fig. 5 shows a magnetic near-field scan for an RDRAM memory device. The device was clocked at 200 MHz and the magnetic field was measured at 200 MHz. The device was measured while executing read and write operations. As the figure illustrates, the current patterns are very different depending on the function of the IC. The write operation is much quieter than the read. However, in both cases the strongest currents flow in the V_{CC} and GND pins. The currents in these nominally low-frequency pins are significantly stronger than the currents in the clock and data pins. Modifying the chip and/or package design (e.g. to reduce shoot-through current or provide decoupling capacitance) might significantly reduce these noise currents without adversely affecting signal integrity.

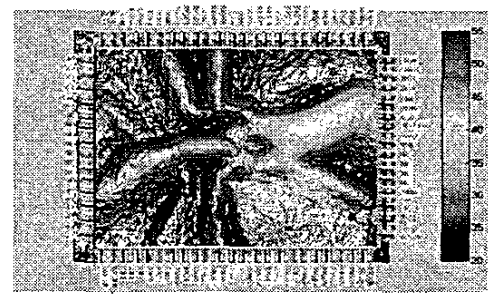
C. *Xilinx Spartan FPGA*

Field Programmable Gate Arrays (FPGAs) present a unique opportunity to investigate chip-level EMC. These devices can be reconfigured at the chip level without changing the package parameters. EMC measurements of the FPGA made before and after changes in the chip's circuitry can provide information on chip-level effects.

Fig. 6 shows the magnetic-field distribution over a Xilinx Spartan-XSC05 FPGA. A simple 8-bit microprocessor was implemented inside the FPGA, which continuously executed a program loop during measurement. While I/O lines were being driven by the FPGA, they were not connected for this measurement. The plot indicates that high-frequency currents are pulled through the power/ground pins and that these currents do not always return to the board through adjacent pins. However unlike the clock driver presented earlier, this current path in the FPGA was determined primarily by the manner in which the external power connections were made.



(a)



(b)

Fig. 5. H-Field surface scan of RDR memory module. (a) Reading (b) Writing

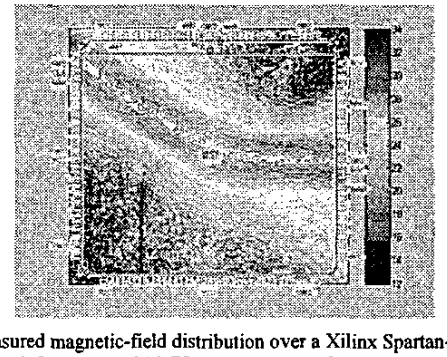


Fig. 6. Measured magnetic-field distribution over a Xilinx Spartan-XCS05 FPGA (Clock frequency - 24 MHz; Measurement frequency - 72 MHz).

Fig. 7 shows another magnetic-field distribution over a Xilinx Spartan-XCS10 FPGA. In one measurement, a simple 8-bit microprocessor was implemented in the FPGA. In the other measurement, additional idle circuits were implemented along with the microprocessor. The I/Os were loaded with 100-pF capacitors. As the figure shows, a significant difference can be observed between the two designs, especially in the I/O lines. The presence of the additional circuitry reduces the noise on the I/O signals. This is possibly due to the inherent decoupling capacitance provided by connecting the idle gates in the second design. Investigation of this phenomenon is continuing.

IV. SUMMARY

ICs are often the primary source of radiated emissions from the electronic products that use them. Near magnetic field scans provide information about the current distributions within IC packages. Information about the current distribution can help EMC engineers to track down problems with an IC design that contribute to system-level EMC problems.

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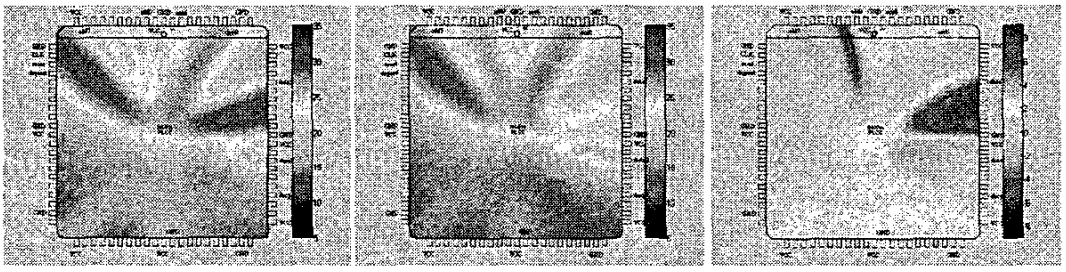

Fig. 7. Magnetic field scan over an FPGA (Clock frequency - 24 MHz; Measurement frequency - 72 MHz)