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Jonathan W. Kimball
Missouri University of Science and Technology, kimballjw@mst.edu

Patrick L. Chapman

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Evaluating Conduction Loss of a Parallel IGBT-MOSFET Combination

Jonathan W. Kimball, *Member*   Patrick L. Chapman, *Member*

Grainger Center for Electric Machinery and Electromechanics
University of Illinois at Urbana-Champaign
1406 W. Green St., Urbana, IL 61801 USA

Abstract – **A variety of power devices are available to designers, each with specific advantages and limitations. For inverters, typically an IGBT combined with a p-i-n diode is used to obtain high current density. Recent developments in high-voltage MOSFETs support other alternatives. For example, a MOSFET can be paralleled with an IGBT to reduce losses at low currents, while the IGBT carries the load at high currents. The current work evaluates conduction losses in this configuration, showing applicability to generic inverters.**

I. INTRODUCTION

In power electronics, different power switch types generally have well-known advantages and disadvantages in terms of switching speed, switching loss, conduction loss, thermal response, etc. For a given application, there are generally accepted solutions that are "best" by some measure. As device technology changes, the designer should re-evaluate the underlying assumptions. Designers should also consider paralleling devices of different types in order to realize the advantages of each type.

An example of a compound device that has received little attention is a parallel combination of a MOSFET and an IGBT. Some work has been done that focuses on switching advantages. The combination was originally proposed in [1] in the context of an active-clamp flyback converter. Later, an application specific integrated circuit (ASIC) was developed to manage the switching timing [2]. Paralleling is briefly discussed in [3] in regard to analyzing the switching transients of the parallel combination. These works emphasize the relative turn-off characteristics of an IGBT versus the IGBT/MOSFET pair.

IGBTs are the workhorse of power converters from 300 V to a few kV. With the gate characteristics of a MOSFET and conduction characteristics of a BJT, high current density can be achieved with moderate gate drive complication. Unfortunately, IGBTs have two disadvantages: unidirectional current flow, and high losses at low currents. Both result from the bipolar nature of the device.

MOSFETs have long been limited to low-voltage or low-current applications. Traditional high-voltage (greater than 100 V) technologies require silicon area that increases as the square of rated breakdown voltage. Newer technologies [4] change the silicon area requirement to a linear relationship with breakdown voltage. This has enabled high-voltage MOSFETs with much greater current density. These new technologies maintain the inherently faster switching of a MOSFET while approaching IGBT current density.

This work uses the latest MOSFET technology to examine potential improvements in conduction loss. In a typical inverter, conduction loss is about half of the total thermal load that needs to be managed. IGBTs and diodes can be modeled as a constant voltage plus some small resistance, $V_{CE} = V_{on} + R_{on}I_C$. MOSFETs, being majority-carrier devices, are modeled as simply a resistance, $V_{DS} = R_{DS,on}I_D$. Below some current, the MOSFET on-state voltage will be less than an IGBT of equivalent size. When the devices are used in parallel, the on-state voltage is reduced at all currents, but particularly at low current. In an inverter producing ac current, and particularly an ASD operating over a wide range of loads, the devices spend much of the time conducting low currents. Additionally, for appliance motor drives, light-load efficiency is an important measure.

In this paper we present some modeling results of various combinations to show possible applications of the parallel combination. Then, we show test results from several experiments. Finally, we summarize with conclusions. We show that there are possible benefits to using a parallel combination, particularly when heat-sink cost or physical size is a priority.

II. MODELING

A MOSFET alone, conducting forward current, is simply modeled as an on-state resistance. This work uses an SPP11N60C3IN device from Infineon with a measured $R_{DS,on}$ of 290.9 mΩ. Naturally, at high current the device begins to saturate and incremental resistance increases. MOSFETs also display a positive temperature coefficient.

An IGBT alone, which only conducts in the forward direction, is modeled as an on-state voltage plus an on-state resistance. This work uses an HGTP12N60B3 device from Fairchild with a measured V_{on} of 1.200 V and R_{on} of 55.6 mΩ. This resistance is maintained up to currents well beyond the usable operating range. In general, V_{on} will have a negative temperature coefficient and R_{on} will have a positive temperature coefficient, resulting in an overall positive temperature coefficient at high currents.

Fig. 1 shows a set of *i-v* curves that illustrates the effect of paralleling an IGBT with a MOSFET, as measured on a TEK371 curve tracer. Five different combinations are shown: each device by itself, the FET-IGBT combination, a FET-FET combination, and an IGBT- "half-FET" combination (that is, a FET that has about half the current capacity of the others). The "1/2FET+IGBT" combination is calculated while the rest of the curves are direct measurements.

The MOSFET has lower losses for currents less than 4.7 A, then the IGBT becomes the preferred device. When connected in parallel, a complicated curve emerges. The MOSFET carries the burden until its forward voltage is equal to the IGBT on-state voltage, placing a corner at (V_x, I_x) given by:

$$V_x = V_{on}$$
$$I_x = \frac{V_{on}}{R_{DS,on}} \tag{1}$$

For currents greater than I_x, the IGBT carries the majority of the load, but the MOSFET is still active. Thus the *incremental* resistance is determined by the parallel combination of the two device resistances and the equivalent on-state voltage is determined by the requirement to pass through (V_x, I_x):

$$R_{on,new} = R_{on} \| R_{DS,on}$$
$$V_{on,new} = \left(R_{DS,on} - R_{on,new} \right) I_x \tag{2}$$

For the devices under study, $R_{on,new}$ is 51.0 mΩ and $V_{on,new}$ is 1.012 V.

Across the load range, the parallel combination is superior to the IGBT alone and at least equal to the MOSFET alone. The reverse characteristics show similar improvements. MOSFETs have the advantage of being bidirectional devices. An IGBT must be paired with an appropriate diode (free-wheeling diode, FWD) in order to
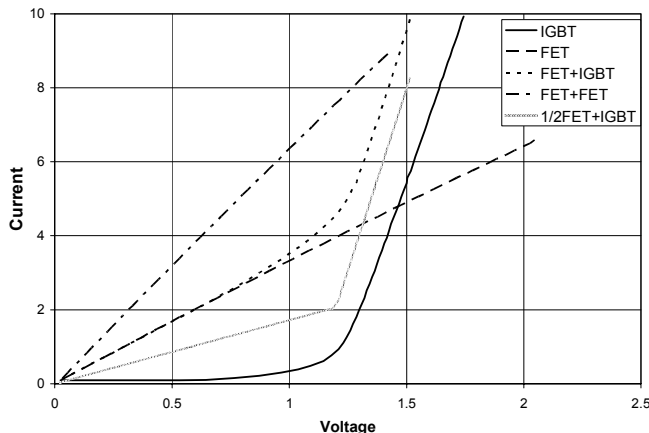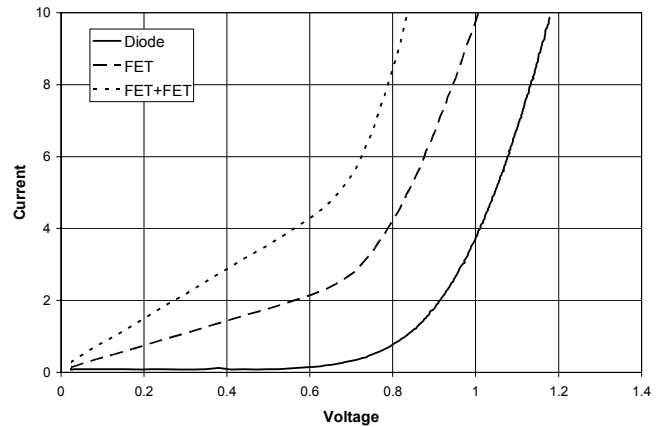

Fig. 2: Reverse Characteristics of Relevant Combinations

carry ac current. This work uses one element of an MUR3060PT, with V_{on} of 0.869 V and R_{on} of 33.3 mΩ. A MOSFET does not need to be paired with a diode, but instead contains an intrinsic diode. Its reverse characteristic shown in Fig. 2 resembles the FET+IGBT forward characteristic. It was measured to have a resistance of 290.9 mΩ for currents less than 2.6 A, identical to the forward $R_{DS,on}$, then an on-state voltage of 0.666 V plus a resistance of 34.8 mΩ for higher currents. Again, one would expect a negative temperature coefficient for all characteristic voltages and a positive temperature coefficient for all resistances.

One other combination was explored: two MOSFETs in parallel. Ordinarily, one would not design a module using small paralleled MOSFETs, but would instead use a single MOSFET of double the size. Showing how far MOSFET technology has progressed, the dual MOSFET curve crosses the IGBT curve, but at quite a high current (greater than 10 A). At this time, there is no conclusion as to which combination is the least expensive and uses the least silicon.

Full optimization has not yet been investigated. Instead, devices were chosen to be similar in size. The MOSFET and IGBT chosen are both in a TO-220 package and have similar current ratings. The MUR3060PT is a TO-218 that contains two elements; experiments and measurements use only one element, with a 15 A rating. It should be clear, however, that any MOSFET added to an IGBT will have lower conduction losses over some range of currents. As an example, an equivalent, hypothetical MOSFET of half the size was placed in parallel with the same IGBT, with forward characteristics calculated shown on Fig. 1 as "1/2 FET + IGBT." Now the IGBT carries more of the load and the total silicon used is less, since the diode has been eliminated. Naturally, full optimization must consider performance across temperature; all experiments and measurements were performed at 22°C.

To be useful, a device needs to be evaluated in a target application. For a simple device (IGBT, MOSFET, or diode) used in a generic inverter, closed-form solutions for power dissipation exist [5]. A compound device requires more

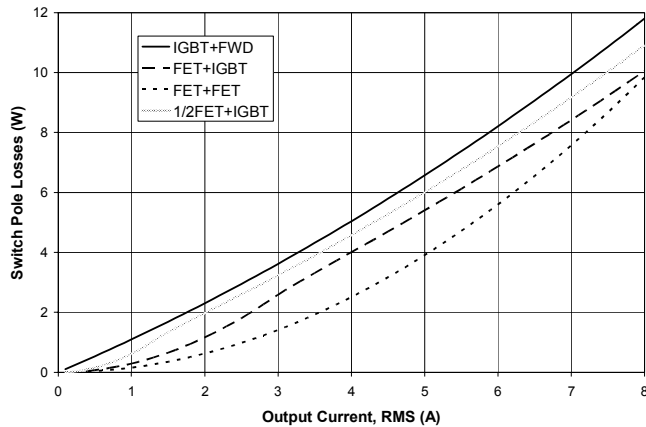Fig. 1: Forward Characteristics of Various Device Configurations
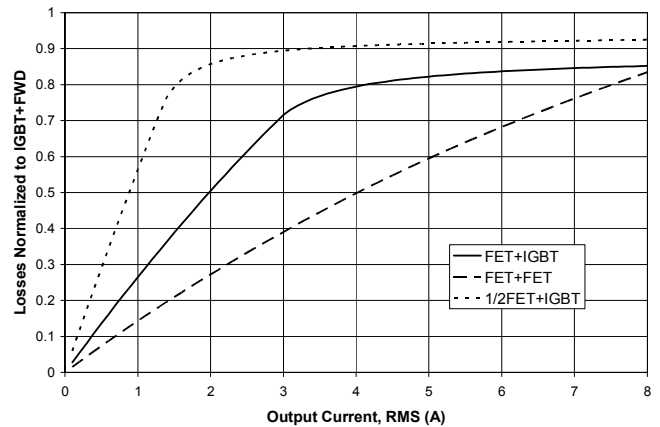
Fig. 3: Conduction Losses in an Inverter

Fig. 4: Conduction Losses in an Inverter, Normalized to IGBT+FWD

sophisticated analysis, or preferably, numerical integration. Conduction loss was calculated in Mathcad using the inverter parameters of Table 1 for all of the above combinations. Fig. 3 shows the estimated conduction loss in watts. To more directly show the advantage, conduction losses are normalized to IGBT+FWD losses in Fig. 4. While the efficiency improvement is important, perhaps of more interest to the designer is the loss reduction. Power dissipation in the switching devices translates directly into heat sink size and other parameters of the thermal management system. By reducing the thermal load due to conduction loss by 15% to 60% over the usable range, the burden on the system design is greatly reduced.

It is important to recognize that although this work focuses on conduction loss reduction, one would expect switching losses to be at least equivalent. The intrinsic diode of a MOSFET is similar to a typical FWD from the perspective of stored charge and reverse-recovery current. By adjusting the relative timing of the gate signals, it is possible to force the IGBT to do all of the commutation. One would expect that adjusting the relative timing in other ways would bring out more of the MOSFET characteristic so that switching loss would decrease. By proper device selection and system design, overall losses in an inverter can be decreased.

Table 1: Parameters for Inverter Calculation

Parameter	Value
Bus Voltage	300 V
Carrier Frequency	2.5 kHz
Output Frequency	60 Hz
Modulation Depth	1.15
Third Harmonic	16.7%
Power Factor	0.85

III. EXPERIMENTAL VERIFICATION

To verify loss reduction in a power converter, a buck converter was built. A three-phase inverter is ultimately built of multiple buck converters operated over a range of duty cycles and currents. The efficiency of an inverter is difficult to measure electrically due to bandwidth and dynamic range requirements. By testing a simple buck converter over a range of current and duty cycle, predictions of inverter performance can be made.

There are many loss mechanisms in a buck converter. Switching loss, inductor core loss, and bus capacitor losses are all proportional to voltage in some way. For example, capacitors rated for lower voltage have lower equivalent series resistance (ESR) than high voltage capacitors of similar size. Other power measurements, such as input and output power, are also proportional to voltage. Conduction loss is the only term that is proportional only to current. So by operating the converter at a greatly reduced voltage while maintaining the current level, conduction losses become the dominant loss term. Measurement fidelity is greatly improved, since the total power being processed is greatly reduced.

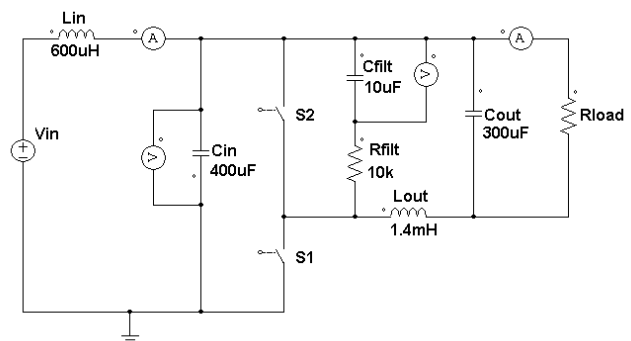Notice the locations of the voltmeters and ammeters in
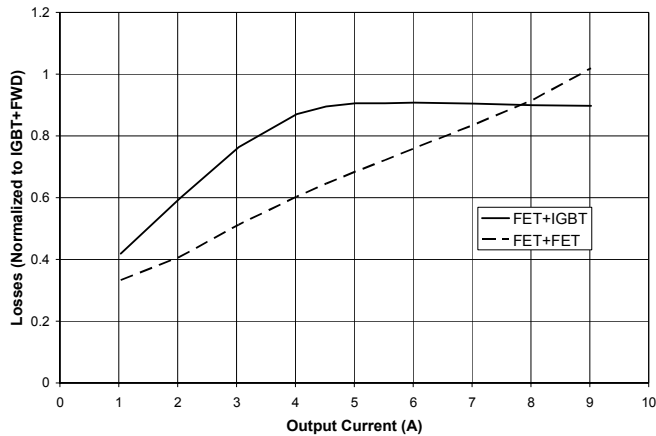

Fig. 5: Experimental Circuit

Fig. 6: Experimental Results, Losses Normalized to IGBT+FWD,
70% Duty Cycle

Fig. 5. The input current is heavily filtered by *Lin* to ensure that the ammeter's finite bandwidth is irrelevant. Similarly, the output voltage is measured as close to the switching pole as possible, with filtering to yield a dc value (the pole is at 1.6 Hz). This location removes any losses in the filters from consideration. *Rload* was swept through a wide range to test the system from 1.0 A output to 9.0 A output. *Vin* was set at approximately 20 V. Switching frequency was set at 5 kHz—high enough that the filters work, but low enough that switching effects are not significant.

Three configurations were tested. The first was the standard solution to the inverter problem, an IGBT for S1 and a diode for S2 (denoted IGBT+FWD). The second was the proposed configuration of a MOSFET in parallel with an IGBT (denoted FET+IGBT) for both S1 and S2. The third used two MOSFETs in parallel for both S1 and S2, the equivalent of using large MOSFETs (denoted FET+FET). For configurations that used a MOSFET for S2, the switches were operated as a synchronous rectifier with approximately 1.5 μs dead-time, as would commonly be done in an inverter. For parallel devices, individual gate resistors were used but no relative timing adjustment was done.

Results are shown in Figs. 6-7. Fig. 6 mirrors Fig. 4, with losses normalized to IGBT+FWD measured losses. At low currents, the FET-based configurations are significantly better. The knee in the FET+IGBT loss curve approximately correlates to the knee in the *i-v* characteristic. Fig. 7 mirrors Fig. 3, showing actual losses. Notice the quadratic nature of the FET+IGBT and FET+FET curves at low current, with FET+IGBT changing to a more linear characteristic above the knee. This experiment validates the contention that conduction loss can be improved in inverters, especially at light load, by replacing the FWD with a MOSFET.

IV. CONCLUSIONS

Modeling and experimentation demonstrate that conduction losses can be reduced in inverters by replacing existing FWDs with MOSFETs of appropriate ratings. The difference is particularly dramatic at low currents. Performance at light load is improved dramatically, and the reduced losses near zero crossing improve performance at all loads.

The MOSFET chosen here is of a similar rating as the IGBT used. More work is necessary to optimize the relative sizing. One would expect that there is a minimum size to each in order to properly commutate the current, and that a MOSFET of any size will improve conduction losses. It is believed that the optimal combination would be a similar amount of total silicon as is currently used in an IGBT/FWD module or co-pack.

The difference in system efficiency is modest. Most inverter designs are not driven by efficiency, though. Rather, the emphasis is on cost minimization, which correlates to total silicon size and total heat sink size. Replacing a FWD with a MOSFET of equal rating results in a significant reduction in conduction losses. It should be possible to reduce system costs by using the FET+IGBT combination mounted on a smaller heat sink (or of a less expensive type, or with a smaller fan).

Further work is necessary to evaluate the switching performance. From [1], one would expect switching loss to be improved by using a MOSFET to commutate current. This presents a challenge in gate drive optimization by introducing several more variables to the system. The simplest solution is to tie the gates of the MOSFET and IGBT together, but more sophistication in relative timing may be necessary to realize full benefits.

Finally, we should recognize that the parts used in these experiments were not designed for the proposed configuration. It may be possible to adjust the optimization of the silicon design to maximize system benefits. For example, MOSFETs can be designed with slightly higher on-state resistance but better switching, while IGBTs can be designed with lower conduction loss and higher switching
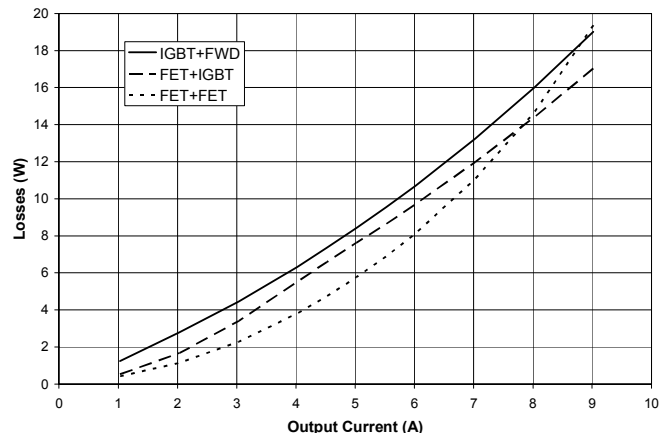

Fig. 7: Experimental Results, Actual Power Loss, 70% Duty Cycle

loss. The combination will still have reduced conduction loss and may see benefits in switching loss, fundamentally changing the trade-offs in silicon design.

V. ACKNOWLEDGEMENT

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