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Chang Qian

Stan Atcitty

Mariesa Crow
Missouri University of Science and Technology, crow@mst.edu

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A Multi-processor Control System Architecture for a Cascaded StatCom with Energy Storage

Chang Qian and Mariesa L. Crow
Department of Electrical and Computer Engineering, University of Missouri-Rolla, Rolla, MO 65409-0040

Stan Atcitty
Energy Storage Systems Analysis & Development, Sandia National Laboratories, Albuquerque, NM 87185

***Abstract* -- This paper presents a multi-processor control system for a general purpose five-level cascaded inverter for real time power system applications. Practical design considerations for the digital controller architecture as well as the power converter are discussed and a 3 kVA laboratory prototype is presented. As a case study, A StatCom with battery energy storage was implemented on this multi-processor controlled inverter system. To eliminate the troublesome PI parameter tuning and the limitation of small signal models, which exist in conventional control for StatComs, a new and simple control method based on large signal model was designed to realize four-quadrant power injections into a grid. Experimental results are provided to support the proposed concept.**

I. INTRODUCTION

Recent studies have shown that many bulk power system instabilities can be mitigated by incorporating modest power injection from an energy storage system (ESS) into a StatCom [1]. One drawback to the StatCom/ESS, however, is that the size of the storage systems for FACTS integration, particularly batteries, may be too high for practical use in transmission level applications. Large battery systems tend to exhibit charge instability when numerous cells are placed in series. One approach to decreasing the required battery voltage is to replace the standard converter with a multilevel inverter [2]-[8]. Multilevel converter based StatComs offer improved voltage quality, decreased switching frequencies, reduced power losses, and decreased stress on the individual power electronic devices. In addition, multilevel converter-based StatComs enable more effective use of energy storage.

As control for complex power electronic circuits became more demanding, programmable digital signal processors (DSPs) enjoyed wide adoption in various fields [9]-[12]. In contrast to common microcontrollers, DSPs are application specific ICs that usually have Harvard architecture, hard-wired logic, 16 or 32 bit word length, leading to high computation capability. These technology advancements have extended DSP applications to real time power electronic circuits: high frequency DC/DC converters, motion control for most types of motors, resonant-commutated converters, and power factor correction. These applications illustrate the advantage of DSPs over micro-controllers and analog control circuits.

However, most reported DSP applications are oriented to relatively simple power electronic circuits such as buck converters and conventional inverters, and usually require coordination of fewer than 6 power switches and 4 channels of A/D. To control more complex power electronic circuits, multiple DSP chips and their coordination are necessary.

This paper is devoted to integrating a multi-processor control system and a five-level cascaded power converter together into a versatile real time system for laboratory multilevel power conversions. Specific problems inevitable in practical designs for both multi-processor digital controller and power converter are discussed and possible solutions are provided. To illustrate the application of this inverter system, a combination of StatCom with battery energy storage (StatCom/BESS) is implemented on a 3 kVA prototype to control active and reactive power exchanges with a laboratory scale power system. Additionally, a new and simple control method is developed for the StatCom/BESS to realize four-quadrant powers injection (absorption). Theoretical analysis and experimental results are provided to demonstrate the validity of the proposed concepts.

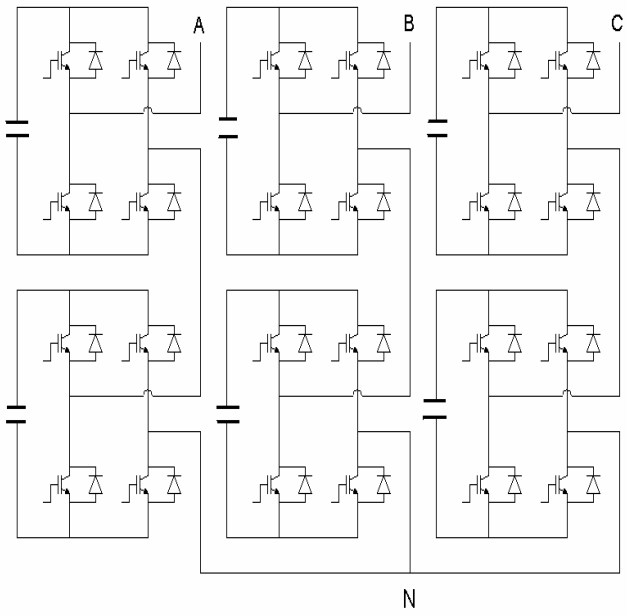

Fig. 1 A 5-level cascaded converter

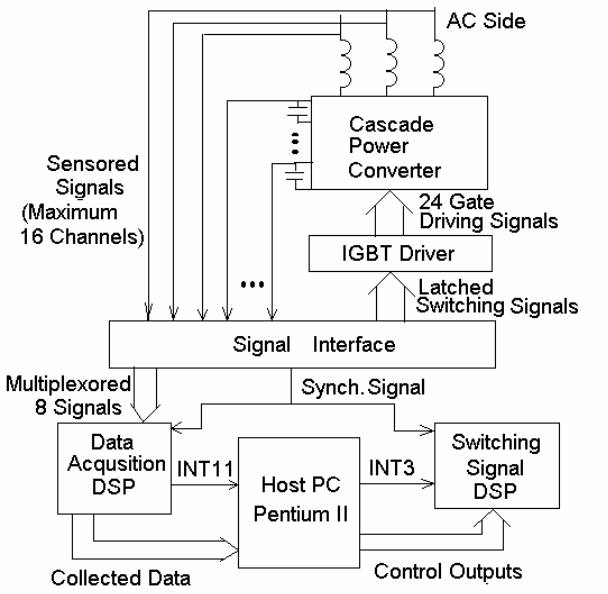

Fig.2 System Diagram

II SYSTEM OVERVIEW

The cascaded converter shown in Figure 1 is composed of 24 IGBTs with six capacitors connected across each H-bridge acting as separate DC voltage sources. The batteries can also be connected in parallel to the DC capacitors in active power applications. Figure 2 shows the functional block diagram of the multi-processor-based controller for the cascaded power converter. The converter output can be connected to AC side loads such as the bulk power system grid or an AC motor.

The IGBT driver boards convert the TTL level switching signals into an isolated ±15V level to trigger the IGBTs. The signal interface board plays an important role in interfacing the power converter and controller: Firstly, it decodes and latches the switching signals generated by the DSP and feeds them to the IGBT driver board. Secondly, it multiplexes 16 channels of sampled signals to 8 channels and sends them to the data acquisition DSP board; and lastly, it generates a shaped synchronizing signal which is very important to the system performance.

Two DSP boards (M5000, TMS320C51 core) are hosted in a PC via an EISA bus and operate concurrently as two slaves of the PC. The TMS320C51 DSP is chosen because of its features: it has a 25 ns instruction cycle, 1056-word dual access RAM on chip, and 16 dedicated I/O ports. In addition, the M5000 board integrates ample hardware resources besides the DSP: it has 128K words of data SRAM and 64K words of program SRAM with 0 wait state, an on-board timer (up to 4 MHz), an interface with the EISA bus, a 12-bit 500Ksps A/D converter (MAX120), and a dual 12-bit D/A converter.

The data acquisition DSP collects data from the on-board A/D and implements real time computational tasks such as low pass filtering, Parks' transformation, and AC phasor calculation. Additionally, it measures the system frequency and monitors any possible system error. The switching signal DSP generates switching signals for the power converter according to the voltage phasor commands sent by host PC. The PC provides supervisory control and an indirect communication link between the DSP boards via interrupts and data storage. The PC collects the processed field data such as system voltage and current from the data acquisition DSP whenever its 11th interrupt is requested. After applying control algorithms, the PC writes the new inverter output voltage commands to the RAM on the switching signal DSP board and then sends an interrupt signal to it. In this way, the host PC receives interrupts from the data acquisition DSP and send interrupts to the switching signal DSP to form a closed loop control system and a communication link between the two DSP boards. Common system-level control algorithms such as PI and fuzzy logic can be easily implemented in the PC by changing software algorithms. Additionally, the host PC provides a user interface and a data logger based on the DOS operating system and C++ development environment.

III DESIGN CONSIDERATIONS

A. Capacitor Sizing

The size of the six DC capacitors should be carefully selected for voltage ripple mitigation. One selection method is to calculate the capacitance using the line current rating and the maximum allowable DC voltage ripple. The capacitor value should be chosen larger than the capacitor charge contributed by line current within ¼ period divided by the maximum allowable DC voltage ripple. Multiplied by a conservative coefficient, the StatCom DC capacitor in this application is chosen to be 2700μF. In addition to voltage ripple, another common problem that occurs is that the wiring stray inductance may cause voltage ringing when the converter output voltage changes levels. An effective way to eliminate this ringing is to add a small "lump snubber" capacitor of 1 μF across each phase leg of H-bridge, as close as possible to the IGBT modules.

B. Dead time and Over-current Protection

The IGBT driving circuits are used to provide the isolated ±15 V gating signals and enough power to trigger on and off these IGBTs. Dead time between complementary switches of a same leg is necessary to avoid shoot through currents that can damage the circuit. In the driving circuit, an adjustable RC delay circuit is incorporated to generate different dead times from 0.5 to 10 μs, which are suitable for various IGBT applications. A 2 μs dead time was adopted in the experiments. A CE22V10 PAL logic device is utilized on this driving board to implement the over-current protection, reset, and preset functions. The logic inside the PAL allows manual start and stop from external control. Once an over-current situation is detected, the PAL will disable all of the IGBTs within 20 ns to protect them from damage and the logic status of "reset" mode occurs. The "reset" status is kept until an external manual start signal is received.

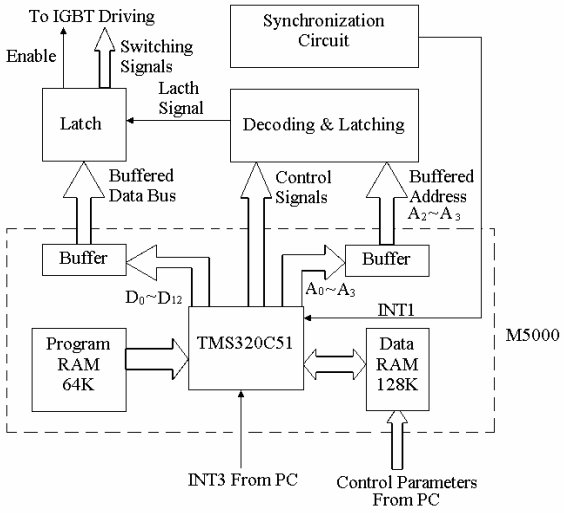

Fig. 3 Switching Signal Generation Hardware

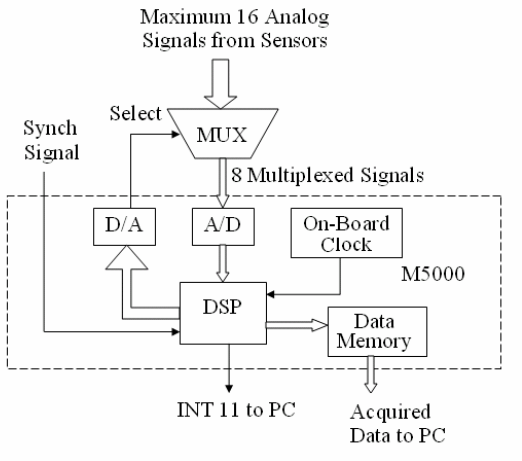

Fig. 4 Data Acquisition Hardware Configuration

C. *Switching Signal Generation*

The function of the switching signal DSP is to generate three-phase sinusoidal voltages of specific amplitude, phase shift and frequency at the multilevel converter output. The switching signal DSP provides 12-bit gating signals on the data bus to control each of the complementary IGBTs in the same leg. The signals on the data bus are decoded, latched, and then fed to the driving board. For safety purposes, the DSP can produce an emergency-blocking signal that will disable all IGBTs during severe system errors.

The structural diagram of the switching signal generation hardware is shown in Figure 3. The DSP board is fed with a synchronizing signal from the signal interface and commanded parameters such as voltage amplitude and phase shift sent from the PC. The DSP will translate the updated control parameters into 12 channels of gate signals that stand for on and off duty cycles for each phase leg of the power converter. The glue logic of decoding and latching was implemented with a CPLD (Complex Programmable Logic Device) on the signal interface board. There are two ways to assign the I/O port address to the IGBT driving board: one way is to assume that only one port is available for both switching combinations. The other method is to assign different ports. With the method of only one port address, the D12 has to be used concurrently with D_0~D_{11}. If two port addresses are assigned, D12 need not be included because D_0 can be multiplexed as an enable signal, thus one signal wire can be saved. Another feature in the glue logic is partial address decoding, which uses part of the address lines the M5000 provides for decoding. Although the M5000 provides 4 address lines (A_0~A_3), the IGBT driving board will occupy at most 2 port addresses in the I/O space range 8 to 15. Address lines A_3 and A_2 will be enough to tell when the IGBT driving port or the enable signal is selected by the DSP. In this way, the decoding logic saves two address signals.

Sinusoidal pulse width modulation (SPWM) is used in this paper to generate the switching signals. To implement the on-line comparison of the sinusoidal waveform with the triangular waveforms at different levels, two function tables are loaded into memory before the assembly code runs. The length of the triangular waveform table is 64 points while the length of the sinusoidal waveform table is 1728 points. The on-chip timer is set for 9.65 μs interrupt in which the triangular values will be compared with sinusoidal values to yield logic level switching signals. A total of 64 points for a triangular waveform is enough for the sampling accuracy and a 32-point table can be used if computation time is tight. Another feature used in the SPWM code is to exploit the 3 auxiliary registers (AR0~AR2) to point to different places in the sinusoidal table with a $2\pi/3$ phase shift. These pointers, AR0 through AR3, move forward in every interrupt period and circular memory addressing automatically returns the pointers to the beginning when the end of the table is reached.

D. *The Data Acquisition DSP*

The data acquisition hardware configuration is shown in Figure 4. Up to 16 channels of analog signals from the sensor circuit are multiplexed by analog switches on the signal interface board to 8 signals that can be handled by the M5000 A/D sampling system. This multilevel converter requires data from all three phase voltages and currents plus 2 DC capacitor voltages for even the simplest operations. For more complicated applications, more DC capacitor voltages and currents or additional AC voltages and currents must to be monitored. In such cases, up to 16 channels of A/D are essential. The DSP has only one on-chip timer which has been occupied by the frequency measurement, thus an on-board configurable clock was exploited to provide the data sampling scheduling which occurs 32 times each line cycle. The on-board clock frequency is initialized to 1.92 KHz, which can be fine-tuned by the frequency measurement subroutine. The unused D/A output is fed to the signal multiplexor to select a signal group for A/D conversion.

The DSP program for data acquisition carries a heavy computation load to be completed within 1/32 of a line cycle.

The end of the A/D conversion is acknowledged by a dedicated signal connected to the DSP and thus a polling method can be used to identify when the A/D conversion is finished and conversion for next signal can be launched. The backbone of the DSP program consists of 2 parallel parts triggered by different interrupt signals. The interrupt routine of the on-board clock will perform A/D conversion for up to 16 channels, and then complete a series of calculations and digital filtering. The calculations include Parks' transformation, RMS value calculation of AC voltages and currents, and complex power computation. Through these computations, V_d, V_q, I_d, I_q, active and reactive power can be obtained and stored in memory for the host PC to fetch. The square root calculation and A/D conversions are the most time consuming parts in this program.

Another important action is the frequency measurement and sampling clock adjustment. Triggered by the synchronizing signal, the DSP calculates the accurate frequency of the AC system and reconfigures the on-board clock according to this frequency. If the measured frequency deviates too much from 60 Hz, a system error will be reported to the host PC. The accuracy of frequency measurement is within 0.2 degrees.

E. Synchronizing Signal Shaping

The synchronization circuit, generally implemented by either a phase lock loop or zero crossing detection circuits, plays an important role in various power conversion applications because it directly affects the frequency measurement and synchronization between the power converter outputs and the AC system. An accurate synchronous signal is critical to both the switching signal generation and data acquisition described above.

Unfortunately, the output of an analog comparator does not provide a high quality zero-crossing signal. The unshaped output of a comparator has several undesirable glitches around every zero-crossing point, which can cause the entire system to behave improperly. In the prototype, the time window in which the glitches occur is 6 μs around the true zero-crossing point. A logic delay circuit was designed to eliminate the undesirable glitches. The unshaped synchronous signal feeds the input of D flip-flop and the clock input is connected to a 555 timer-based oscillator. The clock period can be tuned by selecting different RC values for the oscillator and an 8 μs period was chosen. The only disadvantage of this method is that is a maximum ±8 μs error is introduced to the true zero crossing point. Fortunately this value is negligible compared to the period of 60 Hz signals. Figure 5 depicts how the delay circuit shapes the comparator output to an accurate synchronous signal.

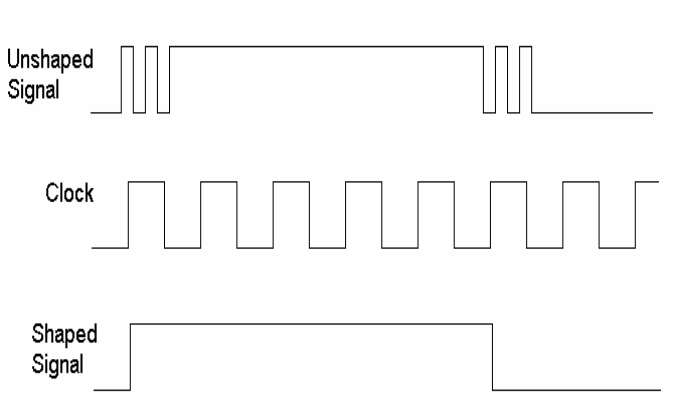

Fig. 5 Synchronizing Signal Shaping

IV. STATCOM WITH ENERGY STORAGE

The voltage-source type multilevel converters are well suited for utility interface and motor drives. Synchronous Static VAR Compensators (StatCom) are an important FACTS device, usually providing reactive power compensation to enhance AC transmission system performance. One disadvantage of the conventional StatCom is it cannot affect active power flow since it does not have an energy source. In recent years, a notable advance in the area of energy storage technology has made integration of multilevel converters and energy storage systems (ESS) an attractive option to utility applications to provide four-quadrant power operation to enhance bulk transmission system capability. Cascaded converters are well suited for detachable energy storage devices such as fuel cells and batteries due to their modularity and simplicity of topology. For these reasons, a laboratory scale StatCom/BESS was built utilizing the multi-functional inverter system described in the previous sections.

To realize four-quadrant PQ control with a StatCom/BESS, a relationship between the injected power and the inverter output voltage must be established. If the inverter output voltage is assumed to be an ideal AC voltage source with controllable amplitude, frequency, and phase angle, there are two control levels for the StatCom/BESS: a low level control implemented by various modulation strategies to provide gate signals for specific inverter voltage output, and a high level control implemented by different control methods based on the system model.

A. StatCom Low Level Control — Multilevel SPWM

The SPWM strategy can be applied to multilevel converters by modifying the conventional SPWM to form a multi-step SPWM. Since the converter output voltage has five possible states from $-2V_{dc}$ to $2V_{dc}$ for every phase, four triangular waveforms at different levels are compared with the sinusoidal reference waveform to yield the switching combinations at each different level. Every leg in an H-bridge has a PWM waveform at a specific level, thus the phase voltage can be synthesized through the comparisons of the sinusoidal waveform with 4 triangular waveforms. With this method, the fundamental output voltage of the inverter is expressed by the phase shift angle and modulation index given in eq. (1).

$$V_{statcom} = 2V_{dc} \cdot M \cdot \cos(\omega t + \alpha) \ , \ 0<M\leq 1 \quad (1)$$

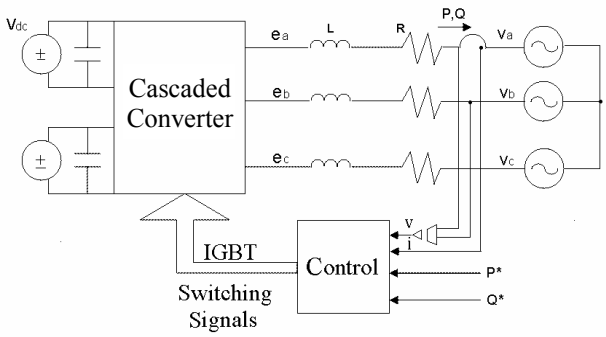

Fig. 6 System Diagram of a StatCom/BESS

Another feature of the SPWM strategy for the cascaded converter is the rotated switching method [7] such that the upper and lower H-bridges exchange their operating mode every half cycle. This balances the charge and discharge for the two DC voltage sources by making the 2 H-bridges in a phase contribute to the line current equally. This balancing capability is a significant advantage of the cascaded topology. Furthermore, with this method the bank capacitor voltages can be easily balanced when the converter operates as a traditional StatCom without energy storage.

B StatCom High Level Control — PQ Injection

The StatCom/BESS system is modeled as an ideal AC voltage source connected to an infinite bus via a line impedance. Figure 6 shows the connection of the StatCom/BESS to a power system. Synchronous rotating coordinates are introduced to simplify the system model and the transform matrix T is given in eq. (2).

$$T=\sqrt{\frac{2}{3}}\begin{bmatrix}\cos(\omega t) & \cos(\omega t-120^\circ) & \cos(\omega t+120^\circ)\\ -\sin(\omega t) & -\sin(\omega t-120^\circ) & -\sin(\omega t+120^\circ)\\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}}\end{bmatrix} \quad (2)$$

The active and reactive power injected into the power system are given in eq. (3).

$$P=V_d i_d+V_q i_q\,,\ Q=V_q i_d-V_d i_q \quad (3)$$

Since the *d* axis of the rotating coordinates is always coincident with the system voltage, V_q should be zero and V_d is equal to system voltage V_s, thus *P* and *Q* will be determined by i_d and i_q respectively:

$$P=V_s i_d\,,\ Q=-V_s i_q \quad (4)$$

The time domain model of the voltage and current can be established as derivative equations (5), in which i_{abc}, e_{abc} and v_{abc} are instantaneous line currents, inverter voltages, and system voltages respectively.

$$\frac{d}{dt}\begin{bmatrix}i_a\\ i_b\\ i_c\end{bmatrix}=-\frac{R}{L}\begin{bmatrix}i_a\\ i_b\\ i_c\end{bmatrix}+\frac{1}{L}\left(\begin{bmatrix}e_a\\ e_b\\ e_c\end{bmatrix}-\begin{bmatrix}v_a\\ v_b\\ v_c\end{bmatrix}\right) \quad (5)$$

Applying the *T* transform to both sides of equation (5), the system model in *dq* coordinates:

$$\frac{d}{dt}\begin{bmatrix}i_d\\ i_q\\ i_o\end{bmatrix}=\begin{bmatrix}\omega i_q\\ -\omega i_d\\ 0\end{bmatrix}-\frac{R}{L}\begin{bmatrix}i_d\\ i_q\\ i_o\end{bmatrix}+\frac{1}{L}\left(\begin{bmatrix}e_d\\ e_q\\ 0\end{bmatrix}-\begin{bmatrix}V_s\\ 0\\ 0\end{bmatrix}\right) \quad (6)$$

In this linear model, i_d and i_q are controlled by the inverter output voltage vectors e_d and e_q. Various control methods such as PI decoupled control can be used to regulate i_d and i_q to the desired values. Combined with eq. (1), equation (6) yields the simplified model:

$$\frac{d}{dt}\begin{bmatrix}i_d\\ i_q\end{bmatrix}+\begin{bmatrix}\frac{R}{L} & -\omega\\ \omega & \frac{R}{L}\end{bmatrix}\begin{bmatrix}i_d\\ i_q\end{bmatrix}=\frac{1}{L}\begin{bmatrix}\sqrt{6}MV_{dc}\cos\alpha-V_s\\ \sqrt{6}MV_{dc}\sin\alpha\end{bmatrix} \quad (7)$$

The control variables α and *M* will vary i_d and i_q, and therefore *P* and *Q*. In steady state, i_d and i_q are constant, therefore the derivative of the currents can be set to zero and *M* and α can be calculated such that:

$$\alpha=arctg\left[\left(\omega L i_d+RI_q\right)/\left(Ri_d-\omega L i_q+V_s\right)\right]$$
$$M=\sqrt{\left(Ri_d-\omega L i_q+V_s\right)^2+\left(\omega L i_d+Ri_q\right)^2}\Big/\sqrt{6}V_{dc} \quad (8)$$

where

$$\begin{bmatrix}i_{d\_ref} & i_{q\_ref}\end{bmatrix}^T=\begin{bmatrix}\frac{P_{ref}}{V_s} & \frac{Q_{ref}}{V_s}\end{bmatrix}^T$$

With the proposed control, any commanded active and reactive powers *P* and *Q* generate the control variables *M* and α that govern the reference sinusoidal waveform for the inverter. The advantage of this model is the elimination of the PI control parameter tuning and breakthrough of the limitation of small signal models in which the PQ injection has to be in the small vicinity of the equilibrium point. The only disadvantage is that accurate parameters of line impedance must be known.

V. EXPERIMENTAL RESULTS

The cascaded inverter-based StatCom/BESS was constructed in the laboratory with the following specifications:

- The battery parallel to every H-bridge is 72 volts,
- The AC line-line voltage is 230 volts at 60 Hz,
- The StatCom is rated at 3 kVA,
- A 1:1.5 step-up transformer with low leakage impedance was utilized to match the voltage amplitude of the power system,

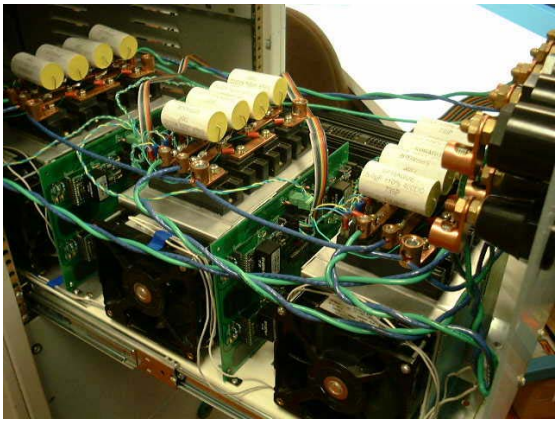

Fig. 7: The Cascaded Inverter

- The total line resistance is 0.5 Ω, the inductance is 16 mH.
- The switching frequency for SPWM is 1620 Hz for low order harmonic mitigation and the speed limit of digital controller.
- The sample frequency of the supervisory control is 1.92 kHz.

Figure 7 shows a photograph of the three-phase cascaded converter.

The line-line inverter output voltage and line current are shown in Figure 8. A five-level inverter can output nine levels for line-to-line voltage, which will reduce the harmonic distortion considerably compared to tradition two level inverters. In addition, a multi-step SPWM was used to produce different voltage amplitudes, which also eliminates low order harmonics. As is evident in Figure 8, the nine-level voltage has a 1.6 kHz modulation at each level and the line current appears nearly sinusoidal without any filtering circuits.

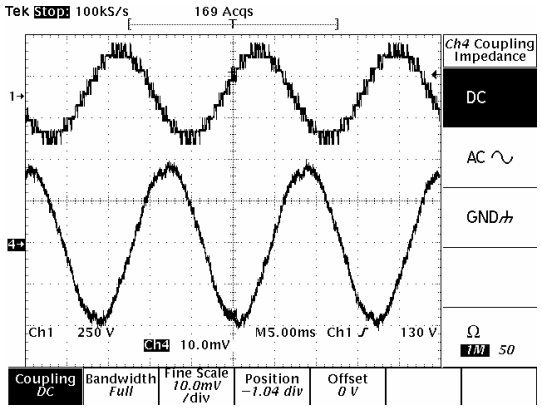

Fig. 8: Inverter line-line voltage and line current (5A/div)

Figures 9 through Figure12 show the experimental results of PQ step change. Different PQ commands in four quadrants are sent via the PC user interface. With the PQ control method introduced in last section, the active and reactive power can keep pace with the reference within one or two cycles. The StatCom/BESS can inject into the AC system both active and reactive power independently and simultaneously without any need for V_{dc} control. The negative injection for active power means the StatCom/BESS absorbs energy from the power system and charges the batteries.

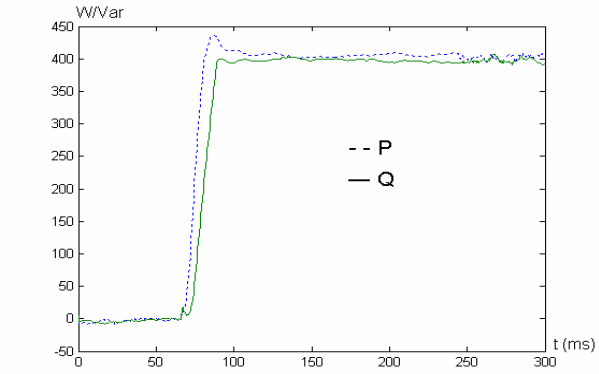

Fig. 9: Experimental PQ step change from (0,0) to (400,400)

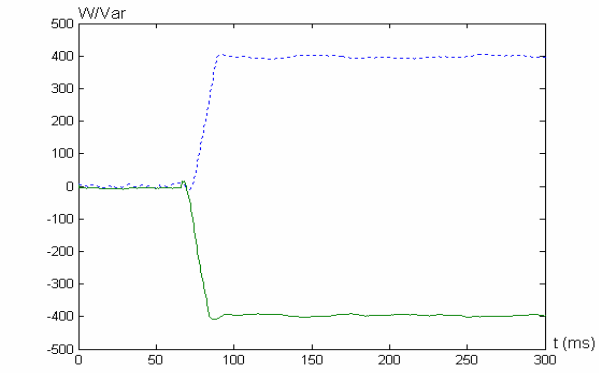

Fig. 10: Experimental PQ step change from (0,0) to (400,-400)

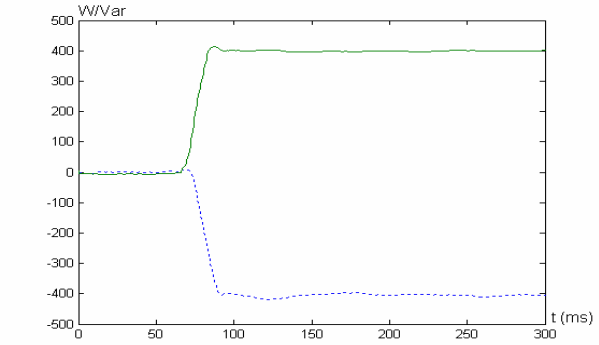

Fig. 11: Experimental PQ step change from (0,0) to (-400,400)

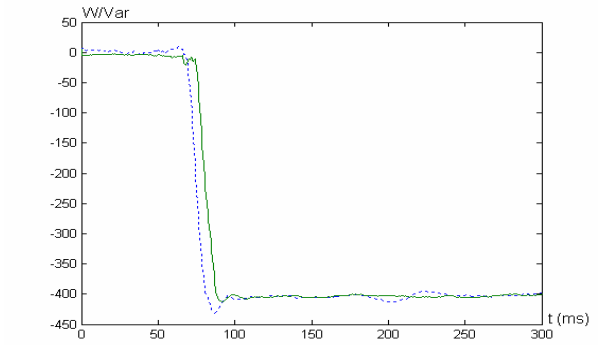

Fig. 12: Experimental PQ step change from (0,0) to (-400,-400)

VI. CONCLUSIONS

This paper presents a multi-processor controller for a five-level cascaded inverter system for real time power system applications. Detailed implementation commentary for both the digital controller and the cascaded inverter is provided. A 3kVA prototype system was built to illustrate that the StatCom/BESS can simultaneously realize active and reactive power injections. A simplified large signal model is derived and a new power control method without PI tuning is developed for this StatCom/BESS. In addition, the proposed control overcomes the limitation of small signal models, which require operating points in the vicinity of the equilibrium point. The experimental results show good agreement to the commanded outputs, indicating the proposed controller and control method are valid for four-quadrant power injections. This multi-functional inverter system shows that the combination of DSPs and multilevel converters has the potential for numerous power applications.

VII. ACKNOWLEDGEMENTS

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