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Estimating the Power Bus Impedance of Printed Circuit Boards With Embedded Capacitance

Minjia Xu, *Member, IEEE,* and Todd H. Hubing, *Senior Member, IEEE*

Abstract—**Embedded capacitance is an alternative to discrete decoupling capacitors and is achieved by enhancing the natural capacitance between closely spaced power and return planes. This paper employs a simple cavity model to investigate the features affecting the power bus impedance of printed circuit boards with embedded capacitance.**

Index Terms—Cavity theory, conduction loss, dielectric loss, embedded capacitance (buried capacitance), power bus decoupling, power bus impedance, power bus modeling, power bus noise (delta-I noise, ground bounce noise, simultaneous switching noise), power bus resonance, power plane, quality factor, return plane.

I. INTRODUCTION

NOISE on the power bus due to a sudden change in the current drawn by active devices (delta-I noise) is a common problem in high-speed printed circuit board (PCB) and multi-chip module (MCM) designs [1], [2]. Delta-I noise can result in signal integrity problems and is a potential source of radiated electromagnetic interference (EMI) [3]. Decoupling capacitors are commonly used to mitigate delta-I noise. Typical high-speed digital designs require dozens or even hundreds of discrete decoupling capacitors. These capacitors take up space and can reduce the reliability of the product. In addition, the effective frequency range of discrete decoupling capacitors on printed circuit boards is generally limited to several hundred megahertz due to the interconnection inductance [4].

Embedded capacitance is an alternative to discrete decoupling capacitors for reducing power bus noise [5]–[7]. This method takes advantage of the natural capacitance between solid power and return planes. In most PCB designs, this natural capacitance is too small to be effective. However, by minimizing the distance between the two solid planes and filling this space with a material that has high relative permittivity, the board capacitance can be greatly enhanced. As a result, it may be possible to eliminate the local decoupling capacitors (e.g., capacitors with a value of 0.01 microfarads or smaller) in boards with embedded capacitance. Normally, bulk decoupling capacitors (e.g., capacitors with a value of 1 microfarad or greater) are still used in boards with embedded capacitance to reduce low-frequency power bus noise.

With closely spaced power–return plane pairs for power distribution, embedded capacitance boards can achieve very low power bus impedance over a wide frequency range (generally

much less than 1 Ω above a few megahertz) [8]. The impedance associated with active devices mounted on the board surface tends to be much higher than the power bus impedance. Therefore, most active devices can be modeled as current sources. The power bus voltage at one location due to the current drawn by a component at another location can be calculated using

$$V_{noise} = I_{device} \times Z_{21} \qquad (1)$$

where Z_{21} is the power bus transfer impedance between these two locations. Several texts and papers have proposed methods to estimate the total transient current drawn by active devices (e.g., [9]–[11]). Regardless of the technique used to determine the source current, the key to reducing the power bus noise voltage is minimizing the power bus transfer impedance at all frequencies of interest.

At low frequencies, the behavior of a closely spaced power–return plane pair can be described by a lumped-element model [4]. However, at frequencies where the dimensions of the board are not electrically small, it is necessary to use complex distributed models. Rubin and Becker have modeled electrically large printed circuit boards using a grid of lumped resistors, capacitors and inductors [12]. Novak used a grid of transmission lines to model power bus structures [13]. Shi and Fan developed a circuit extraction approach based on an integral equation formulation for analyzing power bus systems [14]. Each of these techniques can be used in conjunction with SPICE models of active devices to simulate the behavior of printed circuit boards with power–return plane pairs. In addition, general two-dimensional (2-D) or three-dimensional (3-D) full wave numerical methods such as FDTD, FEM, and MoM have also been applied to model printed circuit boards with power–return plane pairs [15], [16]. However, these models are relatively complex, and they require a significant amount of time and expertise to implement properly.

Several investigators have used a cavity model to characterize the power bus systems of printed circuit boards with solid power and return planes [13], [17]–[20]. The input and the transfer impedance expressions resulting from the cavity model of closely spaced power–return plane pairs are relatively simple and reasonably intuitive. This paper uses a cavity model to analyze printed circuit boards with embedded capacitance. The model results are validated by power bus impedance measurements. According to the cavity model, the magnitude of the power bus impedance near resonances is determined by the quality factor of the cavity structure. This paper examines the quality factor for typical embedded capacitance geometries, and determines the dominant source of loss affecting the amplitude of power bus resonances.
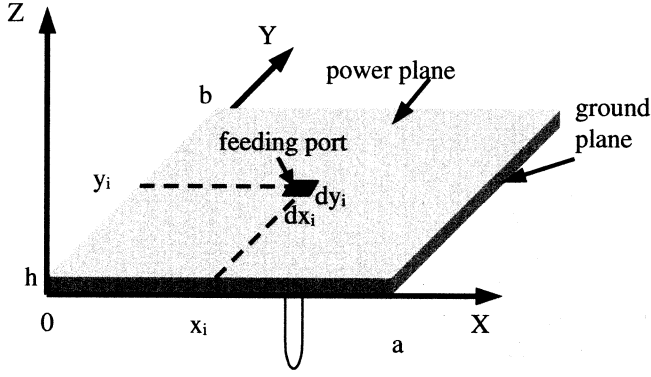
Fig. 1. Geometry of a rectangular power–return plane structure.

II. CAVITY MODEL FOR CLOSELY SPACED POWER-RETURN PLANE PAIRS

The structure under study is a rectangular power–return plane pair separated by a dielectric substrate as shown in Fig. 1. Since embedded capacitance boards are electrically thin, they can be modeled as a 2-D TM_z cavity with two perfect electric conductor (PEC) walls representing the power and return planes. The sides of the rectangular board can be modeled with four perfect magnetic conductor (PMC) sidewalls. The feed port is modeled using a z-directed current source located at (x_i, y_i) with an electrically small rectangular cross section of size (dx_i, dy_i). The receiving port located at (x_j, y_j) has an electrically small rectangular cross section of size (dx_j, dx_j). The transfer impedance between these two ports is given by

$$Z_{ij} = j\omega\mu h \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\chi_{mn}^2}{ab(k_{xm}^2 + k_{yn}^2 - k^2)} \cos(k_{yn}y_i)$$
$$\times \cos(k_{xm}x_i) \operatorname{sinc}\left(\frac{k_{yn}dy_i}{2}\right)\operatorname{sinc}\left(\frac{k_{xm}dx_i}{2}\right)$$
$$\times \cos(k_{yn}y_j)\cos(k_{xm}x_j)\operatorname{sinc}\left(\frac{k_{yn}dy_j}{2}\right)\operatorname{sinc}\left(\frac{k_{xm}dx_j}{2}\right) \tag{2}$$

where $k_{xm} = m\pi/a$, $k_{yn} = n\pi/b$, $k = \omega\sqrt{\varepsilon_0\varepsilon_r\mu}$. $\chi_{mn}^2 = 1$ for $m = n = 0$; $\chi_{mn}^2 = 2$ for $m = 0$ or $n = 0$; $\chi_{mn}^2 = 4$ for $m \neq 0$, $n \neq 0$ [13], [18], [19]. With $i = j$, the input impedance at the feed port becomes

$$Z_{in} = j\omega\mu h \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\chi_{mn}^2 \cos^2(k_{yn}y_i)\cos^2(k_{xm}x_i)}{ab(k_{xm}^2 + k_{yn}^2 - k^2)}$$
$$\times \operatorname{sinc}^2\left(\frac{k_{yn}dy_i}{2}\right)\operatorname{sinc}^2\left(\frac{k_{xm}dx_i}{2}\right). \tag{3}$$

In a typical printed circuit board, the transient current flows through a lead or a via to reach the power or the return plane. For a coaxial feed such as this, the feed port can be represented by a square whose effective cross-section is equal to the area of the circular feed probe [22].

Equations (2) and (3) assume that the structure is lossless. However, power–return plane pairs in real printed circuit boards exhibit losses due to the finite resistance of the copper walls, loss in the dielectric, radiation loss, losses due to surface waves induced on the outer surface of the copper, and losses due to the power dissipated in the components. For an unpopulated thin power–return plane structure with a reasonably good dielectric and conductor, it has been shown that the transfer and input impedance is still approximately determined by (2) and (3) as long as k^2 is replaced by $-\gamma^2$ [23], where

$$\gamma^2 = -k^2\left[1 - \frac{j(1+j)R_s}{kh\eta}\right]. \tag{4}$$

In (4), η is the intrinsic impedance of the dielectric substrate, R_s is the surface impedance of the two conducting planes, and k is the wave number in the lossy dielectric substrate represented by

$$k = \omega\sqrt{\mu_0\varepsilon_0\varepsilon_r(1 - j\tan\delta)} \tag{5}$$

where $\tan\delta$ is the loss tangent of the dielectric substrate between two solid planes.

The input and transfer impedances given by (2) and (3) are expressed as double infinite series that need to be truncated in practical calculations. The number of terms needed for convergence can be determined by the highest frequency of interest [18]. The computation can be accelerated by reducing the double infinite series to a single infinite series using trigonometric Fourier series [24].

To validate the cavity model, the input impedance of a 15.6-cm by 10.6-cm double-sided FR4 board was calculated according to (3)–(5). The dielectric layer between two solid planes was 30 mils thick with a relative permittivity equal to 3.86 and a loss tangent equal to 0.019. The board was fed by an SMA jack at location (4.6 cm, 2.6 cm). The radius of the center conductor for the SMA jack was 30 mils. The input impedance of this test board was measured using an HP4291A impedance analyzer from 1 MHz to 1.8 GHz. The cavity model estimate for the magnitude of the input impedance agreed pretty well with the measurement as demonstrated in Fig. 3. The calculations were performed up to $m = n = 1000$ to achieve a 5% maximum error at all resonant frequencies. Compared to the measurement results, the calculated resonant peaks were slightly higher at the cavity resonance frequencies. This difference may have been due to the PMC boundary assumption in the cavity model, which neglected the fringing field at the board edges.

Fig. 3 provides another example where the cavity model was used to calculate the first null and peak of the input impedance for a 15-cm by 10-cm board [25]. The two planes of the board were separated by a layer of 55-mil FR4 with a relative permittivity equal to 4.3 and a loss tangent equal to 0.2. The board was fed by a low impedance 85-mil semi-rigid probe at (4 cm, 5 cm). The radius of the probe's center conductor was 10-mils. Using an HP4291A impedance analyzer, it was found that the input impedance of the structure exhibited a series resonance at 198 MHz, and a cavity resonance at 488 MHz. The cavity modeling results were obtained by truncating the double infinite series in equation (3) at $m = n = 300$.

As shown in Figs. 2 and 3, the impedance of the power–return plane pair exhibits a series of poles corresponding to the cavity resonances. To help understand this behavior, an equivalent circuit based on the modal expansion method for the power–return plane structure is shown in Fig. 4. In this equivalent cir-
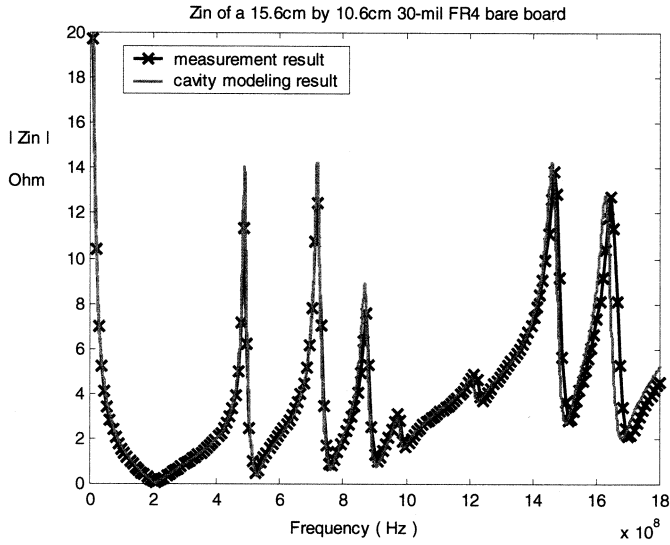
Fig. 2. Input impedance of a 10-mil thick 15.6-cm by 10.6-cm double-side FR4 test board fed by an SMA jack at location (4.6 cm, 2.6 cm): measurement vs. lossy cavity modeling results.
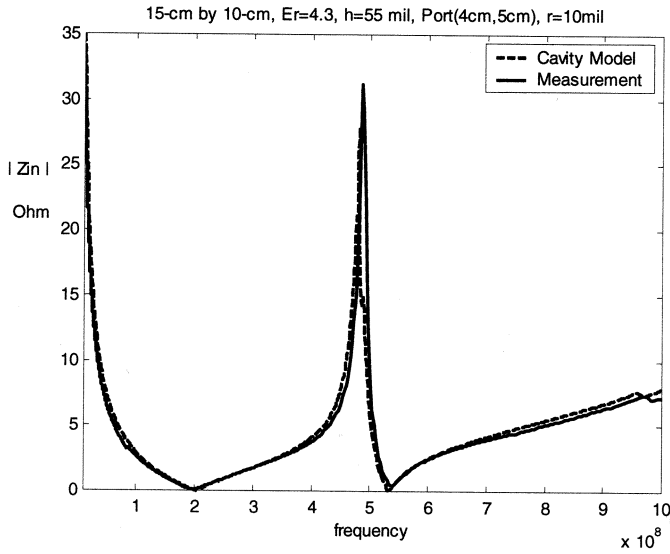

Fig. 3. Input impedance of a 10-mil thick 15-cm by 10-cm double-side FR4 test board fed by an SM jack at location (4 cm, 5 cm): measurement vs. lossy cavity modeling results.

cuit, the impedance contributed by the TM_{mn} mode is modeled by an LCR parallel branch with a resonant frequency equal to the cutoff frequency of this mode. The contribution to the total impedance from the TM_{mn} mode is given by

$$Z_{mn} = \frac{1}{j\omega C_{mn} - j/(\omega L_{mn}) + 1/R_{mn}} \qquad (6)$$

where

$$C_{mn} = \frac{ab\varepsilon_0\varepsilon_r}{h\chi_{mn}^2}\frac{1}{A^2B^2} \qquad L_{mn} = \mu h \frac{\chi_{mn}^2}{ab}\frac{A^2B^2}{k_{xm}^2 + k_{yn}^2}$$

$$A = \operatorname{sinc}\left(\frac{k_{yn}dy_i}{2}\right)\operatorname{sinc}\left(\frac{k_{xm}dx_i}{2}\right)$$

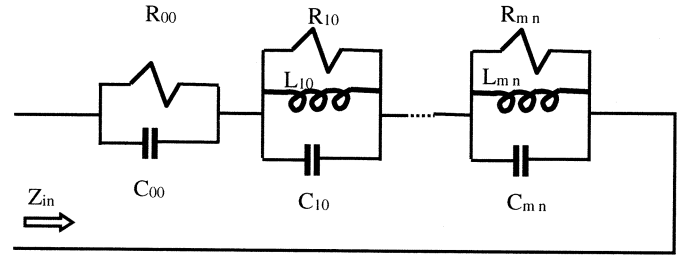$$B = \cos(k_{yn}y_i)\cos(k_{xm}x_i). \qquad (7)$$

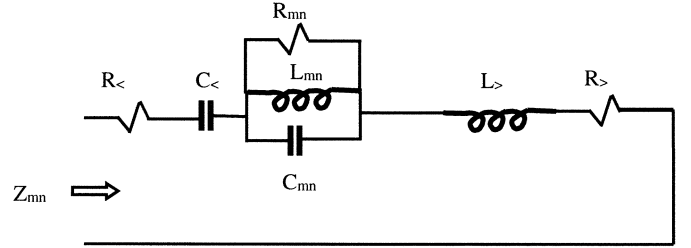Fig. 4. Equivalent circuit for a lossy power–return plane structure.

Fig. 5. Narrow-band equivalent circuit for a lossy power–return plane structure.

The magnitude of the input impedance for the power–return plane pair is finite around the cavity resonances due to the various losses inside the structure. The equivalent loss resistance R_{mn} for the resonant TM_{mn} mode can be expressed as

$$R_{mn} = \frac{Q_{mn}}{\omega_{mn}C_{mn}}. \qquad (8)$$

A narrow-band equivalent circuit for the power–return plane structure near the resonant frequency of the TM_{mn} mode is provided in Fig. 5. In this equivalent circuit, $C_<$ and $R_<$ represent the total contribution to the power bus input impedance from those modes whose cutoff frequency is lower than the cutoff frequency of the TM_{mn} mode, ω_{mn}. $L_>$ and $R_>$ represent the contribution of all modes whose cutoff frequency is higher than ω_{mn}. Although the magnitude of the input impedance around the resonance cannot be directly calculated from R_{mn}, it is generally dominated by the contribution from the resonant branch. At a frequency ω_0 that is slightly higher than ω_{mn}, the contribution from this dominant branch can be calculated using [26]

$$Z_{mn}(\omega_0) = \frac{R_{mn}}{1 + 2jQ_{mn}\frac{(\omega_0 - \omega_{mn})}{\omega_{mn}}}. \qquad (9)$$

Substituting (7) and (8) into (9) yields

$$Z_{mn}(\omega_0) = \frac{\chi^2 A^2 B^2}{C_{Board}} \times \frac{1}{\frac{\omega_{mn}}{Q_{mn}} + 2j(\omega_0 - \omega_{mn})} \qquad (10)$$

where $C_{Board} = ab\varepsilon_0\varepsilon_r/h$. According to (10), the magnitude of the power bus input impedance near the resonances is related to the location and the dimension of the feeding port, the board capacitance, and the quality factor of the structure. Higher loss in the cavity results in a lower quality factor, which in turn leads to a lower power bus impedance near resonant frequencies.

As stated before, power–return plane structures in real printed circuit boards exhibit conductive, dielectric, radiation, surface wave, and component losses. Formulas for the quality factor

due to conductive loss and dielectric loss are well documented [27], [28]. For very thin dielectric layers between power and return planes with arbitrary shape, an approximate formula for the quality factor due to conductive losses in the top and bottom planes is given by

$$Q_c \approx h \sqrt{\pi f \mu \sigma}. \tag{11}$$

The quality factor due to the dielectric loss is given by

$$Q_d = \frac{1}{\tan \delta}. \tag{12}$$

In general, the quality factor due to the radiation loss has to be numerically evaluated for a specific mode. However, an approximate closed-form expression is provided in [21] for the quality factor due to the radiation loss of the dominant TM_{10} mode for rectangular structures with thin dielectric layers. This approximation is

$$Q_{rad} \approx \frac{3}{16} \frac{\varepsilon_r L_e \lambda_0}{p c_1 w_e h} \tag{13}$$

where

$$p = 1 + \frac{a_2}{10} (k_0 w_e)^2 + (a_2^2 + 2a_4) \left(\frac{3}{560} \right) (k_0 w_e)^4$$
$$+ c_2 \left(\frac{1}{5} \right) (k_0 L_e)^2 + a_2 c_2 \left(\frac{1}{70} \right) (k_0 w_e)^2 (k_0 L_e)^2$$
$$a_2 = -0.166\,05 \quad a_4 = 0.007\,61 \quad c_2 = -0.091\,415\,3$$
$$c_1 = \frac{1}{n_1^2} + \frac{2/5}{n_1^4} \quad n_1 = \sqrt{\varepsilon_r \mu_r}. \tag{14}$$

W_e and L_e are the effective dimensions of the structure after accounting for the fringing effect. Surface wave losses are usually very small compared to the other losses in typical power–return pair geometries, and can be safely neglected. Consequently, the overall quality factor for an unpopulated printed circuit board can be approximated as

$$\frac{1}{Q} \approx \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_{rad}}. \tag{15}$$

In general, Q is associated with a specific cavity mode, and is a function of frequency.

III. POWER BUS IMPEDANCE OF EMBEDDED CAPACITANCE BOARDS

As part of research for the embedded decoupling capacitance (EDC) project led by the National Center for Manufacturing Sciences (NCMS), a variety of boards employing embedded capacitance were evaluated [29]. The swept frequency power bus input impedance of each test board was measured using an HP8753D network analyzer between 30 kHz and 5 GHz. In this section, the measured power bus impedance results are analyzed using the cavity model.

A. Power Bus Resonant Frequency Analysis

According to the cavity model, the input impedance of a lossless power–return plane structure is dominated by the board capacitance at frequencies below the first series resonance. At fre-

TABLE I
RESONANT FREQUENCIES FOR THE 15.6 cm BY 10.6 cm FR4 BARE BOARD (MHZ)

Mode	TM 10	TM 01	TM 11	TM 20	TM 21
Modeling	489.4	720.3	870.8	978.8	1215.3
Measured	486.7	718.4	873.5	974.7	1217.6
Mode	TM 02	TM 30	TM 12	TM 31	TM 22
Modeling	1440.5	1468.2	1521.4	1635.4	1741.6
Measured	NA	1469.4	NA	1647.1	NA

quencies above the first resonance, the input impedance is inductive except around cavity resonant frequencies given by

$$f_{mn} = \frac{1}{2\pi \sqrt{\mu \varepsilon}} \sqrt{\left(\frac{m\pi}{a} \right)^2 + \left(\frac{n\pi}{b} \right)^2}. \tag{16}$$

The resonant frequencies for a 15.6-cm by 10.5-cm double-sided FR4 test board were calculated according to (16) up to 1.8 GHz. The calculated resonance frequencies are compared to the measured resonant frequencies in Table I.

Due to the location of the measurement port, some modes were not excited and do not appear in the measurement results plotted in Fig. 2. Nevertheless, the resonant frequencies predicted by (16) are very accurate for this test sample.

When the plane spacing is not very thin at the highest frequency of interest, the effect of fringing fields must be taken into consideration for the resonant frequency calculation. The cavity model assumes there are PMC sidewalls around the structure periphery, yet in reality the field does not stop abruptly at the edge of a test board. Fringing fields at the board edge make the board appear slightly larger than it really is, resulting in a downward shift in the resonant frequencies. Several formulas have been proposed to calculate the resonant frequencies in the presence of a fringing field by adjusting the dimensions of the structure [21], [27]. Fringing is more of a factor in boards that have a smaller ratio of board area to plane spacing. However, in embedded capacitance boards employing very thin dielectric substrates, the fringing effect can normally be neglected.

B. Effect of the Spacing Between the Power and the Return Planes

Fig. 6 compares the measured power bus input impedance of two populated 7.6-cm by 5.1-cm embedded capacitance test boards. These two boards have the exact same layout and the same stack-up. Between the power and the return plane, one test board employs a 4.5-mil layer of FR4 material, while the other uses a special 2.1-mil layer of FR4 material. The experimental results show that the resonant peaks in the 2.1-mil sample are more damped than those in the 4.5-mil sample.

According to (3), the power bus input impedance for a lossless power–return plane pair is proportional to the spacing between the two solid planes (h). In addition, among the three major loss mechanisms, the quality factor due to the conductive loss is proportional to h. Therefore, reducing the power and the return plane spacing will decrease the quality factor associated with the conductive loss of the structure, and lead to lower resonant peaks for the power bus input impedance.
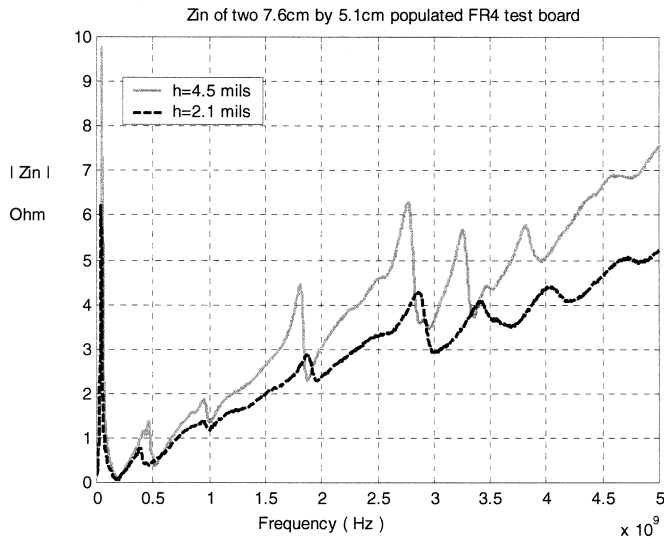
Fig. 6. Measured power bus input impedance of two 7.6-cm by 5.1-cm populated boards with different spacing between the power and the return planes.
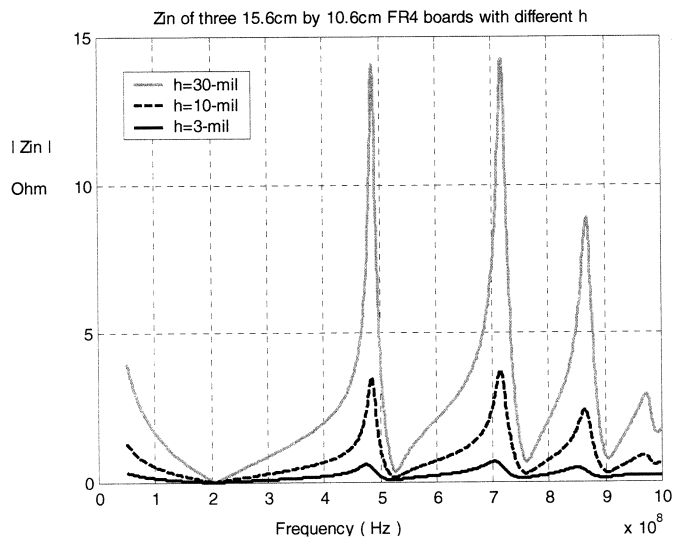

Fig. 7. Cavity modeling results of the input impedance for three 15.6-cm by 10.6-cm FR4 double-side bare boards with different thickness.

The effect of the spacing between the power and return planes is further demonstrated in Fig. 7, which compares the cavity model estimates of the input impedance for three FR4 double-sided bare boards. All three boards are 15.6 cm by 10.6 cm and fed by SMA jacks at (4.6 cm, 2.6 cm). The spacing between the two solid planes for these three test boards is 30 mils, 10 mils, and 3 mils, respectively. According to the simulation results, the 3-mil sample has the lowest input impedance over the whole frequency range. In particular, as the spacing decreases from 30 mils to 3 mils, the magnitude of the power bus input impedance around the resonant frequency at 700 MHz drops from 14.3 Ω to 0.69 Ω. The decrease in the magnitude of these resonances is about 26 dB while the spacing decreased 20 dB. The thinnest test sample has the lowest impedance peaks due to the lower quality factor associated with the conductive loss in the planes.

TABLE II
EMBEDDED CAPACITANCE MATERIALS EVALUATED IN THE STUDY

Material	Dielectric Composition	Thickness	ε_r	$\tan \delta$
EC#1	FR4 epoxy/glass	~2.1 mils	3.8~4.2	0.015~0.02
EC#2	Unsupported epoxy; ceramic powder filled	4.0 mils	36~37	0.01~0.02
EC#3	Unsupported polyimide; ceramic powder filled	1.4 mils	11.6~12	0.008~0.012
EC#4	Unsupported epoxy; ceramic powder filled	~0.3 mils	20~22	0.01~0.1

C. Effect of the Board Dimensions

Board dimensions determine the resonance frequencies of the power bus input impedance as indicated by (16). For a given frequency range, larger boards encounter more board resonances than smaller boards. But that does not necessarily suggest the power bus noise in a large board is more severe. The noise voltage may be excessive if a source harmonic happens to occur around a board resonance with high impedance. Therefore, it is desirable to ensure that all power bus resonances are sufficiently damped. Among the three major loss mechanisms, the quality factors due to the conductive and the dielectric loss do not depend on the board dimensions. The radiation loss decreases with increasing board dimensions. However, since embedded capacitance boards employ ultra-thin power–return plane pairs (usually less than 0.1 mm) for power distribution, the radiation from the board edge is generally not the dominant loss mechanism. As the result, the overall quality factor is relatively independent of the board dimensions for unpopulated boards.

IV. ANALYSIS OF THE QUALITY FACTOR

According to the cavity model discussed in Section II, the input impedance of a power–return plane pair around resonant frequencies is related to the quality factor of the structure. Higher loss in the power–return plane pair yields lower quality factors and lower resonant peaks in the input impedance. A detailed analysis of the quality factor for some typical embedded capacitance boards is performed in this section. Four types of commercially available embedded capacitance materials were evaluated. These materials are described in Table II. The relative permittivity and the loss tangent of each material listed in Table II were measured by NIST [29].

Since surface wave losses can be safely neglected in embedded capacitance boards, the overall quality factor is the combination of the quality factor due to the dielectric loss, the conductive loss and the radiation loss. To determine the dominant loss mechanism in embedded capacitance boards, these three partial quality factors were calculated for the dominant TM_{10} mode for some typical embedded capacitance test boards and their FR4 counterparts using (11)–(14). The total quality factor for the TM_{10} mode of each test board was then calculated according to (15). The results are summarized in Table III.

The data in Table III shows that the radiation loss is relatively small compared to the dielectric loss and conductive loss for all test boards, i.e., Q_{rad} is much higher than Q_d or Q_c. Consequently, radiation loss has little effect on the total quality factor for the TM_{10} mode. The quality factors due to the conductive loss and the dielectric loss are generally of the same order of

TABLE III
QUALITY FACTORS OF THE TM$_{10}$ MODE FOR SOME EMBEDDED
CAPACITANCE BOARDS

Samples	f_{10} (MHz)	Q_d	Q_c	Q_{rad}	Total Q
7.6-cm by 5.1-cm 19.4-mil FR4	997	47.6	235.4	1582	39
7.6-cm by 5.1-cm 4.5-mil FR4	997	47.6	54.6	6819	25
15.7-cm by 10.6-cm 3.3-mil FR4	470	43.5	27.5	21312	17
23.8-cm by 21.8-cm 3.3-mil FR4	310	43.5	22.3	25265	15
7.6-cm by 5.1-cm 2.1-mil EC#1	1002	47.6	25.5	14302	17
15.7-cm by 10.6-cm 2.1-mil EC#1	482	41.7	17.7	29713	12
23.8-cm by 21.8-cm 2.1-mil EC#1	318	41.7	14.4	35790	11
7.6-cm by 5.1-cm 4-mil EC#2	328	66.2	27.8	7.17E+05	20
15.7-cm by 10.6-cm 4-mil EC#2	159	59.5	19.4	1.47E+06	15
23.8-cm by 21.8-cm 4-mil EC#2	104	54.9	15.7	1.77E+06	12
7.6-cm by 5.1-cm 1.4-mil EC#3	567	90.9	12.8	2.23E+05	11
15.7-cm by 10.6-cm 1.4-mil EC#3	277	122	9.0	4.36E+05	8
23.8-cm by 21.8-cm 1.4-mil EC#3	183	122	7.3	5.25E+05	7
7.6-cm by 5.1-cm 5-μm EC#4	426	22.9	1.6	2.00E+06	1.5
15.7-cm by 10.6-cm 5-μm EC#4	206	22.9	1.1	4.04E+06	1.1

Fig. 9. Measured power but input impedance of 15.6-cm by 10.6-cm 3.3-mil FR4 boards: bare board versus fully populated version without discrete decoupling capacitors.

The sharp peak below 100 MHz in the input impedance of the populated board is not a power bus resonance, but a resonance due to the interconnect inductance of the 22-μF bulk decoupling capacitor and the interplane capacitance. Power bus resonances dominate both impedance curves above 500 MHz. The 3-dB quality factors of the first few power bus resonances are calculated from the experimental results and labeled in the plot. Compared with the bare board, the power bus resonances in the populated board are shifted and more damped. The quality factors of the populated board are less than 15, while the quality factors of the bare board are higher than 35.

Similarly, Fig. 9 compares the magnitudes of the measured power bus input impedance of two 15.6-cm by 10.6-cm FR4 boards. Both samples have the same layer stack-up with the power and the return planes next to each other. The spacing between these two planes is 3.3 mils. One test sample is densely populated with components while the other has no components. Again, the power bus input impedance of the densely populated board has a sharp peak below 100 MHz due to the board capacitance and the interconnect inductance of the 4 bulk decoupling capacitors. As labeled in Fig. 9, the quality factors of the power bus resonances in the fully populated board are around 6 to 8. They are much lower than the quality factors of the power bus resonances in the unpopulated sample. The addition losses introduced by equivalent series resistance (ESR) of components help to damp power bus resonances as shown in Figs. 8 and 9. For the 19.4-mil FR4 board and the densely populated 3.3-mil FR4 board, the dominant loss mechanism is the component loss rather than dielectric, conductive or radiation losses. However, the component loss introduced by the active components is not enough to completely eliminate power bus resonances in either example.

Fig. 10 compares the measured power bus input impedance of two 7.6-cm by 5.1-cm EC #2 boards with and without components. The spacing between the power and the return planes is 4.0 mils for both boards. Above 100 MHz, the input impedance curves of both boards are dominated by power bus resonances
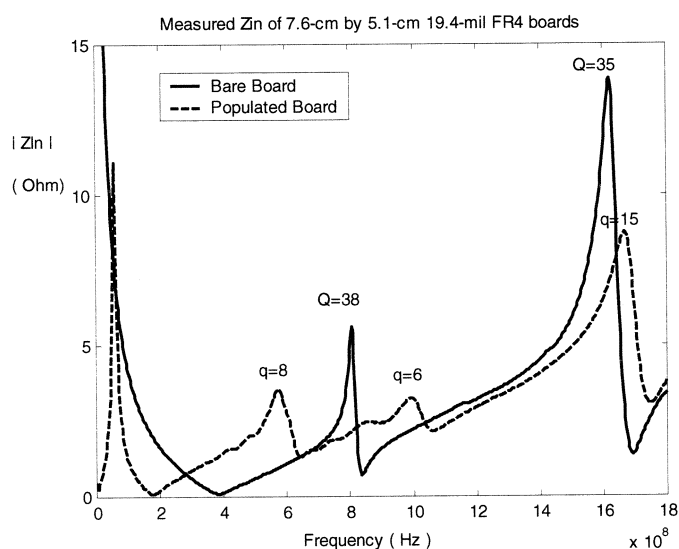

Fig. 8. Measured power bus input impedance of 7.6-cm by 5.1-cm 19.4-mil FR4 boards: bare board versus populated version without discrete decoupling capacitors.

magnitude for these test boards. The loss mechanism that dominates depends on the thickness of the dielectric and the working frequency. Q_c is proportional to the thickness of the dielectric layer and proportional to the square root of the frequency, while Q_d is independent of thickness and nearly independent of frequency. For the closely spaced power–return plane structures used in the embedded capacitance boards, the conductive loss is the dominant factor especially at low frequencies. At higher frequencies and in boards with wider spacing between the power and the return planes, the quality factor is generally dominated by the dielectric loss of the material.

Besides the conductive, dielectric, and radiation loss, extra loss can be introduced by components mounted on a printed circuit board. This effect is demonstrated in Fig. 8, which illustrates the measured power bus input impedance of two 7.6-cm by 5.1-cm FR4 test boards up to 1.8 GHz. One is a bare board while the other is populated with components. Both boards have six layers with the power and the return plane on Layer 2 and Layer 5, respectively. This layer stack-up results a relatively wide 19.4-mil spacing between the power and the return planes.
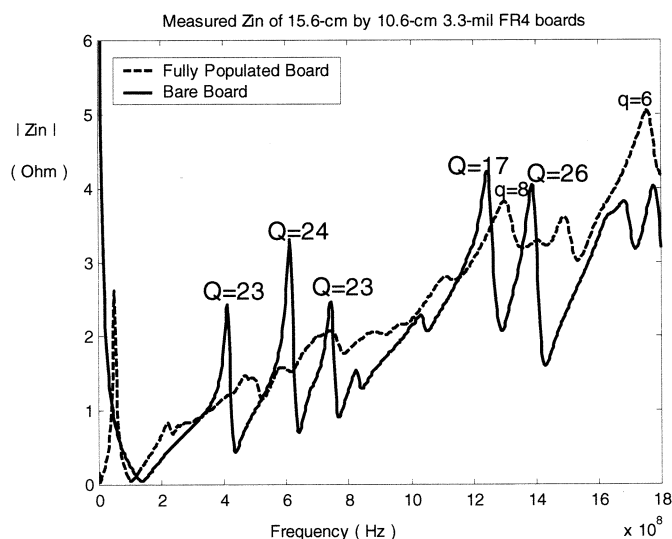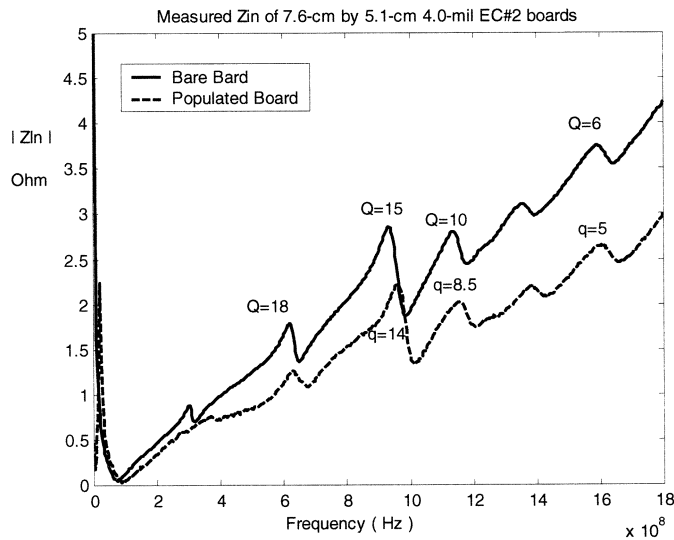
Fig. 10.   Measured power bus input impedance of 7.6-cm by 5.1-cm 4.0-mil EC #2 boards: bare board versus populated version.

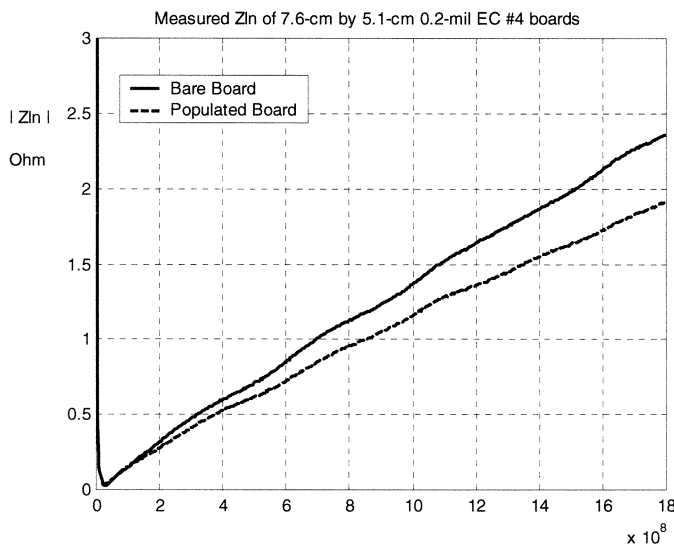Fig. 11.   Measured power bus input impedance of 7.6-cm by 5.1-cm 0.2-mil EC # 2 boards: bare board versus populated version.

Fig. 12.   Measured power bus input impedance of 7.6-cm by 5.1-cm populated boards with various dielectric materials.

along an upward slope. This slope is mainly due to the small ($\sim$120 pH) inductance associated with the connection of the SMA jack to the power and the return plane of the board. The power bus input impedance curve of the populated board has a lower slope due to a smaller SMA connection inductance. As labeled in Fig. 10, the quality factors of the populated board are just a little smaller than the corresponding quality factors in the unpopulated board. The component loss only has marginal effect on power bus resonances for these 4.0-mil EC #2 boards.

Fig. 11 compares the power bus impedance of two 7.6-cm by 5.1-cm EC #4 boards with and without components. The spacing between the power and the return planes is about 0.2 mils for both boards. Again, the populated board has a smaller SMA connection inductance resulting in a lower slope in the power bus impedance curve. Power bus resonances in both curves are eliminated. As shown in Table III, the quality factor
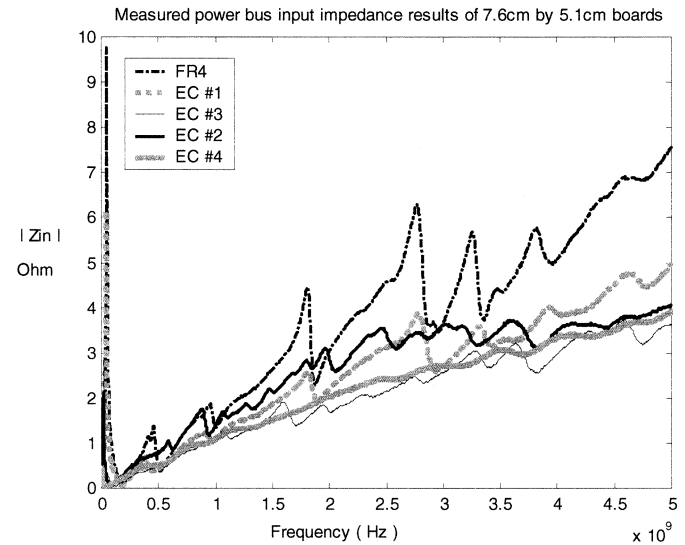
of unpopulated EC #4 is approaching 1, implying that the board is critically damped and exhibits no resonant peaks. The low overall quality factor is due to the low Q_c, which is due to the ultra-thin spacing (approximately 0.2 mils) between the power and the return planes in EC#4 test boards. The component loss is relatively unimportant in the 0.2-mil EC #4 boards.

According to Table III, all test boards employing embedded capacitance materials have lower quality factors (higher loss) than the corresponding FR4 versions for the dominant TM_{10} mode. Fig. 12 compares the measured power bus input impedance for five populated test boards with different dielectric materials [30]. All five boards have the exact same dimension, the same layout, and the same layer stack-up. The only difference is the dielectric material between the power and the return planes of the test boards. Sample 1 has a 4.5-mil layer of FR4; Sample 2 has a 2.1-mil layer of EC#1 (a thinner version of FR4); Sample 3 has a 1.4-mil layer of EC#3; Sample 4 has a 4-mil layer of EC#2; and Sample 5 has a 0.2-mil layer of EC#4. The power bus impedance of these test samples was calculated using the cavity model. The NIST measurements of the relative permittivity and the loss tangent were used in the calculations. Each board was fed by an SMA jack at (2.8 cm, 2.55 cm). The center conductor of the SMA jack had a radius of 28 mils. The modeling results are plotted in Fig. 13. A 120-pH inductance was added to the modeling results of each test sample to account for the SMA connection from board surface to the power plane layer. Since the cavity model only considers the bare power–return plane pair and neglects the effect of vias, fringing fields, and the radiation loss, the simulation results do not match the measurement results exactly. However, both plots show similar trends in the data.

According to the quality factor calculations, the FR4 sample should have the highest quality factor followed by the EC#1, EC#2, EC#3, and EC#4 samples, respectively. In both the measurement and the model results, the FR4 board exhibits significant peaks at power bus resonant frequencies. Several resonant peaks and nulls are also evident in the EC#1 impedance curve.
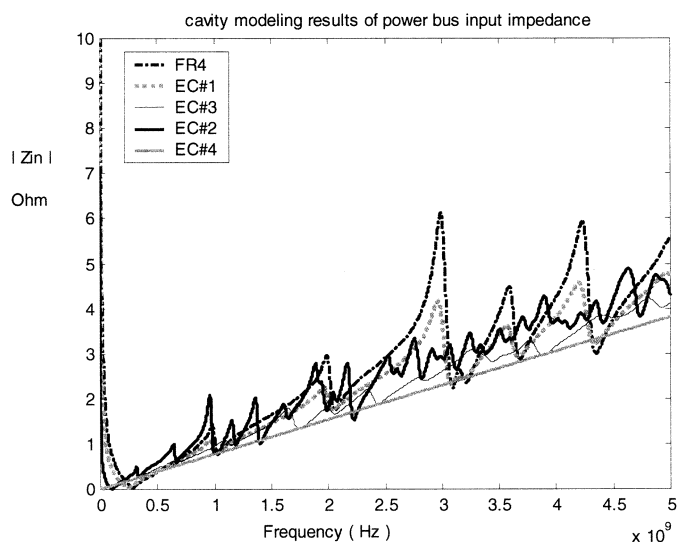
Fig. 13. Cavity modeling results of the power bus input impedance for 7.6-cm by 5.1-cm boards with various dielectric materials.

Ripples in the EC#2 and EC#3 impedance curves are less pronounced, and the EC#4 impedance curve is nearly a straight line corresponding to the lumped inductance of the SMA connection. Such behavior is predicted by the quality factor analysis of the power–return plane structure.

V. CONCLUSION

A simple cavity model was used to characterize closely spaced power–return plane pairs in embedded capacitance boards. The model was validated by power bus input impedance measurements. According to the cavity model, a critical factor affecting the power bus input impedance near resonant frequencies is the quality factor. Boards without sufficient loss will have very high resonant peaks in the power bus impedance. If a noise source harmonic falls near a board resonance that is not sufficiently damped, the power bus noise may be excessive.

Unpopulated printed circuit boards exhibit conductive, dielectric, radiation, and surface wave losses. The conductive loss and dielectric loss are usually more important than the other two loss mechanisms. The dominant loss mechanism depends on the thickness of the dielectric and the working frequency. When the spacing between the two solid planes is on the order of a skin depth in the copper, the conductive loss will dominate. Compared with those in unpopulated samples, the power bus resonances in the populated boards are generally shifted and further damped. The extra loss associated with active components on the board can be important in relatively widely-spaced (>10 mils) or densely populated FR4 boards. However, the component loss was small relative to the copper loss in the planes for the embedded capacitance boards evaluated in this study.

Compared to PCB's with widely spaced power–return plane pairs, the resonant peaks of all embedded capacitance boards were significantly damped due to the conductive loss in the closely spaced power–return plane structure. The boards with a 0.2-mil spacing essentially eliminated all power bus resonances. In general, according to (11), power bus resonances will be essentially eliminated when the spacing between the power and the return planes is on the order of a skin depth in the copper.

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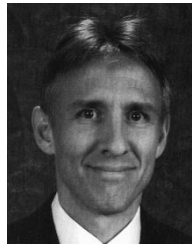
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