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Modeling Noise Coupling from Non-parallel PCB Trace Routing

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Abstract

Coupling between PCB signal traces in proximity is of concern to PCB designers and EMC engineers. The behavior of noise coupling between non-parallel microstrip lines is studied in this paper by a full-wave numerical modeling method CEMPIE, designating a circuit extraction approach based on a mixed-potential integral equation formulation. Good agreement between the numerical results and measurements was obtained.

Introduction

Electromagnetic coupling, or crosstalk between transmission lines is a key issue that can affect the circuit performance and complexity, along with the flexibility of PCB routing. Prior work focused on the theoretical analysis and the methods to reduce crosstalk between coupled transmission lines [1]-[3]. Most of these studies involved parallel transmission lines. In practical PCB routing, noise coupling between non-parallel transmission lines is common. In this paper, the coupling mechanism of non-parallel transmission lines is studied using a full-wave modeling method and measurements.

The full-wave modeling approach used in this work is a mixed-potential integral equation formulation with circuit extraction, denoted CEMPIE. It is an application of the partial element equivalent circuit (PEEC) method in multilayer dielectric media, and very suitable for DC power bus and other multi-layer planar circuit modeling [4], [5]. It extracts a SPICE-compatible equivalent circuit from the Maxwell equation formulation.

A typical structure of coupled non-parallel PCB traces is studied. The coupling of non-parallel PCB traces is being studied to better understand the coupling physics and develop a lumped element model due to the local coupling between the closely-spaced ends, or distributed coupling over the length of the traces. The coupling will be a function of the trace separation, as well as the angle between non-parallel lines. From this knowledge, CAD models that are suitable for SPICE simulation can be developed.

CEMPIE Approach

The CEMPIE approach is based on a Mixed-Potential Integral Equation (MPIE) formulation. An equivalent circuit is extracted from the MPIE formulation instead of solving the matrix equation directly. CEMPIE is an extension of the PEEC method to general multilayer dielectric media. PEEC uses free-space Green's function and treats finite dielectrics in a volume-integral formulation, while CEMPIE employs Green's function for an infinite multi-layered medium. Thus, the difficulties and complexity of a volume integral equation formulation due to an inhomogeneous medium can be transferred to the calculation of the Green's functions. The formulation of the Green's functions for layered media is tedious, but the calculation is relatively fast.

The CEMPIE formulation is similar to the formulation of classical scattering problems. An incident electric field is assumed. Conducting surfaces are then replaced by induced surface currents and charges. By enforcing boundary conditions on the conducting surfaces for the vector sum of the incident and induced electric fields, an integral equation is formed. This equation is discretized and tested by a standard Method of Moments (MOM) procedure. By further assuming the electric potential over each mesh cell is constant, a final system matrix equation is established as [6]

$$[Y][\phi] = -[I^e], \qquad (1)$$

where $[I^e]$ is the impressed node current vector; $[Y]$ is the system admittance matrix and $[\phi]$ is the node based scalar electric potential vector.

If the number of external nodes is N and the total number of nodes is M, the equation (1) can be written as

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$$\begin{bmatrix} Y_{11} & \cdots & Y_{1N} & Y_{1(N+1)} & \cdots & Y_{1M} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ Y_{N1} & \cdots & Y_{NN} & Y_{N(N+1)} & \cdots & Y_{NM} \\ Y_{(N+1)1} & \cdots & Y_{(N+1)N} & Y_{(N+1)(N+1)} & \cdots & Y_{(N+1)M} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ Y_{M1} & \cdots & Y_{MN} & Y_{M(N+1)} & \cdots & Y_{MM} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_N \\ V_{(N+1)} \\ \vdots \\ V_M \end{bmatrix} = \begin{bmatrix} I_1 \\ \vdots \\ I_N \\ 0 \\ \vdots \\ 0 \end{bmatrix}. \quad (2)$$

A lumped circuit model can be constructed for an arbitrary interconnect geometry on the basis of physics associated with the geometry. For an N-port network, Kirchhoff's Voltage Law (KVL) gives a matrix equation that relates the port voltages to the port currents as

$$[Y_{lumped}] \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix}, \quad (3)$$

where $[Y_{lumped}]$ is the admittance matrix for the lumped circuit prototype with unknown element values; $[V_1 \quad V_2 \quad \cdots \quad V_N]^T$ is the port voltage vector; and $[I_1 \quad I_2 \quad \cdots \quad I_N]^T$ is the port current vector.

Comparing equations (2) and (3), it is possible to relate the CEMPIE-based admittance matrix and that for lumped circuit CAD model as

$$[A - BD^{-1}C] = [Y_{lumped}], \quad (4)$$

where

$$[A] = \begin{bmatrix} Y_{11} & \cdots & Y_{1N} \\ \vdots & \ddots & \vdots \\ Y_{N1} & \cdots & Y_{NN} \end{bmatrix}, [B] = \begin{bmatrix} Y_{1(N+1)} & \cdots & Y_{1M} \\ \vdots & \ddots & \vdots \\ Y_{N(N+1)} & \cdots & Y_{NM} \end{bmatrix},$$

$$[C] = \begin{bmatrix} Y_{(N+1)1} & \cdots & Y_{(N+1)N} \\ \vdots & \ddots & \vdots \\ Y_{M1} & \cdots & Y_{MN} \end{bmatrix},$$

$$[D] = \begin{bmatrix} Y_{(N+1)(N+1)} & \cdots & Y_{(N+1)M} \\ \vdots & \ddots & \vdots \\ Y_{M(N+1)} & \cdots & Y_{MM} \end{bmatrix}.$$

Then the values of the lumped circuit elements in the physics-based CAD model can be extracted as in [7].

Case Study

A typical structure of coupled non-parallel PCB traces is studied. Figure 1 shows the top view of the experimental board. Two microstrip lines are angled at 45 degrees. The width of each line is 3 mm and the length is 150 mm. The distance between near ends is 13 mm, but the distance between far ends is 127.8 mm. The lines are placed on a 1.6 mm thick FR4 substrate. The bottom layer is the entire ground plane. A PCB mounted SMA jack was placed at each end of the microstrip lines. The diameter of the via to fix the SMA jack was 1.27 mm. Four port S-parameters were simulated and measured using an Agilent HP8753D network analyzer to study the coupling between the two microstrip lines.

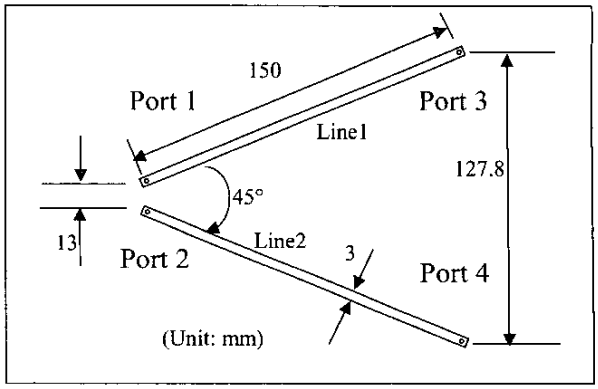

Figure 1: Top view of the coupled non-parallel PCB traces (microstrip lines).

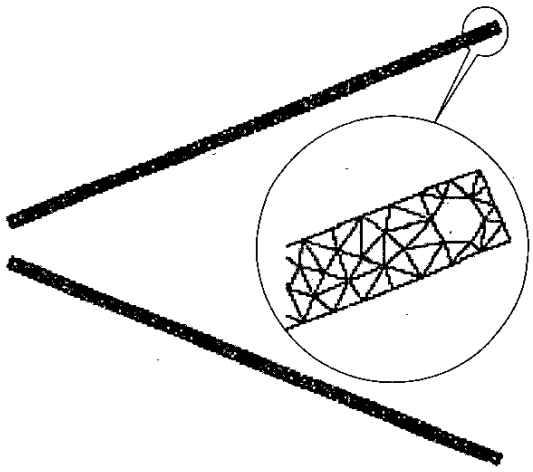

Figure 2: Mesh pattern for the CEMPIE modeling.

Triangular patches were used in CEMPIE to discretize the horizontal conducting plane and rectangular patches on the vertical conducting surfaces. Figure 2 shows the mesh pattern of the top layer for the CEMPIE modeling. There are two ways to deal with the bottom layer (ground plane)

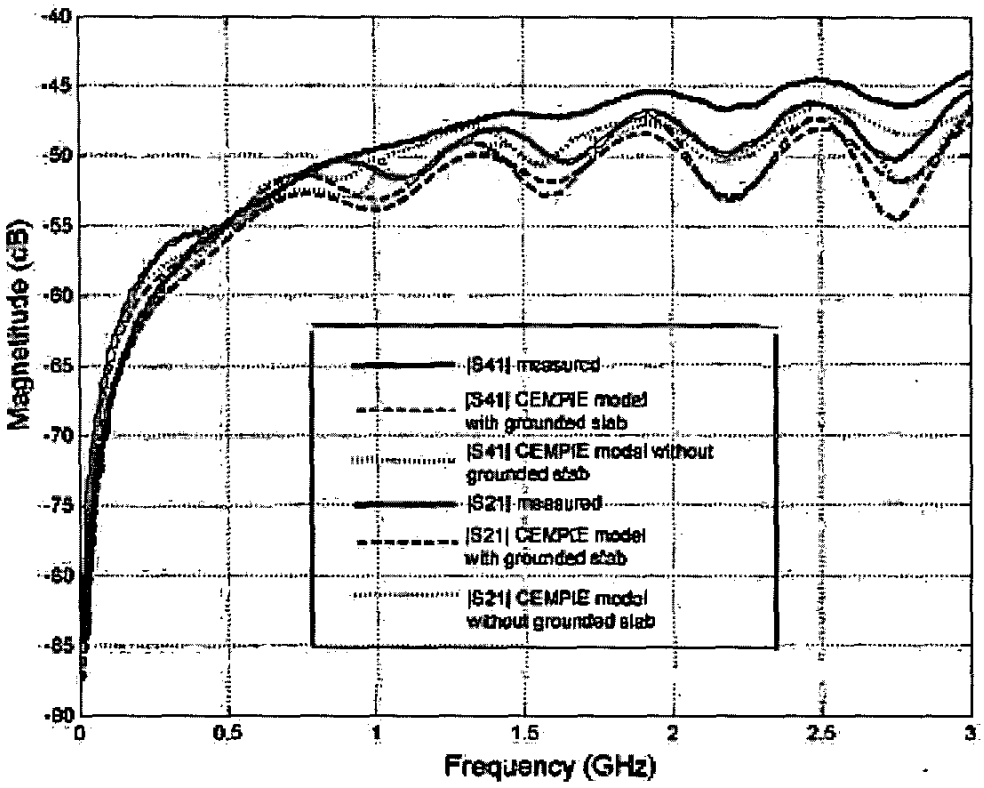

Figure 3: Magnitude comparison of the measured and modeled S-parameter results for the non-parallel microstrip lines shown in Figure 1.

in the CEMPIE procedure. The first one is to incorporate the ground plane into the Green's functions. The condition is that the ground plane can be considered as infinite. So the entire ground plane is one reference circuit node and the Green's functions for layered media with an infinite grounded slab are calculated. The benefit of this method is that it decreases the computational complexity, because the ground plane does not need to be meshed and the cell number is decreased. So the size of the matrix becomes smaller. The second method is more accurate, but time and memory consuming. All metal layers, including the ground plane, are meshed and partial elements between every two patches are calculated.

The S_{21} and S_{41} for the CEMPIE model and the measurement are compared in Figures 3 and 4. The agreement is good. The deviation is less than 3 dB for the CEMPIE model without an infinite grounded slab and the difference is less than 5 dB for CEMPIE model with an infinite grounded slab. The magnitude and the phase of the S-parameters indicate that the coupling between these two lines is dominated by lumped element physics near the end in proximity. As seen in Figure 3, $|S_{21}|$ and $|S_{41}|$ differ by less then 3 dB over the entire frequency range, and there is not a linear phase shift inherent in transmission-line coupling for S_{21}. The linear phase shift in S_{41} results from the propagation along the line 2 of the noise signal after coupling between the ports 1 and 2 that are in proximity.

Conclusion

The coupling of non-parallel PCB traces is being studied in this paper. The agreement between the CEMPIE model and measurement is achieved. The coupling is dominated by the lumped element physics at the near end. From this knowledge, simplified CAD models suitable for SPICE simulation can be developed

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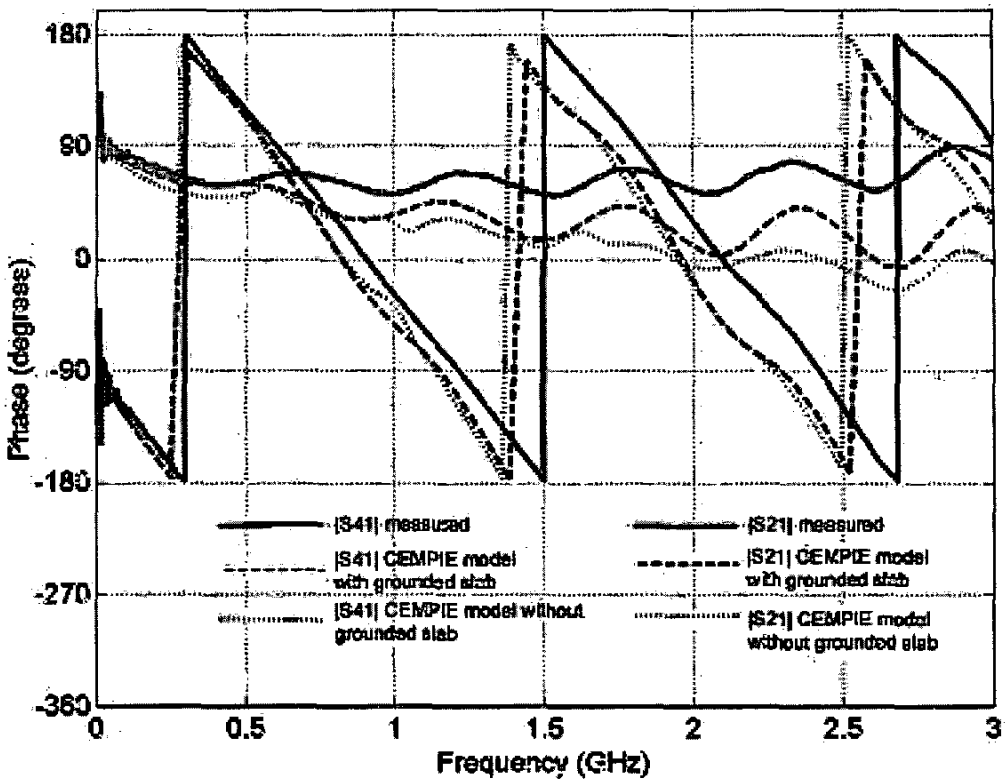

Figure 4: Phase comparison between the measured and modeled S-parameter results for the non-parallel microstrip lines shown in Figure 1.

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