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Modeling Power Bus Decoupling on Multilayer Printed Circuit Boards

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Abstract

Power bus decoupling designs on multilayer printed circuit boards must adequately account for the power bus interplane capacitance and its consequences for the design. Lumped element models for a power bus on a multilayer printed circuit board where an appreciable or entire portion of a layer is devoted to power and ground have been developed. The models are applicable below the distributed resonances of the board. Analytical, circuit simulation, and experimental studies have been conducted to test the models, investigate the effects of the distributed interplane capacitance of the power bus, and the effect of interconnect inductance associated with surface-mount decoupling capacitors.

1 Introduction

Noise is introduced on the power bus by the current demands of a switching digital device. This delta-I noise, or ground bounce, can cause faulty switching and EMI problems. Decoupling capacitors are typically added to the power bus in an attempt to mitigate this noise. Previous work has demonstrated, using lumped element modeling, difficulties with some commonly held design maxims for power bus decoupling [1]. With the widespread use of multilayer printed circuit boards (PCB), the interplane capacitance of the layers devoted to power and ground offers additional "pure" capacitance for decoupling. This capacitance is directly connected to the power pins of a device, without the interconnects associated with surface-mount decoupling capacitors. The potential benefits of this capacitance have been demonstrated experimentally [2].

In the present study, a lumped element model is developed for the power bus of a multilayer PCB. The noise voltage generated on the power bus by a low to high transition of a gate is related to the power bus impedance. It is shown that designing for low noise voltage can be achieved by proper design of the power bus impedance. The result is intuitive since ideally it is desirable to add only capacitance to the power bus without the parasitic interconnect inductance. Analytical and SPICE results are presented that demonstrate the effects of inductance associated with interconnects of surface-mount decoupling capacitors. The benefits of maximizing the power bus interplane capacitance are also shown. The validity of the lumped element model up to frequencies of several hundred megahertz is demonstrated experimentally. The

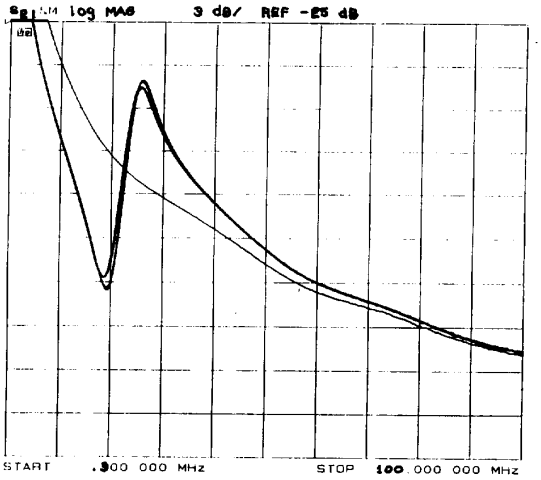

Figure 1: Experimental results of the power bus impedance ($| Z_B | = | S_{21} | + 28\ dB$) for a 7" × 8" 10 layer PCB with an interplane capacitance of 15.3 nF. A single 10 nF capacitor is placed at several locations covering the entire PCB, in each case through identical interconnect inductance and resistance.

effects of interconnect inductance are also demonstrated experimentally, and measurements of the interconnect inductance for several geometries are given. One particular geometry achieves a subnanohenry inductance.

2 Lumped Element Modeling

In a multilayer PCB with entire planes devoted to power and ground, the inductance associated with the planes is typically much smaller than the inductance of the interconnects of surface-mount decoupling capacitors or gates connected to the power plane. The total capacitance of the power bus, comprised of the power bus interplane capacitance plus all surface-mount capacitors, is then global, or shared by all devices connected to the power bus. For frequencies below the distributed resonances, the power bus can be modeled with lumped elements. The lumped element behavior of the power plane is illustrated with the measurements in Figure 1. Measurements of S_{21}, which will be shown to be related to the impedance of the power planes, are made on a 7" × 8" ten layer PCB with a single layer devoted to power. A 10 nF capacitor was connected at five different locations over the board through an iden-

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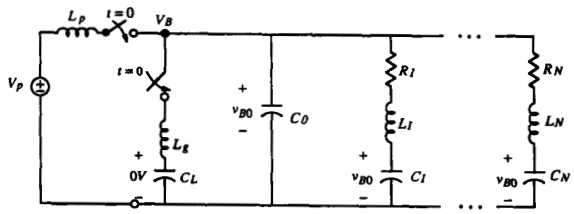

Figure 2: Lumped element model of a power bus on a multilayer PCB with surface-mount decoupling capacitors, a switching digital device, and power supply.

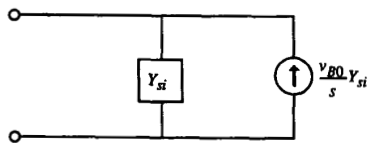

Figure 3: Equivalent current source and shunt admittance for the decoupling capacitor branch, with an initial voltage of v_{B0} on the capacitor.

tical inductance interconnect at all locations. As can be seen from the measurements, the $|\ S_{21}\ |$, is nearly identical, differing only as a result of two slightly varying values of the two nominal 10 nF capacitors employed. A lumped element approximation is therefore useful for frequencies below the transmission line resonances of the power bus. For PCBs with dimensions on the order of $6-10$" the applicable frequencies extend to $200-300\ MHz$.

A lumped element model of a power bus in a multilayer PCB is shown in Figure 2. The power supply is modeled as a DC supply with a series inductance. In order to apply linear time-invariant analysis techniques, the switching digital device is modeled simply as a series inductance with a capacitive load connected through a switch. The interplane capacitance of the power bus is modeled with C_o, and each surface-mount decoupling capacitor is modeled with a series RLC in shunt with the power bus capacitance. The inductance and resistance in the decoupling capacitor branch are associated with the traces and vias connecting the capacitor to the power bus. For 10 mil layers and single vias the values typically range from $2-10\ nH$ and $20-50\ m\Omega$ for inductance and resistance, respectively. Relative to these values of inductance, the incremental inductance of the power planes is negligible as can be discerned from the measurements in Figure 1. Simple parallel plate transmission line calculations yield an inductance on the order of $10^{-2}\ \frac{nH}{cm}$ for 10" wide boards with a 10 mil spacing.

Laplace transform techniques can be applied to the circuit of Figure 2 allowing for the initial conditions to be easily incorporated into the development. A series of transformations on the sources resulting from the initial conditions can be made to yield a current source with a shunt admittance for each decoupling capacitor branch as shown in Figure 3, where

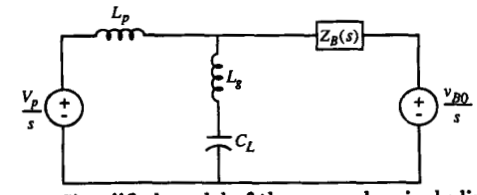

Figure 4: Simplified model of the power bus including the power supply and impedance of a switching device.

$$Y_{si} = \frac{1}{L_i}\ \frac{s}{s^2 + s\frac{R_i}{L_i} + \frac{1}{L_iC_i}} \tag{1}$$

and v_{B0} is the initial state of the bus voltage. The equivalent shunt current source and admittance for the interplane power bus capacitance is $C_o v_{B0}$ and sC_o, respectively. The parallel current sources and admittances can then be added and transformed to a voltage source $\frac{v_{B0}}{s}$ in series with an impedance

$$Z_B = \frac{1}{Y_B} = \left[sC_o + \sum_{i=0}^{N}\left(\frac{1}{L_i}\ \frac{s}{s^2 + s\frac{R_i}{L_i} + \frac{1}{L_iC_i}}\right)\right]^{-1} \tag{2}$$

where Z_B is defined to be the board impedance, i.e., the impedance seen looking into terminals at the power pins of a device. The resulting circuit including a simplified model of the switching device and power supply, as shown in Figure 4, is then easily analyzed to determine the voltage on the power bus as

$$V_B(s) = \left(\frac{1}{1 + \frac{Z_BZ_p}{Z_BZ_g + Z_pZ_g}}\right)\frac{v_{B0}}{s} \tag{3}$$

where s is the transform variable, Z_p is the power supply impedance, and Z_g is the impedance seen looking into the gate in the on state. For $Z_p >> Z_B$, Eq.(3) becomes

$$V_B(s) \simeq \left(\frac{1}{1 + \frac{Z_B}{Z_g}}\right)\frac{v_{B0}}{s} \tag{4}$$

Taking the inverse Laplace transform to obtain the bus voltage as a function of time yields

$$v_B(t) = \mathrm{L}^{-1}\left\{\frac{1}{1 + \frac{Z_B}{Z_g}}\right\} * v_{B0} \tag{5}$$

where L^{-1} denotes the inverse Laplace transform. The ringing on the power bus is then determined by the behavior of $1/\left(1 + \frac{Z_B}{Z_g}\right)$. In the frequency range up to several hundred megahertz this function is dominated by the poles of Z_B. Minimizing the ringing on the power bus in the time-domain corresponds to $1/\left(1 + \frac{Z_B}{Z_g}\right) \rightarrow 1$, which corresponds to minimizing the power bus impedance Z_B. The optimal decoupling strategy is then to add "pure" capacitance, then $Z_B = \frac{1}{j\omega C}$. Ideally for $Z_B \rightarrow 0$, the inverse Laplace transform of $V_B(s)$ then gives a constant value in time equal to the initial DC state of the

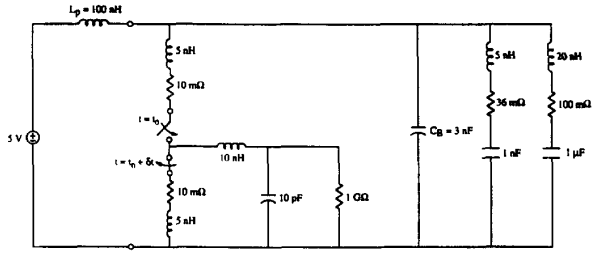

Figure 5: Lumped element circuit for SPICE simulations and $| Z_B |$ analysis.

bus. However, Z_B has numerous poles and zeros that alternate in frequency, and which are associated with the interconnect inductance of the surface-mount decoupling capacitors. The poles of Z_B correspond to ringing in the time-domain at the power bus lumped element resonances. A power bus design strategy for minimizing ground bounce for the frequency range over which the model is applicable (below approximately 300 MHz) is then to minimize the power bus impedance $| Z_B |$. A design strategy that minimizes $| Z_B |$ is pursued by reducing the series inductance of the surface-mount decoupling capacitor interconnects, maximizing the interplane power bus capacitance, and judiciously adding loss into the power bus design to reduce the Q of the poles of Z_B where necessary.

3 Analytical Results and SPICE Simulations

Extensive SPICE simulations have been pursued for the purpose of comparing the ring frequencies of the power bus noise with the pole frequencies of the power bus impedance Z_B. One such circuit model is shown in Figure 5. The low to high transition of a switching digital device is modeled as two switches which are simultaneously closed for $\delta t = 10\ ps$. The Fourier transform of the time-domain SPICE simulations are compared with the power bus impedance in Figure 6. The ring frequencies of the power bus voltage very nearly correspond to the poles of Z_B.

The effect of reducing the interconnect inductance from 5 nH to 2 nH in the high frequency decoupling branch is illustrated in Figure 7 for the circuit of Figure 5. In both Figures 7 and 8 the frequency response is plotted starting at 1 MHz. As a result of a zero at low megaherts frequencies, the pole at zero frequency is not plotted on these graphs. Reducing the interconnect inductance serves to move the associated pole to higher frequencies as well as reducing the Q associated with the pole. As a result, the frequency range over which the surface-mount capacitor provides effective decoupling is extended. At frequencies beyond the pole associated with a decoupling capacitor branch, the series impedance of the branch is dominated by the inductance. At higher frequencies, the decoupling capacitor is ineffective and the decoupling is provided by the interplane capacitance of the power bus, or other decoupling capacitors that have not gone through series and parallel resonance.

The effect of increasing the interplane capacitance of

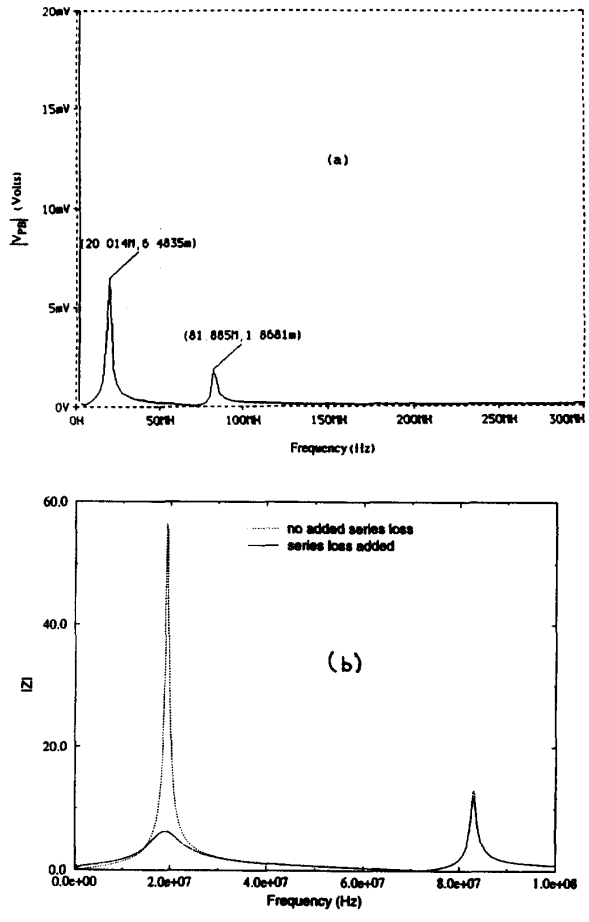

Figure 6: a) Fourier transform of SPICE simulation results for the noise voltage on the power bus, and b) the magnitude of the power bus impedance for the model of Figure 3 with (solid) and without (dashed) an added 1 Ω series resistance in the bulk decoupling branch.

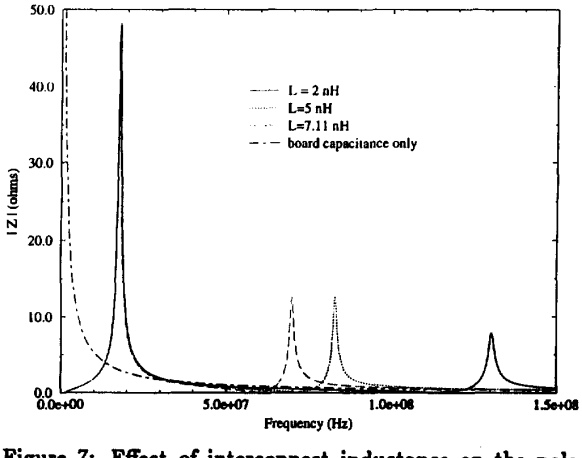

Figure 7: Effect of interconnect inductance on the pole frequency and Q.

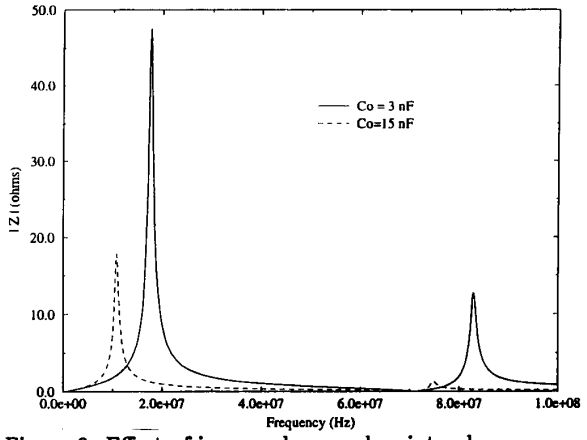

Figure 8: Effect of increased power bus interplane capacitance on the board impedance.

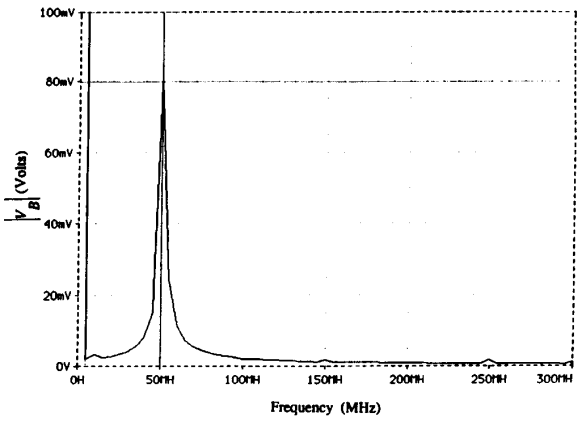

Figure 9: Results of SPICE simulations for $| V_B |$ for a periodic switching at a resonance frequency of Z_B.

the power bus is illustrated in Figure 8, where the $| Z_B |$ is shown for the circuit in Figure 5, with board capacitances of 3 nF, and 15 nF. These values of power bus interplane capacitance correspond to a segmented power plane versus entire planes devoted to power in a 7" x 8" PCB with 10 *mil* spacing. While the added capacitance is insufficient to make any difference for frequencies below approximately 1 MHz, Figure 8 shows that the high frequency decoupling can be significantly enhanced through this additional "pure" capacitance. While the case shown is simple the benefits at higher frequencies of maximizing the interplane capacitance is more general.

Values of capacitance in the 1 μF range added for low-frequency decoupling together with several nanohenries of interconnect inductance results in a pole in the board impedance function Z_B, as shown in Figures 6 (a) and (b), and hence the bus voltage. In both the bus voltage and impedance plots, the pole at approximately 20 MHz is a result of the interconnect inductance of the decoupling capacitor resonating with the interplane power bus capacitance. The Q of this pole can be potentially large compromising the noise performance of the power bus near the pole frequency. The Q of this pole can be reduced by adding series loss to the low-frequency decoupling branch as seen in Figure 6 (b).

The results of a SPICE simulation in Figure 6 (a) were for a single low to high transition. The resulting noise voltage on the power bus at the resonance frequency of the bus was on the order of a few millivolts. While this voltage is not significant, a greater difficulty occurs when a clock harmonic coincides with one of the resonant frequencies of the power bus. In this case a large noise voltage on the power bus can result. The Fourier transform of a SPICE simulation for a periodic switching of the circuit shown in Figure 5 is shown in Figure 9. In this case the 1 nF decoupling capacitor has been replaced by a 10 nF capacitor to yield a parallel resonance or pole frequency of 50 MHz. The circuit is switched with a period of 20 ns (corresponding to a fundamental frequency of 50 MHz to excite this power bus resonance. For both the low to high and high to low transitions both switches are closed simultaneously for a short time $\delta t = 10$ ps. The pulse

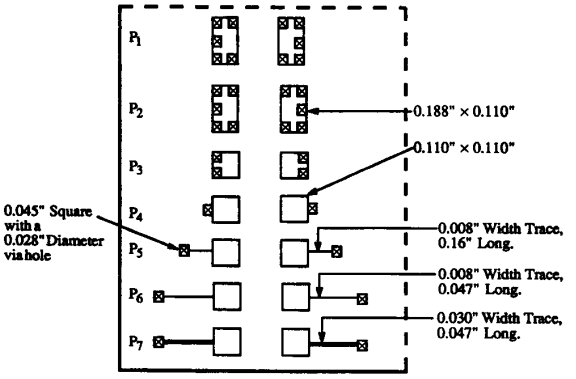

Figure 10: Geometry of the interconnects for the test board.

width of the switching waveform is 10 ns, with a period of 20 ns corresponding to a 50 MHz switching frequency. The noise voltage on the power bus in this case is 80 mV at 50 MHz, which is a result entirely of a switching frequency exciting one of the natural resonances of the power bus. For other switching frequencies the noise voltage at any frequency including bus resonance frequencies does not exceed 10 mV.

4 Experimental Results

The effects of interconnect inductance, series loss, and geometries for reducing interconnect inductance were investigated experimentally. Two-port measurements with an HP8753C were conducted on a specially designed 7" x 8", 10-layer, 10 *mil* layer-spacing board. A single layer was devoted to power with an interplane capacitance of 15.3 nF. The different interconnect geometries tested are shown in Figure 10. The test area comprised of the seven interconnect geometries shown was reproduced nine times over the entire area of the PCB. The ports of the network

Table 1: Interconnect Inductance Values

Interconnect	Resistance ($m\Omega$)	Inductance
P_2	12	0.61
P_3	17	1.32
P_4	22	2.00
P_5	54	7.11
P_6	95	15.7
P_7	53	10.3

analyzer were connected to the PCB power bus through low inductance interconnects P_1. The center conductor of a 0.085" coaxial cable probe was soldered to one bonding pad, and the outer shield soldered to the other. The PCB power bus impedance Z_B can be directly related to the measured S_{21} between the attached coaxial cable probes as

$$S_{21} = \frac{Z_B}{Z_B + \frac{1}{2}Z_o} \tag{6}$$

where Z_B is the PCB impedance, and $Z_o = 50\ \Omega$ is the characteristic impedance of the measurement system. For $Z_B \ll Z_o$, which is generally the case, except possibly at the parallel resonance frequencies,

$$| S_{21} | \simeq \frac{| Z_B |}{25} = (| Z_B | - 28)\, dB \tag{7}$$

In addition to measuring the PCB impedance with the HP8753C, the series resistance of the decoupling capacitor interconnects can be obtained from measurements of S_{11}. The interconnect inductance was obtained for each interconnect configuration by shorting the bonding pads with a wide connecting strap, and the resonance frequency measured. The interconnect inductance as well as series resistance for the six different configurations are shown in Table 1. One particular multi-hole interconnect geometry with the vias in the bonding pad resulted in a subnanohenry inductance. While the area of the bonding pads is greater than is typically employed, the advantage is an associated pole at a higher frequency, thereby extending the effective decoupling range of the capacitor, as well as a lower Q of the pole.

The effect of increasing interconnect inductance is shown in Figure 11 for a 10 nF capacitor attached to the PCB through interconnect inductances of 2.00, 1.32, and 0.61 nH, for traces (2), (3), and (4), respectively. Trace (1) is for the board with no surface-mount capacitor added, and is the 15.3 nF power bus interplane capacitance alone. For decreasing interconnect inductance, the pole associated with the decoupling branch shifts to a higher frequency, and the Q of the pole is decreased. In comparing the traces for an added decoupling capacitor with that of the bare board, it is seen that the surface-mount decoupling capacitor is not providing any decoupling for frequencies higher than the parallel resonance frequency associated with that decoupling branch. In this simple case the decoupling is provided entirely by the interplane capacitance of the power bus beyond the pole frequency of the decoupling branch. For numerous decoupling capacitors, the power bus interplane capacitance provides all the decoupling at frequencies above the last

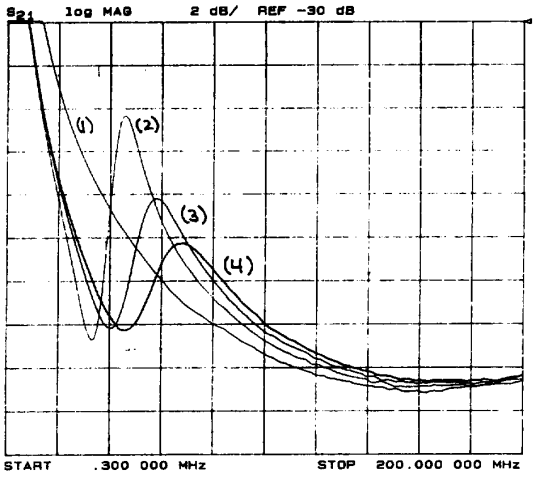

Figure 11: Measured results for interconnect inductances of 2.00 nH (2); 1.32 nH (3); and 0.61 nH (4).

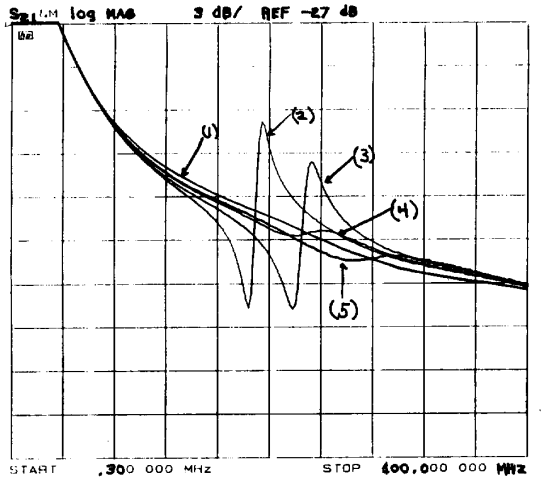

Figure 12: $| S_{21} |$ for low-loss versus lossy 1 nF capacitors connected through inductances of 10.3 and 7.11 nH of inductance.

parallel resonance. For large capacitance and interconnect inductance values, this resonance can easily occur below 100 MHz.

The effect of loss in the decoupling capacitor is demonstrated experimentally in Figure 12. The $| S_{21} |$ is shown for two types of 1 nF capacitors attached to the 15.3 nF power bus. Trace (1) shows the measured value for the bare board, and Traces (2) and (3) show the results for a low-loss capacitor attached through interconnects P_7 and P_5, respectively. The results for a higher loss capacitor attached through the same interconnect are shown in Traces (4) and (5). The Q of the pole is reduced significantly for the higher loss capacitor. In the time-domain, this loss causes the circuit to ring down faster. Adding loss to a decoupling branch may be of most benefit in the bulk or low-frequency decoupling branch. Here the loss can sig-

nificantly reduce the Q of the pole associated with this branch.

5 Summary

A lumped element model has been developed for decoupling on a multilayer PCB. The model is valid for frequencies below the distributed resonances of the power bus, which for PCBs on the order of $6 - 10$" is approximately $200 - 300\ MHz$. The noise voltage incurred on the power bus for a single low to high transition was related analytically to the power bus impedance. From these results it was shown that minimizing the noise on the power bus corresponded to minimizing the power bus impedance. SPICE simulations support these results and demonstrated that switching at a frequency corresponding to a resonance of the power bus resulted in significant noise voltage at that frequency.

Experimental results supported the analytical conclusions. The effect of interconnect inductance on the board impedance was demonstrated, and measured values of inductance for several interconnects were presented. The benefit of a small amount of loss was also shown, which may be of greatest benefit for low-frequency decoupling.

Power bus designs on multilayer PCBs, where entire layers are devoted to power and ground, achieve the best noise performance over the widest range of frequencies then by minimizing the interconnect inductance and maximizing the interplane capacitance of the bus. Experimental results show that the location of the decoupling capacitor is not critical to performance in the frequency range below several hundred megahertz (where a lumped element model is valid). Decoupling capacitors can then be placed in an area that will allow for minimal inductance interconnects.

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