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Reduced-Parts-count Multilevel Rectifiers

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***Abstract*—Multilevel power converters have gained much attention in recent years due to their high power quality, low switching losses, and high-voltage capability. These advantages make the multilevel converter a candidate topology for the next generation of naval ship prolusion systems. The primary disadvantage of these systems is the large number of semiconductors involved. This paper presents a reduced-parts-count rectifier which is well suited for naval rectifier applications where bidirectional power flow is not required. The proposed converter is analyzed and experimentally verified on an 18-kW four-level rectifier/inverter system.**

***Index Terms*—Four-level converters, multilevel converters, multilevel rectifiers, reduced parts count.**

I. Introduction

THE general trend in power electronics has been to switch power semiconductors at increasingly high frequencies in order to minimize harmonics and reduce passive component sizes. However, the increase in switching frequency increases the switching losses which become significant at high power levels. Several methods for decreasing switching losses and, at the same time improving power quality, have been proposed including constructing resonant converters and multilevel converters [1].

Resonant converters avoid switching losses by adding an *LC* resonant circuit to the hard switched inverter topology. The inverter transistors can be switched when their voltage or current is zero, thus mitigating switching losses. Examples of this type of converter include the resonant dc link [2], and the auxiliary resonant commutated-pole inverter (ARCP) [3], [4]. One disadvantage of resonant inverters is that the added resonant circuitry will increase the complexity and cost of the converter control. Furthermore, high insulated gate bipolar transistor (IGBT) switching edge rates can create switch-level control problems.

Multilevel converters offer another approach to providing high power quality. In particular, these converters offer a high number of switching states so that the output voltage can be "stepped" in smaller increments [5]–[11]. This allows mitigation of harmonics at low switching frequencies, thereby reducing switching losses. In addition, electromagnetic compatibility (EMC) concerns are reduced through the lower common mode current facilitated by lower dv/dt's produced by the smaller voltage steps. One disadvantage of these techniques is that they require a high number of switching devices. Although the devices are rated at a lower voltage, gate drive and control circuitry must still be provided. The primary disadvantage of multilevel inverters is that they must be supplied from isolated dc voltage sources or a bank of series capacitors with balanced voltages. In systems where isolated dc sources are not practical, capacitor voltage balancing becomes the principal limitation for multilevel converters.

Considering the advantages of multilevel power conversion for high-voltage high-power applications, this technology appears suitable for future naval propulsion systems. As an example, the U.S. Navy's integrated power system (IPS) program involves a land-based engineering site (LBES) which consists of a rectifier/inverter setup. The rectifier is an uncontrolled three-phase topology for converting the generator voltage (4160 V, 60 Hz) to a dc voltage of 6000 V. The inverter is a 15-phase H-bridge system which supplies a 19-MW induction motor [12]. This system is particularly suitable for four-level rectifier/inverter power conversion considering 3.3-kV IGBTs.

Research in the area of multilevel rectifiers has involved reducing the number of IGBTs required for a three-level rectifier [13], [14]. By this method, the rectifier cost can be reduced. However, the performance is limited. In this paper, an alternate method of reducing the number of IGBTs is presented. The new method is applicable to rectifiers with any number of voltage levels. The analysis is presented and it is shown that the performance limitation is less severe for rectifiers involving four or more voltage levels. The proposed rectifier is experimentally verified on a four-level laboratory rectifier/inverter system.

II. Four-Level Drive System Description

Fig. 1 shows the four-level rectifier/inverter system described herein. The fixed-frequency ac source and input inductors may represent a utility grid or a synchronous generator on a naval ship power system. The four-level rectifier and associated control ensures that the capacitor dc voltages v_{c1}, v_{c2}, and v_{c3} are identical. With these voltages balanced, the four-level inverter and associated control can properly supply the induction motor with high power quality waveforms. The induction motor is a standard NEMA type B industrial design having a well-established model [15]. Since the power electronic conversion is the main focus of this paper, details of the machine equations will not be included here.

A. Four-Level Converter

Herein, the term converter will be used to describe any power electronic conversion device. Specific terms such as rectifier or inverter are used to specify a particular converter. Fig. 2 shows the topological detail of the four-level inverter. Despite the high number of switching devices, the power converter operation is

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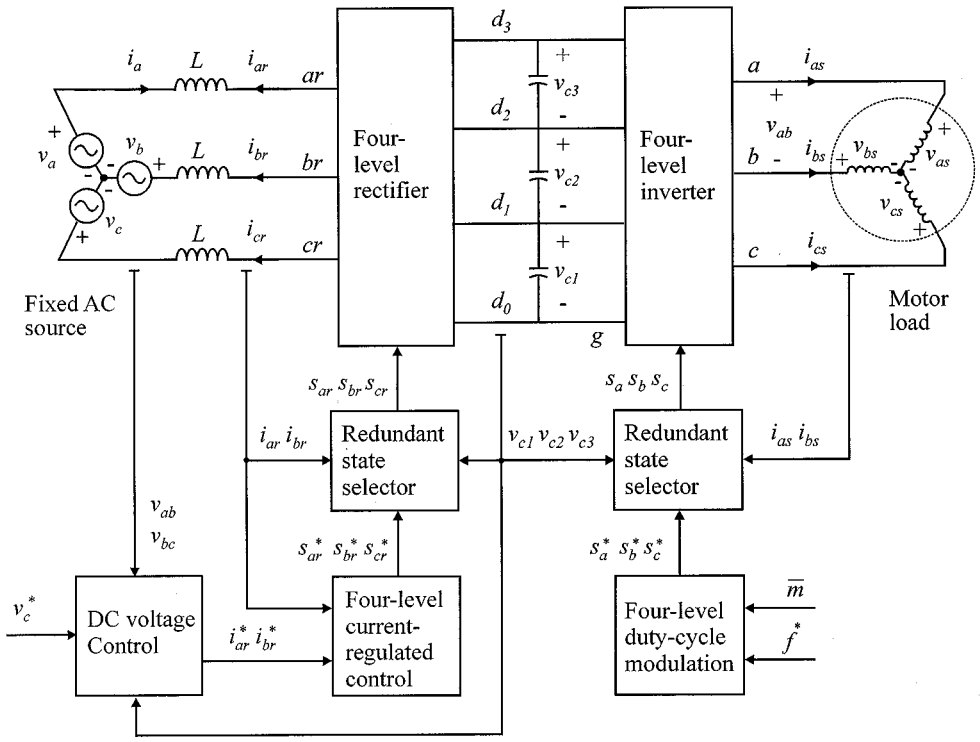

Fig. 1. Four-level rectifier/inverter system and associated control.

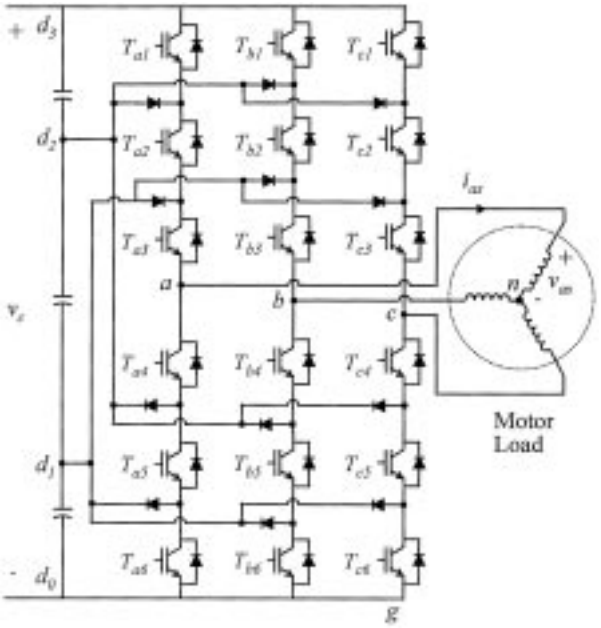

Fig. 2. Four-level inverter topology.

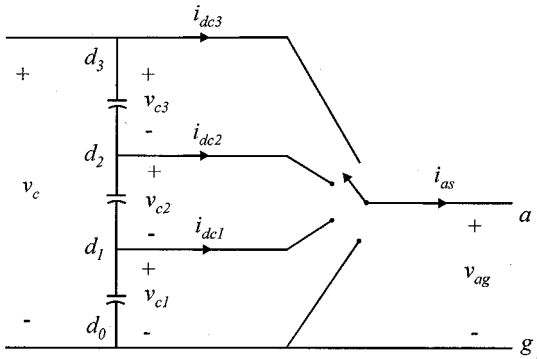

Fig. 3. Four-level inverter a-phase equivalent switching.

fairly straightforward. Each phase of the inverter or rectifier can be connected to the points d_0, d_1, d_2, or d_3 through suitable switching of the converter transistors [5]–[11]. The resulting operation is similar to that of a positional switch as shown in Fig. 3 for the inverter a phase. The inverter line-to-ground voltage for a particular phase is determined from the switching state and capacitor voltages by

$$v_{xg} = \sum_{i=0}^{s_x} v_{ci} \tag{1}$$

where x represents the phase and may be a, b, or c. The switching state s_x in (1) is determined by the pulsewidth modulation (PWM) control and has the values 0, 1, 2, or 3 for the four-level inverter. Since the induction motor is wye connected, it can be shown that the motor voltages are related to the inverter line-to-ground voltages by [15]

$$v_{as} = \frac{2}{3}v_{ag} - \frac{1}{3}v_{bg} - \frac{1}{3}v_{cg} \tag{2}$$

$$v_{bs} = \frac{2}{3}v_{bg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{cg} \tag{3}$$

$$v_{cs} = \frac{2}{3}v_{cg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{bg}. \tag{4}$$

The four-level rectifier structure is identical to that of the four-level inverter. As with the inverter, the phases ar, br, and cr, may be connected to any of the capacitor junctions d_0, d_1, d_2, or d_3 resulting in similar phase-to-ground voltages of

$$v_{xrg} = \sum_{i=0}^{s_{xr}} v_{ci} \tag{5}$$

where s_{xr} represents the rectifier phase x switching state. The ac supply voltages are then calculated from

$$v_{ar} = \frac{2}{3}v_{arg} - \frac{1}{3}v_{brg} - \frac{1}{3}v_{crg} \tag{6}$$

$$v_{br} = \frac{2}{3}v_{brg} - \frac{1}{3}v_{arg} - \frac{1}{3}v_{crg} \tag{7}$$

$$v_{cr} = \frac{2}{3}v_{crg} - \frac{1}{3}v_{\mathrm{arg}} - \frac{1}{3}v_{brg}. \tag{8}$$

Voltages (6)–(8) are defined from the rectifier phases to the neutral connection of the source.

B. Duty-Cycle Modulation

The goal of duty-cycle modulation is to regulate the inverter switching states s_x so that the desired motor voltages v_{as}, v_{bs}, and v_{cs} are obtained. The desired motor phase voltages may be expressed as

$$v_{as}^* = \sqrt{2}v_s^* \cos(\theta_c) \tag{9}$$

$$v_{bs}^* = \sqrt{2}v_s^* \cos\left(\theta_c - \frac{2\pi}{3}\right) \tag{10}$$

$$v_{cs}^* = \sqrt{2}v_s^* \cos\left(\theta_c + \frac{2\pi}{3}\right) \tag{11}$$

where v_s^* is the desired rms voltage magnitude and θ_c is the desired electrical angle including phase shift which may be expressed

$$\theta_c = \theta_e + \phi_v. \tag{12}$$

The electrical angle can be related to a desired electrical frequency by

$$\theta_e = 2\pi \int_0^t f^* d\tau. \tag{13}$$

It can be seen from (1), that the PWM switching has direct control of the inverter line-to-ground voltages v_{ag}, v_{bg}, v_{cg}. However, from (2)–(4) it can be seen that it is not possible to directly solve for commanded line-to-ground voltages from commanded motor phase voltages. This is the case since zero-sequence components of v_{ag}, v_{bg}, and v_{cg} will cancel in (2)–(4). In a three-phase system, the zero-sequence components of v_{ag}, v_{bg}, and v_{cg}, include dc offset and any triplen harmonics of θ_e. It has been demonstrated that adding a certain amount of third-harmonic content to the line-to-ground voltages can maximize the inverter output voltage [16]. In particular, maximum inverter voltage utilization is achieved if the commanded line-to-ground voltages are set to

$$v_{ag}^* = \frac{v_c}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \tag{14}$$

$$v_{bg}^* = \frac{v_c}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{15}$$

$$v_{cg}^* = \frac{v_c}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{16}$$

where v_c is the sum of the capacitor voltages

$$v_c = v_{c1} + v_{c2} + v_{c3} \tag{17}$$

and m is the modulation index having a range of

$$0 \le m \le \frac{2}{\sqrt{3}}. \tag{18}$$

It is often convenient to define a modulation index that has a range from 0% to 100% by

$$\overline{m} = \frac{\sqrt{3}}{2}m. \tag{19}$$

The motor phase voltage resulting from the commanded line-to-ground voltages can be determined by substituting (14)–(16) into (2)–(4) yielding

$$v_{as} = \frac{mv_c}{2}\cos(\theta_c) \tag{20}$$

$$v_{bs} = \frac{mv_c}{2}\cos\left(\theta_c - \frac{2\pi}{3}\right) \tag{21}$$

$$v_{cs} = \frac{mv_c}{2}\cos\left(\theta_c + \frac{2\pi}{3}\right). \tag{22}$$

By comparing (20)–(22) to (9)–(11), it can be seen that the commanded voltages are obtained if the modulation index is set to

$$m = \frac{2\sqrt{2}v_s^*}{v_c}. \tag{23}$$

PWM switching is typically accomplished by defining duty cycles based on the normalized commanded line-to-ground voltages which may be expressed as

$$d_a = \frac{1}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \tag{24}$$

$$d_b = \frac{1}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{25}$$

$$d_c = \frac{1}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right]. \tag{26}$$

The inverter switching states s_x may be determined by comparing the duty cycles to multiple triangle waveforms [9], [11]. Alternatively, some drive systems utilize a digital signal processor (DSP) implementation in which definition of the triangle waveforms is not necessary. As an example, consider the a-phase switching state. The first step is to integerize the duty cycle to determine the nearest switching states

$$l_a = \mathrm{INT}(3d_a) \tag{27}$$

where INT is the integerization function which will return the nearest integer less than or equal to its argument. The nearest switching states are then $s_a = l_a$ and $s_a = l_a + 1$. If the clock frequency of the controller is T_s, then the a-phase switching states for one DSP cycle are

$$s_a = \begin{cases} l_a + 1, & 0 \le t < t_a \\ l_a, & t_a \le t \le T_s \end{cases} \tag{28}$$

where

$$t_a = (3d_a - l_a)T_s. \tag{29}$$

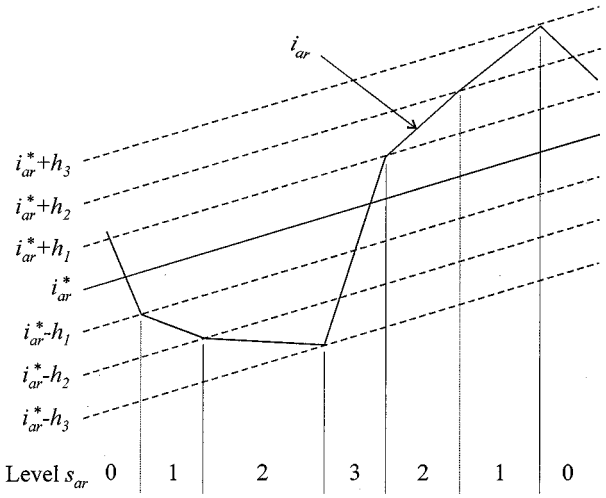

Fig. 4. Four-level current-regulated control switching.

The b- and c-phase switching states are computed in a similar manner. Typically, the switching frequency is set to roughly 100 times the fundamental frequency $(1/T_s > 100f^*)$.

C. Hysteresis Current Regulator

The multilevel hysteresis current regulator is based on defining a set of $n-1$ hysteresis levels, n being the number of converter voltage levels. Denoting the maximum allowable excursion of the actual current from the desired current as the largest hysteresis level $h_{(n-1)}$, the remaining $n-2$ hysteresis levels are computed from

$$h_j = \frac{j}{n-1} h_{(n-1)}, \qquad j = 1, 2, \ldots, (n-2). \tag{30}$$

Four the four-level rectifier, $n = 4$ and thus three hysteresis levels are defined. The current error for a particular phase is defined by

$$i_{x\text{rerr}} = i_{xr}^* - i_{xr}. \tag{31}$$

When the current error is positive, the controller decreases the level of phase x by one each time the error crosses a hysteresis level. Likewise, the phase level is increased when the current error is negative and crosses a hysteresis level. Fig. 4 shows an example reference current and a-phase current for the four-level rectifier. The a-phase voltage level is shown to illustrate the converter switching. As can be seen, the primary goal of the rectifier switching is to regulate the current. Capacitor voltage balance is achieved through redundant state selection described in Section II-D.

D. Redundant State Selector

In order for the four-level power conversion processes (rectifier and inverter) to operate properly, the voltages on all three capacitors must be equal. However, current drawn from the junctions d_1 and d_2 will tend to unbalance the capacitor voltages. Assuming that the capacitor voltage error is small, redundant switching states can be used which result in the same ac load voltages but have different effect on the charging and discharging of the capacitors [10], [11]. For the four-level inverter, the problem may be reduced to four cases defined by the number of capacitors that the phases are connected across [10]. Fig. 5 shows examples of the four cases. The redundant switching states of these cases may be found by incrementing or decrementing the switching states of all three phases. For example, case 0 is obtained by setting $(s_a = 1, s_b = 1, s_c = 1)$. The induction motor voltages will be the same if the redundant states $(s_a = 0, s_b = 0, s_c = 0)$ or $(s_a = 2, s_b = 2, s_c = 2)$ or $(s_a = 3, s_b = 3, s_c = 3)$ are used. However, for case 0, the redundant states do not change the currents drawn from the capacitor junctions. Therefore, redundant state selection is not applied to case 0. From Fig. 5, it can be seen that the switching state $(s_a = 2, s_b = 1, s_c = 1)$ will charge or discharge capacitor voltage v_{c2} depending on the direction of the a-phase current. This is an example of case 1 where the phases are connected across one capacitor. If the a-phase current is positive the phases will tend to discharge the capacitor and the phases should be connected across the capacitor with the highest voltage by selecting between the appropriate redundant states which in this example are $(s_a = 1, s_b = 0, s_c = 0)$ and $(s_a = 3, s_b = 2, s_c = 2)$. If the a-phase current is negative, the phases should be connected across the capacitor with the lowest voltage. There are two ways in which the phases may span two capacitors. These are shown in Fig. 5 as "case 2a" and "case 2b." As can be seen, case 2a has the potential to change the voltages on any capacitor. A decision about the most appropriate redundant state for this case should be based on the primary goal of controlling the voltage v_{c2} and a secondary goal of controlling the voltages v_{c1} and v_{c3}. The purpose of these goals is that the connection of the motor phases to the capacitor junctions will tend to discharge the center capacitor when commanding high load voltage [10], [11]. From the example shown in Fig. 5, it can be seen that the c-phase current direction will determine the center capacitor charge or discharge for the state shown $(s_a = 3, s_b = 2, s_c = 1)$. For the redundant state $(s_a = 2, s_b = 1, s_c = 0)$, the a-phase current will depict the capacitor charge or discharge. In the event that neither state improves the center capacitor voltage balance, the decision is made based on capacitor voltages v_{c1} and v_{c3}. Case 2b in Fig. 5 will not assist in controlling the center capacitor voltage since the state shown $(s_a = 3, s_b = 1, s_c = 1)$ and the redundant state $(s_a = 2, s_b = 0, s_c = 0)$ have the same charging or discharging effect on v_{c2}. In this case, the redundant state could be used to balance the capacitor voltages v_{c1} and v_{c3}. However, this imbalance is typically not a difficulty and redundant state selection in this case will only increase the switching frequency [10]. There are no redundant states that correspond to case 3 and, therefore, redundant state selection is not applied.

All cases discussed above can be analyzed offline and programmed as a table into an erasable programmable read-only memory (EPROM) or erasable programmable logic device (EPLD). Based on the direction of the desired switching state (s_a^*, s_b^*, s_c^*), the phase currents and capacitor voltages, the memory or logic device will select the appropriate state [10]. The redundant state selector for the four-level rectifier is identical to that of the inverter.

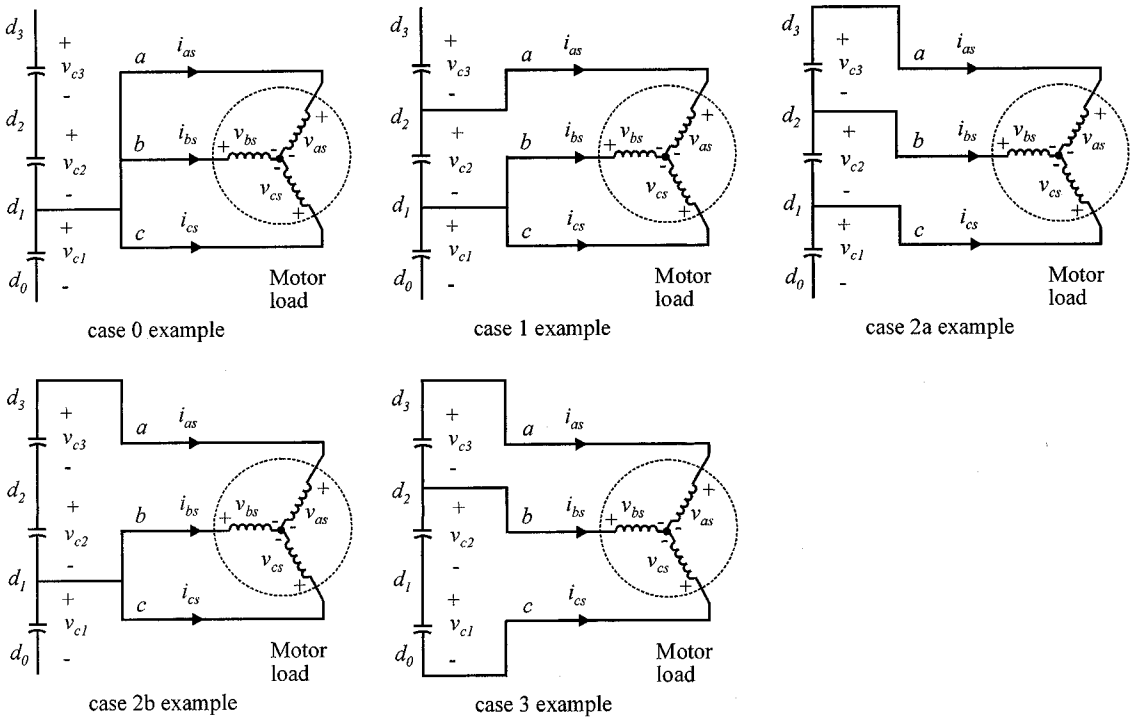

Fig. 5. Redundant state selection examples.

E. DC-Link Voltage Control

The overall dc-link voltage v_c is regulated through standard synchronous current regulation [17]. The source voltages may be described by

$$v_a = \sqrt{\frac{2}{3}} V_{LL} \cos(\theta_u) \tag{32}$$

$$v_b = \sqrt{\frac{2}{3}} V_{LL} \cos\left(\theta_u - \frac{2\pi}{3}\right) \tag{33}$$

$$v_c = \sqrt{\frac{2}{3}} V_{LL} \cos\left(\theta_u + \frac{2\pi}{3}\right) \tag{34}$$

where θ_u is defined as the voltage source electrical angle or "utility" angle and V_{LL} is the rms magnitude of the utility voltages. Transformation to the utility reference frame yields a q-axis voltage equal to the peak phase voltage and a d-axis voltage equal to zero [15]. For unity power factor operation, it is necessary to command the d-axis rectifier current to zero. The q-axis current can be used to regulate the dc link voltage resulting in commanded currents of

$$i_{qr}^{u^*} = -K_p e_v - K_i \int_0^t e_v d\tau \tag{35}$$

and

$$i_{dr}^{u^*} = 0 \tag{36}$$

where the constants K_p and K_i are the controller proportional and integral gains respectively. The error term e_v is the dc voltage error defined by

$$e_v = v_c^* - v_c \tag{37}$$

where V_c^* is the commanded dc voltage. The inverse transformation necessary to determine i_{ar}^*, i_{br}^*, and i_{cr}^* relies on knowledge of the input electrical position θ_u. Methods for aligning the transformation to this reference frame include using a phase-locked loop, voltage sensors, or an online observer. For this system, the voltage sensor method was used. These sensors have the advantage of straightforward and accurate implementation and relatively low cost. Helpful transformation terms may be directly computed from the measured voltages as

$$\cos\left(\theta_u + \frac{\pi}{6}\right) = \frac{v_{ab}}{\sqrt{2} V_{LL}} \tag{38}$$

$$\cos\left(\theta_u - \frac{\pi}{2}\right) = \frac{v_{bc}}{\sqrt{2} V_{LL}}. \tag{39}$$

All necessary transformation terms can be determined from these terms using trigonometric identities [15]. Harmonics in the line voltages will appear in the sensor outputs, but may eliminated using a low-pass filter. Compensation for the filter amplitude attenuation and phase delay can be incorporated in the control software since the source voltage magnitude and frequency are known.

III. Reduced-Parts-Count Multilevel Rectifiers

A reduced-parts-count three-level rectifier was first introduced in 1993 [13]. The general idea behind this topology was a rearrangement of IGBTs and diodes in a thee-level rectifier to obtain the circuit shown in Fig. 6(a). Although not discussed in the literature, this topology is also valid for rectifiers with a higher number of voltage levels such as the four-level topology shown in Fig. 6(b). The general idea of the reduced-parts-count rectifier proposed herein is that the uppermost and lowermost IGBTs in the multilevel structure may not be necessary for

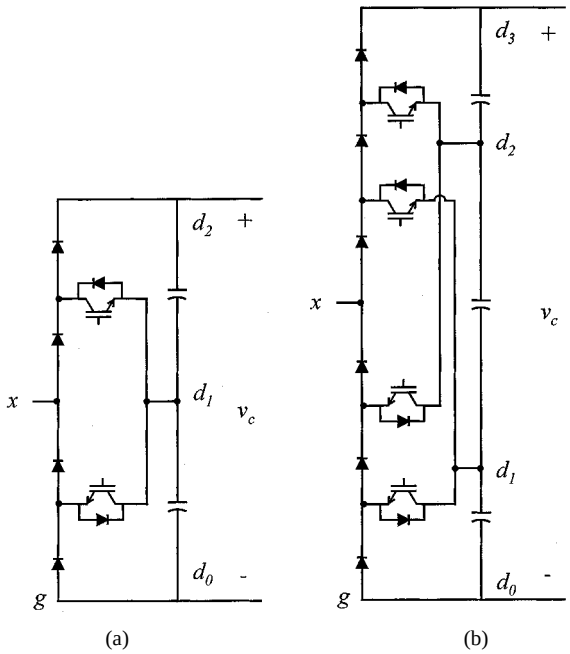

Fig. 6. Reduced-parts-count rectifier topologies.

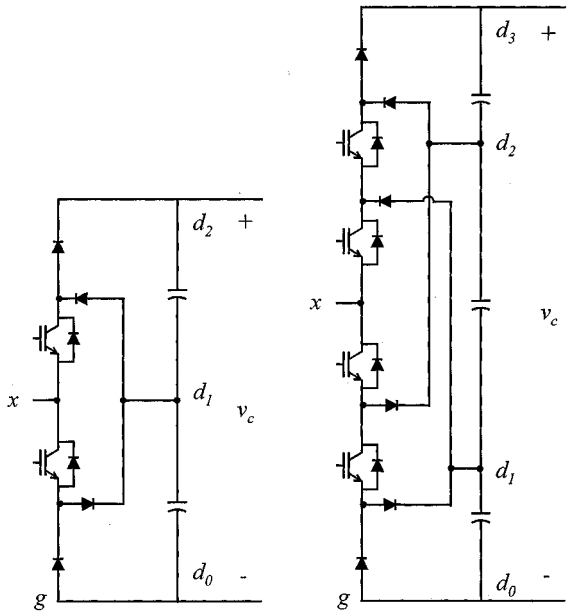

Fig. 7. Proposed reduced-parts-count rectifier.

rectifier operation. Fig. 7 displays the proposed topology for the three- and four-level case (although the circuit is valid for any number of voltage levels). The circuit is also valid for other switching devices (such as integrated gate-commutated thyristors (IGCTs) or MOSFETs). The performance of the rectifier circuits shown in Fig. 7 is identical to those shown in Fig. 6 when considering switching states. However, there is an important difference to note when the number of voltage levels is greater than three. For the four-level circuit shown in Fig. 6, the inner most IGBTs require a rating of $(2/3)v_c$, whereas the outermost IGBTs require a voltage rating of $(1/3)v_c$. The imbalance of voltage ratings precludes the use of dual IGBT modules in this topology. For high-voltage applications, two

TABLE I
NUMBER OF RECTIFIER SWITCHING COMPONENTS

Voltage Levels	Fully- Active Rectifier	Reduced-Parts Count Rectifier
3	12	6
4	18	12
5	24	18
6	30	24

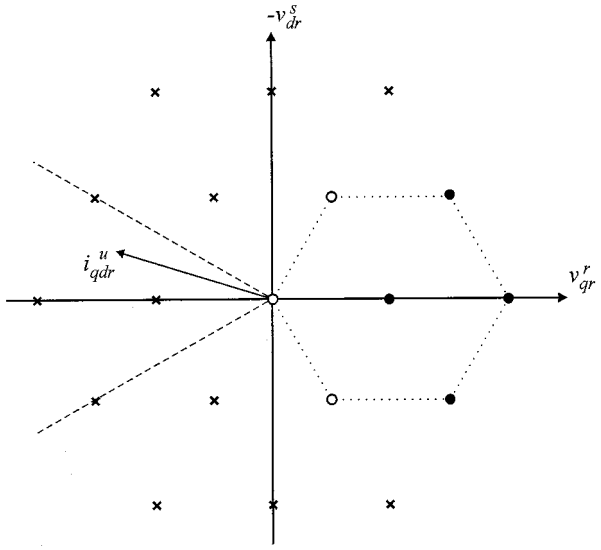

Fig. 8. Voltage vector plot for the three-level rectifier.

IGBTs in series may be used for the high-voltage IGBTs. However, this solution increases the parts count to that of a fully active four-level rectifier. In the proposed four-level topology, the innermost diodes must be rated at $(2/3)v_c$. This is not much of a problem compared to high-voltage IGBTs since locating high-voltage diodes or series-connecting diodes is straightforward. It should be pointed out that this voltage rating problem becomes more significant for higher level topologies.

Table I shows the number of IGBTs required for the fully active multilevel rectifier and the reduced-parts-count rectifier assuming a three-phase system. As can bee seen, the IBGT savings effectively allows higher level operation with the same number of IGBTs as a fully active rectifier having a lower number of voltage levels. Naval propulsion systems typically involve a large number of phases for redundancy. In this case, the semiconductor savings is even greater than that of a three-phase system.

The primary concern with reduced-parts-count rectifier is the limitation on performance due to the reduced number of transistors. This is usually a function of the power factor on the input and can be evaluated by plotting the rectifier voltage vectors [13], [14] obtainable by transforming (6)–(8) to the stationary reference frame [6]–[8]. Fig. 8 shows the rectifier voltage vectors for the three-level rectifier. The current vector in the utility reference frame is also shown on the vector plot. This is obtained by transforming the rectifier currents i_{ar}, i_{br}, and i_{cr} to the utility reference frame and then defining the vector as

$$i_{qdr}^{u} = i_{qr}^{u} - j i_{dr}^{u}. \tag{40}$$

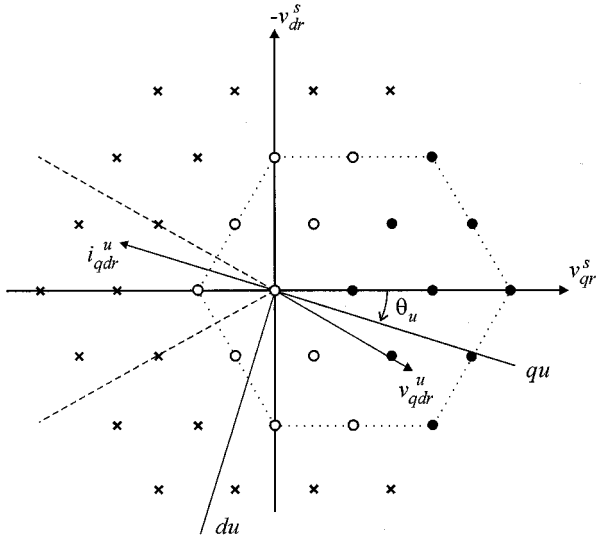

Fig. 9. Voltage vector plot for the four-level rectifier.

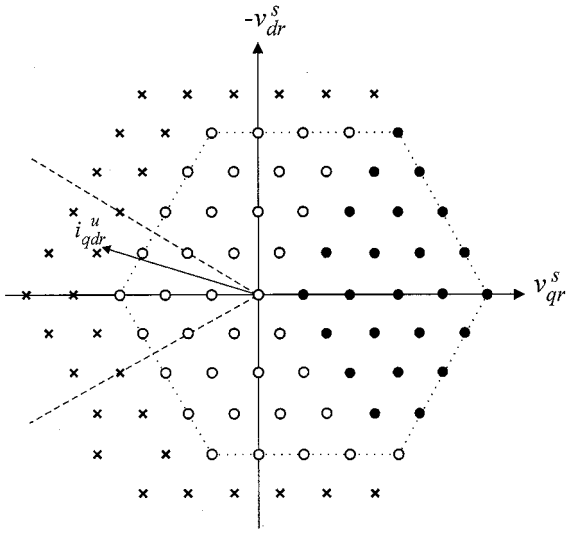

Fig. 10. Voltage vector plot for the six-level rectifier.

Consider the case where the current vector lies between the dashed lines as shown in Fig. 8. In this case, the a-phase current is negative and the lowest voltage level is not available in this phase due to the absence of the transistor. Likewise, the b- and c-phase currents are positive which excludes the highest voltage level for these phases. For this reason, the voltage vectors marked with an $\mathbf{x}$ are not available when the current vector is in this region. The remaining voltage vectors are available for use by the modulation. However, all redundant states are not available for the vectors indicated by the open circles. The resulting area available for voltage synthesis is indicated by the dotted hexagon. Figs. 9 and 10 show similar voltage vector plots for four- and six-level rectifiers respectively. As can be seen, a wider area is opened up for voltage synthesis as the number of voltage levels is increased.

In order to determine the limitation imposed on the reduced-parts-count rectifier, consider the case of the four-level rectifier with the voltage vector plot shown in Fig. 9. Therein, the utility reference frame axes qu and du are included along with the voltage vector v^u_{qdr}. In this case, the voltage vector must lie inside the dotted hexagon. The right-most edges of the hexagon are typical limitations due to the dc-link voltage. The primary limitation then becomes the bottom-most edge of the hexagon requiring that

$$v^s_{dr} \leq \frac{2\sqrt{3}}{9} v^*_c. \tag{41}$$

It would be useful to express this limitation as a function of the commanded current. This can be accomplished by transforming the rectifier input voltage and inductance to the utility reference frame. In the steady state, these equations become

$$v^u_{qr} = \omega_u L i^u_{dr} + v^u_q \tag{42}$$

$$v^u_{dr} = -\omega_u L i^u_{qr} + v^u_d \tag{43}$$

where ω_u is the utility radian frequency (the derivative of θ_u). In the utility reference frame,

$$v^u_q = \sqrt{\frac{2}{3}} V_{LL} \tag{44}$$

$$v^u_d = 0. \tag{45}$$

Since unity power factor is commanded, the d-axis utility reference frame current is set to zero and the q-axis current is regulated to a negative value as per (35) and (36). Using this information, and transforming the rectifier voltages to the stationary reference frame yields a d-axis voltage of

$$v^s_{dr} = -\sqrt{\frac{2}{3}} V_{LL} \sin(\theta_u) - \omega_u L i^{u^*}_{qr} \cos(\theta_u). \tag{46}$$

As can be seen from Fig. 9, the worst case operating condition, in terms of violating the voltage constraint, is when $\theta_u = -\pi/6$. Under these conditions, it can be seen from (41) and (46) than the limit on the commanded q-axis current is

$$\left| i^{u^*}_{qr} \right| \leq \frac{1}{\omega_u L} \left[\frac{4 v^*_c}{9} - \frac{\sqrt{2} V_{LL}}{3} \right]. \tag{47}$$

Equation (47) may be used to evaluate the suitability of the four-level reduced-parts-count rectifier under specific operating conditions. Notice that the limit is increased with increasing commanded dc voltage and decreasing input voltage. Furthermore, lower values of line inductance and voltage source frequency will increase the limit on q-axis current.

IV. Laboratory Verification

An 18-kW laboratory test system with the structure shown in Fig. 1 has been constructed for rectifier validation. The input source is a 60-Hz source with $V_{LL} = 421$ V and $L = 2.7$ mH. The rectifier control proportional plus integral (PI) gains are set to $K_p = 1$ A/V and $K_i = 10$ A/V $\cdot$ sec in order to regulate the dc-link voltage to $v^*_c = 660$ V. The hysteresis level has been set to $h_3 = 1$ A. The inverter modulation control parameters have been set to $\overline{m} = 0.98$ and $f^* = 100$ Hz. The induction motor parameters are show in Table II [15].

TABLE II
INDUCTION MACHINE PARAMETERS

$P = 4$	$M = 55$ mH
$r_s = 0.2\ \Omega$	$L_{ls} = 1.91$ mH
$r_r' = 0.326\ \Omega$	$L_{lr}' = 2.32$ mH

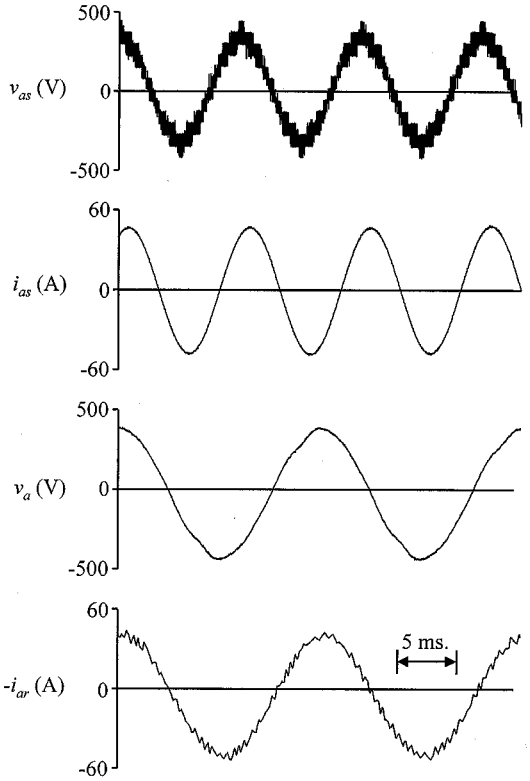

Fig. 11. Four-level system performance with fully active rectifier.

For the studies that follow, the induction motor is mechanically loaded using a synchronous generator. In this system, reduced-parts-count rectifier operation was obtained by gating off the uppermost and lowermost IGBTs in the rectifier.

Based on the parameters and operating conditions, it can be determined from (47) that the magnitude of the q-axis current must be limited to 93.2 A if a reduced-parts-count rectifier is used. With this current limitation and unity-power-factor operation, the rectifier input power is limited to 48 kW which is more than enough for the 18-kW load.

Figs. 11 and 12 show the system steady-state performance for the fully active rectifier and reduced-parts-count rectifier, respectively. Therein, the motor phase voltage v_{as}, phase current i_{as}, source voltage v_a, and rectifier current i_{ar} are shown. The rectifier current has been inverted so that unity power factor operation can be readily displayed. As can be seen, the performance of the reduced parts count rectifier is identical to that of the fully active rectifier. Capacitor voltage balance is ensured leading to even voltage steps in the motor phase voltage and high power quality.

Figs. 13 and 14 demonstrate the system performance under a step change in load for the fully active rectifier and reduced-parts-count rectifier respectively. In this study, the motor load is

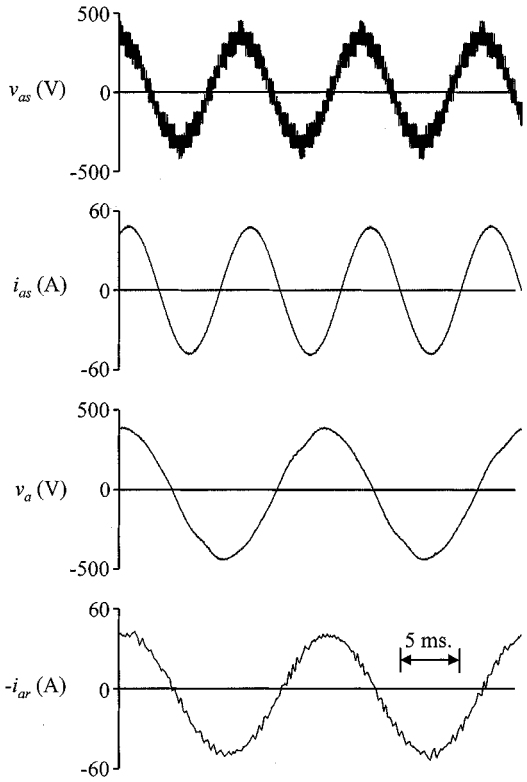

Fig. 12. Four-level system performance with reduced-parts-count rectifier.

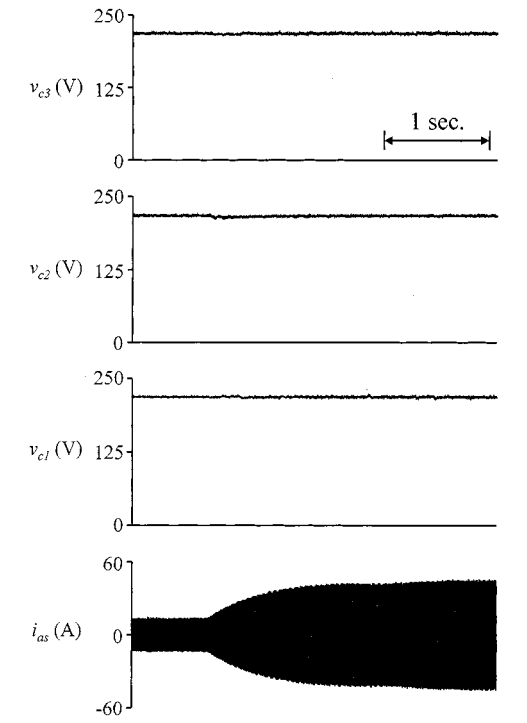

Fig. 13. Four-level system transient performance with fully active rectifier.

stepped from no-load to rated operation. The capacitor voltages v_{c1}, v_{c2}, and v_{c3} as well as the motor current i_{as} are shown. As can be seen, the PI regulator ensures capacitor voltage balance. It is also seen that the reduced-parts-count rectifier performance is the same as that of the fully active rectifier.

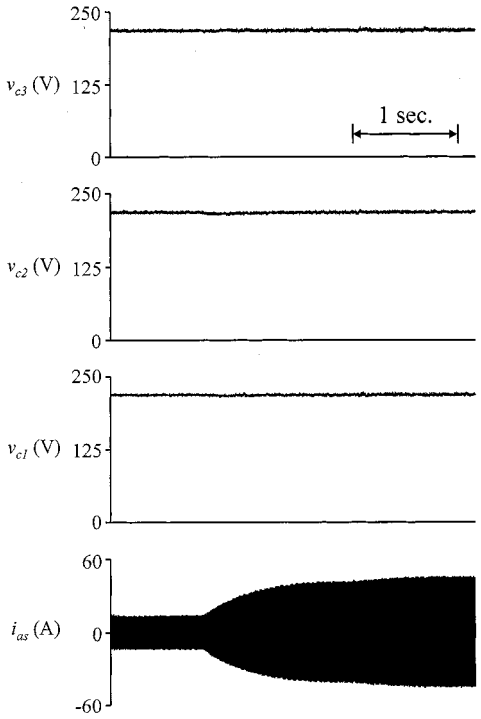

Fig. 14. Four-level system transient performance with reduced-parts-count rectifier.

V. Conclusion

A new type of reduced-parts-count multilevel rectifier has been introduced. The analysis is presented and it has been shown that there is no performance limitation for rectifiers where the voltage levels number four or greater. However, the operation is limited to unidirectional power flow, hence, making it suitable for naval propulsion system applications. Laboratory studies compare a four-level reduced-parts-count rectifier to a standard four-level rectifier and indicate identical performance. However, the reduced-parts-count rectifier utilizes 12 IGBTs, whereas the fully active rectifier utilizes 18.

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