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BIST Design for CCD based Digital Imaging System

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Abstract *– This paper presents a BIST design for CCD-based digital imaging system. Pixels on a CCD are not free from defective or faulty pixels due to numerous causes such as imperfect fabrication, excessive exposure to light, radiation, sensing element aging, and excessive mechanical shock, to mention a few. Today's high demand for high-resolution CCDs is dictating defect/fault- tolerance in such devices. Especially, traditional on-device BIST cannot be readily employed on the imaging devices such as CCD due to the unique requirement that no pixel can be utilized to repair or bypass a defect on any other pixels. Therefore, the BIST technique designed and simulated in this paper is a technique to test and repair the defects on pixels off the device, referred to as off-device tolerance. The basic idea was proposed in our previous work in [2] where the off-device defect/fault tolerance was investigated and a soft-test/repair technique was theoretically proposed in order to demonstrate the efficiency and effectiveness in terms of reliability, referred to as virtual yield. A Verilog-based design and simulation is provided to demonstrate the validity of the off-device soft-test/repair in terms of reliability (or virtual yield) enhancement and performance.*

Keywords *– CCD (Charge Coupled Device), defect/fault tolerance, soft-test/repair, BIST.*

I. INTRODUCTION

There are various causes for the pixel defects on CCD. Imperfect fabrication and improper processing may induce defects (referred to as *hard-defects*) on the photo-sensitive pixels and supporting system components in CCD. In [1], the main causes of CCD hard-defects are the target defects in this work.

A built-in self-test (BIST) circuitry is employed in order to demonstrate the validity of the proposed theoretical soft-testing/repair on the level of circuit design and simulation. The BIST performs a self-testing function online without intervention with the normal CCD operations. As the proposed BIST operates concurrently with the normal operations (i.e., on-line), it is expected to reduce the overall turnaround time for testing as well as the required normal operational time. In certain circumstances such as mission and safety critical military or medical image processing devices or systems, a stringent system turnaround time is dictated to guarantee the delay of image processing to stay within the required range. Therefore, the proposed on-line BIST is a right design choice to meet the requirements in such devices or systems.

For the purpose of cost-effectiveness, the BIST will be realized in the CCD controller that performs the normal operations in order to utilize the existing control modules as much as possible to maintain the complexity and overhead of the circuit within an economically-justifiable range. In order to address the performance issue, a parallel BIST architecture will be employed. This will enable the BIST to catch up with the possibly bulky data to be processed as the size of CCD increases. The cost will be justified versus its performance gain.

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Furthermore, various testing strategies will be developed in an effort to exploit various possible optimal testing algorithms under the pixel-defect distributions. The efficiency and effectiveness of the testing algorithms depend on various test-design factors such as test-scheduling, sampling of pixels for testing, and granularity of test-window, to mention a few. Each proposed testing algorithm will be evaluated with respect to the issues stated above and optimized in terms of the various test-design factors.

The objectives of the proposed design are to provide concurrent (or on-line) testing capability; to realize cost effectiveness by utilizing and sharing the existing CCD control circuitry; and to enhance the performance by employing parallel architecture.

This paper is organized as follows: In Section II, previous works are reviewed, and the proposed BIST architecture is presented. In Section III, the design and implementation of the proposed soft-test algorithm is presented. In Section IV, a parametric analysis with respect to CCD virtual yield and testing time. Conclusions and discussions are presented in Section V.

II. REVIEW AND PRELIMINARIES

The fault model simulated in this design is stuck high, stuck low, low sensitivity, and high sensitivity. As for the input test image for controlling the proposed fault model, an external test vector generator is employed to inject the test into the BIST.

The proposed method of manipulating the testing and repair process in a sequence of small windows of testing/repair enables to maintain the storage requirement for buffering the pixel defect information of the entire CCD to the size of a window. Therefore, each round of testing/repair process can detect and repair those pixels falling in the window, and as more test inputs injected the pixel defect-map will be cumulatively constructed in a flash memory and eventually become stabilized. Note that this is one of the novel features the proposed soft-testing can offer because the pixel-defect map is determined by the physical and permanent defects on the pixels on the CCD and they are finite, therefore the soft-testing routine is expected to end in a finite amount time. This lets the proposed soft-testing method substantially depart from the conventional off-line image filtering method, in which the filtering algorithms run against each different image off the processor and each different image downloaded must go through a new filtering process in an ad-hoc manner reaching no stabilized and finite database of the faults on the incoming supposedly infinite number of images.

Also, in order to validate the theoretical results on the impact of the distribution of the pixel defects on the yield, the random pixel defect distribution as was investigated in [2] will be simulated and tested by using the following distribution function as reported in [3] and the clustered pixel defect distribution as was investigated in [2].

Regarding the observability of the tests, the required amount of buffers for the test output signatures can be also only limited by the size of the window of testing/repair process. Each supposed-to-be normal test output signatures for each test input can be memorized in the BIST logic to test against the test output signatures either with a fault or not.

Furthermore, the testability of the soft-testing algorithms will be evaluated in order to sort out possible inability to detect a fault in the image mapped on the memory (so-called test escape) due to defects that hit on a or multiple pixels required to be normal for a complete fault detection process. The testability is defined as the probability to be able to detect a fault induced and mapped by a pixel defect on the CCD within a given testing/repair window. It will be analyzed that how many and which pixels to survive the defects for a normal soft-testing within a given window size; and in this regard the confidence-level of the soft-testing can be determined.

Regarding the controllability of the tests, the proposed BIST circuit cooperates with the CCD controller as shown in Figure (1). It is one n bit input and one n bit output system which are controlled by BIST. The captured input image is stored in a frame memory in Figure (1). Therefore, the BIST then access the stored input image for the controllability. The testing is performed through CCD controller by calculating the pixel values, which are stored in the frame memory. Note that the objective of the testing is CCD itself, not the memory. It is assumed that the memory is defect/fault-free.

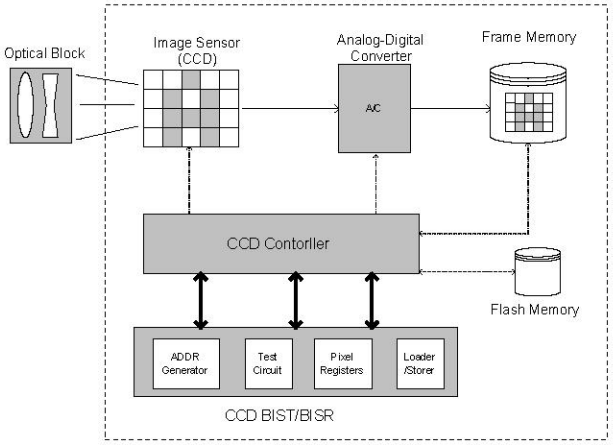

Fig. 1. BIST/BISR Architecture

In order to demonstrate the validity of the proposed theoretical soft-testing/repair[2] on the circuit design and simulation level, a testing circuitry is designed and presented as shown in Figure (1). The proposed BIST consists of the following primary modules. Address Generator, CCD Controller, Testing Circuit, Frame Memory, Flash Memory, Loader/Storer, and Pixel Registers.

Address generator computes an address to load a pixel value from the frame memory to a pixel register. The sequence of the addresses to be loaded is determined by the soft-testing/repair algorithm to be employed. The window size used in this work

as a criterion is 3×3 involving total 9 pixels' values.

The Loader/Storer reads a pixel value from the frame memory and writes in a pixel register, respectively. Note that one read/write port is used on the frame memory as an ordinary SRAM.

The frame memory is the primary storage for the image captured by the CCD. The size of the frame memory is determined by the resolution of the ADC and the number of pixels. For example, if the system uses a 12-bit ADC and a 6 Mega pixel CCD, then the size of the frame memory is 12×6 Mega bit.

The testing circuit computes the pixel values by the proposed testing algorithm, and in order to address the performance issue, a parallel BIST can be employed as to be detailed in Section IV.

The Pixel Registers hold the pixel values loaded from the frame memory and the test circuitry retrieves the stored pixel values from the pixel registers. A pixel register can be accessed from several test circuits simultaneously by the parallel BIST. The proposed BIST-based architecture is shown in Figure (2).

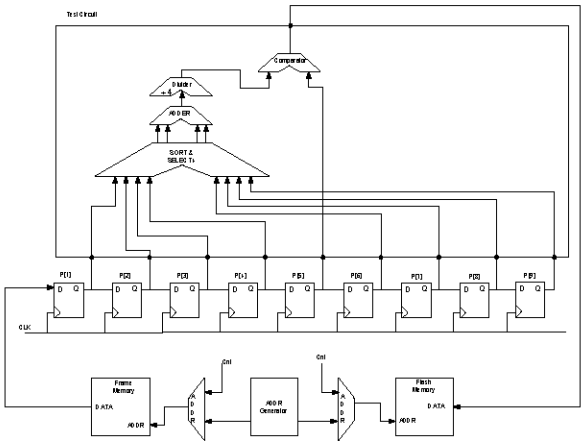

Fig. 2. The proposed BIST circuit

The SORT & SELECT 4 module sorts the 8 pixel values surrounding the center pixel under test, and then forward medium 4 pixel values to the adder. The algorithm and flow of the operations of the test circuitry will be detailed in Section III.

The comparator decides if the center pixel under test is normal or abnormal based on the computed values by the proposed soft-test algorithm, and then the test result will be stored (or marked) in the flash memory as a cumulative defective pixel map as follows: 000: Stuck Low, 001: Low Sensitive, 010: Stuck High, 011: Stuck Low, 100: Normal.

Note that this map will be referenced in the following round of testing and repair.

III. PROPOSED BIST ALGORITHM

In this section, the design and implementation of the proposed soft-testing algorithm is presented based on the threshold testing model as was introduced in [2] and is shown below.

$$\left| \frac{\sum_{k=1}^{4} P(k) + \sum_{k=6}^{9} P(k)}{N} - P(5) \right| \leq C, \qquad (1)$$

where $P(1) \cdots P(N)$ are those pixels surrounding the pixel $P(5)$ under test; and notice that this is a BIST architecture with $N = 8$. A detailed principle has been presented in [2] and is based on the general observation in digital imaging systems that the pixels tend to exhibit similar values around the average. The constant C is the threshold for determining whether the pixel under test is defective or not. The constant C will be calculated by using *Mean Medium Four* (MMF) such that the brightest two pixels and the darkest two pixels are excluded in the computation for the average value. Then, the remaining 4 pixels participate in the computation for the average value.

The design and implementation algorithm of the the proposed BIST circuitry based on Equation (1) is as follows.

```
CCD-BIST
1  WHILE given time
2      DO PICK-WINDOW
3         SOFT-TEST(P[])
```

In line 2, the PICK-WINDOW selects which testing window to be tested next. In line 3, the SOFT-TEST procedure is called and is implemented as follows.

```
SOFT-TEST(P[])
1 FOR j <- 1 to NO_OF_COLUMN_INWINDOW
2   DO FOR i <- to NO_OF_ROW_INWINDOW
3         DO LOAD(i,j,P[])
4            SORT(P[])
5            SUM <- P[3]+P[4]+P[6]+P[7]
6            AVG <- SUM / 4
7            VAL <- ABS(AVG - P[5])
8            VAL <-  VAL / AVG
9            IF VAL < 0.1
10              THEN STORE(i,j,NORMAL)
11              ELSE STORE(i,j,ABNORMAL)
```

The computations to be taken in the above SOFT-TEST procedure are: the for loop in line 1-2 iterates the test procedure as many times as the product of the number of columns and rows on the CCD pixel-matrix, in each iteration a specific window of pixels are processed as defined; in line 3, the pixel values are loaded from the frame memory into the register pixels as an array P[ ]; in line 4, those pixel values are sorted, and in line 5-6 computes the average value (AVG) of the four core pixels excluding the top 2 darkest and the bottom 2 brightest; in line 7 the difference of the pixel value of P[5] from the AVG and store the result in VAL; in line 8 the ratio of the the VAL over AVG is computed; in line 9 the VAL to the threshold constant C is compared ($C = 0.1$ is employed as an example) such that if the computed ratio is smaller than C, then a normal pixel

value is stored in the defective pixel map, otherwise the detected abnormal value is stored in the defective pixel map for use during the repair process later.

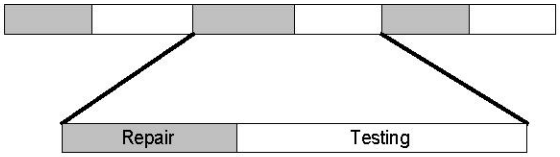

Fig. 3. Sequence of combined soft-testing/repair cycles

Figure (3) shows the sequence of combined testing and repair cycles. Each unit cycle time of combined testing and repair determines the execution time of each round of such operation and is referred to as *window*. Within each window, a repair process is performed followed by a testing process. Initially, a null repair process is performed since there is no recording made in the defective pixel map in the flash memory. Once defective pixel map starts to record detected defective pixels, the repair cycle within each window starts to map those recorded defective pixels from the defective pixel map in the flash memory with a normal data. Thus, a new incoming pixels are tested against a certain recorded-defective pixels repaired a priori in order to avoid redundant repair and testing process.

In order to address the performance, a parallel BIST architecture is employed. This will enable the BIST to reduce testing time and catch up with the possibly bulky data to be processed depending on the size of CCD within a given time. The number of CCD pixels currently using CCD is over 10 Mega pixels in general. The cost will be justified versus its performance gain.

The flash memory is the sole overhead for the BIST. As the proposed BIST does not require for the test pattern generation and signature analysis, the total overhead is kept low. Note that the proposed BIST shares many functional parts with CCD controllers.

In order to investigate the improvement by the parallel BIST, Verilog HDL simulation is performed as follows:

1. Input the number of pixels of CCDs as follows: 64×64, 128×128, 256×256, 512×512, 1024×1024, 2408×2048, 4096×4096.
2. Generate 10% of defective pixels in each CCD model.
3. Input the number of test circuit : 1, 3, 5.
4. Test each CCD model.
5. Record testing time of the CCD model.

The simulation results are shown in Figure (4).

Analyzing the result in Figure (4), the followings are observed.

- The single Test Circuit takes the longest time, and five Test Circuit takes the least time.
- It is observed that there is no considerable difference between 3 Test Circuit and 5 Test Circuit. Therefore, 3 Test Circuit is a more cost effective BIST structure without sacrificing significant performance.
- With 2048x2048 (4M pixels), the test time of single Test Circuit is twice the test time of 3 or 5 Test Circuits. However, at 4096x4096 (16M pixels), the test time of single Test Circuit is three times the test time of 3 or 5 Test Circuits.
- From the above high resolution CCDs require a long testing time. Thus, the parallel BIST can provide a solution to reduce testing time considerably.

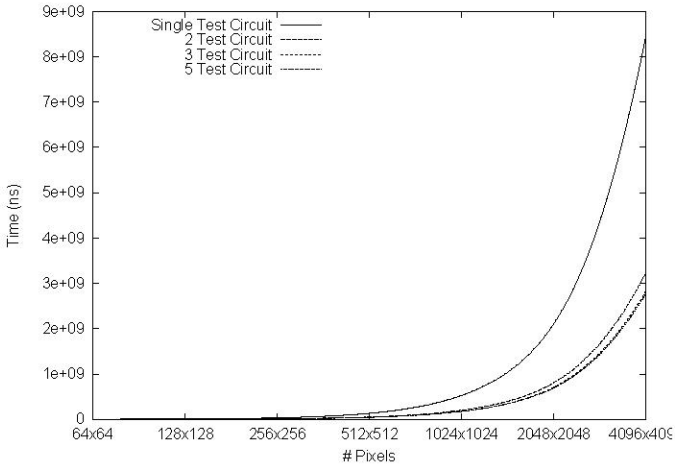

Fig. 4. Testing time vs. # pixels

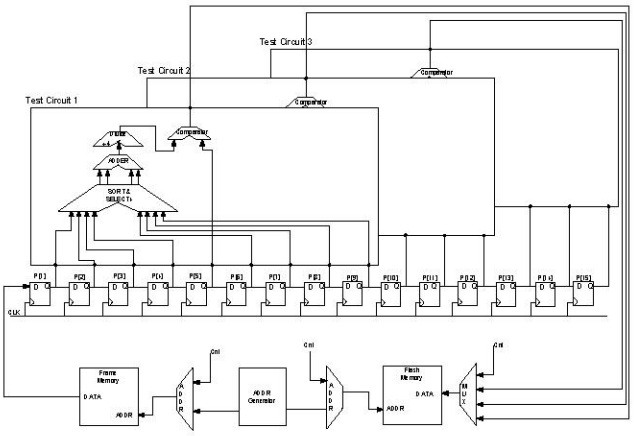

Fig. 5. The proposed BIST circuit (3 Test Circuit)

A 3 Test Circuit BIST is presented in Figure (5), which is implemented for high speed but minimal cost.

Figure (6) shows the sequence of loading pixels to the registers in 3 Test Circuit BIST. The reason to load in vertical sequence is to save time and share the loaded pixels to the Test Circuits. Notice that loading zone each shares 6 pixels with its neighboring zone.

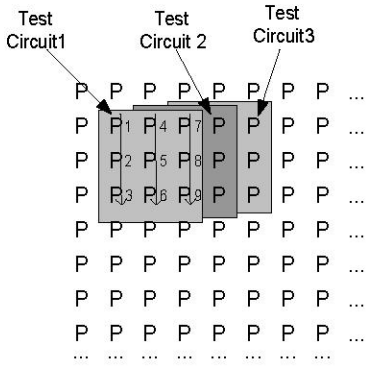

Fig. 6. Pixel Loading Sequence (3 Test Circuits)

The optimal number of registers is determined by the following equation.

$$N_{register}(N_{TestCircuit}) = 9 + 3(N_{TestCircuit} - 1) \quad (2)$$

where $N_{register}(n)$ is the number of registers, and $N_{TestCircuit}$ is the number of Test Circuits and it is assumed $N_{TestCircuit} \geq 1$. From Figure (6), each Test Circuit loads nine pixels to test at a time. However, six pixels are overlapped as shown in Figure (6). For example, in case of 3 Test Circuit BIST, $9 + 3 \times 2 = 15$ pixels have to be loaded.

IV. SIMULATIONS

In this section, the effect of the BIST on the CCD virtual yield will be evaluated through a Verilog HDL simulation.

CCDs of 16 Mega pixels (4096×4096) are simulated, in which three CCDs containing 10%, 7% and 3% defective pixels are simulated, respectively. Defective images are generated randomly and it is assumed that the pixel values should be in the median range (i.e., gray color, not white, not black). Then, a normal pixel value corrects any defective pixel value (i.e., white or black). It is also assumed the ratio of white and black is equal. For example, if a CCD contains 10% defective pixel, the CCD contains 5% of white and 5% of black pixel value.

For the simulation, six different window sizes are used: $W = 5 \times 10^9 unit$, $W = 3 \times 10^9 unit$, $W = 1 \times 10^9 unit$, $W = 5 \times 10^8 unit$, $W = 3 \times 10^8 unit$, and $1 = 5 \times 10^8 unit$ where the unit is in nano seconds.

It is revealed that the yield improvement of previous theoretical simulations in [2] show similar pattern with the yield of single Test Circuit BIST/BISR, Figures (7)-(9).

Figures (7)-(9) demonstrate the yield improvement by single Test Circuit for hard yield 90%, 93%, 97%, respectively. The higher hard yield CCD has, the less time it takes to approach 100% yield. When the smallest window is chosen, the repair time is 12 times longer than the one with largest window chosen. Therefore, it is clear that a proper window size should be chosen for performance.

Figures (10)-(12) and Figures (13)-(15) show similar patterns with Figures (7)-(9), respectively. The speed up by multiple Test Circuit is remarkable. However, notice that there is not much difference between 3 and 5 Test Circuit. From these simulations, it is revealed that 3 Test Circuit is the most efficient and cost effective design for the proposed BIST under the assumed simulation environment.

V. DISCUSSION AND CONCLUSIONS

This paper has presented a BIST design for CCD-based digital imaging system. Imperfect fabrication, excessive exposure to light, radiation, sensing element aging, and excessive mechanical shock, to mention a few, were considered in this work. Traditional on-device BIST cannot be readily employed on the imaging devices such as CCD due to the unique requirement that no pixel can be utilized to repair or bypass a defect on any other pixels. The BIST technique designed and simulated in this paper is a technique to test and repair the defects on pixels off the device, referred to as *off-device defect/fault tolerance*, and has incorporated a repair process to demonstrate the yield enhancement. A Verilog-based design and simulation is provided to demonstrate the validity of the off-device soft-test/repair in terms of reliability (or virtual yield) enhancement and performance against various combinations of design parameters such as test window size and sequence of combined soft-test/repair cycles; and also the performance impact of parallel testing has been demonstrated.

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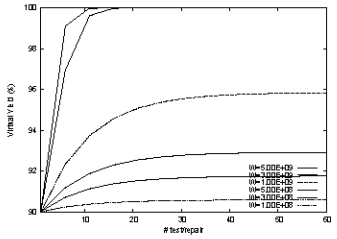

Fig. 7. Test and Repair (Single Test Circuit and Hard Yield=90%)

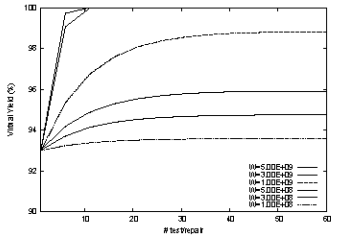

Fig. 8. Test and Repair (Single Test Circuit and Hard Yield=93%)

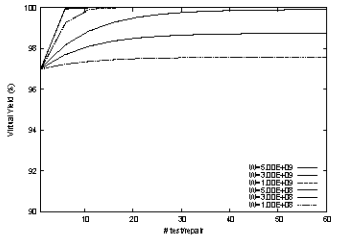

Fig. 9. Test and Repair (Single Test Circuit and Hard Yield=97%)

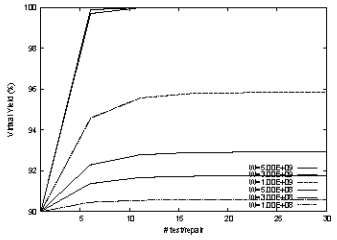

Fig. 10. Test and Repair (3 Test Circuit and Hard Yield=90%)

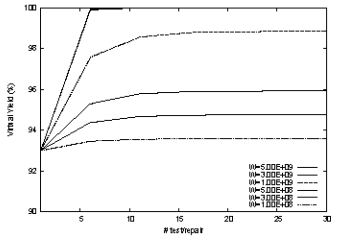

Fig. 11. Test and Repair (3 Test Circuit and Hard Yield=93%)

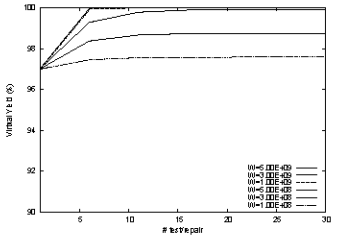

Fig. 12. Test and Repair (3 Test Circuit and Hard Yield=97%)

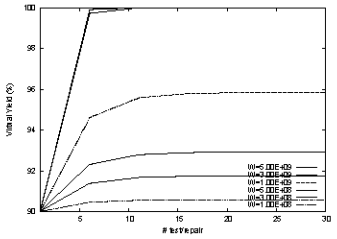

Fig. 13. Test and Repair (5 Test Circuit and Hard Yield=90%)

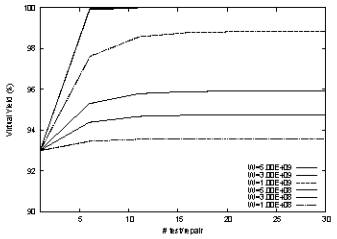

Fig. 14. Test and Repair (5 Test Circuit and Hard Yield=93%)

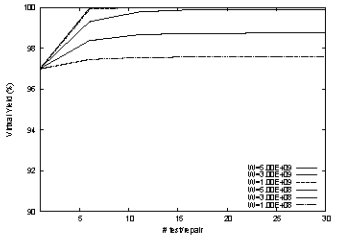

Fig. 15. Test and Repair (5 Test Circuit and Hard Yield=97%)