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A Study on Influence of Guard Band on Common-Mode Current Related to a Microstrip Line

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Abstract:
Influence of guard band on common-mode (CM) current related to a microstrip line (trace) has been studied experimental and FDTD simulation. As the guard band, copper tape is connected along the entire edge of the ground plane. It is cleared that a guard band parallel to and near a trace is most effective in suppressing the CM current. An empirical formula to quantify the relationship between the position of a trace and CM current of the case with a guard band is proposed. Calculated results using the empirical formula and FDTD modeling are in good agreement, which indicates this empirical formula should be useful for developing EMI design guidelines.

Keywords
Printed circuit board, Electromagnetic interference, Common-mode current, guard band, FDTD method

I. Introduction

Common-mode (CM) radiation from cables attached to a printed circuit board (PCB), as well as CM radiation from the PCB itself, is a common electromagnetic interference (EMI) problem. It is necessary to suppress the CM current to reduce radiation [1]. CM radiation from cables attached to PCBs will be largest near a resonance frequency of the effective "EMI antenna" [2]. Mechanisms by which differential-mode (DM) signals are converted to CM noise sources resulting in EMI have been demonstrated, and two classes of coupling mechanisms are voltage driven and current driven [3]. In the considered frequency range, the current driven mechanism is of particular importance for a trace near a PCB edge herein for this application. The EMI coupling physics at lower frequencies is dominated by the magnetic field. PCB has magnetic flux lines that close below the plane, and the ground plane will have a non-zero impedance [1], [3], [4]. The voltage drop across the non-zero impedance of the ground plane can result in CM radiation [5]. The CM current I_{CM} at frequencies below the radiator resonances is approximately

$$I_{CM} \approx -\omega^2 C_{ant} L_{return} \frac{V_{DM}}{R}, \quad (1)$$

where V_{DM} is source voltage, C_{ant} is capacitance between two extensions of the lower conductors, R is terminating resistor, and L_{return} is inductance between two portions of extended ground [3].

So far, EMI resulting from a trace near a PCB edge has been investigated experimentally and with numerical modeling [6], [7]. As the trace is moved closer to the PCB edge, CM current increases. The suppression method of CM current is required.

In this paper, influence of a guard band on CM current related to a trace is investigated experimental and finite-difference time-domain (FDTD) modeling. As the guard band, copper tape is connected along the entire edge of the ground plane. The influence of the guard band on CM current is discussed, and an empirical formula to quantify the relationship between the position of a trace and CM current with a guard band is proposed.

II. Experimental and Modeling Methods

II-A. PCB Geometry

The geometry of a PCB layout is illustrated in Fig. 1. The PCB has two layers, with the upper layer for a signal trace and the lower for the ground plane. The size of PCB is 150 mm length, 100 mm width, and 1.09 mm thickness of the dielectric substrate with ε_r=4.5. The trace, with 0.508 mm width and 50 mm length, was centered lengthwise on a dielectric substrate. Several different configurations in which the distance d_1 between the trace and the PCB edge, as shown in Table 1, were prepared for the measurements. As the guard band, copper tape is used and connected along the entire edge of the ground plane to upper layer through the side of the PCB. The width w_{GB} of the guard band was 5 mm. The characteristic impedance of the case with guard band was the same as the case without guard band. The terminating resistance was the same value as the characteristic impedance determined from TDR measurements, as shown in Table. 1. The PCB was driven by a 0.085"semi-rigid coaxial cable running along the center of the PCB on the reverse-side. The coaxial cable extended 30 mm beyond the PCB edge and an SMA connector was used for the driving point of the signal trace.

II-B. Experimental Method

The CM current on the outer shield of the feed cable was measured using a current probe (Fischer F-2000), and a network analyzer (HP 8753D), as shown in Fig. 2 [6]. A 600 mm×600 mm aluminum plate was used to isolate the PCB from the cable dressing leading to the network analyzer. The $|S_{21}|$ with the location of Port 1 (the voltage source for the signal trace) and Port 2 (current probe on the semi-rigid cable) was measured in the frequency range from 50 MHz to 1 GHz. The calibration of the network analyzer and the current probe were done by using a shorted copper ring which encircled the current probe. The voltage at Port 2 is related to the CM current by $|V_2^-| = 50|I_{CM}|/2$, where the source impedance of the network analyzer is 50 Ω. The input voltage at Port 1 is $|V_1^+| = |V_S|/2$, where V_S is the source voltage of the network analyzer, since the source impedance is matched to the characteristic impedance of the cable. Since $|S_{21}|$ is the ratio of the voltage at Port 2 to the voltage at Port 1, the relationship between the $|S_{21}|$ and CM current is given by

$$|S_{21}| = \frac{50|I_{CM}|}{|V_S|}. \quad (2)$$

Equation (2) is used to compare experimental and numerical results.

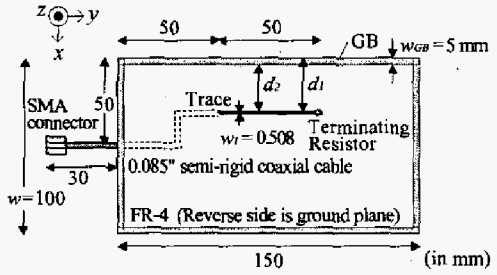

Fig. 1 Geometry of PCB layout used in the experimentation.

Table 1 PCBs under test
(d_1: distance between the trace and the PCB edge, h: thickness of the dielectric substrate, and w_{GB}: width of the guard band)

	d_1 [mm]	$d_1/(\frac{w}{2})$	guard band	Terminating resistor [Ω]
d50	1.27	0.025	—	100
d100	2.54	0.051	—	100
d250	6.35	0.127	—	100
d250GB			w_{GB}=5 mm	
d300	7.62	0.152	—	91
d400	10.16	0.203	—	91
d400GB			w_{GB}=5 mm	
d600	15.24	0.305	—	91
d600GB			w_{GB}=5 mm	
center	49.75	0.995	—	91
centerGB			w_{GB}=5 mm	

II-C. Method of FDTD Modeling

The FDTD method [8] is used for simulating CM current on the PCB. Fig. 3 shows the computational domain, as a typical example. The cell size was Δx=0.254, Δy=2.5 and Δz=0.546 mm. PMLs (Perfectly Matched Layers) of eight cells deep, were used as the absorbing boundary condition. The total computational domain was 491×114×183 cells, in the x, y, and z dimensions, respectively. The time step was Δt=6.35×10^{-13} s from the Courant stability condition [8]. The trace, the ground plane, and aluminum plate were modeled as PEC (Perfect Electric Conductor). The aluminum plate was included as an infinite ground plane. The PCB substrate was modeled as a dielectric with two cells deep and relative permittivity ε_r=4.5. A sinusoidally modulated Gaussian pulse was used as the source with source resistance 50 Ω. The CM current was calculated by the loop integral of the magnetic field around the cable at the current probe position. To shorten the calculation time, the vector and parallel computation method for a super computer SX-4 (NEC) was developed [9].

III. Influence of the guard band on the CM current

At first, the PCB without guard band is discussed. The $|S_{21}|$ related to CM current is shown in Fig. 4. As the trace is moved closer to the PCB edge, $|S_{21}|$ increases. The curve is shifted nearly uniformly in magnitude over the considered frequency range. The difference between "center" and "d50" is approximately 12 dB. The calculated and measured results are in good agreement.

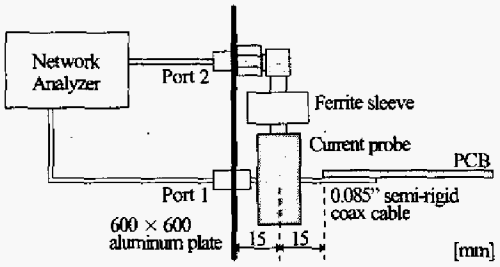

Fig. 2 Experiment setup for common-mode current measurement.

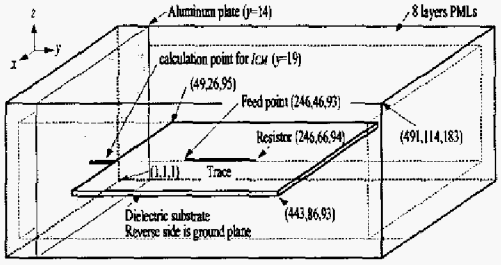

Fig. 3 Computational domain for the FDTD simulation, with a centered trace.

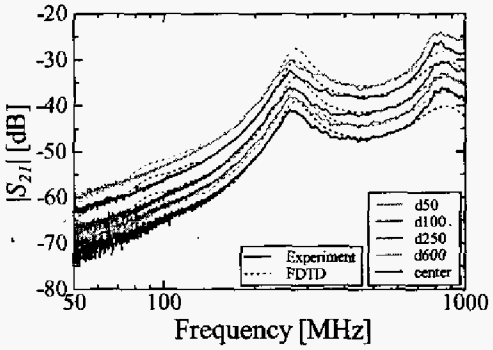

Fig. 4 Comparison of measured and simulated $|S_{21}|$ frequency responses for the PCBs under test (see Table 1).

So far, a formula for the inductance L'_{CM} [nH/cm] of the PCB ground plane without guard band was derived analytically by Leone, as

$$L'_{CM} \simeq 4\frac{h}{w}\frac{1}{\sqrt{1-4(1-2h/w)(s/w)^2}}, \qquad (3)$$

where w is the width of PCB, h is thickness of the dielectric substrate, s is the distance between the center of the PCB and the center of trace ($s = w/2 - w_t/2 - d_1$), w_t is the width of trace and d_1 is distance between the trace and the PCB edge [10]. Using Eqs. (1) and (3), $|S_{21}|_{\rm norm}$ [dB], which is the normalized value to the "h=$h_{\rm ref}$, centered trace (s=0) and without GB" (center) case, is given by

$$\begin{aligned} |S_{21}|_{\rm norm} &= |S_{21}|_s^h - |S_{21}|_{s=0}^{h=h_{\rm ref}} \\ &= 20\log_{10}\frac{(h/h_{\rm ref})/(R_{\rm ref}/R)}{\sqrt{1-4(1-2h/w)(s/w)^2}}, \end{aligned} \qquad (4)$$

where $h_{\rm ref}$ is reference thickness, i.e., 1.09 mm in this study,

R is terminating resistance, and R_{ref} that of the "center" case with h_{ref}.

Using PCBs shown in Fig. 1 and Table 1, the effect of the guard band (GB) is compared with the case without the guard band by measurement and FDTD modeling. In order to study the effect of the guard band position, four configurations with GB, GB1, GB2, and GB3, as shown in Fig. 5, were modeled with the FDTD method, where the width w_{GB} of guard band was 5 mm. As an example, the measured and calculated results for the "d_1=6.35 mm (d250)" case are shown in Fig. 6. The calculated and measured results are in good agreement. The $|S_{21}|$ in the cases with the GB1 and GB2 is almost the same as the case with GB which is connected along the all edges, and these curves overlay. On the other hand, the GB3 has no effect in suppressing $|S_{21}|$. Consequently, the results of the cases with GB2 and GB3 are omitted in Fig. 6. These results indicate that the guard band parallel to and near a trace is most effective in suppressing the CM current.

Empirical expressions to quantify the relationship between the position of the trace and CM current for the case with a guard band can be developed from the FDTD modeling. The cross-sectional dimensions of a part of the PCB with the guard band, related to the formulation, is shown in Fig. 7. To investigate the effect of the guard band with the position of the signal trace, the width of the GB1, i.e. w_{GB}, was varied with 0, 2.5 and 5.0 mm. In Fig. 7, w_{GB}=0 mm means that there is a vertical metallic part of guard band on the PCB edge, but with no horizontal metallic part on the top of the PCB. In addition, the thickness of the dielectric substrate h was varied with 1.09, 1.64 and 2.18 mm. The signal trace was terminated in a matched load Z_0.

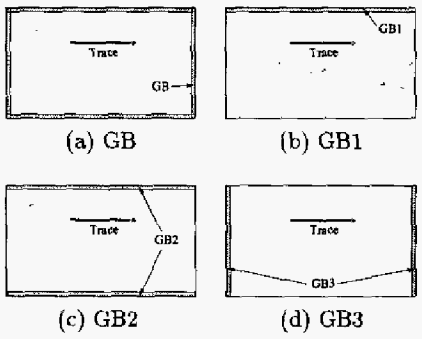

Fig. 5 Position of the guard band on the PCB.

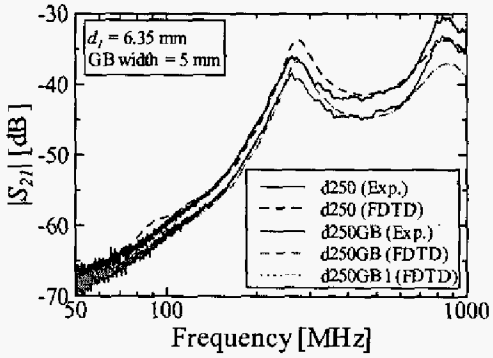

Fig. 6 An example of $|S_{21}|$ in the case with and without the guard band with 5 mm width (d_1=6.35 mm).

The guard band effect GBE [dB], which is the difference between the $|S_{21}|$ with GB1 ($|S_{21}|_{GB}$) and $|S_{21}|$ without the guard band ($|S_{21}|$), is defined herein as

$$GBE \equiv |S_{21}| - |S_{21}|_{GB}. \tag{5}$$

As an example, GBE in the case of "d_1=6.35 mm, w_{GB}=5.0 mm", i.e., "d250GB", is shown in Fig. 8. Since the GBE is approximately constant over the considered frequency range, the average value in the considered frequency range is used as GBE value. Using the distance d_2 between the trace and GB1, and h, the relationship between GBE and d_2/h is shown in Fig. 9. The GBE can be expressed as an empirical equation with parameters determined with a correlation coefficient of 0.99 by the least squares method,

$$GBE \approx 3.46 \left(\frac{d_2}{h}\right)^{-0.92}, \tag{6}$$

where d_2 is the distance between the trace and the edge of GB1 ($d_2 = d_1 - w_{GB}$), and w_{GB} is the width of the guard band. The solid line in Fig. 9 is least squares curve given by Eq. (6). As d_2 decreases and/or h increases, the GBE increases significantly.

Now, the guard band effect GBE is considered in $|S_{21}|_{GB\ norm}$. Using Eq.(4)~(6), the $|S_{21}|_{GB\ norm}$ is given as an empirical equation

$$|S_{21}|_{GB\ norm} = |S_{21}|_{norm} - GBE$$
$$= 20\log_{10}\left(\frac{(h/h_{ref})/(R_{ref}/R)}{\sqrt{1-4(1-2h/w)(s/w)^2}}\right) - 3.46\left(\frac{d_2}{h}\right)^{-0.92} \tag{7}$$

The relationship between normalized $|S_{21}|$ and d_1 is shown in Fig. 10. In the case of "h=1.09 mm", the normalized $|S_{21}|$ is not calculated for $6.35 \le d_1 \le 7.62$ mm, because the terminating resistor R in the case with $d_1 \ge$7.62 mm is different from that with $d_1 \le$6.35 mm, as shown in Table 1. As d_1 decreases and/or h increases, the normalized $|S_{21}|$ in the case

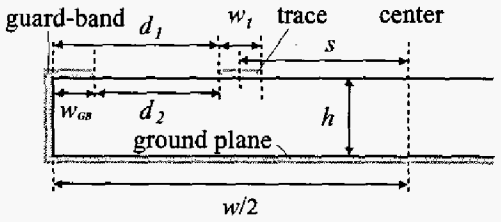

Fig. 7 Cross-section of PCB showing the relevant dimensions

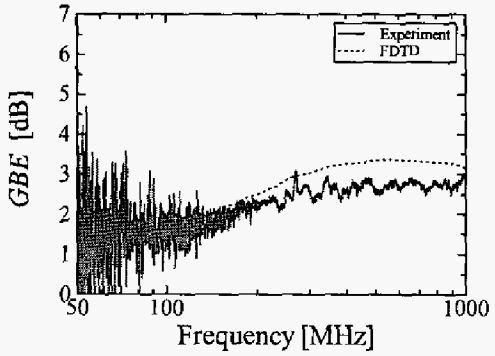

Fig. 8 GBE vs. frequency (ex. d_1=6.35 mm, w_{GB}=5 mm)

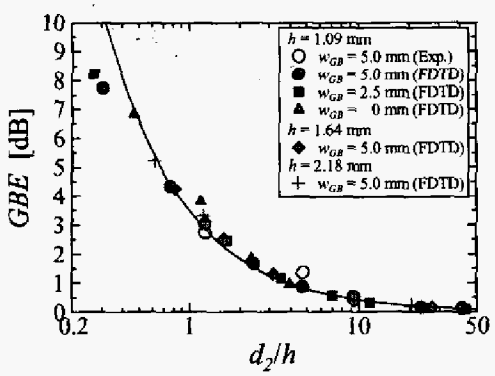

Fig. 9 *GBE* vs. d_2/h

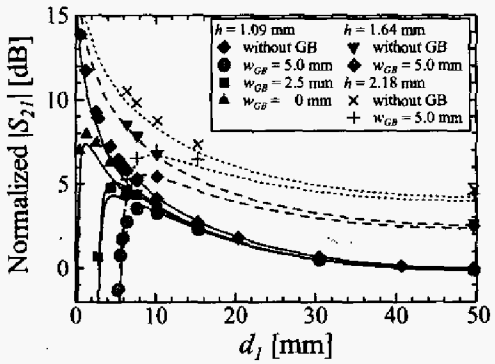

Fig. 10 Normalized $|S_{21}|$ vs. d_1. Lines are calculated results by Eq. (4) and (7), and symbols are FDTD calculated results.

without the guard band increases. On the other hand, the normalized $|S_{21}|$ in the case with a guard band has a peak and then decreases as d_1 is smaller. This indicates that the guard band allows for a trace to be routed near a PCB edge. The calculated results (lines in Fig. 10) using Eq. (4) and (7) agree well with the FDTD calculated results (symbols). This indicates the effect of the guard band to suppress the CM current can be estimated using Eq.(7). Therefore, a guard band will be effective for high-density PCB packaging with high-speed traces.

IV. Conclusions

Influence of guard band on CM current related to a trace was studied experimental and FDTD modeling. The guard band is effective in suppressing the CM current, and allows for a trace to be routed near a PCB edge. An empirical formula should be useful for developing EMI design guidelines.

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