View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by Missouri University of Science and Technology (Missouri S&T): Scholars' Mine

Missouri University of Science and Technology
Scholars' Mine

Electrical and Computer Engineering Faculty Research & Creative Works
Electrical and Computer Engineering

01 Aug 2004

Extraction of a SPICE Via Model from Full-Wave Modeling for Differential Signaling

Shaofeng Luan

Giuseppe Selli

James L. Drewniak
Missouri University of Science and Technology, drewniak@mst.edu

Andrea de Luca

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1619

Follow this and additional works at: https://scholarsmine.mst.edu/ele_comeng_facwork

Part of the Electrical and Computer Engineering Commons

Recommended Citation

S. Luan and G. Selli and J. L. Drewniak and A. de Luca and G. Antonini and A. Orlandi and A. C. Scogna and J. Fan and J. L. Knighten and N. W. Smith and R. Alexander, "Extraction of a SPICE Via Model from Full-Wave Modeling for Differential Signaling," *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility (2004, Santa Clara, CA)*, vol. 2, pp. 577-582, Institute of Electrical and Electronics Engineers (IEEE), Aug 2004.
The definitive version is available at https://doi.org/10.1109/ISEMC.2004.1349862

This Article - Conference proceedings is brought to you for free and open access by Scholars' Mine. It has been accepted for inclusion in Electrical and Computer Engineering Faculty Research & Creative Works by an authorized administrator of Scholars' Mine. This work is protected by U. S. Copyright Law. Unauthorized use including reproduction for redistribution requires the permission of the copyright holder. For more information, please contact scholarsmine@mst.edu.

Extraction of a SPICE Via Model from Full-Wave Modeling for Differential Signaling

Shaofeng Luan, Giuseppe Selli, James L. Drewniak
EMC Lab., Department of ECE
University of Missouri – Rolla
Rolla, MO, USA
luan@umr.edu

Andrea De Luca, Giulio Antonini, Antonio Ciccomancini Scogna, Antonio Orlandi
UAq EMC Lab. Dept. of EE
University of L'Aquila
L'Aquila, Italy

Jun Fan, James L. Knighten, Norman W. Smith, Ray Alexander
NCR Corporation
San Diego, CA, USA

***Abstract*— This paper presents a procedure for building SPICE models for via transitions in differential signaling. The method of extracting parameters of SPICE models from a full-wave simulation tool is demonstrated. Then the validity of the SPICE models is studied by comparing the solution from the SPICE models with that from the full-wave simulation.**

Keywords-PCB; SPICE; via transition; differential signaling

I. INTRODUCTION

In high-speed digital designs, signal via transitions on printed circuit boards (PCBs) are becoming an important signal integrity issue. As the data rates increase into the multi-giga-bit per second range, via transitions can degrade the signal. Efficient and accurate models for via transitions are necessary for high bit-rate digital circuit system designs. Further, these models should be compatible with fast simulation tools.

A number of models for differential vias have been published. The method in [1] and [2] modeled the coupled vias as a cascade of capacitances and inductances. A 3-D electrostatic solver was used to calculate the capacitances while the formula of a bifilar transmission line was applied to computation of the inductance values. Another method in [3] modeled vias in differential transmission lines as transmission line segments. A layer peeling process was proposed to model via transitions of single-ended signaling on multi-layer PCBs in [4-5]. In this paper, this procedure was used to model the via pair for a differential signal pair. SPICE models for various vias on a specified PCB stackup are constructed by cascading "building blocks", which are SPICE models for elements of the via structure. Full-wave numerical modeling was used to simulate the 4-port S-parameters of these "building blocks".

II. LAYER PEELING PROCESS

It was shown in the previous work that single-ended via transition in the multi-layer PCBs could be modeled using a peeling and partitioning process [4-5]. A via is segmented into several parts, and each part is modeled as a SPICE passive network. The various via transitions in a practical design can be modeled by putting these basic building blocks together. This method is denoted as a layer peeling process in this paper. The models of these parts are called " building blocks" or "blocks". Solid planes inside the PCBs were used as natural boundaries for separating the blocks of a via. Similarly, this process was applied to build the via model library for differential signaling.

The main advantage of the layer peeling process is that it has the flexibility to model various via transitions connecting signal lines on different layers using a few SPICE building blocks. It decreases the requirement of time and complexity of full-wave simulation for model extraction. For a through-hole via differential signal pair, the via model library includes only four kinds of building blocks: the transition between coupled microstrip lines and differential via pair (Block A in Fig. 1), the differential via pair across two solid planes (Block D), the transition between coupled striplines and a differential via pair (Block B), differential via stubs (Block C). At first, simple combinations of blocks associated with the geometry variantion were simulated using full-wave tools to acquire n-port S-parameters. Then a physics-based SPICE model for each block was built. The values of these elements were extracted by fitting the S-parameters from full-wave models.

To demonstrate the procedure detailed above, a model library was constructed for differential signaling on a 10-layer board. A typical through-hole via pair for differential signaling is shown in Fig. 1.

After applying the layer peeling process, the six building blocks were identified and their SPICE model was constructed as shown in Fig. 2- Fig. 5. The SPICE model for Block A can be seen as two coupled π-type circuits. C_1 models the capacitance between the pad and the reference plane, while C_{m1} models the mutual capacitance between two pads. C_2 represents the capacitance between the via cylinder and the reference plane, while C_{m2} models the capacitive coupling between two via cylinders. L is the equivalent inductance of the via and M models the mutual inductive coupling between two vias.

The SPICE model for Block B was built using a similar method. Because Block B has six ports and two reference planes, it requires two different models. One is for the geometry when the signal comes from top layer and the ends of vias near the bottom layer connects to via stubs as shown in Fig. 3(a). The other case is for the situation when signal comes from the bottom layer and the top layer connects to via stubs as shown in Fig. 3(b). In Fig. 3(a), Port 1, 2, 5 and Port 6 share one reference plane and Port 3 and Port 4 use another reference plane. C_{ip} represents the inter-plane capacitance between two solid planes. In Fig. 3(b), Port 1 and Port 2 share one reference plane and Port 3, 4, 5 and Port 6 use another reference plane.

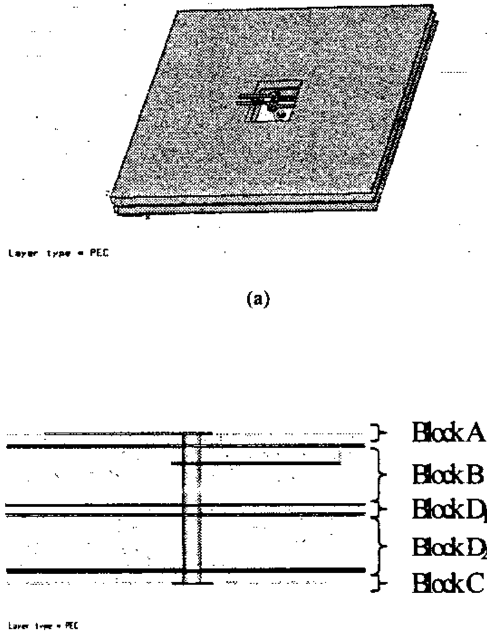


Figure 1. A typcial through hole via pair for differential signaling, (a) perspecitve view, (b) side view.

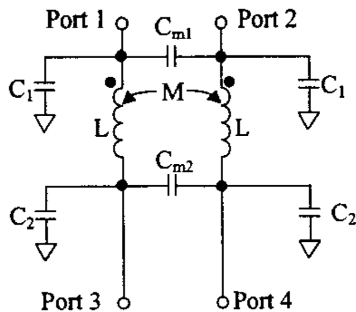


Figure 2. SPICE model for Block A.

Fig. 4 shows the SPICE model for Block C. For this example, the thickness of the dielectric layer of Block C is 0.105 mm, so that the inductance associated with the via stub is very small and can be neglected. SPICE model for Block D as shown in Fig. 5 is similar to that for Block A. The difference is that four Ports do not share one common reference plane as shown in Block A. Zin represents the input impedance of the powerbus structure. For this case, when the size of board is 15 mm by 15 mm and the frequency range is below 5GHz, it can be modeled as one capacitor. In practical designs, the boards are generally larger than this example. More complex models (such as cavity model) for power/ground planes should be used instead of a simple capacitance.

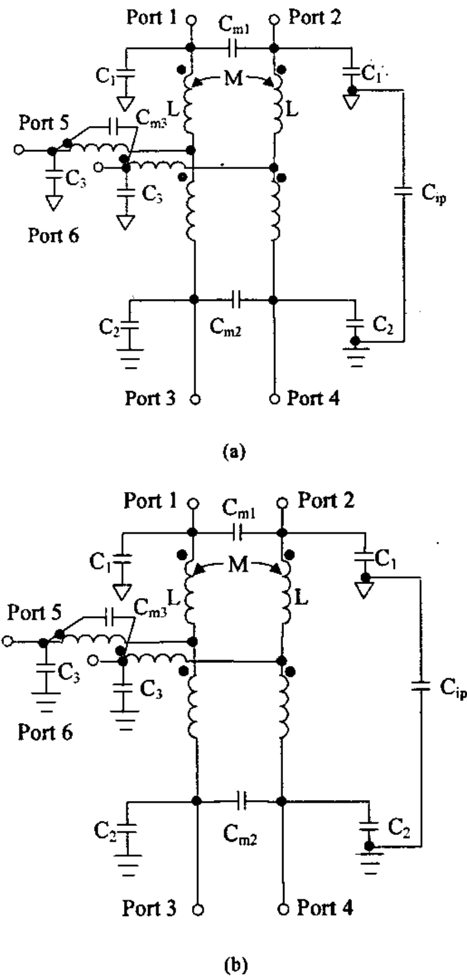


Figure 3. SPICE models for Block B, (a) when signal comes from the upper layers and via stubs are in the lower layers, and (b) when signal comes from the lower layers and via stubs are in the upper layers.

0-7803-8443-1/04/$20.00 © IEEE.

Figure 4. SPICE model for Block C

Figure 5. SPICE model for Block D.

III. Circuit Extraciton for Blocks

To avoid the difficulty of setting the port at the lower edge of a via and anti-pad, a test geometry as shown in Fig. 6, which consists of two Block As, was used to extract circuit parameters for Block A. After the simulation using a full-wave commercial tool using finite integration technique, the circuit parameters of Block A were extracted by fitting the S-parameters.

Figure 6. Geometry used to extract the SPICE model for Block A

Using the method described above, the SPICE model was extracted and the following equivalent-circuit values were:

$L = 1.44$ nH;

$M = 0.648$ nH;

$C_1 = 0.0964$ pF;

$C_2 = 0.0481$ pF;

$C_{m1} = 4.53e\text{-}013$ pF;

$C_{m2} = 0.0295$ pF.

Fig. 7 shows a geometry used to extract the SPICE model for block D_1, while a block D_1 was insert into two block A to form a four layer structure. After the full-wave simulation, the SPICE model parameters of block D_1 were extracted as:

$C_{m1} = 0.0137$ pF;

$C_1 = 0.0163$ pF;

$L = 0.138$ nH;

$M = 7.08e\text{-}4$ nH;

$C_{ip} = 14.7$ pF;

Similarly, the model of block D_2 was extracted using the same method. The values of components were:

$C_{m1} = 3.39e\text{-}3$ pF;

$C_1 = 6.02e\text{-}4$ pF;

$L = 0.0146$ nH;

$M = 8.38e\text{-}4$ nH;

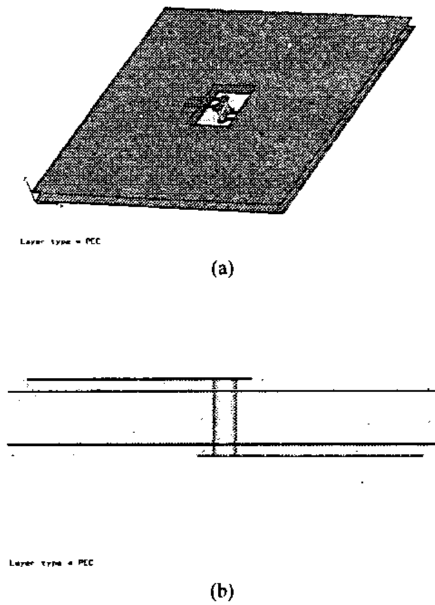
$C_{ip} = 101$ pF.

All parameters of other blocks were extracted using the similar procedure.

IV. Modeling Results

To check the SPICE results from the extracted circuits, a test case for a differential via transition on a 10-layer board was simulated using full-wave simulation tools as shown in Fig. 8. It consists of Block A, D_1, D_2, B and C. Differential signal traces on first and seventh layer were connected by a pair of through hole vias. The third, fourth and eighth layer are also signal layers, which can be seen in Fig. 8 as dashed lines. Fig. 9 – Fig. 12 shows the comparison of the SPICE model and full-wave simulation results. The difference of magnitudes of S_{dd11} is within 3dB while the difference of magnitudes of S_{dd21} is within 0.05dB.

0-7803-8443-1/04/$20.00 © IEEE.



(a)

(b)

Figure 7. Geometry used to extract SPICE model for Block D_1, (a) perspective view, and (b) side view.

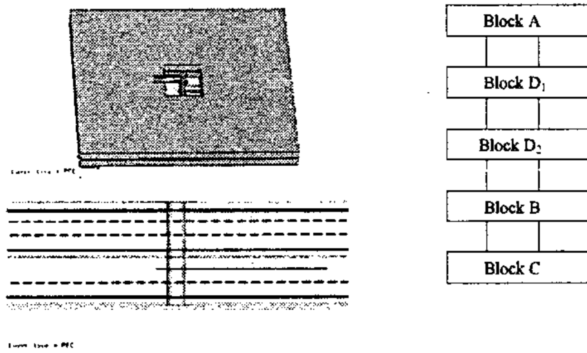


Figure 8. A test case of differential via transition on 10-layer board

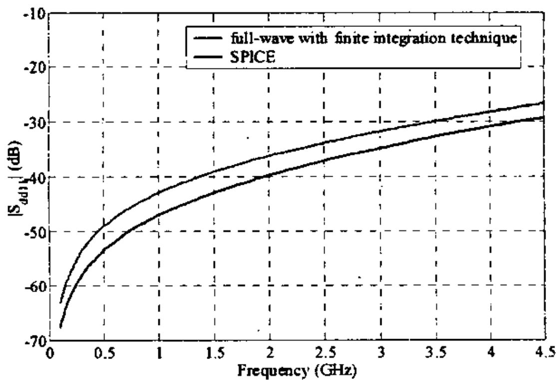


Figure 9. Modeling results – $|S_{dd11}|$ for the test case in Fig. 8.

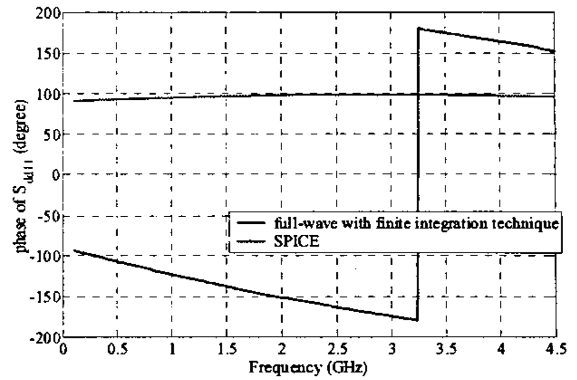


Figure 10. Modeling results – $\angle S_{dd11}$ for the test case in Fig. 8.

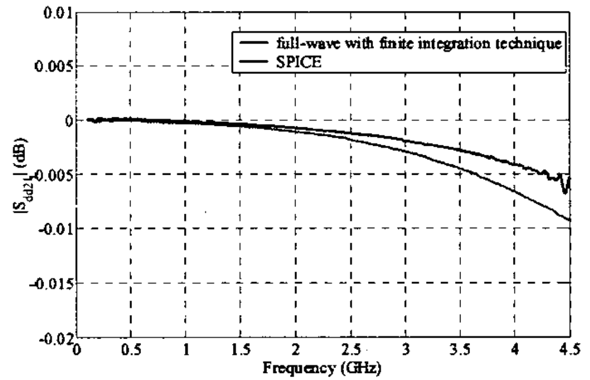


Figure 11. Modeling results – $|S_{dd21}|$ for the test case in Fig. 8.

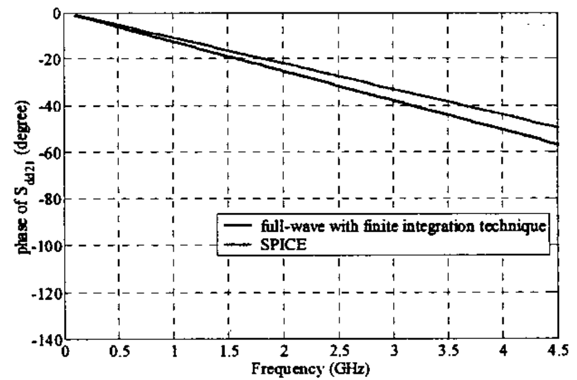


Figure 12. Modeling results – $\angle S_{dd21}$ for the test case in Fig. 8.

Another test case for the differential via transition on a 10-layer board was simulated using full-wave simulation tools as shown in Fig. 13. It consists of Block A, B, D_2, D_1 and C. Fig. 14 – Fig. 17 shows the comparison of SPICE model and full-

wave simulation results. The difference is within 3dB up to 5GHz.

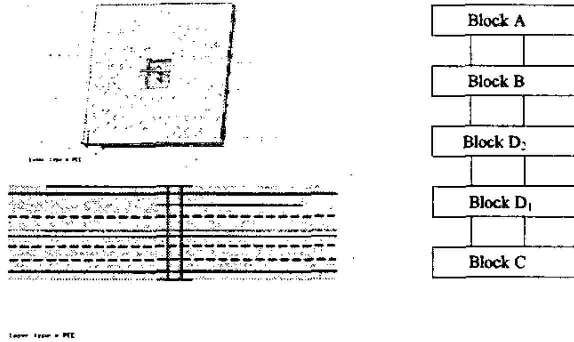


Figure 13. Another test case of differential via transition on 10-layer board.

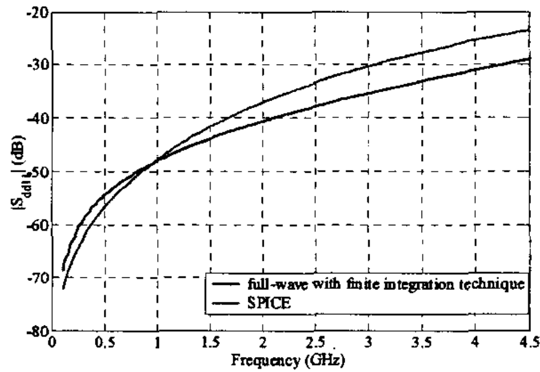


Figure 14. Modeling results – $|S_{dd11}|$ for the test case in Fig. 13.

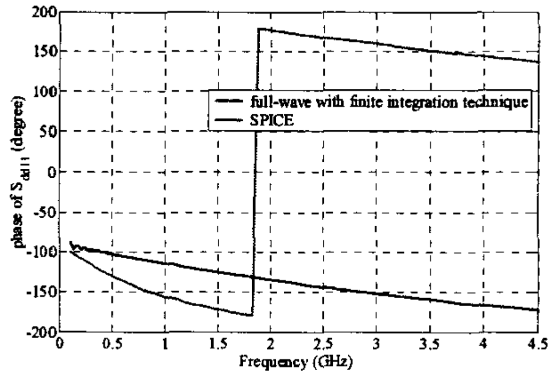


Figure 15. Modeling results – $\angle S_{dd11}$ for the test case in Fig. 13.

V. CONCLUSION

With the study in this paper, it is shown that, for a given stackup of PCB, a SPICE model library for via transition of differential signaling can be built using the proposed method and every via on the board can be modeled by a few cascaded blocks in this library.

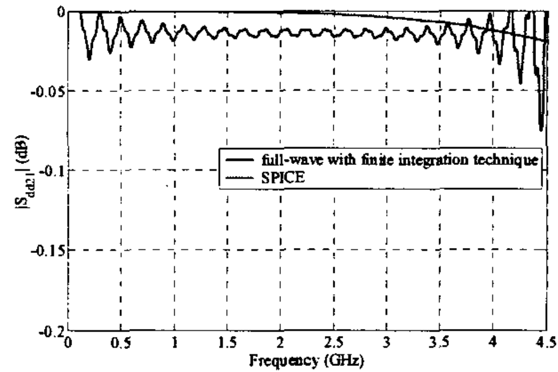


Figure 16. Modeling results – $|S_{dd21}|$ for the test case in Fig. 13.

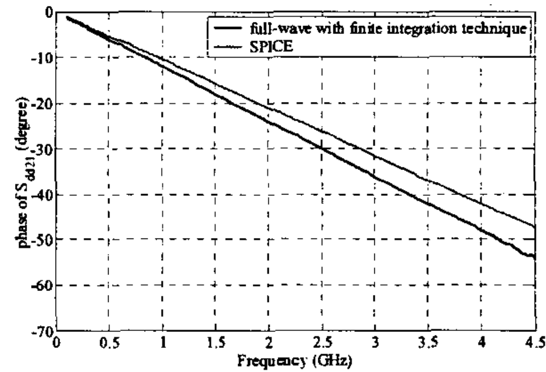


Figure 17. Modeling results – $\angle S_{dd21}$ for the test case in Fig. 13.

ACKNOWLEDGMENT

The authors wish to thank CST (Computer Simulation Technology) for providing them with Microwave Studio electromagnetic field simulation tool.

REFERENCES

[1] E. Laermans, J. De Geest, D. De Zutter, F. Olyslager, S. Sercu, and D. Morlion, "Modeling differential via holes," in Proc. 9th Topical Meeting Elect. Performance Electron. Packag., Scottsdale, AZ, Oct. 2000, pp. 127-130.

[2] E.Laermans, J. De Geest, D. De Zutter, F. Olyslager, S. Sercu, and D. Morlion, "Modeling differential via holes," IEEE Trans. Adv. Packag., vol. 24, pp.357-363, Aug. 2001.

[3] Chen Wang, Drewniak, J.L., Jun Fan, Knighten, J.L., Smith, N.W., Alexander, R., "Transmission line modeling of vias in differential signals", in *Proc. IEEE Int.Symp. Electromagn. Compat.*, 2002. pp. 249-252.

[4] Luan, S., Selli, G., Fan, J., Lai, M., Knighten, J.L., Smith, N.W., Alexander, R., Antonini, G., Ciccomancini, A., Orlandi, A., Drewniak, J.L., "SPICE model libraries for via transitions," in *Proc. IEEE Int.Symp. Electromagn. Compat.*. 2003. pp.859-864.

[5] G. Antonini, A.C. Scogna, A. Orlandi, "S-Parameters characterization of through, blind, and buried via holes," *IEEE Trans. on Mobile Computing*, vol. 2, Issue 2, pp 174-184, April-June 2003.

0-7803-8443-1/04/$20.00 © IEEE.