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A Novel Thin Film Transistor Using Double Amorphous Silicon Active Layer

Jong Hyun Choi, Chang Soo Kim, Byung Cheon Lim, and Jin Jang

***Abstract*—We have fabricated a novel low off-state leakage current thin-film transistor (TFT) using a chlorine incorporated amorphous silicon [a-Si : H(: Cl)] and amorphous silicon (a-Si : H) stacked active layer, in which conduction channel is formed in a-Si : H and a-Si : H(: Cl) is photo-insensitive material. The off-state photo-leakage current of the a-Si : H(: Cl)/a-Si : H TFT is much lower than that a conventional a-Si : H TFT.**

I. Introduction

Thin-film transistors (TFT's) including an active layer of hydrogenated amorphous silicon (a-Si : H) or polycrystalline silicon have been widely employed as the pixel-driving elements of a liquid crystal display (LCD). Particularly, the a-Si : H TFT is widely used in the production of large screen displays [1]. When employing a-Si : H TFT for multimedia displays which require a high intensity backlight compared to conventional notebook personal computers, the main issue is to reduce the off-state leakage current under light illumination.

A-Si : H has high photoconductivity which results in a high off-state leakage current for an a-Si : H TFT under backlight illumination [2].

Cl incorporated hydrogenated amorphous silicon [a-Si : H(: Cl)] has been prepared by various deposition methods using SiH_2Cl_2 mixtures to improve film quality [3], to improve the stability [4], or to increase the deposition rate [5].

The off-state leakage current of a-Si : H TFT under light illumination is related with its photoconductivity. The photoconductivity of a-Si : H(: Cl) is at least two orders of magnitude lower than that of undoped a-Si : H [6]. However, the performance of the a-Si : H(: Cl) TFT's was found to degrade with increasing $[SiH_2Cl_2]/[SiH_4]$ ratio which was used to deposit the a-Si : H(: Cl) [7]. The degradation is especially very severe when the ratio is higher than 0.08. In the present work an a-Si : H(: Cl)/a-Si : H stacked layer was employed as the active layer for the TFT.

The a-Si : H(: Cl)/a-Si : H TFT's show much lower off-state photo-leakage current than that of conventional a-Si : H TFT, and higher field effect mobility than that of an a-Si : H(: Cl) TFT.

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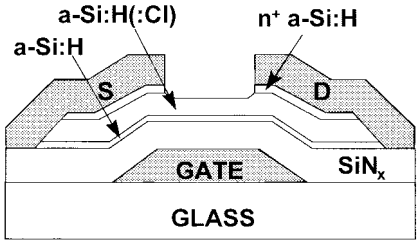

Fig. 1. A cross-sectional view of a-Si : H TFT using a-Si : H(: Cl)/a-Si : H active layer.

II. Experiments

The a-Si : H(: Cl) films were deposited by remote plasma chemical vapor deposition (RPCVD) using $SiH_4/SiH_2Cl_2/H_2$/He mixtures [8]. We used He as a nondepositing, exciting species. Helium was passed through the plasma generating region contained inside a cylindrical quartz tube of a diameter of 3.8 cm. Downstream from the plasma, in the deposition area, $SiH_4/SiH_2Cl_2/H_2$ was added for deposition of a-Si : H(: Cl) films. The flow rates of He, H_2, and SiH_4 were fixed at 100, 2, and 1 sccm, respectively. The substrate temperature was fixed at 300 °C throughout the deposition.

Fig. 1 shows a cross-sectional view of the a-Si : H(: Cl)/a-Si : H TFT. The transistor used in this study is a conventional inverted staggered structure. Four layers of 350 nm thick SiN_x, 30 nm thick a-Si : H, 130 nm thick a-Si : H(: Cl), and 50 nm thick n^+ a-Si : H were consecutively deposited in an RPCVD reactor. The SiN_x layer was deposited by using a gas mixture of SiH_4 and NH_3 with 1.8% SiH_4 in NH_3 at the substrate temperature of 300°C. The undoped a-Si : H(: Cl) and the n^+ a-Si : H were deposited from the gas mixtures of SiH_2Cl_2 and SiH_4, and a mixture of 1% PH_3 and 99% SiH_4, respectively. The n^+ a-Si : H, of resistivity ~100 Ω cm, was used to ensure an ohmic contact with the source/drain metals. The Al was evaporated on the n^+ a-Si : H and then patterned to be used as source/drain contacts. The n^+ layer in the channel was etched using a CF_4 plasma. The ratio of channel width to channel length of the TFT was 60 μm/30 μm. The device was illuminated using the backlight of a TFT-LCD module to compare the differences in the off-state leakage currents under illumination between a-Si : H(: Cl)/a-Si : H TFT, a-Si : H(: Cl) TFT, and a-Si : H TFT's.

III. Results and Discussion

Fig. 2 shows the comparison of square root of drain current (I_d) versus gate voltage (V_g) plots between an a-Si : H TFT, an a-Si : H(: Cl)/a-Si : H TFT, and an a-Si : H(: Cl) TFT deposited under the same conditions except the gas flow rates. The a-Si : H(: Cl) was deposited with a gas mixture of $[SiH_2Cl_2]/[SiH_4] = 0.08$. The field effect mobility and the threshold voltage of an a-Si : H(: Cl) TFT are 0.30 cm^2/Vs and 7.51 V, respectively. However, the a-Si : H(: Cl)/a-Si : H TFT's exhibited a field effect mobility of 0.45 cm^2/Vs, and a threshold voltage of 5.09 V. Both the field effect mobility and the threshold voltage could be improved by adopting a two-layer

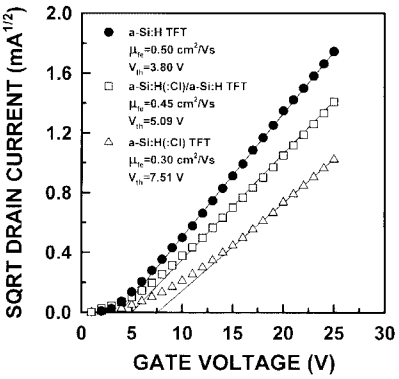

Fig. 2. The comparison of $\sqrt{I_d}$–V_g plots between a-Si : H, a-Si : H(: Cl)/a-Si : H TFT and a-Si : H(: Cl) TFT, in which a-Si : H(: Cl) was deposited with a gas mixture of $[SiH_2Cl_2]/[SiH_4] = 0.08$.

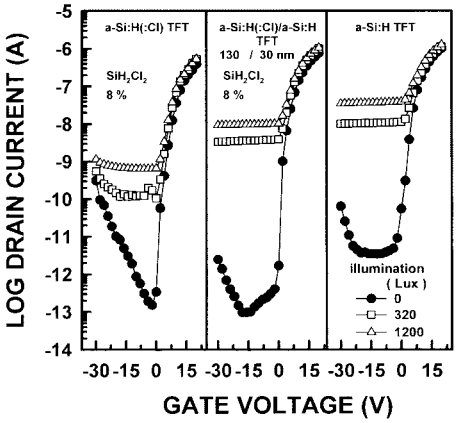

Fig. 3. Comparison of the I_d–V_g characteristics between a-Si : H(: Cl)/a-Si : H TFT, a-Si : H TFT, and a-Si : H(: Cl) TFT under backlight illumination.

structure. It is noted that the a-Si : H TFT exhibited a field effect mobility of 0.5 cm^2/Vs, and a threshold voltage of 3.80 V.

Fig. 3 shows the comparison of the I_d–V_g characteristics between an a-Si : H(: Cl)/a-Si : H TFT, an a-Si : H(: Cl) TFT, and conventional a-Si : H TFT under backlight illumination. The On/Off current ratios of an a-Si : H(: Cl)/a-Si : H TFT, an a-Si : H(: Cl) TFT, and conventional a-Si : H TFT are 5.45×10^7, 4.63×10^7 and 1.18×10^6, respectively. The on-current of the a-Si : H(: Cl)/a-Si : H TFT is slightly less than that of a-Si : H TFT. However, the leakage current is much lower than that of a conventional a-Si : H TFT. It is noted that the a-Si : H(: Cl) TFT exhibited lowest photo-leakage currents, whereas the off-state dark leakage currents increase rapidly with decreasing gate voltage at $V_g < -15$ V. The rapidly increasing off currents appear to be presumably due to the less density of states in the gap below the midgap of a-Si : H(: Cl).

Fig. 4 shows the field effect mobility and threshold voltage as a function of a-Si : H thickness for the a-Si : H(: Cl)/a-Si : H TFT's. The thickness of active layer of a-Si : H(: Cl)/a-Si : H was fixed at 160 nm. With increasing a-Si : H layer thickness, the field effect mobility increases at first and then saturates and the threshold voltage decreases slightly. The a-Si : H layer should be at least 30 nm to obtain the field effect mobility higher than 0.45 cm^2/Vs. It is noted that the photo-leakage current of the a-Si : H(: Cl)/a-Si : H TFT increases with a-Si : H layer thickness.

The off-state drain current of an a-Si : H(: Cl)/a-Si : H TFT deposited with $[SiH_2Cl_2]/[SiH_4] = 0.08$ is much lower than those of

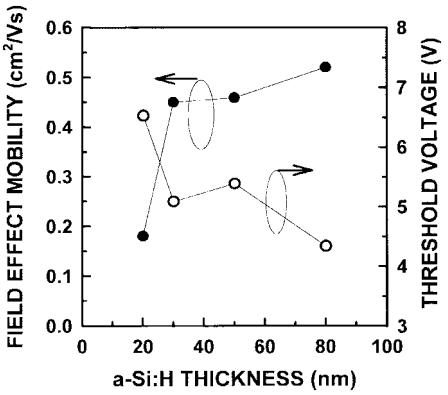

Fig. 4. The field effect mobility and threshold voltage as a function of a-Si : H layer thickness for the a-Si : H(: Cl)/a-Si : H TFT's.

an equivalent a-Si : H TFT. With increasing $[SiH_2Cl_2]/[SiH_4]$ ratio, the room temperature conductivity and conductivity activation energy decrease at first and then saturate [6], which is in contrast to conventional a-Si : H, in which the room temperature dark conductivity decreases if the conductivity activation energy increases because all conventional, undoped a-Si : H films show n-type conduction. The anomalous relationship between room temperature conductivity and conductivity activation energy appears to be due to the p-type behavior of a-Si : H(: Cl) films [6]. The a-Si : H(: Cl) films deposited between $[SiH_2Cl_2]/[SiH_4]$ ratio = 0.04 and $[SiH_2Cl_2]/[SiH_4]$ ratio = 0.12 are p-type. The p-type a-Si : H has less photoconductivity because the drift mobility of hole is much less than that of electron [9].

IV. Conclusion

We have fabricated low off-state leakage current TFT's using a stack with Cl incorporated amorphous silicon [a-Si : H(: Cl)] and amorphous silicon (a-Si : H) as the active layer. The field effect mobility and threshold voltage of the a-Si : H(: Cl)/a-Si : H TFT's are better than those of a-Si : H(: Cl) TFT's. The a-Si : H(: Cl)/a-Si : H TFT's exhibited a field effect mobility of 0.45 cm^2/Vs, a threshold voltage of 5.09 V, and an on/off current ratio of $>10^7$. The off-state leakage currents of a-Si : H(: Cl)/a-Si : H TFT under front as well as backlight illumination are much lower than those of conventional a-Si : H TFT's. By adopting a-Si : H(: Cl)/a-Si : H as an active layer in a TFT, the photo-leakage current can be decreased with only a small degradation in field effect mobility.

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Improved Output ESD Protection by Dynamic Gate Floating Design

Hun-Hsien Chang and Ming-Dou Ker

***Abstract*—A dynamic gate floating design is proposed to improve ESD robustness of the CMOS output buffers with small drive capability. By using this novel design, the human-body-model (machine-model) ESD failure threshold of a 2-mA CMOS output buffer has been practically improved from 1 KV (100 V) to greater than 8 KV (1500 V) in a 0.35-μm CMOS process.**

***Index Terms*—ESD, ESD protection, output buffer.**

I. Introduction

Electrostatic discharge (ESD) robustness of CMOS IC's had been found to be seriously degraded by the advanced deep-submicron CMOS technologies [1]–[3]. To improve ESD robustness of the output transistors, the ESD-implant process and the silicide-blocking process had been widely used in the deep-submicron CMOS technologies [3]–[5]. Besides the advanced process modifications to improve ESD robustness of the output buffers, the symmetrical layout structure had been emphasized to realize the large-dimension output transistors by ensuring the uniform turn-on phenomenon along the multiple fingers of the output transistor [6]. To further enhance the uniform turn-on phenomenon among the multiple fingers of the output transistors, a gate coupling design had been reported to achieve uniform ESD power distribution on the large-dimension output transistors [7]–[11]. But in the practical applications, the output buffers in a cell library have different drive capability specifications, for example, 2, 4, 8, $\cdots$, 24 mA, etc. But, the cell layouts of the output buffers with different drive capabilities are still drawn in the same layout style and area for programmable application. To adjust the different output sink (drive) currents of the output buffer, different fingers of the poly gates in the output NMOS (PMOS) are connected to the pre-buffer circuit, while the other unused poly-gate fingers are connected to ground (VDD). Due to the asymmetrical connection on the poly-gate fingers of the output NMOS in the layout, the ESD turn-on phenomenon among the fingers becomes quite different even if the layout is still symmetrical. This generally causes a very low ESD level for the output buffer, even if the output buffer has a total large device area.

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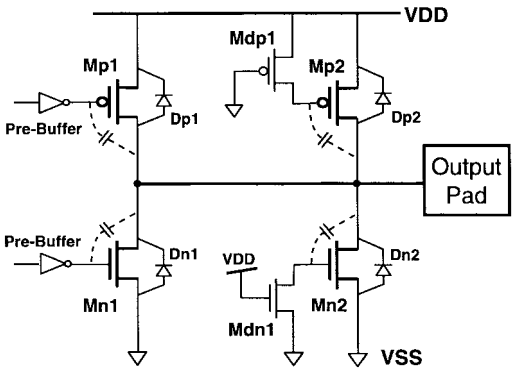

Fig. 1. The output buffer with a small drive capability in a 0.35-μm CMOS process. The gate of the unused Mn2 (Mp2) is connected to VSS (VDD) through a small-dimension Mdn1 (Mdp1) to perform the traditional gate coupling effect for ESD protection.

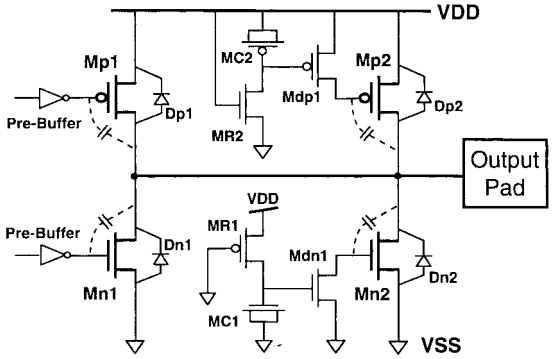

Fig. 2. The dynamic gate floating design to improve ESD level of the output buffers with small drive capability in a 0.35-μm CMOS process.

In this paper, a dynamic gate floating design is proposed to improve ESD level of the output buffers with different drive capabilities in a 0.35-μm CMOS process [12].

II. Output ESD Protection Design

A. Traditional Gate Coupling Design

To enhance the turn-on uniformity of the output buffers, the poly gates of the unused NMOS (PMOS) in the output buffers are connected to VSS (VDD) through a small-dimension NMOS Mdn1 (PMOS Mdp1) [10], as shown in Fig. 1. The Mdn1 (Mdp1) cooperated with the parasitic drain-to-gate capacitance in the Mn2 (Mp2) performs the gate coupling effect to turn on the Mn2 (Mp2) during the ESD stress [9]–[11]. In the normal operating conditions, the gate of Mp2 (Mn2) is connected to VDD (VSS) through the turned-on Mdp1 (Mdn1) to keep the Mp2 (Mn2) off. The output drive (sink) current is provided by the Mp1 (Mn1). For an output buffer with a smaller drive capability, such as only 2mA, the device dimension of the Mn1 (Mp1) is much smaller than that of the Mn2 (Mp2). In a 0.35-μm CMOS cell library, a 2-mA output buffer has the device dimension (W/L) of 30/0.5 (μm/μm) for both the Mn1 and Mp1. But, in the cell layout of the 2-mA output buffer, it also has the device dimension of 450/0.5 (690/0.5) for the Mn2 (Mp2). The gate to drain contact distance in the Mn2, Mp2, Mn1, and Mp1