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A Unique Fault-tolerant Design for Flying Capacitor Multilevel Inverters

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***Abstract* – This paper presents a unique design for flying capacitor type multilevel inverters with fault-tolerant features. When a single-switch fault per phase occurs, the new design can still provide the same number of converting levels by shorting the fault power semiconductors and reconfiguring the gate controls. The most attractive point of the proposed design is that it can undertake the single-switch fault per phase without scarifying power converting quality. This paper will also discuss the capacitor balancing approach under fault-conditions, which is an essential part of controlling flying capacitor type multilevel inverters. Suggested fault diagnosing methods are also discussed in this paper. Computer simulation and lab results validate the proposed controls.**

Keywords: Fault-tolerant, multilevel inverter, multilevel converter, flying capacitor, capacitor balancing.

I. Introduction

The heart of many modern dc/ac inverter designs include multilevel concept, which improves the power quality by inserting a number of small voltage steps in the line-to-ground voltages. Lower losses and improved EMC are additional benefits of multi-level converters [1-7]. The main disadvantage of multilevel converters is that they require more power semiconductors. Most studies on multilevel inverters are focused on the topology and control aspects, with some focus on fault-tolerance [8-12]. Fault-tolerance is an important area considering reduction of downtime in industrial processes and survivability of Naval ship propulsion systems. When typical two-level inverters are applied to a safety-critical system, duplex or even triplex redundant models can be used to handle the fault situation. However, this can be an impractical solution for most multilevel inverters due to cost and size concerns. Nevertheless, redundancy, which can be viewed from several different aspects, is still the crux in designing fault-tolerant systems. Even though providing duplex or triplex redundant multilevel converter models is not an ideal solution, another type of redundancy, topology configuration redundancy, highlights a direction for designing the multilevel inverter system with fault-tolerant features. A multilevel inverter system has this type of redundancy available if its topology has several different switching configurations for generating the same numbers of line-to-ground voltage levels. The diode-clamped multilevel inverter (DCMI) [1,2] and the flying capacitor multilevel inverter (FCMI) [3,4] are two of the most popular multilevel inverter topologies. References [8-12] discuss the fault-tolerant features of the DCMI and FCMI, which present fault-tolerant solutions by scarifying some of the converting levels when a fault occurs. This paper will present a unique solution for the 4-level fault-tolerant multilevel inverter which can keep consistent converting levels even under single-switch fault per phase conditions. Compared to DCMI, FCMI topology has more switching state redundancy per voltage converting level and the large number of redundant voltage levels allows extra opportunities for capacitor voltage balancing [7]. Therefore, the FCMI topology is adopted in this fault-tolerant design.

II. 3-Cell 4-Level FCMI Topology Review and Its Topology Redundancy

Fig. 1 shows the per phase topology of a 3-cell 4-level FCMI. The line-to-ground voltage of the xth phase can be expressed as

$$v_{xg} = \frac{s_x}{3} v_{dc}, \quad s_x = 0,1,...3 \tag{1}$$

where x represents the phase a, b or c, and s_x represents the phase switching states selected by the gating signals. The line-to-neutral voltages are given by [13]

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \tag{2}$$

The conventional m-cell FCMI topology [2], where each cell includes one dc source and one pair of complementary switches, sets dc voltages to:

$$v_{xi} = \frac{i}{m} v_{dc}, \quad (i = 1,2,...m) \tag{3}$$

This voltage setting yields $n = m + 1$ line-to-ground voltage levels. Specifically, the 3-cell FCMI as shown in Fig. 1 sets dc voltage ratio as $v_{x1} : v_{x2} : v_{x3} = 1 : 2 : 3$, which yields four line-to-ground voltage levels. Recent research shows that different line-to-ground levels may be obtained by varying the dc link voltage ratio settings. A new full binary combination scheme (FBCS) is reported in [4], which covers the maximum switching state combinations thus generating more converting levels. FBCS 1 sets dc voltages to

$$v_{xi} = \left(\frac{2^i - 1}{2^m - 1} \right) \cdot v_{dc} \tag{4}$$

TABLE I.
TWO-CELL 4-LEVEL FBCS INVERTER

	T_{x1}	T_{x2}	s_x	v_{xg}
FBCS 1,2	0	0	0	0
FBCS 1	0	1	1	$v_{dc}/3$
FBCS 2	1	0		
FBCS 1	1	0	2	$2v_{dc}/3$
FBCS 2	0	1		
FBCS 1,2	1	1	3	v_{dc}

TABLE II.
ACTIONS FOR SINGLE SWITCH FAULTS

Fault switch	Bypassed switch	Forced closed	Opened DC link branch
T_1	T_1	$\bar{T}_1$	v_{x2} branch
T_2	T_2	$\bar{T}_2$	v_{x2} branch
T_3	T_3	$\bar{T}_3$	v_{x1} branch
$\bar{T}_1$	$\bar{T}_1$	T_1	v_{x2} branch
$\bar{T}_2$	$\bar{T}_2$	T_2	v_{x2} branch
$\bar{T}_3$	$\bar{T}_3$	T_3	v_{x1} branch

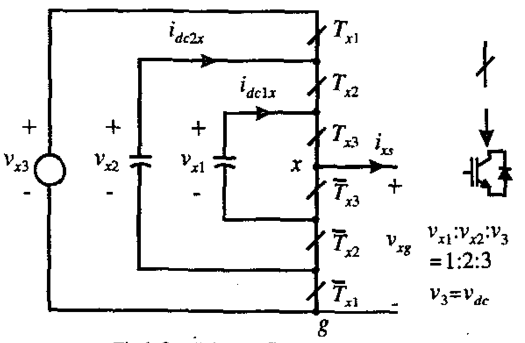


Fig 1. 3-cell 4-level flying capacitor topology

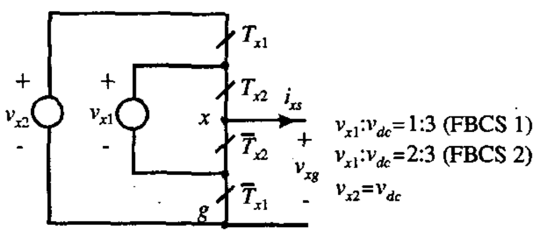


Fig 2. 2-cell 4-level floating voltage source inverter topology

FBCS2 sets DC voltages to:

$$v_{xi} = \left(1 - \frac{2^{m-i} - 1}{2^m - 1}\right) \cdot v_{dc} \qquad (5)$$

Both FBCS 1 and FBCS 2 result in 2^m levels of v_{xg}. According to FBCS, a 2-cell FCMI as shown in Fig. 2 can generate four line-to-ground voltage converting levels either by setting the voltage ratio to $v_{x1} : v_{x2} = 1 : 3$ (FBCS 1) or 2 : 3 (FBCS 2). Table I shows the switching states and the related line-to-ground voltage converting levels. Note that the 3-cell 4-level FCMI topology as shown in Fig. 1b actually includes the 2-cell 4-level FBCS topologies. Suppose that the capacitors are balanced, when one takes the v_{x2} dc branch out from the 3-cell topology and forces T_{x1} and T_{x2} open or closed together, it will be identical to the topology shown in Fig. 2 with $v_{x1} : v_{x2} = 1 : 3$. Similarly, if one takes the v_{x1} dc branch out from the 3-cell topology and force T_2 and T_3 open or closed synchronously, it will be identical to the topology shown in Fig. 2 with $v_{x1} : v_{x2} = 2 : 3$. The 2-cell FBCS configurations can be treated as the topology configuration redundancies of the conventional 3-cell FCMI. This new discovery has a very special meaning to the fault-tolerant design of the 3-cell 4-level multilevel inverter.

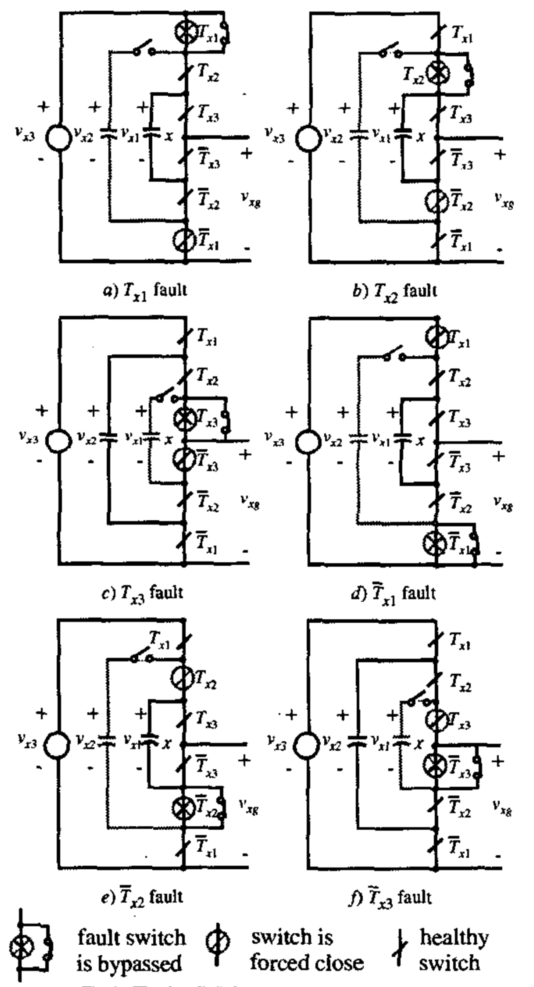


Fig 3. The 3-cell flying capacitor multilevel inverter circuitry reconfiguration under single switch fault conditions

When single switch fault happens, if one can reconfigure the switching connections and gate controls so as to acquire an equivalent 2-cell FBCS topology as well as the effective capacitor balancing approach, then the inverter can always provide four line-to-ground voltage levels. This paper will present such a fault-tolerant inverter design which may provide four consistent line-to-ground converting levels even under single-switch-per-phase fault situation. For clarity, Section III will focus on the discussion of the circuitry reconfiguration under fault conditions with the assumption that the dc capacitor voltages have no balancing problem. Section IV will release the assumption for discussing the dc capacitor voltage balancing approach and related controls. Computer simulation studies and lab validation are included in Sections V and VI, respectively.

III. FAULT ANALYSIS FOR THE 3-CELL 4-LEVEL FCMI

A. Single Switch Faults

The 3-cell FCMI topology, as shown in Fig. 1, includes three pairs of complementary power semiconductors in each phase. No matter which semiconductor is faulted, **it is always possible to reconfigure the inverter topology to make it work as a 2-cell FBCS inverter**, which can still guarantee four line-to-ground converting levels. For instance, when a T_{x1} fault is detected, one may bypass the fault semiconductor T_{x1} and force $\overline{T}_{x1}$ to be closed, and at the same time separate the v_{x2} branch from the main circuitry. Then equivalently, v_{x1} branch, v_{x3} branch, T_{x2} , $\overline{T}_{x2}$, T_{x3} and $\overline{T}_{x3}$ form a 2-cell 4-level FBCS inverter phase leg. This inverter will work under the configuration of two healthy 3-cell FCMI phase legs and one equivalent 2-cell FBCS phase leg, which can still provide four voltage-converting levels. Table II lists the related actions taken under the different fault cases. Fig. 3 shows all the possible circuitry configurations for the six single-switch-fault cases per phase.

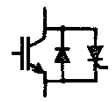
B. Multiple Switch Faults

If more than one switch is faulted in the same phase, it may be impossible to reconfigure the circuitry to work as a 2-cell FBCS inverter. Therefore, the method discussed in part *A* of this Section is no longer effective. However, if the faults are distributed in the three different phases and the maximum number of faulty switches per phase is one, then it is still possible to have the inverter provide four line-to-ground converting levels by configuring the related fault phases to the FBCS structure. For example, if T_{a1} and T_{b3} are faulted, one can reconfigure phase *a* as FBCS 1, phase *b* as FBCS 2, and keep phase *c* as a normal 3-cell phase leg.

IV. THE 4-LEVEL FCMI FAULT TOLERANCE DESIGN

A. Fault Type And Fault Switch Handling

IGBTs have been widely used in power converter system due to the relatively high rated voltages and switching frequencies. Most commercial IGBT modules are also integrated with a shunt diode for undertaking the free-wheeling current. The fault type of the IGBTs can either be an open circuit fault or a short circuit fault. When a fault happens, it is suggested that the fault device is bypassed by adding additional SCRs in parallel to the power semiconductors. Fig. 4 shows the proposed structures. Once a fault is detected, the related SCRs can be gated on to short the fault semiconductor so that it will not be involved in the FBCS configurations. When the structure in Fig. 4b is adopted for handling both the IGBT and diode fault cases, the total number of semiconductors will be the same as the utilization of a redundant converter for fault tolerance purposes. However, It is not necessary for the SCRs to be high frequency devices, therefore, the cost can be lower than using two redundant converters. In this paper, only the IGBT faults are considered and the structure as in Fig. 4a is adopted.


a). IGBT fault handling circuit

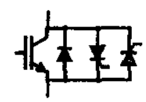

b). IGBT or diode fault handling circuit

Fig. 4. Suggested power switch modules for fault handling.

B. General Structure of the Fault-Tolerant Design

The main circuitry of the proposed fault-tolerant inverter design is shown in Fig. 5, which can keep consistent line-to-ground voltage converting levels even when a single-switch-fault per phase occurs. In each phase, two more switches, T_{dc1x} and T_{dc2x} are added to the dc branch, which will be used to disconnect the related dc branch when a fault occurs. Since these two switches are not operated as frequently as the other power semiconductors, they can be treated as fault-free devices in this fault-tolerant design. As discussed in Section III, this design can either work under normal 3-cell 4-level FCMI operation mode or the single-switch-fault per phase operation mode by properly configuring the semiconductors. Figure 6 gives the general control diagram for the proposed design. It can be seen that both three-phase joint redundant states selector (Joint RSS) and per phase redundant states selector (*x*-phase RSS) are utilized in the fault-tolerant control for maintaining balanced capacitor voltages. Detailed discussions about the RSS controls can be found in the consecutive part of this Section.

C. Modulation Techniques

The goal of the modulation technique is to control the gating signals so that power semiconductors switch on/off as desired. The gating signals are directly related to the switching states (or levels) s_x. A voltage-source duty-cycle modulation method, which is adopted in this design, has been presented in [5]. This method is discrete in nature and is suitable for digital signal processor (DSP) implementation. Alternatively, the multi-level sine-triangle modulation method [6] may also be used to generate the switching states s_x. Fig. 7 demonstrates the sine-triangle modulation process. Since the proposed design features providing four converting levels under both fault-free and single-switch-fault per phase modes, four switching states need to be guaranteed.

D. Fault Free Operation and the Per-Phase Redundancy

As can be seen from Fig. 4, no additional circuitry is added to balance the dc link capacitors; therefore, the capacitor balancing approach is the linchpin of this fault-tolerant design. One of the most important advantages of FCMI topology is that large numbers of redundant switching states are available for generating the same line-to-line or line-to-ground voltage levels. Those redundancies can always be considered as the remedy for capacitor balancing under fault or fault-free situations. Under fault free operation, switches T_{dc1x} and T_{dc2x} are closed and all the SCRs in parallel with the IGBTs are in off states. This device will work as a conventional 3-cell 4-level FCMI. Although one may utilize the large number of 3-phase joint redundant switching states to balance the capacitors, it needs to be pointed out that the unsuitable selection of the joint switching states may limit the choice of modulation index, and also increase the control complexity. Therefore, one need give priority to the balance of the capacitor voltages by using the per-phase line-to-ground voltage redundancies, if possible. Table III shows the relationship between the per-phase switching states and the line-to-ground voltages. Therein it can be seen that $s_x = 0$ and 3 have no redundancies available, however, these two states do not have the capacitor voltages involved, so there are no balancing concerns. When $s_x = 1$ or 2, the capacitor voltages are involved so it is possible that a capacitor will be charged or discharged under certain conditions. Because there are three redundant switching states available for generating the same line-to-ground voltage levels, they can be used to balance the capacitors. In a practical implementation, sensors measure the phase currents and capacitor voltages. An analog-to-digital conversion is performed to determine the current direction and capacitor imbalance [4]. Let F_{ix} denote the current direction flag, Fv_{x1} and Fv_{x2} denote the capacitor imbalance flags of phase x. These flags are defined by

$$F_{ix} = \begin{cases} 0 & i_{xs} < 0 \\ 1 & i_{xs} \geq 0 \end{cases} \tag{6}$$

$$Fv_{x1} = \begin{cases} 0 & v_{x1} < \dfrac{v_{dc}}{3} \\ 1 & v_{x1} \geq \dfrac{v_{dc}}{3} \end{cases} \tag{7}$$

$$Fv_{x2} = \begin{cases} 0 & v_{x2} < \dfrac{2v_{dc}}{3} \\ 1 & v_{x2} \geq \dfrac{2v_{dc}}{3} \end{cases}. \tag{8}$$

The per-phase redundancy selection table can be found from Table IV. In Fig. 6, the joint redundancy states selector (Joint RSS) can simply bypass the original switching states generated by the modulation block and send them to the per-phase RSS, when the "*Fault Mode*" signal indicates fault-free operation.

E. Three-Phase Joint Switching State Redundancy

When single switch fault is detected, the SCR in parallel with the fault switch is gated on and its complementary switch will be gated on all the time. Meanwhile, switches T_{dc1x} or T_{dc2x} in the fault phase x will be opened to separate the related dc link capacitor branch so that the fault phase can be reconfigured to work as an FBCS phase leg as described in section III. For the faulted phase, each switching state refers to a unique v_{xg} level as shown in Table I, and no redundant switching combinations are available in terms of per-phase switching states. Therefore, if capacitors are used to form the dc link voltages, there is no direct approach to balance the capacitor voltages on a per-phase basis as in the fault-free operation, and one has no choice but to use the redundancies of the three-phase joint switching states.

Transforming the a- b- and c-phase stator voltages to the q- and d-axis stationary reference frame results in the stator voltage vectors plot achievable from the switching states of the multilevel inverters. Fig. 8 shows the space vector plot of the 4-level FCMI in terms of the three-phase joint switching states. Therein, each vector is listed as s_a, s_b, s_c. From Fig. 8, one may clearly see the distribution of 3-phase joint switching state redundancy. In general, a redundant state may be found for a given switching state by incrementing or decrementing the states for all three phases since this results in changing the zero-sequence line-to-ground voltage, which does not affect the load voltages. The boundary states are the joint states with the highest switching level or the lowest switching level in some phases. In Fig. 8, for instance, the redundancies of the switching state (1,2,1) can be found by adding 1 to or subtracting 1 from each states so as to achieve (0,1,0), (2,3,2), all of which refer to the same space vector. It is helpful to define s_{max}, s_{min} and rd (redundant degree) as

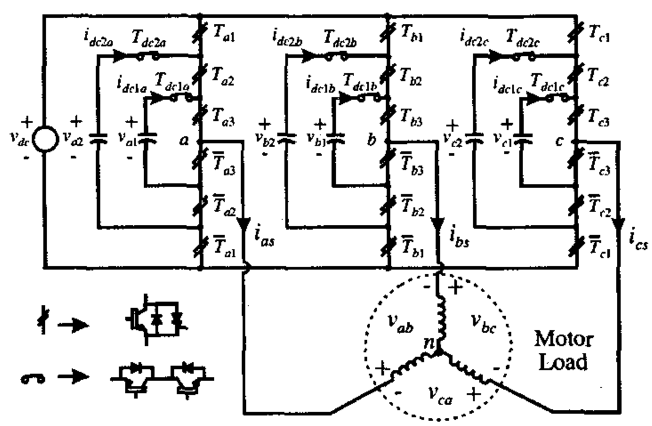


Fig. 5. 3-cell 4-level flying capacitor fault-tolerant design with capacitor balancing feature ($v_{x1} : v_{x2} : v_{dc}$ = 1:2:3)

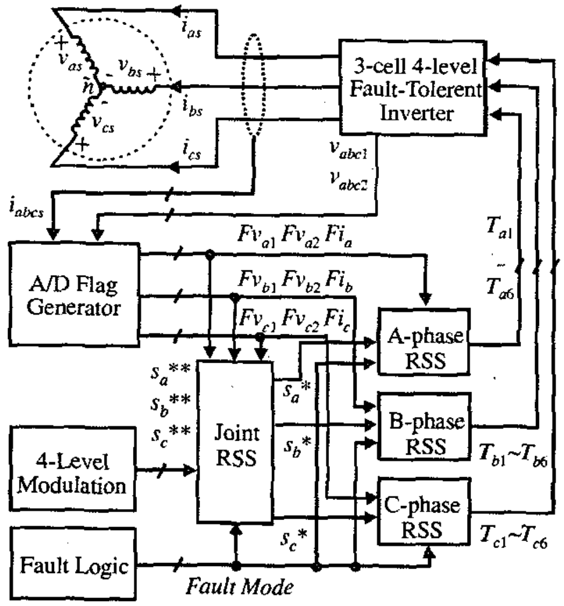


Fig. 6. Control diagram for the 3-cell 4-level inverter with single-switch-fault per phase.

TABLE III
3-CELL 4-LEVEL FCMI INVERTER REDUNDANCIES

s_x	T_{x1}	T_{x2}	T_{x3}	v_{xg}
0	0	0	0	0
1	0	0	1	$v_{dc}/3$
	0	1	0	$v_{dc}/3$
	1	0	0	$v_{dc}/3$
2	0	1	1	$2v_{dc}/3$
	1	0	1	$2v_{dc}/3$
	1	1	0	$2v_{dc}/3$
3	1	1	1	v_{dc}

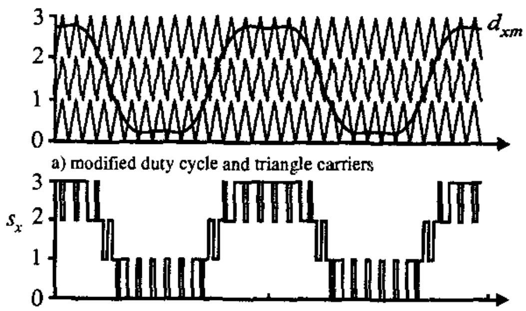
TABLE IV
3-CELL 4-LEVEL FCMI PER-PHASE REDUNDANCY SELECTIONS

s_x	T_{x1}	T_{x2}	T_{x3}	Flag Conditions
0	0	0	0	Don't care
1	0	0	1	$Fi_x = 0$ and $Fv_{x1}=0$
				$Fi_x = 1$ and $Fv_{x1}=1$ and $Fv_{x2}=1$
	0	1	0	$Fi_x = 0$ and $Fv_{x1}=1$ and $Fv_{x2}=0$
				$Fi_x = 1$ and $Fv_{x1}=0$ and $Fv_{x2}=1$
	1	0	0	$Fi_x = 0$ and $Fv_{x1}=1$ and $Fv_{x2}=1$
				$Fi_x = 1$ and $Fv_{x2}=0$
2	0	1	1	$Fi_x = 0$ and $Fv_{x1}=0$ and $Fv_{x2}=0$
				$Fi_x = 1$ and $Fv_{x2}=1$
	1	0	1	$Fi_x = 0$ and $Fv_{x1}=0$ and $Fv_{x2}=1$
				$Fi_x = 1$ and $Fv_{x1}=1$ and $Fv_{x2}=0$
	1	1	0	$Fi_x = 0$ and $Fv_{x1}=1$
				$Fi_x = 1$ and $Fv_{x1}=0$ and $Fv_{x2}=0$
3	1	1	1	Don't care

TABLE V
SUMMARY OF THE GOODNESS DEGREE FOR THE FAULTY PHASE

s_f	Fv_f	Fi_f	gd_f	
			FBCS 1	FBCS 2
0	X	X	0	0
1	0	0	1	-1
	0	1	-1	1
	1	0	-1	1
	1	1	1	-1
2	0	0	-1	1
	0	1	1	-1
	1	0	1	-1
	1	1	-1	1
3	X	X	0	0

Notes: $Fv_f = Fv_{f1}$, for FBCS 1 reconfiguration. $Fv_f = Fv_{f2}$, for FBCS 2 reconfiguration. The fault phase f can be phase a, b or c.



a) modified duty cycle and triangle carriers

b) switching state

Fig. 7. Four-level sine-triangle modulation technique.

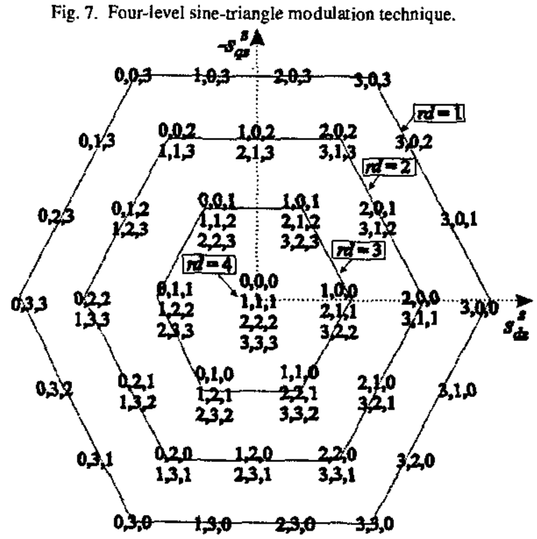


Fig. 8. Space vector plot of the 3-cell 4-level FCMI

$$s_{\max} = \mathrm{MAX}(s_a, s_b, s_c) \tag{9}$$

$$s_{\min} = \mathrm{MIN}(s_a, s_b, s_c) \tag{10}$$

$$rd = nl - (s_{\max} - s_{\min}) \tag{11}$$

where the MAX function returns the maximum switching state among the three-phase joint switching states s_a s_b s_c and the MIN function returns the minimum. The variable nl

represents the number of converting levels, which equals 4 in this design. The term, redundant degree, is used to represents the number of the redundant joint switching states $s_a\, s_b\, s_c$, which refer to the same voltage space vector. For example, the *rd* of the joint switching states of $s_a s_b s_c$ (100) is 3, which means two other joint switching states (211), and (322) are available for providing the same voltage space vector as (100). The single-switch fault per phase can be classified into three cases:

1) Only one phase includes a fault switch.
2) Two phases each includes a fault switch.
3) All three phases each includes a fault switch.

For case 1, suppose T_{a2} is faulted. The faulty phase a will be reconfigured as a FBCS1 inverter including only the v_{a1} branch. A term goodness degree (*gd*) can then be used to evaluate the capacitor voltage-balancing situation of the faulty phase. As can be seen from Fig. 3, when $s_a = 0$ or 3, the dc capacitor voltage v_{a1} will not be involved in providing the line-to-ground voltage, therefore there is no capacitor charging or discharging concerns and $gd_a = 0$. When $s_a = 1$, the dc voltage v_{a1} will be involved. The desired situation is that when v_{a1} is larger than $v_{dc}/3$ ($F_{va1} = 1$), the current i_{as} is positive ($F_{ia} = 1$) so as to discharge the capacitor, and when v_{a1} is lower than $v_{dc}/3$ ($F_{va1} = 0$), the current i_{as} is negative ($F_{ia} = 1$) so as to charge the capacitor. The goodness degree $gd_a = 1$ will be set for the most desired case. If the capacitor is involved but it is not the desired case, $gd_a = -1$. Similarly, one can set the goodness degree for $s_a = 2$. Let s_f denote the switching state of the faulty phase, Table V summaries the goodness degree settings for the faulty phase f. For capacitor balancing purposes, the final selection of the joint redundant switching states ends up with the determination of the joint switching state that has the highest goodness degree. It should be pointed out that although the 3-phase joint switching state redundancies have to be used to balance capacitor voltage of the faulty phase, two healthy phase legs do exist and it is still possible to utilize the per phase redundancy to balance the healthy phases. Therefore, when the single switch fault occurs, the capacitor balancing approach can be divided into two stages, Joint switching state redundancy selection stage

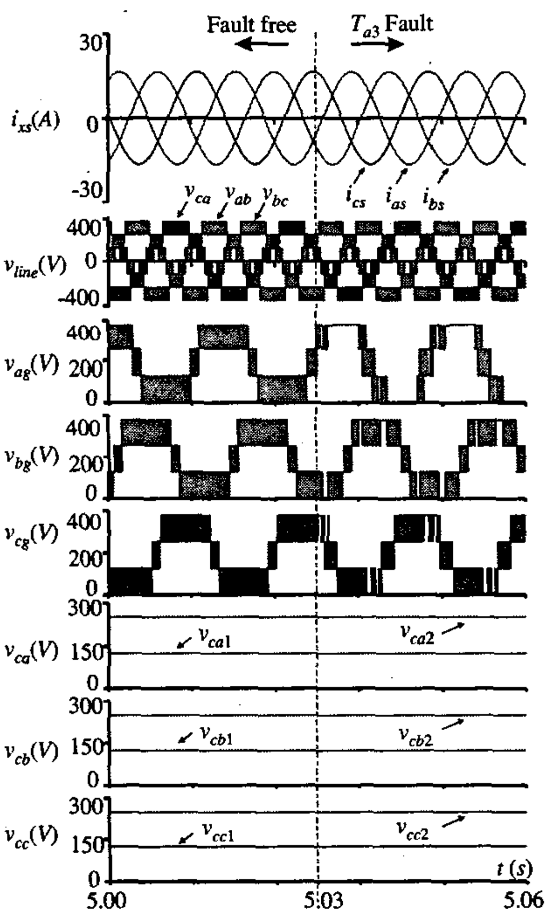


Fig. 9. Simulation waveforms for the 3-cell 4-level inverter under single-switch-fault mode (ignoring fault diagnosis time)

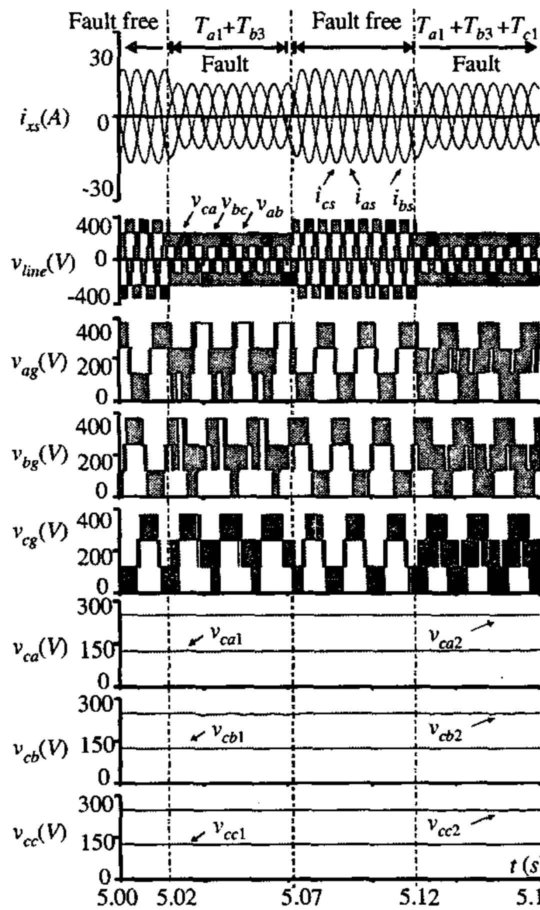


Fig. 10. Simulation waveforms for the 3-cell 4-level inverter under multiple-switch-fault mode

and per-phase switching state redundancy selection stage as shown in Fig. 6. The Joint RSS will first find a joint redundant state that has the highest goodness degree for the faulty phase, then send it into the per phase RSS for further processing. For the fault phase f, the per-phase RSS will be inactive and the switching state acquired from the joint RSS will be used since there is no per phase redundancy available for FBCS configurations. For the healthy phases, the per-phase RSS will balance the capacitor voltages.

For case 2 where two phases have faulty switches, the joint redundancy selection process is similar to that of case 1 except that the switching states will be determined by the summarized goodness degree of the two faulty phases and only one healthy phase is processed by the per phase RSS.

For case 3, all phases include single-switch-fault per phase; therefore the selection of the joint switching states will be based on the total goodness degree

$$gd_{total} = gd_{fa} + gd_{fb} + gd_{fc} \qquad (12)$$

and all of the three per phase RSS will be bypassed. It also needs to be pointed out that the choice of the modulation index is limited by the load characteristics and available switching redundancies. Choosing a modulation index value beyond the limit might deteriorate the balance of the capacitor voltages. Generally, highly inductive load may undertake higher modulation index, and the more the number of fault switches is, the lower the modulation index can be.

F. *Fault Diagnosis*

Many commercial gate drives have over-current or over-voltage protection capabilities, which could be used to identify a faulty switch. When an over-current or over-voltage presents, the gate drives will stop all control signal channels to protect the IGBTs. If the inverter device is shut down by the gate drives, testing signals can be assigned to control signal channels and by measuring the currents and voltage drops cross the IGBTs, it is possible to recognize the faulted switches. The fault diagnosis technique for a 3-cell 4-level FCMI introduced in [10] can be a useful reference to interested readers. The diversity of multilevel inverter structures leaves the fault diagnosis issue an open area for further studies.

V. COMPUTER SIMULATION

A computer simulation model with a three-phase R-L load has been created to verify the proposed design. The input DC voltage is 375V and the AC main frequency is 60Hz. Fig. 9 shows the fault-free and single-phase-fault performance. It can be seen that the per-phase capacitor balancing method works effectively for generating four line-to-ground voltage levels under fault-free mode. When T_{a3} fault occurs, the inverter can still provide four line-to-ground voltage levels and the capacitor voltages can still be balanced by using the joint RSS and per-phase RSS. The modulation index used in the study of Fig. 9 was 1.0 and this was found to be the maximum in order to maintain capacitor balance under single-switch-fault operation. It needs to be mentioned that under fault-free operation, the modulation index can be set to the maximum limit considering the third harmonics injection [5]. Fig. 10 shows inverter performance of the double-switch-fault and triple-switch-fault cases. The modulation index for the fault-free case is set to 1.0, and it is lowered down to 0.7 when double- or triple-switch-fault occurs, so as to keep the capacitor voltages balanced around their desired values. Figures 9, 10 verify that the proposed design can provide four consistent line-to-ground levels even when the single-switch-fault per phase occurs. The two-stage capacitor balancing method, the per-phase RSS and the goodness degree based three-phase joint RSS successfully synthesize the dc link capacitor voltages.

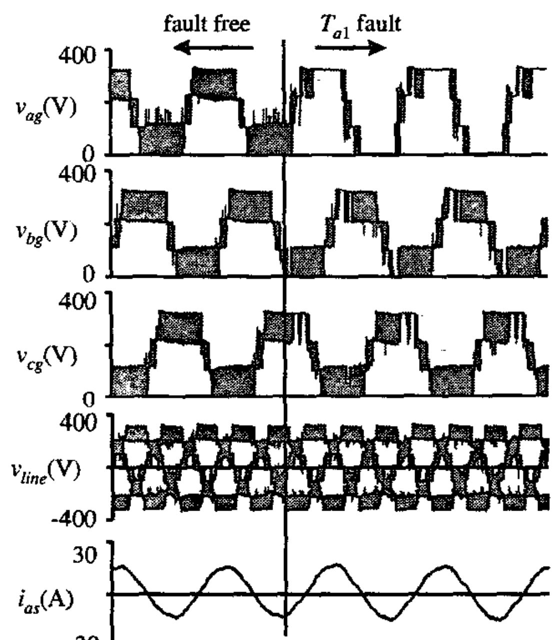


Fig. 11. Experimental result

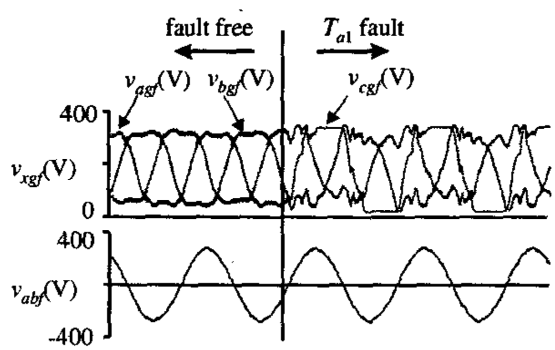


Fig. 12. Filtered experimental results

VI. LAB VALIDATION

To verify the proposed fault-tolerant inverter design for single-switch fault, a laboratory 3-cell 4-level FCMI prototype has been established to drive a 3.7KW induction motor load, where the dc input voltage is 330V and the ac main frequency is set to 60Hz. The inverter modulation was accomplished using a CPLD with a PWM pattern pre-programmed, which has a switching frequency of 10kHz and a modulation index of 1.0.

In this lab study, the inverter is switched from the fault-free mode to the single-switch-fault mode immediately after T_{a1} is shorted. Fig. 11 shows the related waveforms. As can be seen, four line-to-ground voltage-converting levels are generated under both fault-free and single-switch-fault situations. Although the line-to-ground voltage shape looks different, the joint RSS takes effect when T_{a1} is faulted and the line-to-line voltages show consistent performance for both fault-free and single-switch-fault cases. Fig. 12 shows the filtered version of the line-to-ground voltages and line-to-line voltage. It can be seen that in fault free mode, the line-to-ground voltage shows the shape of the third harmonic injection. When the T_{a1} fault happens, the three-phase joint redundancy selector takes effect, which leads to a clear and sinusoidal line-to-line voltage waveform under both fault and fault-free mode. The low-frequency harmonics in the current waveform in Fig. 11 are due to the induction motor non-linearity. It can be seen that the experimental results match the simulation results shown in Fig. 9.

VII. CONCLUSION

This paper has presented novel fault-tolerant design for multilevel inverters. Instead of scarifying some of the line-to-ground voltage converting levels, the proposed design can guarantee consistent line-to-ground converting levels when a single-switch-fault per phase occurs. This fault-tolerant design tightly relates to the discussion of the following conceptions: 1). The reconfiguration of the original inverter circuitry by utilizing its FBCS topology configuration redundancy; 2) the per-phase switching state redundancy selection rules; 3) the goodness degree based three-phase joint switching state redundancy selection rules. Computer simulation and experimental results have been presented to verify the proposed design.

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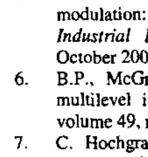

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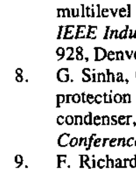

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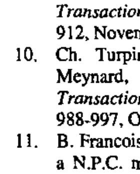

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