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Full Binary Combination Schema for Floating Voltage Source Multi-Level Inverters

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***Abstract* - This paper presents schema of operation for floating voltage source multi-level inverters. The primary advantage of the proposed schema is that the number of voltage levels (and thus power quality) can be increased for a given number of semiconductor devices when compared to the conventional "flying capacitor" topology. However, the new schema requires fixed floating sources instead of capacitors and therefore is more suitable for battery power applications such as electric vehicles, flexible AC transmission systems and submarine propulsion. Alternatively transformer/rectifier circuits may be used to supply the floating sources in a similar way to cascaded H-bridge inverters. Computer simulation results are presented for 4-, 8- and 16-level inverter topologies. A 4-level laboratory test verifies the proposed method.**

Keywords: Multi-level inverters, Pulse-width modulation, voltage-source, Flying capacitor.

I. INTRODUCTION

DC/AC inverters are widely used in motor control systems. The harmonics generated on the AC side greatly influence the power quality of the control system. The multi-level inverter improves the AC power quality by performing the power conversion in small voltage steps leading to lower harmonics [1-3]. For this reason, researchers have done considerable work on multi-level inverters in recent years. The floating voltage source multi-level inverter topology, also known as the flying capacitor inverter [4-15], is one of the typical methods for reducing the harmonics by increasing the inverter levels. A new method, Full Binary Combination Scheme (FBCS), based on the FS topology is described herein. With the same amount of power switches, FBCS can utilize all the possible switch combinations and generate a higher number of levels compared to the conventional floating source method.

II. THE CONVENTIONAL FS MULTI-LEVEL INVERTER

A. The Two-Cell FS Inverter Topology

The conventional floating source (FS) topology for a three-level inverter is shown in Fig. 1. In this topology, two voltage sources and four power switches (IGBTs) are used for each phase. This topology can also be called the two-cell FS topology, where each cell includes one voltage source and two complementary switches.

The DC voltage ratio of the traditional two-cell inverter [5] is $v_1 : v_2 = 1 : 2$. If $v_2 = E$ the relationship between the switching states and the line-to-ground voltage can be shown in Table I, where "x" represents phase a, phase b or phase c. From Table I it can be seen that the switches have four possible combinations while the line-to-ground voltage generated on AC side has only three possible values.

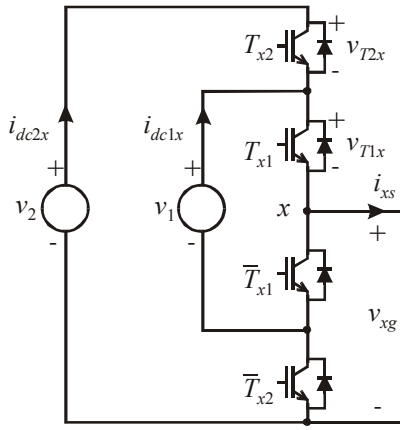

Figure 1. Two-cell FS topology

Table I. Traditional two-cell inverter		
T_{x2}	T_{x1}	v_{xg}
0	0	0
0	1	$E/2$
1	0	E/2
1	1	E

B. The Three-Cell FS Inverter Topology

Using the topology shown in Fig. 2, a four-level inverter can be realized, if the DC voltage ratio of the traditional three-cell inverter is $v_1 : v_2 : v_3 = 1 : 2 : 3$. Assuming $v_3 = E$ the relationship between the switching states and the line to ground voltage is shown in Table II. It can be seen that the three switches of each phase have $2^3 = 8$ possible combinations while the line-to-ground voltage v_{xg} generated on the AC side only has four possible values. This indicates an underutilization of switching states.

C. The n-Cell FS Inverter Topology

Conventional FS inverters with other cell numbers can be studied where DC voltage sources are set to

$$v_i = \frac{i}{nc}E, \quad (1 \le i \le nc) \qquad \textbf{(1)}$$

where nc is the number of cells. The results are summarized

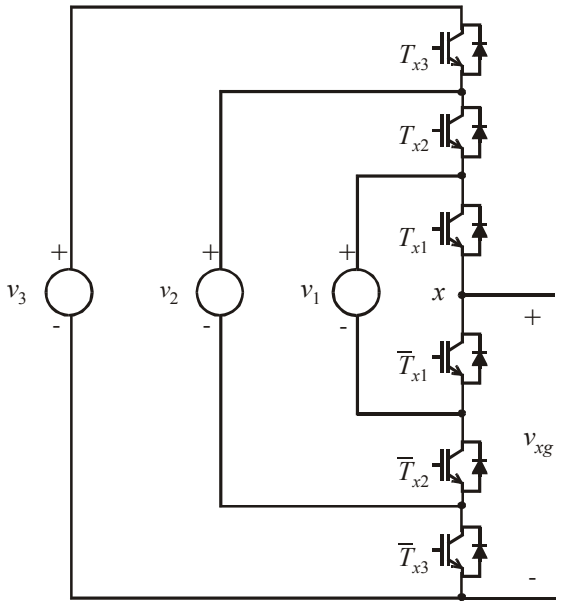

Figure 2. Three-cell FS topology.

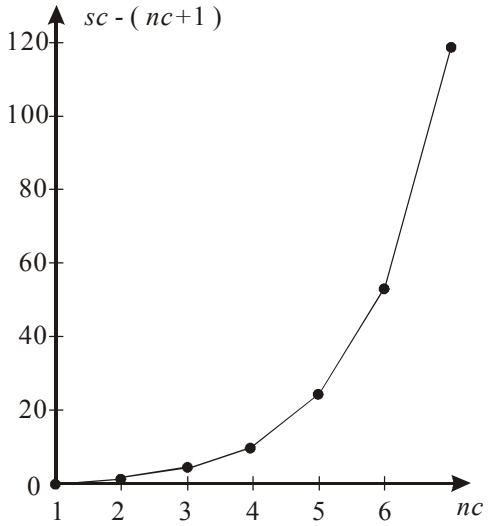

Figure 3. Unused switch combinations in conventional FS inverter.

Table II. Traditional three-cell inverter.			
T_{x3}	T_{x2}	T_{x1}	v_{xg}
0	0	0	0
0	0	1	$E/3$
0	1	0	$E/3$
0	1	1	$2E/3$
1	0	0	$E/3$
1	0	1	$2E/3$
1	1	0	$2E/3$
1	1	1	E

Table III. Summary of conventional FS topology (nc>1).			
nc	ns	sc	nl
2	$2\times2=4$	$2^2=4$	3
3	$2\times3=6$	$2^3=8$	4
4	$2\times4=8$	$2^4=16$	5
. .	. .	. .	. .
n	$2n$	2^n	n+1

in Table III where

ns = number of switches

sc = number of switch combinations

nl = number of voltage levels

Table III shows that each cell added increases inverter voltage levels by one. It can be seen that the conventional FS topology only uses part of the switching combinations, and $2^n - (n + 1)$ switching combinations are not utilized. Figure 4 shows that with increasing nc, the unused switching combinations increase dramatically.

III. Full Binary Combination Schema (FBCS)

A. A 4-Level Design for the Two-Cell Inverter

From Table I and Fig. 1, it can be seen that the circuit generates the same line-to-ground voltage for the "01" and "10" switching combinations. If a new design can refer "01" or "10" switching states to different voltages, a four-level inverter will result instead of a 3-level inverter. Table IV shows the results of a new design for a two-cell inverter by using the same topology shown in Fig. 1. Here the ratio $v_1 : v_2$ is changed from 1 : 2 to 1 : 3. From Table IV it can be seen that if a suitable ratio of v_1 and v_2 is chosen, all four switching combinations can be utilized, and a 4-level inverter can be created by using the same topology as Fig. 1.

Table IV. Two-cell 4-level inverter.		
T_{x2}	T_{x1}	v_{xg}
0	0	0
0	1	$E/3$
1	0	$2E/3$
1	1	E

Table V. Three-cell 8-level inverter.			
T_{x3}	T_{x2}	T_{x1}	v_{xg}
0	0	0	0
0	0	1	$E/7$
0	1	0	$2E/7$
0	1	1	$3E/7$
1	0	0	$4E/7$
1	0	1	$5E/7$
1	1	0	$6E/7$
1	1	1	E

B. An 8-Level Design for the Three-Cell Inverter

Table V shows the results of an 8-level inverter design using the same topology as Fig. 2. The voltage ratio of v_1, v_2 and v_3

Table VI. Four-cell 16-level inverter applying FBCS.							
T_{x4}	T_{x3}	T_{x2}	T_{x1}	v_{xg} Formulas	v_{xg} (FBCS 1) 1:3:7:15	v_{xg} (FBCS 2) 8:12:14:15	v_{xg} (AFBCS) 1:5:13:15
0	0	0	0	0	0	0	0
0	0	0	1	v_1	E/15	8E/15	E/15
0	0	1	0	$v_2 - v_1$	2E/15	4E/15	4E/15
0	0	1	1	v_2	3E/15	12E/15	5E/15
0	1	0	0	$v_3 - v_2$	4E/15	2E/15	8E/15
0	1	0	1	$v_3 - v_2 + v_1$	5E/15	10E/15	9E/15
0	1	1	0	$v_3 - v_1$	6E/15	6E/15	12E/15
0	1	1	1	v_3	7E/15	14E/15	13E/15
1	0	0	0	$v_4 - v_3$	8E/15	E/15	2E/15
1	0	0	1	$v_4 - v_3 + v_1$	9E/15	9E/15	3E/15
1	0	1	0	$v_4 - v_3 + v_2 - v_1$	10E/15	5E/15	6E/15
1	0	1	1	$v_4 - v_3 + v_2$	11E/15	13E/15	7E/15
1	1	0	0	$v_4 - v_2$	12E/15	3E/15	10E/15
1	1	0	1	$v_4 - v_2 + v_1$	13E/15	11E/15	11E/15
1	1	1	0	$v_4 - v_1$	14E/15	7E/15	14E/15
1	1	1	1	v_4	E	E	E

is changed from 1 : 2 : 3 to 1 : 3 : 7. The relationship between switching states and v_{xg} is shown on Table V. Therein, it can be seen that if a suitable ratio of $v_1 : v_2 : v_3$ is chosen, all the eight switching combinations can be utilized and an 8-level inverter can be created by using the same topology as Fig. 2.

C. General Representation for FBCS

The previous sections have presented examples of how the switching states may be maximized in a floating source inverter. The crux of this method relies on the selection of an appropriate ratio for the DC voltages. In general, there are several ways to do this. This section presents two methods to choose the DC voltages v_i for setting the voltage ratios. The first method, referred to as full binary combination schema 1 (FBCS1), is to set the DC voltage ratio v_i as

$$v_i = \left(\frac{2^i - 1}{2^{nc} - 1}\right)E \quad (1 \le i \le nc) \tag{2}$$

On the AC side, the inverter can always generate $nl = 2^{nc}$ levels of line-to-ground voltage, which also equals the entire binary number combinations of the switches. The second method, referred to as full binary combination schema 2 (FBCS 2), is to set DC voltage ratio v_i as

$$v_i = \left(1 - \frac{2^{nc-i} - 1}{2^{nc} - 1}\right)E \quad (1 \le i \le nc) \tag{3}$$

FBCS 1 and FBCS 2 are two efficient ways to cover the maximum binary combinations of the switches. However, there are still some other possibilities on choosing v_i to cover all the binary combinations. The term AFBCS (Additional Full Binary Combination Schema) is used to represent the other methods for setting DC voltage ratios to obtain the maximum binary combinations of the switches.

D. A Four-Cell FBCS Design

Consider the design of a four-cell FBCS multi-level inverter. In this case, $nc = 4$, $nl = 2nc = 2^4 = 16$. From FBCS 1, the DC voltages for each phase can be set to:

$$\begin{cases} v_1 = \left(\dfrac{2^1 - 1}{2^4 - 1}\right)E = \dfrac{1}{15}E \\ v_2 = \left(\dfrac{2^2 - 1}{2^4 - 1}\right)E = \dfrac{3}{15}E \\ v_3 = \left(\dfrac{2^3 - 1}{2^4 - 1}\right)E = \dfrac{7}{15}E \\ v_4 = E \end{cases} \tag{4}$$

From FBCS 2, the DC voltages for each phase can be set to:

$$\begin{cases} v_1 = \left(1 - \dfrac{2^{(4-1)} - 1}{2^4 - 1}\right)E = \dfrac{8}{15}E \\ v_2 = \left(1 - \dfrac{2^{(4-2)} - 1}{2^4 - 1}\right)E = \dfrac{12}{15}E \\ v_3 = \left(1 - \dfrac{2^{(4-3)} - 1}{2^4 - 1}\right)E = \dfrac{14}{15}E \\ v_4 = E \end{cases} \tag{5}$$

As an AFBCS example, a 4-cell,16-level inverter can also be generated by setting the DC voltage ratio as :

$$v_1 : v_2 : v_3 : v_4 = 1 : 5 : 13 : 15 \tag{6}$$

Table VI shows the relationship between the switching states and the line-to-ground voltage by applying the basic circuit laws and FBCS. It can be seen that FBCS 1, FBCS 2 and the AFBCS example all result in 16 different line-to-ground values, which also means that by applying FBCS, it is possible to realize a four-cell, 16-level inverter. The

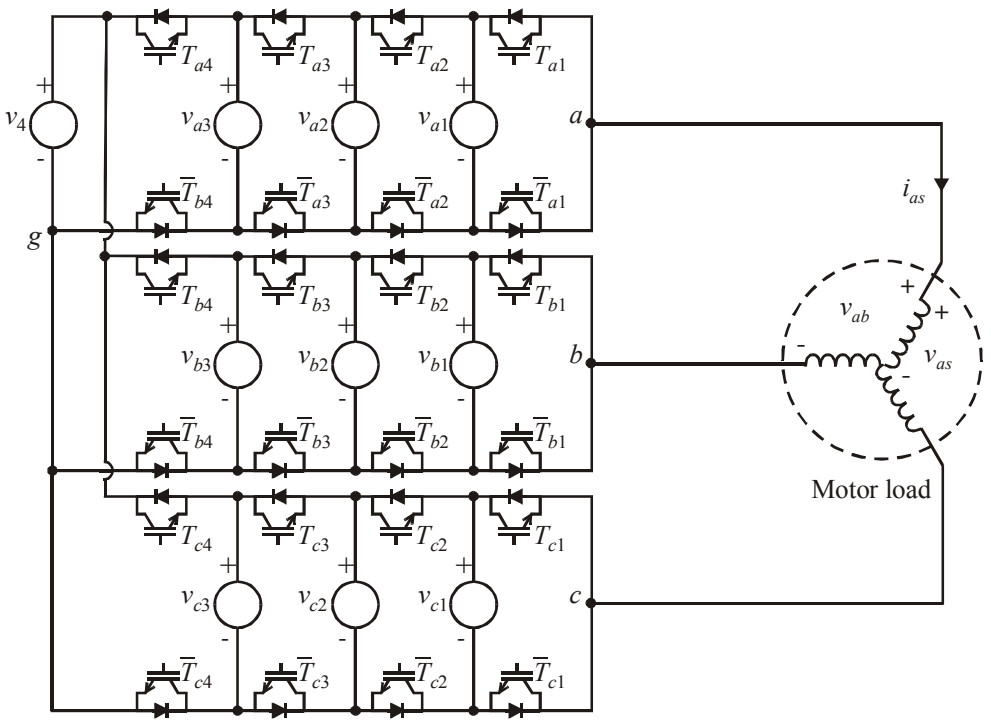

Figure 4. Four-cell inverter topology.

conventional four-cell FS topology design merely yields a 5-level inverter. The FBCS method was also demonstrated for converters with a higher number of voltage levels using a C++ program. Figure 4 shows the 16-level inverter topology.

IV. Comparison Between the Conventional N-Cell FS Topology and FBCS

A. Voltage Levels

Table VII shows a comparison between the conventional FS schema and FBCS. It can be seen that FBCS can generate a higher number of converter levels per number of semiconductors than the conventional FS schema and also covers the maximum 0,1 binary combinations of switches.

Table VII. Inverter levels comparison.

nc	*sc*	*nl* (Conventional FS)	*nl* (FBCS)
1	2	2	2
2	4	3	4
3	8	4	8
4	16	5	16
5	32	6	32
6	64	7	64
…	…	…	…
n	2*n*	*n*+1	2*n*

B. Semiconductor Voltages

In designing multi-level inverters, it may be convenient to choose all the switches of the same rated voltage. For the conventional FS schema, the blocking voltage of each IGBT is distributed evenly; while in FBCS, the blocking voltage of IGBTs are different. For instance, in the design of a two-cell multi-level inverter as shown in Fig. 1, the blocking voltages for T_{x1} and T_{x2} will be different for FBCS as shown in table VIII.

Table VIII. The blocking voltages of two-cell inverters

	Conventional FS ($v_1 : v_2 = 1 : 2$)	FBCS 1 ($v_1 : v_2 = 1 : 3$)
v_{T1x}	$E/2$	$E/3$
v_{T2x}	$E/2$	$2E/3$

From the average cost point of view, there is no difference between the two designs. However, regarding convenience, all switches will be designed to have the same rated voltage, which means that the rated voltage will be chosen as $2E/3$ instead of $E/2$ when applying FBCS 1.

C. Floating Source Currents

For the conventional FS topology, the redundant switching combinations give the choice between positive and negative source current. This can guarantee that the current flowing through the voltage source will be zero on average. Therefore no source-charging problem exists. However, for

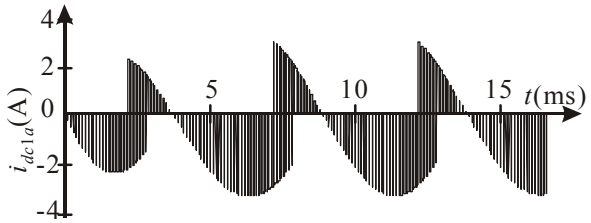

Figure 5. Current curve of battery 1 applying FBSC 1.

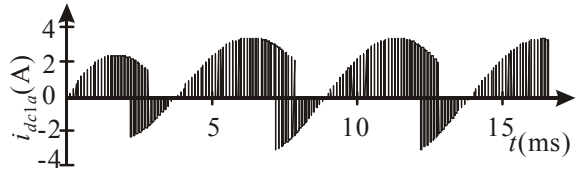

Figure 6. Current curve of battery 1 applying FBSC 2.

FBCS, the average current into the DC sources will be positive or negative. For example, Figures 5 and 6 show the simulated current in voltage source v_1 of a two-cell, 4-level inverter applying FBCS 1 and FBCS 2. In this simulation, a three-phase R-L load is used as the load of the inverter, where $R = 8\,\Omega$ and $L = 12\,\text{mH}$. From Fig. 5 it can be seen that if the voltage ratio is chosen as $v_1 : v_2 = 1 : 3$ by applying FBCS 1, a charging current results. When the voltage ratio is chosen as $v_1 : v_2 = 2 : 3$ by applying FBCS 2, a discharging current results as shown in Fig. 6. Therefore for a 4-level inverter, it is preferable to choose FBCS 2 instead of FBCS 1. It should be mentioned that FBCS requires fixed floating sources instead of capacitors, because it is not possible to keep the capacitors balanced. For this reason, FBCS is more suitable for battery power applications. Alternatively transformer/rectifier circuits may be used to supply the floating sources.

V. Computer Simulating Results

A computer simulation system with a three-phase R-L load has been created to verify the FBCS method. Figure 7, Fig. 8 and Fig. 9 show the computer simulation results of the line-to-ground voltage and the line-to neutral voltage for 4-, 8-, and 16-level inverters respectively.

VI. Laboratory Validation

A two-cell 4-level FS inverter was constructed in the laboratory. A 3.7 kW induction motor [2] was used as a load. The inverter modulation was accomplished using multi-level sine-triangle modulation [3] with a switching frequency of 10kHz and a modulation index of 1.13. The commanded fundamental frequency was 60Hz.

The first study involved using batteries for the floating sources in order to demonstrate the negative and positive source currents for FBCS1 and FBCS2 respectively. In this setup, a battery voltage of v_1 = 24 V was used. Since the voltage for the battery studies was considerably less than the rated motor voltage, the rotor was blocked and it acted as an R-L load. Figure 10 shows the laboratory measurements for

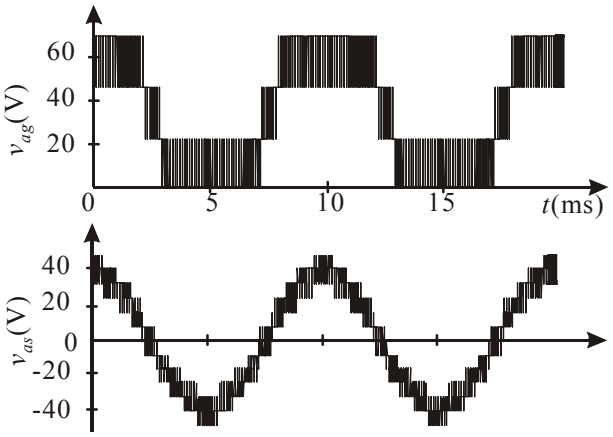

Figure 7. Two-cell 4-level inverter with FBCS

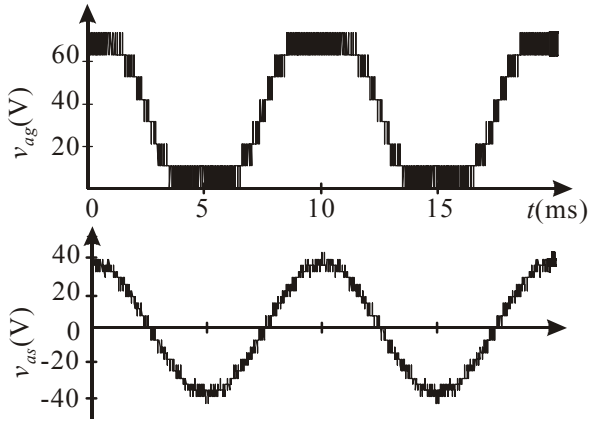

Figure 8. Three-cell 8-level inverter with FBCS

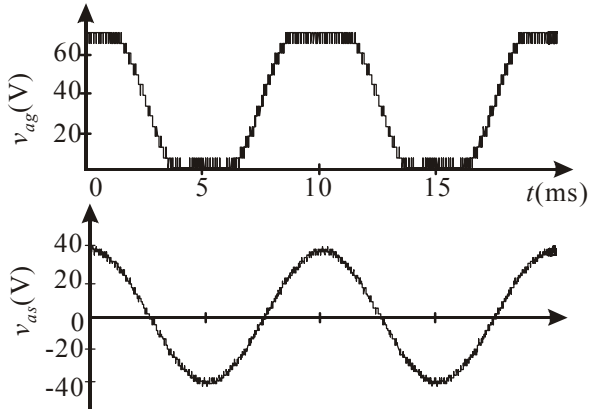

Figure 9. Four-cell 16-level inverter with FBCS

FBCS1 where v_2 = 72 V. Therein, the upper transistor voltages, DC source current, line-to-ground voltage, line-to-line voltage, and line current for the *a*-phase are shown. As can be seen, the transistors with a high blocking voltage have a low switching frequency and visa versa. This is a common feature that results in maximally distended converters [2] and is desirable since it matches the market reality where higher voltage power switches are lower-rated in switching frequency. The DC source current is negative on average as expected from the simulation results. The

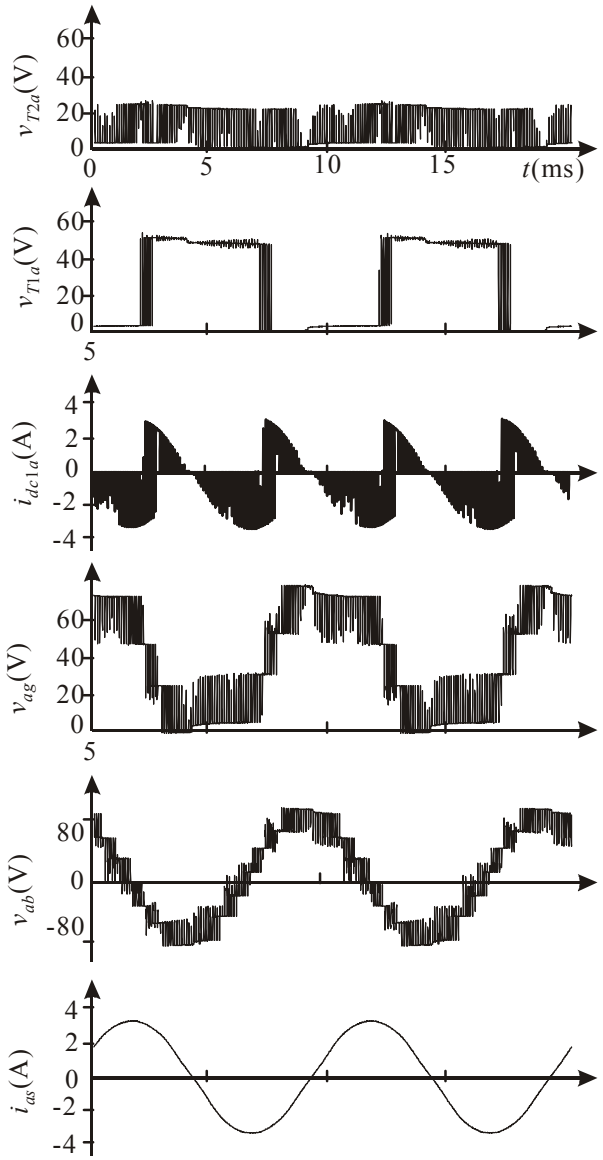

Figure 10. Test results using FBSC 1 (using battery sources).

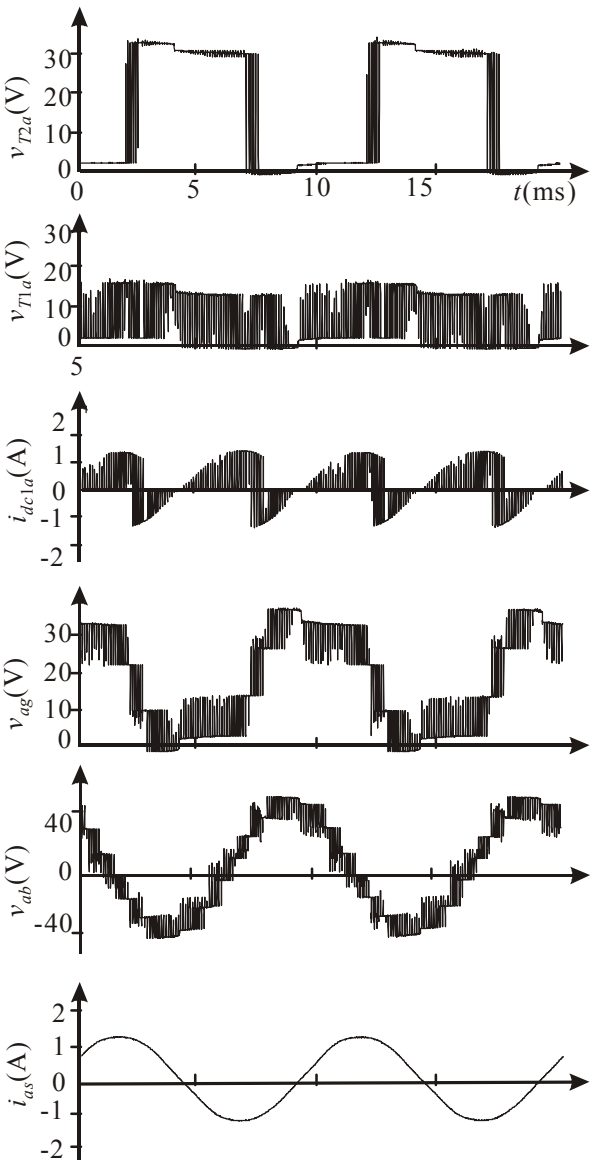

Figure 11. Test results using FBSC 2 (using battery sources).

voltage and currents exhibit typical 4-level inverter performance. Since the DC voltage is low for this study, the effect of semiconductor voltage drops can be seen in the line-to-ground voltage. Figure 11 shows the laboratory results for FBSC 2 where the DC voltage has been set to v_2 = 36 V in accordance with (3). In this case, the DC source current has a positive average value.

In the next study, transformer/rectifier sources were used to supply v_1 = 220 V in each phase. The DC link voltage was set to v_2 = 330 V in accordance with FBCS2 so that the rectifier currents will be positive on average. These voltage levels were chosen since they correspond to rated voltage on the motor. The motor was operated at rated load. Figure 12 shows the laboratory measurements. In this study, it can be seen that the semiconductor voltage drops are negligible. The low-frequency harmonics in the current waveform are due to induction motor saturation.

VII. Conclusion

This paper has presented new full binary combination schema for floating source multi-level inverters. The new schema provides an efficient method for constructing multi-level DC/AC inverters. Comparing this with the conventional FS multi-level inverters, the proposed schema use less power electronic switches while yielding a higher number of voltage levels. The proposed method has been analyzed in terms of voltage levels, device voltage stresses and floating source currents. Computer simulation and laboratory measurements have been presented.

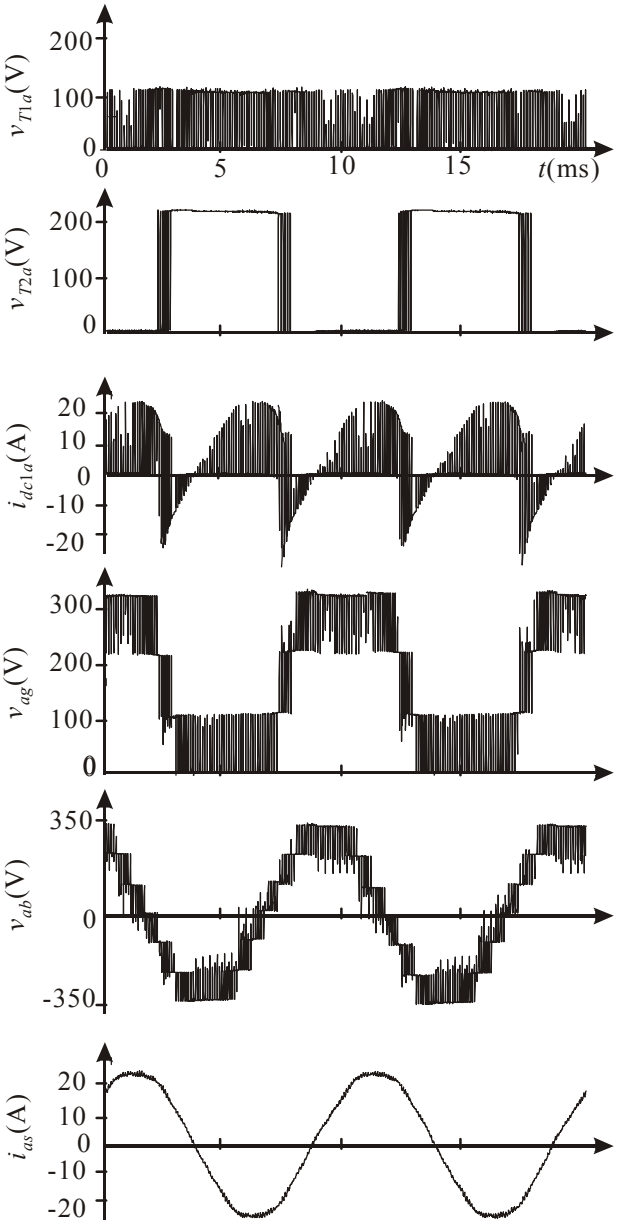

Figure 12. Test results using FBSC 2 (using rectifier sources).

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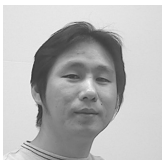

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