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N. J. Park

Bin Jin

Koshy M. George

Nohpill Park

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1072

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High Confidence Testing for Instrumentation System-on-Chip with Unknown-Good-Yield

N.-J. Park¹, B. Jin¹, K.M. George¹, N. Park¹ and Minsu Choi² ¹Dept. of Computer Science, Oklahoma State University, Stillwater, OK, 74078-1053, USA {noh, byungj, kmg, npark}@a.cs.okstate.edu ²Dept. of Electrical and Computer Eng., University of Missouri-Rolla, Rolla, MO, 65409-0040 choim@umr.edu

Abstract - Today, System-on-Chip (SoC) is one of the most commonly used integration and fabrication technology for complex hybrid electronic instrumentation. SoCs (System on Chip) are in general built with embedded Intellectual Property (IP) Cores, each of which procured from different IP providers with no prior information on Known-Good-Yield (KGY). In practice, partial testing is a practical choice for assuring the yield of the product under the stringent time-to-market requirement in today's high density/complexity electronic devices such as SoCs built by using deep submicron technology. Therefore, a proper sampling technique is a key to high con dence testing and cost effectiveness. An Experimental Characterization-based Testing (referred to as ET) method for SoC has been proposed prior to this work [13], in which a strati ed sampling method was employed based on environmental-based characterization and experimental design technique to enhance the con dence level of the estimated yield. Based on the work done in the previous research, this paper is to propose a novel statistical testing technique for increasingly hybrid integrated systems fabricated on a single silicon die with no a-priori empirical yield data. This problem is referred to as Unknown-Good-Yield (UKGY) problem. The proposed testing method, referred to as Regressive Testing (RegT), in this paper exploits another way around by using parameters (referred to as Assistant Variables (AV)) that are employed to evaluate the yields of randomly sampled SoCs and thereby estimating the good yield by using regression analysis method with regard to con dence interval. Numerous numerical simulations are conducted to demonstrate the ef ciency and effectiveness of the proposed RegT in comparison with the ET method.

Keywords – Systems-on-Chip (SoC), fault coverage, defect level, Good Yield Rate (GYR), Unknown-Good-Yield (UKGY), correlation analysis, assistant variable, random testing, experimental testing, regressive testing.

I. INTRODUCTION

The increasing demand on operation speed, integration density, and customizability for tomorrow's high-performance instrumentation has motivated high performance system development. System-on-Chip (SoC) technology provides potential advantages of high integration density, small interconnection delay and high system performance [1], [2], [3], [4], [5], [6], [7], [8], [9]. Thus, SoC is one of the key technology choices for high-performance instrumentation development [10].

The rapid advances in technology for manufacturing complex integrated circuits have been made possible by the high density integration of a large number of components and devices; today, a complete system can be integrated and assembled on a single chip (SoC). Due to density and complexity, conventional fabrication methods are facing tremendous challenges when manufacturing SoCs. The miniaturized size and light weight as well as performance benefits (such as power consumption, high speed and thermal distribution) have made SoC a rapidly expanding market with great potential.

However, SoC manufacturing is encountering major hurdles as related to achieving an acceptable yield at high confidence level with an efficient testing technique. For SoC, conventional testing methods are impractical and costly; methods based on Very Large Scale Integration (VLSI) technology for implementing ASIC (Application-Specific IC) and MCM (Multichip Module) are not effective because they may not capture the new processes involved in SoC manufacturing.

An SoC is assembled by using Intellectual Property (IP) cores as components. As IP cores are deeply embedded in a single chip, it is not readily possible to rely on conventional testing and yield evaluation methods. There is no a-priori information or data available on the yield of the components, referred to as *Unknown-Good-Yield*. Moreover, wafer or chip level information has limited relevance due to the disparate integration processes of the IP cores and the lack of known physical-level yield. This is substantially different from custom optimized ASIC with a well-exercised yield, or MCM with known-goodyield. Since there is no significant information available during the integration and test of the embedded IP cores, past work on correlation between fabrication and related features (such as yield and fault rate), is not applicable.

In our previous work [13], a method for accurate GYR has been established by using a novel method in which highly correlated EPs (Environmental-based Parameters) are categorized at different levels through a characterization of different environmental parameters and a statistical analysis of their interactions.

The objective of this paper is to propose another theoretical testing method, referred to as *regressive testing* (RegT) around for estimating GYR of SoC with *Unknown Good Yield* (UKGY) with reference to a novel criteria, referred to as *Assis*- *tant Variable (AV).* AVs are employed to evaluate the yields of randomly sampled SoCs and thereby estimating the good yield by using regression analysis method with regard to confidence interval. This paper focuses on identifying *Assistant Variables* and correlation analysis technique between GYR and assistant variables to estimate Good Yield Rate (GYR) of SoC. Assistant variables are supposed to be simple and inexpensive (i.e. the cost to estimate EP in our previous paper is expensive) for observation and highly correlated with GYR to make the testing and yield estimating process free from UKGY. For instance, assistant variables may be weight, thermal conductivity, power consumption, or thermal resistance of SoCs, to mention a few. This differentiates the proposed RegT from the previous ET method. However, note that any method may be chosen depending on the availability of such information as EP or AV.

This paper is organized as follows. In section II, literature review and preliminary works are briefly presented. The basic principles and details of the proposed method are described in section III. The confidence of the proposed method is evaluated in section IV. In the final section, discussion and conclusion are presented.

II. REVIEW AND PRELIMINARIES

Today's electronic devices packaging technology allows design of complex systems on a single chip at deep-submicron. This makes it practically impossible to test those devices exhaustively due to an excessive time overhead and severe limitation in available electrical access. This severely restricts the use of conventional testing approaches.

Using an SoC, it is possible to integrate the many digital and analog functions needed for consumer electronic products (such as home appliances and advanced mobile devices) on a single Very Large Scale Integrated (VLSI) chip. A SoC can accommodate complex functions usually associated with today's systems. However, it is difficult to test and assure the quality of a SoC using conventional VLSI test methodologies due to the high density and complexity at deep sub-micron scale.

In the past few years a *stratified test* method has been proposed for testing Multi-Chip Module (MCM) systems. Its advantages are the improvement in quality level and cost-effectiveness. This approach referred to as the Lowest Yield-Stratum First-Testing (LYSFT) considers the unevenness of Known-Good-Yield (KGY) of stratification as a criterion for testing the chips on a MCM for quality enhancement [27] - [28].

Traditionally, the number of tests and test generation complexity are reduced by random testing (RT) [20], [21], [22], [23], [24]. Extensive research has been performed on random testing of VLSI [20], [21], [22], [23], [24].

There have been extensive studies reported on statistical approaches for testing ICs. Sequential statistical analysis has been employed as a standard vehicle to manipulate the correlation among Defect Level (DL), yield, random test length, and detection probability. Instead of using deterministic DL analysis, a sequential statistical analysis directly examines the random behavior of test vectors and results in an elegant derivation of the DL. The DL derived by using this method can be then used to find the average confidence in the probability of faultfree chips, which in turn is represented by the yield and the coverage [29] - [34]. The DL obtained through random testing can be evaluated by a probability distribution rather than a value as pointed out in [29]. The probability density function of a DL can be approximated by using the standard normal distribution; the confidence degree on the defect level can thus be derived. It has been shown that the high confidence degree of a specific DL can be achieved using large sample chips [35].

Environmental based characterization of SoC for stratified testing [13] has been recently proposed to feature the scattered problem on SoC with the following component:

- To identify EP levels highly co-related with Good Yield Rate (GYR) by using experimental design and test technique;
- To conduct stratified sampling-based testing with respect to the focused EP levels as its stratification criteria without additional chips to test;
- 3. To estimate GYR with ratio estimation.

The proposed Regressive Testing (RegT) will theoretically demonstrate that the method with Assistant Variables which satisfy the following specific three conditions result in higher confidence level yield estimation at lower cost than ET, the method proposed in [13].

- 1. Simple and inexpensive for observation.
- 2. Highly correlated with GYR.
- 3. Free from UKGY problem.

III. PROPOSED METHOD

The proposed method is to statistically estimate and predict the good yield of SoC by using variables that are highly correlated with the good yield. The proposed Regressive Testing (RT) employs the linear regression estimation method [38], [39], [40]. The procedure of the proposed method to estimate the GYR is shown in Figure 1. Upon fabrication of a batch of N identical SoCs, n SoCs are sampled and tested only. At the same time, assistant variables are derived and regressive correlation analysis to predict the overall GYR is conducted. Then, the estimated GYR is used to calculate the overall quality level. The proposed method selects and tests n-out-of-N devices under test while assuring an acceptable level of testing confidence. Details on the proposed RegT will be discuss in the following subsections.



Fig. 1. Regressive Testing Procedure

A. Correlation Analysis

The fundamentals of the correlation analysis method used in the proposed RegT is described in this subsection.

Suppose ρ is the correlation coefficient between two random variables x and y, then ρ represents the linear relation between x and y [37], and defined as follows.

$$\rho = \frac{cov(x,y)}{\sigma_x \sigma_y} \tag{1}$$

where

•
$$cov(x,y) = E(x-\overline{X})(y-\overline{Y}) = \frac{1}{N} \sum_{i=1}^{N} (x_i - \overline{X})(y_i - \overline{Y})$$

- σ_x is standard deviation of x
- σ_y is standard deviation of y

The above equation shows that the correlation coefficient (ρ) of variables x and y is the covariance of x and y divided by the multiplication of standard deviation of x and y. The range of ρ is $-1_i\rho_i1$, and as ρ approaches near 1, there is a higher correlation between x and y [38] [39] [40]. By using this method, the most correlated variables with the good yield of SoC can be identified as follows.

B. Regression Estimator

In the proposed Regressive Testing (RegT), the followings are assumed.

1. y_i is the core variable which is difficult and expensive to observe in the sample and population.

- 2. x_i is the assistant variable which can be relatively efficiently and inexpensively observed in the sample and population.
- 3. x_i should be the one(s) most correlated with y_i .

For example, let y_i be the good yield from the sampled SoC, then x_i can be the weight of SoC or other physical characteristics of SoC simple and inexpensive for observation.

The pair (x_i, y_i) observed from the selected samples and the population mean (\overline{X}) of x can be observed easily. Then, the population mean (\overline{Y}) of y, that is good yield rate, can be estimated by the equation as follows.

$$\overline{y}_{re} = \overline{y} + b(\overline{X} - \overline{x}) \tag{2}$$

where

- \overline{y}_{re} is regressive estimator of good yield
- b is the estimator of regressive coefficient such as;

$$b = \frac{\sum_{i=1}^{n} (y_i - \overline{y})(x_i - \overline{x})}{\sum_{i=1}^{n} (x_i - \overline{x})^2}$$
(3)

C. Variance of Regressive Estimator

The proposed regressive estimator (\overline{y}_{re}) is a biased estimator because there is another parameter ,b - an estimator of regressive coefficient, to be estimated in it.

Let $\Delta \overline{y} = \frac{\overline{y} - \overline{Y}}{\overline{Y}}, \Delta \overline{x} = \frac{\overline{x} - \overline{X}}{\overline{X}}, \Delta b = \frac{b - B}{B}$, and insert them into Formula2. Then, the result is as follows:

$$\overline{y}_{re} = \overline{Y} + \overline{Y}\Delta\overline{y} + (B + B\Delta b)(-\overline{X}\Delta\overline{x})$$
$$= \overline{Y} + (\overline{Y}\Delta\overline{y} - B\overline{x}\Delta\overline{x}) - B\overline{X}\Delta b\Delta\overline{x}$$
(4)

As $E\Delta \overline{y} = E\Delta \overline{x} = 0$, the bias of the regressive estimation is as follows.

$$B(\overline{y}_{re}) = E(\overline{y}_{re}) - \overline{Y} = -B\overline{X}E(\Delta b\Delta \overline{x}) = -cov(\overline{x}, b)$$
(5)

Using this property, the bias of the regressive estimator can be removed and the result is as follows.

$$\overline{y}_{re}^* = \overline{y} + b(\overline{X} - \overline{x}) - cov(\overline{x}, b) \tag{6}$$

where

• \overline{y}_{re}^* is unbiased regressive estimator

In the proposed method, if the sample size is large enough, $B\overline{X}\Delta b\Delta \overline{x}$ in Equation 4 asymptotically converges to 0, and then \overline{y}_{re} becomes an unbiased estimator. Its variance is defined as follows.

$$V(\overline{y}_{re}) = V(\overline{y}) - 2Bcov(\overline{x}, \overline{y}) + B^2 V(\overline{x})$$
⁽⁷⁾

Then, substituting $B = \frac{cov(\overline{x},\overline{y})}{V(\overline{x})}$, the variance is determined as follows.

$$V(\overline{y}_{re}) = \frac{N-n}{Nn} S_y^2 (1-\rho^2) \tag{8}$$

where

- \overline{y}_{re} is the GYR of SoCs in certain population group
- N is the size of population
- n is the sample size
- S_u^2 is sample variance of good yield of SoC
- ρ is the correlation coefficient

IV. NUMERICAL SIMULATION

In this section, the efficiency of the proposed RegT is demonstrated in comparison with Random Testing as a criteria comparative study with respect to confidence interval of their estimated yield values and GYR.

The parameter estimator(i.e. GYR) on certain group of SoCs for RegT (i.e., denoted by \overline{y}_{reg} in the following equations) and RT (i.e., denoted by \overline{y}_{ran} in the following equations) are as follows, respectively.

$$\overline{y}_{reg} = \overline{y} + b(\overline{X} - \overline{x}) \tag{9}$$

$$\overline{y}_{ran} = \frac{\sum_{i=1}^{n} y_i}{n} \tag{10}$$

The variance of each estimator is as follows.

$$V(\overline{y}_{reg}) = \frac{N-n}{Nn} S_y^2 (1-\rho^2) \tag{11}$$

$$V(\overline{y}_{ran}) = \frac{N-n}{Nn}S_y^2 \tag{12}$$

As shown in Equations 11 and 12, the variance of regressive estimator is always less than that of random estimator by the size of ρ^2 , which is the square of correlation coefficient between good yield and assistant variable of SoC. Therefore, the proposed Regressive Testing is more efficient and effective than Random Testing for estimating the GYR of SoC. For simulation purpose, it is assumed that the total number of SoCs to be tested (i.e., sample size) is from 100 to 1000, and the real value of GYR is assumed to be 86.7.

The estimation of GYR by the proposed RegT and random testing are calculated by using the sampled SoC variance for various sample sizes as shown in Table I.

The GYR estimators and confidence intervals of ReqT for different sample sizes (e.g. $n = 100, 200, \dots, 1000$) are shown in the second, third, fourth and fifth through nineth columns in Table I, respectively. Comparison is made with respect to the confidence interval of the two testing methods (i.e., regressive testing and random testing) for true value of GYR 86.73. The results shown in Figure 2 is for RT, in which upper and lower confidence intervals are too wide; therefore, RT should be avoided in practice. There are extensive simulation results in Figures 3 for RegT with ρ =.7, 4 for RegT with ρ =.8, 5 for RegT with $\rho=9$, 6 for RegT with $\rho=1$, in which note that $\rho=1$ is the case of perfect correlation (i.e. 100%) between GYR and assistant variable. It is observed that there is a significant decrease in confidence intervals as ρ increases. This indicates that if the assistant variable in the proposed method is identified and properly used as proposed, then it improves both the accuracy of GYR and its confidence level significantly.

V. DISCUSSION AND CONCLUSIONS

This paper has presented a testing method for electronic devices with Unknown-Good-Yield (UKGY) problem. The UGKY problem of Systems-on-Chip (SoC) is discussed in this paper as SoCs are in general built with embedded Intellectual Property (IP) Cores, each of which procured from IP providers with no information on Known-Good-Yield (KGY). In general, partial testing is a practical choice for assuring the yield of the product under the stringent time-to-market requirement in today's high density/complexity electronic devices such as SoC built by deep submicron or nano technology. Therefore, proper sampling technique is a key to the success of high confidence testing. The proposed testing method, referred to as Regressive Testing (RegT), in this paper exploits another way around by using parameters (referred to as Assistant Variables (AV)) that are employed to evaluate the yields of randomly sampled SoCs and thereby estimating the good yield by using regression analysis method with regard to confidence interval. A numerical simulation results have demonstrated the efficiency and effectiveness of the proposed RegT in comparison with generic random testing method as criteria. It is observed that there is a significant drop in confidence interval as ρ increases. This indicates that if the assistant variable in the proposed method is identified and properly used as proposed, then it improves both the accuracy of GYR and its confidence level significantly.

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Fig. 2. Confi dence interval of random testing

Sample size	Random Testing		Regressive Testing				
			GVB estimator (v)	Confidence interval (Sy reg)			
	GYR estimator(y _{ran})	Confidence inteval(Sy ran)	(y reg)	$\rho = .7$	$\rho = .8$	ρ = .9	$\rho = 1$
100	83.8	8.24	86.5	4.20	2.97	1.57	0.00
200	85.2	8.80	87.4	4.49	3.17	1.67	0.00
300	85.2	9.25	86.1	4.72	3.33	1.76	0.00
400	85.3	8.87	86.8	4.52	3.19	1.69	0.00
500	85.6	8.58	86.8	4.38	3.09	1.63	0.00
600	86.4	8.40	86.5	4.28	3.02	1.60	0.00
700	86.5	8.47	86.6	4.32	3.05	1.61	0.00
800	87.1	8.28	86.8	4.22	2.98	1.57	0.00
900	86.9	8.24	86.7	4.20	2.97	1.57	0.00
1000	86.7	-	86.7	-	-	-	-

 TABLE I

 ACCURACY COMPARISON FOR RANDOM TESTING VERSUS REGRESSIVE TESTING



Fig. 3. Confidence interval of regressive testing with $\rho = .7$



Fig. 4. Confidence interval of regressive testing with $\rho = 0.8$



Fig. 5. Confidence interval of regressive testing with $\rho = .9$



Fig. 6. Confidence interval of regressive testing with $\rho = 1$