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PERFORMANCE CHARACTERISTICS OF A
CASCADED TWO-LEVEL CONVERTER

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Abstract - **A cascaded two-level converter is proposed which utilizes two six-transistor inverters and is capable of producing voltages which are identical to those of three-level and four-level converters. Since the machine voltages are the same, the converter performance is the same as is verified through laboratory tests. The advantages and disadvantages of the proposed cascaded converter are explored. The proposed converter is simpler to construct and offers more non-redundant switching states per number of active semiconductors than standard multi-level converters.**

I. INTRODUCTION

The general trend in power electronics devices has been to switch power semiconductors at increasingly high frequencies in order to minimize harmonics and reduce passive component sizes. The increase in switching frequency, however, increases the switching losses which become especially significant at high power levels.

One proposed method for decreasing the switching losses is to construct resonant converters by adding an LC resonant circuit to the hard switched inverter topology. Examples of this type of converter include the resonant DC link [1], and the auxiliary commutated resonant pole converter [2]. In the case of the resonant DC link, the resonant circuit causes the inverter voltage to oscillate between zero and twice the DC source voltage. The inverter transistors can be switched when the voltage is zero, thus reducing switching losses. One disadvantage of resonant converters is that the inverter voltage or current peak values are considerably higher than those of corresponding hard switched devices, which increases the required device ratings. An additional disadvantage is that the added resonant circuitry will increase the complexity and cost of the inverter control.

Another method for decreasing the switching losses is to construct an inverter with a high number of switching states such as a multi-level converter [3]. With more switching states, the inverter output voltage can be "stepped" in smaller increments. This allows mitigation of harmonics at a low switching frequencies thereby reducing switching losses. In

addition, EMC concerns are reduced through the lower common mode current facilitated by lower dv/dt's produced by the smaller voltage steps. This paper proposes a new converter topology which features a higher number of available states for a given number of active semiconductors than is obtained using multi-level converters. The new topology is also of a form which makes the best possible use of different types of active semiconductors. Herein, the performance of the new converter is explained in the context of a three-phase induction motor drive. A three way experimental comparison between the proposed converter, a three-level converter, and a four-level converter is made.

II. MULTI-LEVEL CONVERTERS

Figure 1 illustrates the multi-level converter. Therein, the capacitors splits the dc rail voltage allowing three different voltage levels to be selected for the phase-to-ground voltages v_{ag}, v_{bg}, and v_{cg} depending on the inverter gating signals. For example, the phase voltage v_{ag} will be 0 if the two lower transistors in the a-phase are gated on, $\frac{1}{2}v_{dc}$ if the two center transistors are gated on, and v_{dc} if the two upper transistors are gated on. In general, for an n-level inverter, the phase-to-ground voltages can be expressed as

$$v_{xg} = \frac{l_x}{(n-1)}v_{dc} \qquad l_x = 0, 1, ...(n-1) \qquad (1)$$

where x represents the phase which can be a, b, or c, and l_x represents the phase level selected by the gating signals as described above. For the purpose of discussing the multi-level converter, it is convenient to define the switching state as a function of the phase voltage levels. In particular,
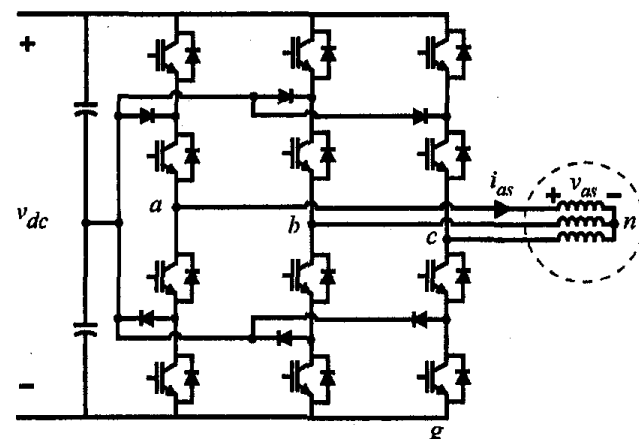

Figure 1. Three-level converter topology.

$$sw = (n)^2 l_a + (n)^1 l_b + (n)^0 l_c \qquad (2)$$

The number of possible switching states for a multi-level converter is given by

$$n_{sw} = (n)^p \qquad (3)$$

where p is the number of phase legs. For the three-phase three-level converter, the number of possible switching states is 27.

The voltages applied to the machine stator windings can be calculated in the same manner as with a standard six-transistor inverter since the machine connections to the inverter are the same, and the machine is wye connected. The stator voltages are thus given by [4]

$$v_{as} = \frac{2}{3}v_{ag} - \frac{1}{3}v_{bg} - \frac{1}{3}v_{cg} \qquad (4)$$

$$v_{bs} = \frac{2}{3}v_{bg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{cg} \qquad (5)$$

$$v_{cs} = \frac{2}{3}v_{cg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{bg} \qquad (6)$$

The stator voltage vectors achievable from the switching states can be plotted by transforming the a-, b- and c-phase stator voltages to the q- and d-axis stationary reference frame. The transformation to the arbitrary reference frame is given by [1]

$$v_{qs}^s = \frac{2}{3}\left(v_{as}\cos(\theta) + v_{bs}\cos\left(\theta - \frac{2\pi}{3}\right) + v_{cs}\cos\left(\theta + \frac{2\pi}{3}\right)\right) \qquad (7)$$

$$v_{ds}^s = \frac{2}{3}\left(v_{as}\sin(\theta) + v_{bs}\sin\left(\theta - \frac{2\pi}{3}\right) + v_{cs}\sin\left(\theta + \frac{2\pi}{3}\right)\right) \qquad (8)$$

In the stationary reference frame, θ is zero.

Figure 2 depicts the plot of the stator voltage vectors for the three-level converter. Each vector is numbered v_{sw} where sw is the switching state which will produce the voltage vector. The phase-to-ground voltages can be determined for a particular voltage vector in Fig. 2 by converting the switching state number sw into base three mathematics (or base n in general for the n-level converter). For example, switching state 24 is 220 in base three. Switching the a-phase to level 2, the b-phase to level 2, and the c-phase to level 0 will produce the switching state 24. As can be seen, there are only 19 unique voltage vectors produced from the 27 switching states due to switching state redundancy.

In order to increase the number of switching states, the DC voltage can be divided equally by three capacitors as shown in Fig. 3 to form the four-level converter. This converter has four phase to ground voltage levels $(0, \frac{1}{3}v_{dc}, \frac{2}{3}v_{dc},$ and $v_{dc})$ selectable by gating on three transistors per phase [5]. Since there are now four voltage-levels, the number of possible switching states is 64 from (3). The stator voltage vector diagram is shown in Fig. 4. As can be seen, there are only 37 unique voltage vectors due to switching state redundancy.

III. PROPOSED CASCADED CONVERTER

The proposed cascaded converter is shown in Fig. 5. This topology is constructed by splitting the neutral connection of

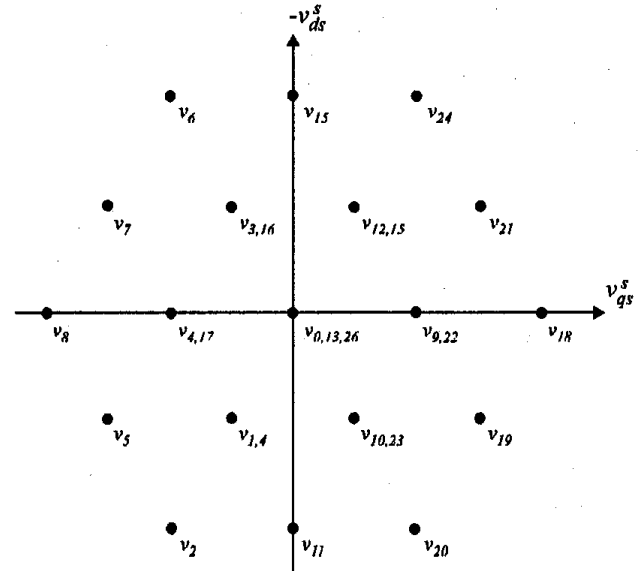
Figure 2. Voltage vector plot for the three-level converter.

the machine and connecting both ends of each phase coil to a two-level inverter. The inverters are supplied by two separate DC sources. Referring to Fig. 5, the machine voltages equations can be written using Kirchoff's voltage law as

$$v_{as} = v_{a1g1} + v_{g1g2} - v_{a2g2} \qquad (9)$$
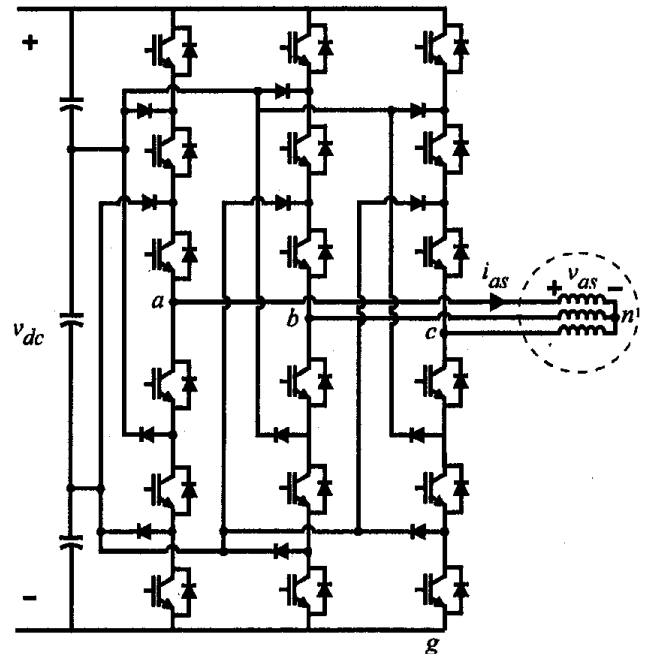

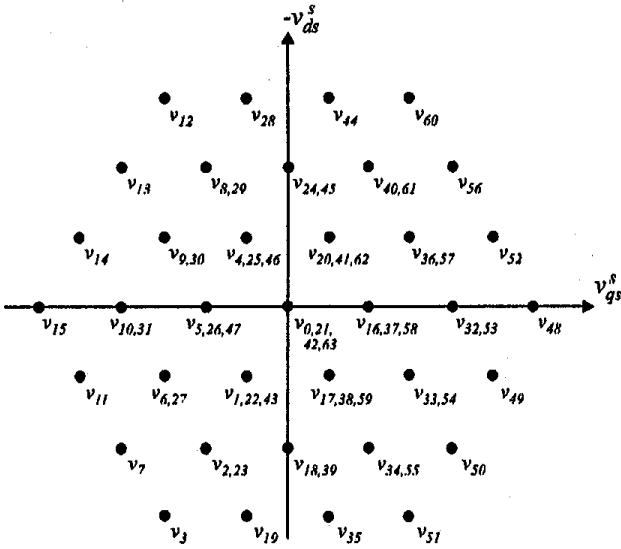Figure 3. Four-level converter topology.

Figure 4. Voltage vector plot for the four-level converter.

$$v_{bs} = v_{b1g1} + v_{g1g2} - v_{b2g2} \qquad (10)$$

$$v_{cs} = v_{c1g1} + v_{g1g2} - v_{c2g2} \qquad (11)$$

Since both inverters are supplied from separate DC voltage sources, they can be thought of as independent nodes in a network and thus Kirckoff's current law yields

$$i_{as} + i_{bs} + i_{cs} = 0 \qquad (12)$$

It can be shown from the machine equations that the phase voltages sum to zero if the currents sum to zero. Given this fact, (8-10) can be added and the result can be solved for v_{g1g2} to yield
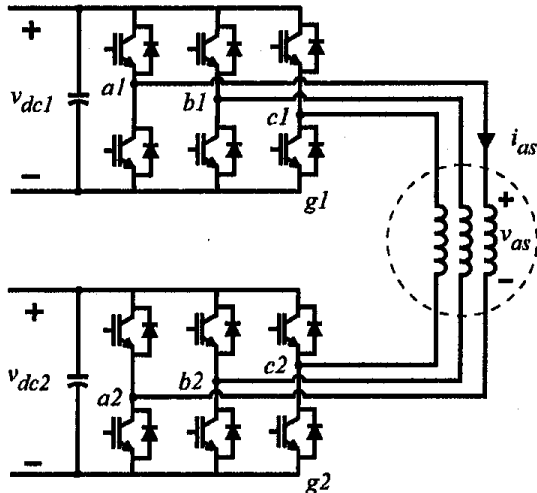

Figure 5. The proposed cascaded converter.

$$v_{g1g2} = \frac{1}{3}(v_{a2g2} + v_{b2g2} + v_{c2g2} - v_{a1g1} - v_{b1g1} - v_{c1g1}) \qquad (13)$$

Substituting (13) into (9-11), the machine voltages may be related to the phase to ground voltages as

$$v_{as} = \frac{2}{3}(v_{a1g1} - v_{a2g2}) - \frac{1}{3}(v_{b1g1} - v_{b2g2}) - \frac{1}{3}(v_{c1g1} - v_{c2g2}) \qquad (14)$$

$$v_{bs} = \frac{2}{3}(v_{b1g1} - v_{b2g2}) - \frac{1}{3}(v_{a1g1} - v_{a2g2}) - \frac{1}{3}(v_{c1g1} - v_{c2g2}) \qquad (15)$$

$$v_{cs} = \frac{2}{3}(v_{c1g1} - v_{c2g2}) - \frac{1}{3}(v_{a1g1} - v_{a2g2}) - \frac{1}{3}(v_{b1g1} - v_{b2g2}) \qquad (16)$$

The voltage vector diagram can be produced by substituting (14-16) into (7-8) for all possible switching states. The number of possible switching states can be computed from (3). For the proposed converter, there are two voltage levels per inverter phase leg (0 and v_{dc1} or v_{dc2}) and six phase legs. Thus, there are 64 possible switching states.

Figure 6 shows the voltage vector patterns for the cascaded converter for several different dc source voltage ratios. The sum of the dc voltages is kept constant as the ratio of one dc voltage to the other is varied. For the case where $v_{dc2} = 0$, the voltage vector plot is the same as that of a two-level converter (or standard six-transistor converter). This is to be expected since the lower converter is essentially a short circuit. As v_{dc2} is increased slightly to $v_{dc2} = \frac{1}{5}v_{dc1}$, the voltage vectors assume a pattern which appears to be that of a two-level converter with a small two-level converter pattern around each voltage vector. This is also to be expected since the converter is constructed from two two-level converters. With $v_{dc2} = \frac{1}{2}v_{dc1}$, some voltage vectors overlap and the pattern is the same as that of a four-level converter. With $v_{dc2} = v_{dc1}$, there is a substantial amount of redundancy and the voltage vector pattern is the same as that of a three-level converter. Thus, the proposed converter can be made to operate as a two-level, three-level, or four-level converter.

Figure 7 shows the voltage vector diagram of the cascaded converter for the case where $v_{dc1} = v_{dc2}$. Since the pattern is identical to that of the three-level converter, the cascaded converter with $v_{dc1} = v_{dc2}$ will be referred to as the cascaded converter in three-level mode. Due to the cascade connection, the switching state notation is somewhat different for the cascaded converter than for standard multi-level converters. The switching state notation for the cascaded converter is given by

$$sw = (n)^{16} I_{a1} + (n)^8 \overline{I}_{a2} + (n)^4 I_{b1} + \cdots$$

$$(n)^2 \overline{I}_{b2} + (n)^1 I_{c1} + (n)^0 \overline{I}_{c2} \qquad (17)$$

where I_{x1} and I_{x2} are used to indicate the levels for phase x in converters 1 and 2 respectively. The overscore in (17) is used to represent the inverse of the level. In the case of the cascaded converter, the levels range from 0 to 1; level 0 being produced by switching the lower transistor on and level 1 produced by switching the upper transistor on. The switching state to produce a particular voltage vector can be found by converting the numbers in Fig. 7 to base two (or
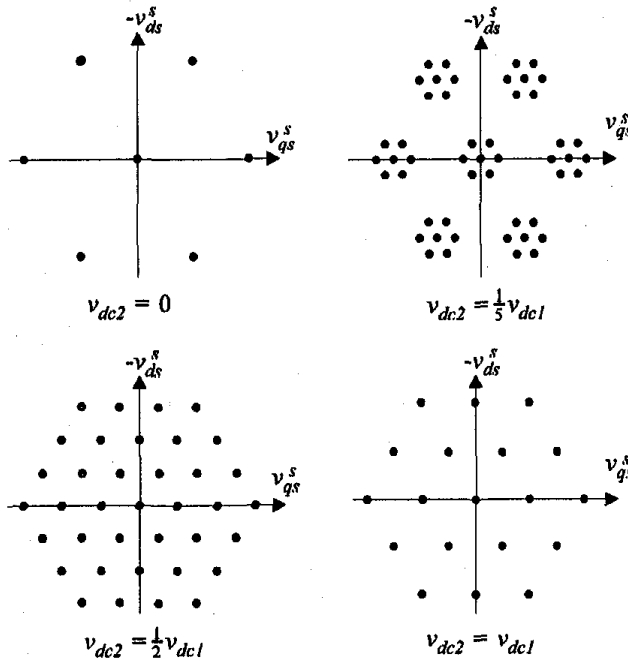
Figure 6. Voltage vector plot for the cascaded converter.

binary) and inverting the odd bits. For example, converting vector 60 to binary yields 111100. Inverting the odd bits produces 101001. Thus setting the inverter voltage levels to $I_{a1} = 1$, $I_{a2} = 0$, $I_{b1} = 1$, $I_{b2} = 0$, $I_{c1} = 0$, and $I_{c2} = 1$ will produce the voltage vector v_{60}.

It is important to relate v_{dc1} and v_{dc2} of the cascaded converter to v_{dc} of the three-level converter so that the
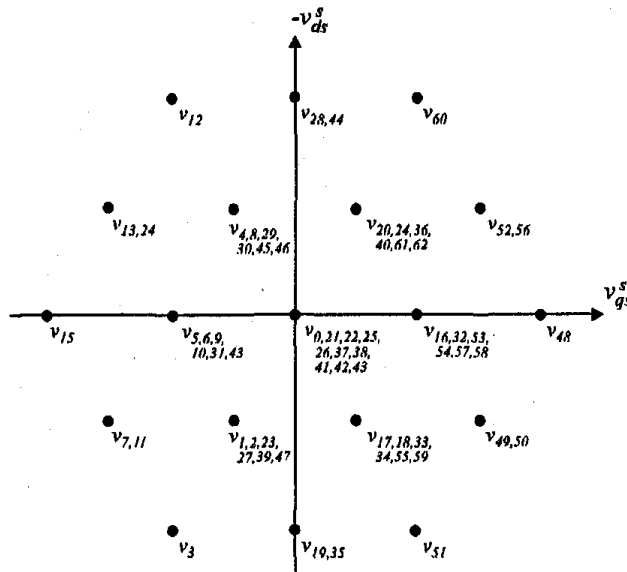

Figure 7. Voltage vector plot for the cascaded converter with $v_{dc1} = v_{dc2}$.

discrete voltage vectors will have the same magnitude for both types of inverters. This will ensure that the performance of the cascaded converter in three-level mode will be exactly the same as that of the three-level converter. Consider the voltage vector v_{18} of the three-level converter and the corresponding vector v_{48} for the cascaded converter. The q- and d-axis voltages for the vector v_{18} are

$$v_{qs}^s = \frac{2}{3} v_{dc} \qquad (18)$$

$$v_{ds}^s = 0 \qquad (19)$$

For the cascaded converter the state v_{48} produces the q- and d-axis voltages

$$v_{qs}^s = \frac{2}{3}(v_{dc1} + v_{dc2}) \qquad (20)$$

$$v_{ds}^s = 0 \qquad (21)$$

From (18-21) it can be seen that for the voltage vectors v_{18} of the three level converter and voltage vector v_{48} of the cascaded converter to have an equivalent magnitude for both converters, it is necessary to set $v_{dc1} = v_{dc2} = \frac{1}{2} v_{dc}$. Although the vectors v_{18} and v_{48} were used for this calculation, any two vectors in the same position of the voltage vector plot patterns will give the same results.

By adjusting the DC voltages so that $v_{dc1} = 2 v_{dc2}$, it is possible to increase the number of unique voltage vectors to 37 and achieve a switching pattern exactly the same as that of a four-level converter. This converter configuration will be referred to as the cascaded converter in four-level mode. Due to the choice of numbering for the stator voltage vectors, the voltage vector plot of this type of converter is identical to that of a four level converter shown in Fig. 4. As with the case where $v_{dc1} = v_{dc2}$, it is necessary to set the stator voltage vectors to the same magnitude so that the performance of the cascaded converter in four-level mode will be the same as that of the four-level converter. The vector v_{48} in the four-level converter gives q- and d-axis voltages expressed by (18-19). For the cascaded converter with $v_{dc1} = 2 v_{dc2}$ the vector v_{48} results in q- and d-axis voltages of

$$v_{qs}^s = v_{dc1} \qquad (22)$$

$$v_{ds}^s = 0 \qquad (23)$$

Comparing (22-23) to (18-19), it can be seen that equivalent performance between the four-level and cascaded converters will be achieved if $v_{dc1} = \frac{2}{3} v_{dc}$ and $v_{dc2} = \frac{1}{3} v_{dc}$.

IV. COMPARISON OF CONVERTER FEATURES

It has been shown from the voltage vector plots that the cascaded converter can be made to emulate a three-level or a four-level converter; having 19 or 37 voltage vectors depending on the dc voltage ratios. It is now appropriate to compare the cascaded converter in three- and four-level modes to the three-level and four-level converters.

All converters considered herein with the exception of the four-level converter have 12 active semiconductors. The

four-level converter has 18. The total device costs is not directly related to the number of devices, however. Instead, for a given power level, the device cost is proportional to the switching stress factor [6] defined as

$$F = \sum_{i=1}^{N} V_{pi} I_{pi} \qquad (24)$$

where N is the number of converter devices, and V_{pi} and I_{pi} are the peak voltage and current of device i respectively. Table I shows the device stresses and switch stress factor for the four converters.

Table I. Converter device stresses and stress factors.				
	V_p	I_p	N	F
Three-level	$\frac{1}{2}v_{dc}$	$|i_{as}|$	12	$\frac{6v_{dc}|i_{as}|}{P_{out}}$
Cascade-3	$\frac{1}{2}v_{dc} / \frac{1}{2}v_{dc}$	$|i_{as}|$	6 / 6	$\frac{6v_{dc}|i_{as}|}{P_{out}}$
Four-level	$\frac{1}{3}v_{dc}$	$|i_{as}|$	18	$\frac{6v_{dc}|i_{as}|}{P_{out}}$
Cascade-4	$\frac{2}{3}v_{dc} / \frac{1}{3}v_{dc}$	$|i_{as}|$	6 / 6	$\frac{6v_{dc}|i_{as}|}{P_{out}}$

In the case of the cascaded converters, two values of V_p and N are listed; one for the upper converter transistors and one for the lower converter transistors. In Table I, Cascade-3 and Cascade-4 are used to represent the cascaded converter in three- and four-level modes respectively. Since the semiconductors are effectively connected in series with the machine load, the peak current each transistor carries is the magnitude of the phase current. As can be seen, although the device peak voltages are different for each converter, the switch stress factor is the same due to the number of transistors. This would indicate that the converter installed cost would be the same for all converters. However, in reality there is some cost associated with the number of devices in addition to the stress factor (this is especially true at low power levels). In addition, since there are 18 devices in the four-level converter, it is expected that it will have higher conduction losses when compared to the other converters. Note that the cascaded converter in four-level mode has peak voltage ratings in the upper converter of $\frac{2}{3}v_{dc}$ which is higher than the voltage ratings of the other topologies. This can be a disadvantage for high voltage applications where the total dc voltage is limited by the maximum ratings of the devices available.

The cascaded converter has some advantages over the multi-level converter in regards to the arrangement of the semiconductors. It is simpler to construct since it is made from two standard six-transistor modules which are readily available. Multi-level converters require special interconnections with added diodes which cannot be made from six-transistor modules and must instead be made from dual pack modules and diode modules. Another advantage of the cascaded converter topology is that it avoids voltage sharing problems that some authors have noted occur in multi-level converters [7,8]. The voltage sharing problem arises when a particular phase of the multi-level converter is switched to the highest or lowest level. Under this condition, the voltages on the inner transistors are not necessarily even due to the current blocking action of the added diodes.

Solutions to this problem involve adding capacitors to the multi-level converter topology.

Another difficulty with multi-level inverters is dividing the DC voltage evenly with capacitors. Several solutions to this problem have been proposed including adding voltage balancing resistors in parallel with the capacitors [5], using PWM methods take advantage of the switching state redundancy to balance the capacitor voltages [9], and sensing the capacitor voltages and incorporating a negative feedback control system into the main control algorithm [10]. Although capacitor voltage balancing is not an issue for the cascaded converter, it requires two isolated dc voltage sources. For some applications, supplying these isolated sources is no more difficult than supplying a single voltage source. For example, in battery power applications (such as electric vehicles) isolated voltage sources can easily be made available by using separate battery packs. In a motor drive system that requires a transformer / rectifier circuit to supply the dc link voltage, a transformer with two secondary windings can be used to supply a cascaded converter. It should be noted, however, that since transformer / rectifier sources are not capable of absorbing power, care must be taken to ensure that the average dc currents supplied by the sources are positive. This is particularly a concern with the cascaded converter in four-level mode where the high-voltage converter could transfer power to the low-voltage converter. This problem can be avoided by careful selection of the redundant voltage vectors in the PWM switching sequence [11].

VI. COMPARISON OF CONVERTER PERFORMANCE

In order to experimentally verify the proposed cascaded converter, its performance is compared to the three- and four-level converters using a laboratory test system consisting of a reconfigurable converter (constructed from dual pack IGBT modules) and a 4-pole 3.7 kW induction machine with the parameters listed in Table II. The dc voltages were supplied from isolated rectified three-phase sources and in the case of the multi-level converters, the isolated sources were used to supply the capacitor voltages.

Table II. 3.7 kW INDUCTION MACHINE PARAMETERS	
$P = 4$	$L_m = 64.43$ mH
$r_s = 0.3996\ \Omega$	$L_{ls} = 5.73$ mH
$r'_r = 0.227\ \Omega$	$L'_{lr} = 4.64$ mH

Although many control techniques are available for multi-level converters, the space vector modulation (SVM) strategy was chosen as a baseline for comparing the converters. Using this method a commanded stator voltage vector is defined by

$$v^* = v_{qs}^{s*} - jv_{ds}^{s*} = \sqrt{2}\, v_s e^{j\omega_e t} \qquad (25)$$

where V_s is the rated RMS value of the machine voltage and ω_e is the rated electrical frequency in radians per second. The first step in the space vector modulation strategy is to approximate the commanded voltage vector by the discrete vector

$$v_k^* = \sqrt{2}\, v_s e^{j\frac{2\pi}{pn}k} \qquad k = 1, 2, \ldots pn \qquad (26)$$

In (26), pn is the number of discrete voltage vectors per cycle and is referred to as the pulse number. The pulse number is selected based on the desired performance; a higher pulse number yielding a higher switching frequency and thus better performance. The portion of time allocated for each discrete vector is referred to as the sampling time and can be calculated from

$$t_s = \frac{2\pi}{pn * \omega_e} \qquad (27)$$

The next step is to approximate each discrete commanded voltage vector by PWM switching to the nearest three voltage vectors [12]. This is accomplished by first locating the nearest three vectors and then computing the fraction of t, that should be spent at each vector in order for the fast average of the switching to be equivalent to the discrete vector. These times can be computed on-line using a fast microcomputer or computed off-line and stored in EPROMs. The advantage of computing the switching times on-line is that flexibility is provided for obtaining transient values of commanded voltage v^*, although methods for incorporating a variable commanded voltage using EPROM storage have

been proposed [13,14]. The advantage of using EPROM storage is that hardware construction is simpler. For the comparisons that follow, the PWM switching sequences are stored in EPROMs for a fixed value of commanded voltage magnitude.

For the studies presented herein, the various converters were used to create phase voltage waveforms with a 60 Hz, 187.8 V peak fundamental component. The induction machine was operated at a speed of 183.3 rad/sec. In making a comparison between the different converters it must be realized that for each converter a tradeoff can be made between current ripple and switching frequency. For this reason, in the studies set forth herein the pulse number and switching sequence have been chosen such that the current waveform THD is about 5.1%. In this case, the advantage of a large number of switching states is seen through a reduction in switching frequency.

Figures 8 and 9 illustrate the system performance of the three-level converter and the cascaded converter in three-level mode respectively. In both figures, the a-phase voltage and current are shown. As can be seen both converters exhibit identical performance. This is because the voltage vector diagrams and PWM switching sequences are the same. For
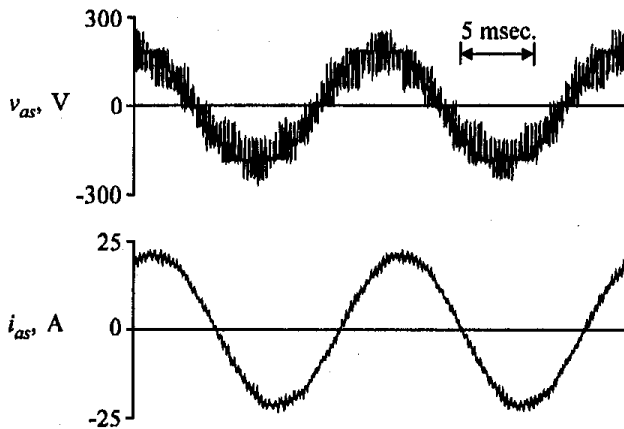
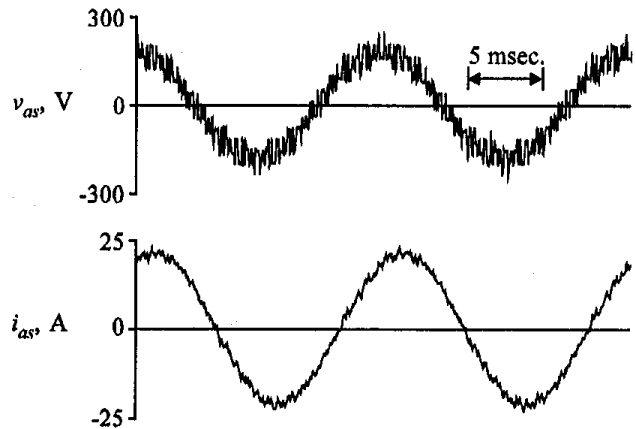Figure 8. Three-level converter performance.
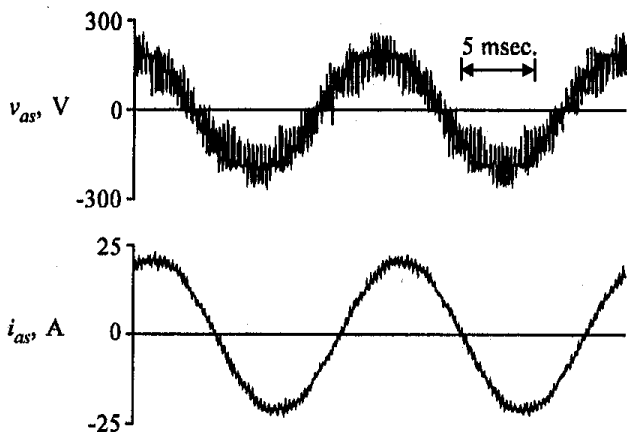
Figure 10. Four-level converter performance.

Figure 9. Cascaded converter performance ($v_{dc1} = v_{dc2}$).
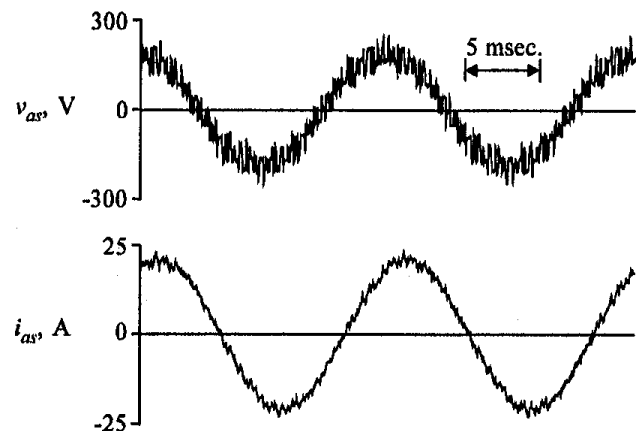
Figure 11. Cascaded converter performance ($v_{dc1} = 2v_{dc2}$).

both converters the pulse number is 60 and the voltage waveform THD is 34%. The individual transistors in the three-level converter were switching at 1.26 kHz. For the cascaded converter, the transistors were switching at a slightly higher frequency of 1.4 kHz due to constraints placed on the redundant voltage vectors in the PWM sequence necessary to ensure that the dc current supplied by the sources was positive on average [11]. It should be pointed out, however, that due to the amount of redundancy in the cascaded converter voltage vectors, it is possible to pick a switching sequence with the same voltage vectors as in the study, but one that uses different switching states. Switching sequences can be chosen that yield the same phase voltages with a switching frequency of 300 Hz in the upper converter and 2.34 kHz in the lower converter or vise versa.

Figures 10 and 11 show the *a*-phase voltage and current of the four-level converter and the cascaded converter in four-level mode respectively. Therein, it can again be seen that the performances of both converters are identical. The pulse number is 36 and the voltage waveform THD is reduced from the three-level case to 23%. The switching frequency in the case of the four-level converter is 420 Hz for the center two transistors in each phase and 720 Hz for the remaining transistors. The cascaded converter in four-level mode does not have the amount of redundancy that it does in three-level mode and consequently, there is little flexibility in distributing the switching frequencies. For large values of commanded voltage, the upper converter will have a low switching frequency and the lower converter will have a high switching frequency. This is fortunate since high-voltage low-frequency devices such as GTOs can be used for the upper converter and low-voltage high-frequency devices such as IGBTs can be used for the lower converter. With the sequence chosen, the switching frequency of the upper converter transistors is 300 Hz while the switching frequency of the lower transistors is 1.74 kHz. As with the cascaded converter in three-level mode, the sequence was chosen to ensure positive average dc current.

VII. CONCLUSION

A new type of converter is proposed which is constructed from two standard six-transistor (or two-level) converters. This topology is capable of producing voltage vectors that are the same as those of three- and four-level converters. An advantage of the proposed converter is that it has twelve active semiconductor devices whereas the four-level converter has eighteen. The new converter is easier to construct and capacitor voltage balancing is not a concern (although the new converter does require two isolated dc sources). The converter performance is verified experimentally using a 3.7 kW induction motor drive system.

VIII. ACKNOWLEDGMENTS

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