01 Oct 2003

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ELECTROMAGNETIC compatibility (EMC) is the engineering of electronic components and systems to ensure the overall functioning in a complex electromagnetic environment. Historically, this has included many aspects of the design, such as compliance with electromagnetic interference (EMI) regulatory standards, and insuring immunity of electronics to the electrical noise, i.e., interference generated by a neighboring system or external source. Electrostatic discharge (ESD) is one aspect of electronic immunity that can lead to failure at the IC, module, or system level that is again becoming a major concern in electronic design. EMC has traditionally also included wave-shaping and ensuring signal fidelity, as well as design of an adequately low-noise power distribution network to minimize EMI, and not compromise signal fidelity. Historically, EMC has been characterized as a "copper-tape-and-ferrites," trial-and-error discipline that reflects a postdesign approach to EMC. As design cycles have decreased, this approach to EMC has changed dramatically over the course of the past five to seven years. Within the commercial electronics community, the need and demand for EMC computer-aided design tools grew as rapidly as the design cycles decreased, and the complexity and data rates of designs increased. However, suitable tools had not been developed and, in many cases, the underlying noise coupling and immunity physics were not well understood. In large part, this state of affairs resulted from a lack of funding for more basic research and CAD tool development, and the complexity of the problem. The immediate demand for sophisticated EMC design tools that were undeveloped gave rise to focused research in EMC to understand the coupling physics and develop design methodologies and tools in industry and academia alike. Many individual companies have made significant investments in in-house EMC research, as well as funding of university research. The demand for a basic understanding of interference coupling physics, as well as design approaches and tools led to the development of focused EMC research within the UMR EMC Consortium at the University of Missouri-Rolla, as well as a significant research emphasis in other electronics and packaging centers such as the Packaging Research Center at Georgia Tech and the CALCE Electronic Products and Research Center at the University of Maryland.

The field of EMC has grown into a number of specialty areas, in particular, in the past five years, which reflects the present challenges associated with electronic design. This has resulted in part from increasing data rates and clock frequencies, decreasing logic levels resulting from increased power requirements, decreasing design densities, mixed-signal analog/digital designs within the same package, and higher frequency switching power supplies, among a host of other issues. There is still a significant need for a basic understanding of EMC in many aspects of high-speed digital and mixed-signal design including EMI (including radio-frequency interference (RFI)), immunity (including ESD), signal integrity (SI), and power integrity, in particular, at the IC, and IC substrate and packaging level. In addition, the need for modeling approaches and CAD tools in all areas of electromagnetic compatibility is acute. In an engineering design environment, the models and tools must be suitable for rapid computation and be within the expertise of a component or system designer to use. In practice, this reduces to circuit and transmission-line modeling, i.e., the typical SPICE-type environment.

The performance of first-pass engineering design validation hardware is often plagued by undesirable parasitics that compromise the signal fidelity and/or level, and dominate the coupling in the case of EMI and immunity. The coupling is through the electric field (capacitive coupling), magnetic field (inductive coupling), or through a common current return path, intended or unintended. In short, EMC is "about the things that are not on the circuit schematic," i.e., parasitic effects. There is a critical need for design methodologies and CAD tools that are based on well-understood parasitic effects and coupling physics, and can anticipate or extract suitable parasitic lumped circuit element models from a layout geometry. Presently, there are no such mature CAD tools. There are well-developed tools for the numerical solution of Maxwell's equations, RF circuit design tools, and circuit simulation tools. However, tools for anticipating parasitic effects are predominantly still at a beginning stage of development. To use a literature analogy, the complexity of the problem demands a solution with the sophistication of Tolstoy, but the available tools are at a grade-school primer stage of development.

Among the most challenging of electronics designs for EMC are those associated with mobile computing. These designs are typically battery powered with no real-time generation, and are low-power. In addition, the designs

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For information on obtaining reprints of this article, please send e-mail to: tmc@computer.org, and reference IEEECS Log Number 01-092003.

Published by the IEEE CS, CASS, ComSoc, IES, & SPS

often have wireless sections for data transmission and reception and, of course, the digital computing section for information and data processing. The three distinct functions, i.e., power distribution and management, digital computing, and RF wireless communication have very different bandwidths, as well as voltage and current levels, yet in a typical mobile device, must share the same printed circuit board and/or packaging substrate in a very dense design. The resulting parasitics and interference poses significant design challenges and requires considerable trial-and-error to produce hardware that meets the design requirements.

Four papers are presented in this topical section on EMC that are focused on modeling and circuit extraction of nonideal effects and power integrity. The first two papers by G. Antonini, and G. Antonini and A. Ruehli present varying aspects of the partial element equivalent circuit (PEEC) method. This method is a first principles formulation, i.e., begins from Maxwell's equations and is based on an exact integral representation of the solution to the Helmholtz or wave equation. However, the result of the method is not a numerical solution of Maxwell's equations, with current densities and electromagnetic fields, rather it is a circuit that is suitable for SPICE-type simulation and is extracted for both frequency- and time-domain analysis. Since the formulation is from first principles, all coupling and parasitic effects are included to the extent that the relevant geometry is modeled. In general, the extracted circuit can be quite large and computation of the circuit elements time consuming, however, the simulation time can be reduced by combining the PEEC method with a fast-solver approach, the fast multipole method (FMM) from traditional computational electromagnetics. The application of the FMM for PEEC analysis is presented, with applications.

The second set of papers addresses aspects of power integrity. The first paper by J. Choi, S.-H. Min, J.-H. Kim, M. Swaminathan, W. Beyene, and X. Yuan presents an approach for modeling and analysis of power distribution networks in high-speed digital designs. The power distribution network in multigigabit designs are not typically electrically small and, hence, require a Maxwell's equation formulation to adequately capture effects that will have a significant impact on the system response, in this case current draw by a digital device, and the noise voltage on the power distribution network. However, a Maxwell equation formulation to the problem is unsuitable for circuit simulation and engineering design discovery. Choi et al. overcome this limitation by first using a fast simulation approach for the power distribution network, which includes the electromagnetic effects and extracts a macromodel by representing the frequency response as a rational function. The poles and residues are determined in such a fashion that ensures stability and passivity representative of a linear, time-invariant system. The macromodel of the power distribution network is then combined with transmission-line and device models to anticipate the noise on the power distribution network resulting from device switching.

The final paper by V. Ricchiuti addresses the impact on the power distribution network using embedded capacitance for the power/ground layers. This approach uses closely spaced power/ground layers, on the order of one-quarter to two mils, for the spacing to achieve a low-impedance power bus structure that effectively mitigates noise propagation on the parallel plate transmission-line geometry. The work presents experimental results comparing the impedance and resulting measured electric fields for a test vehicle with two plane sets of differing embedded capacitance.

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Guest Editors

Antonio Orlandi (M'90-SM'97) received the Laurea degree in electrical engineering from the University of Rome "La Sapienza," Italy, in 1988. He was with the Department of Electrical Engineering, University of Rome "La Sapienza" from 1988 to 1990. Since 1990, he has been with the Department of Electrical Engineering at the University of L'Aquila where he is currently a full professor. He is the author of more than 100 technical papers he has published in the field of electromagnetic compatibility in lightning protection systems and power drive systems. His current research interests are in the field of numerical methods and modeling techniques to approach signal integrity and EMC/EMI issues in high-speed digital systems. Dr. Orlandi received the *IEEE Transactions on Electromagnetic Compatibility* Best Paper Award in 1997 and the IEEE EMC Society Technical Achievement Award in 2003. He is member of the Education, TC-9 Computational Electromagnetics, and TC-10 Signal Integrity committees of the IEEE EMC Society, chairman of the "EMC Innovation" Technical Committee of the International Zurich Symposium and Technical Exhibition on EMC. From 1996 to 2000, he was an associate editor of the *IEEE Transactions on Electromagnetic Compatibility* and now serves as an associate editor of the *IEEE Transactions on Mobile Computing*.

James L. Drewniak received the BS, MS, and PhD degrees in electrical engineering from the University of Illinois at Urbana-Champaign in 1985, 1987, and 1991, respectively. He joined the Electrical Engineering Department at the University of Missouri-Rolla in 1991, where he is one of the principle faculty in the Electromagnetic Compatibility Laboratory. His research and teaching interests include electromagnetic compatibility in high-speed digital and mixed signal designs, electronic packaging, and electromagnetic compatibility in power electronic based systems. Dr. Drewniak is an associate editor of the *IEEE Transactions on Electromagnetic Compatibility*, and chair of the EMC Society technical committee TC-10 Signal Integrity.