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Giulio Antonini

James L. Drewniak
*Missouri University of Science and Technology*, drewniak@mst.edu

Marco Leone

Antonio Orlandi

*et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1892*



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# STATISTICAL APPROACH TO THE EMI MODELING OF LARGE ASICS BY A SINGLE NOISE-CURRENT SOURCE

G.Antonini *, J.L.Drewniak °, M.Leone +, A.Orlandi *, V.Ricchiuti ^,

* *UAq EMC Laboratory,* Dept. of Electrical Engineering, University of L'Aquila, L'Aquila, Italy
FAX: +39-0862-434403, e-mail: antonini@ing.univaq.it, orlandi@ing.univaq.it
° *UMR EMC Laboratory,* ECE Dept., University of Missouri-Rolla, Rolla, MO, USA
FAX: +001-573-341-4532, e-mail: drewniak@ece.umr.edu
\+ SIEMENS AG, Corporate Technology, Erlangen, Germany
FAX: +49-9131-7-33190, e-mail: marco.leone@siemens.com
^ CNX S.p.A. – A SIEMENS Company – L'Aquila, Italy
FAX: +39-0862-335527, e-mail: vittorio.ricchiuti@siemens.com

***Abstract* – Large and complex ASICs are source of propagating noise inside the powerbus planes. A lumped noise source model is proposed and validated by means of a statistics based method.**

## I. INTRODUCTION

Nowadays on-chip integration leading to system-on-chip (SOC) is the most dominant approach to electronic systems. However, it starts to be clear that complete mixed signal SOC-based systems are not realistic. Because of this, system-in-package (SIP) or system-on-package (SOP) are actual fields of research [1]. All of these systems have in common the implementation and use of large and complex ASICs. Due to their high power consumption and fast and highly simultaneous switching activity, these integrated components are often the most relevant source of power-bus noise. This is caused by the fast transient current drawn from the power bus by the power/ground (PWR/GND) pins of the ASIC during the switching of the transistors within the core, the logic units and the I/O. These transients excite electromagnetic waves propagating in the cavity formed by the power and reference planes, bouncing back and forth between the boards' boundaries, giving rise to signal integrity (SI) and radiated emissions problems. Printed circuit board (PCB) designers must have a knowledge of the simultaneous switching noise (SSN) in order to predict the level of these effects. For simulation purposes, both a model of the power bus and of the ASICs noise are required. Recently a lot of work has been done to the power bus modeling: [2,3] and their reference lists are only an example among a number of significant contributions. At the modeling of large ASICs it has not been given, up to now, too much attention. For small integrated circuits (IC) the number of switching drivers is known and the IC's parameters such as the power dissipation capacitance $C_{pd}$ and the switching time interval $\Delta t$ are usually available and can be used for calculating the noise current spectrum [4,5]. For physically large ASICs these parameters are not known or very difficult to be extracted due to the ASIC complex circuitry [6]. Furthermore, multiple pins, spatially distributed under the ASIC's footprint, are connected to the same power bus supplying different parts of the IC (core, I/O, etc.). Because of this, a lumped noise current source model is not self evident. Aim of this work is to analyze the relevance of the position of the power supplying pins to the generation and propagation of interferences inside the power bus and hence to asses the possibility to approximately represent the ASIC's noise behavior by a single source of noise.

## II. THE CAVITY RESONATOR MODEL

According to the well established cavity-resonator model [2], the two planes forming a power bus are considered as a solid planar structure, of dimensions $a$ and $b$, separated by a dielectric of thickness $h$. By solving the radial wave propagation problem between the planes, the Green's function with respect to the source and observation point $\mathbf{r} \equiv (x,y)$, $\mathbf{r}' \equiv (x',y')$, respectively, results in [2]

$$G(\mathbf{r},\mathbf{r}') = \frac{j\omega\mu h}{ab}\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\frac{c_n c_m}{k_{mn}^2 - k^2}\left[\cos(m\pi x/a)\cos(n\pi y/b)\cos(m\pi x'/a)s\cos(n\pi y'/b)\right] \qquad (1)$$

in which $n$ and $m$ are the modes indices, the wave number is $k_{mn}^2 = (m\pi/a)^2 + (n\pi/b)^2$ and the ports' dimensions are considered infinitesimal. The coefficients $c_{m,n}$ are equal to 1 for $m,n = 0$ and and equal to $\sqrt{2}$ otherwise. The wave number

$$k = \omega\sqrt{\mu\varepsilon}\left(1 - j\frac{1}{2}\left(tg\delta + \frac{t}{h}\right)\right), \qquad (1)$$

with the angular frequency $\omega$, the magnetic permeability and electric permittivity of the dielectric $\mu$ and $\varepsilon$, respectively, includes the dielectric and ohmic losses, as specified by the loss angle $\delta$ and the skin depth $t$. Eq.(1) represents the voltage between the two planes at point **r**, due to a unit current injected at **r'**.

## III. STATISTICAL CONSIDERATIONS

A large ASIC is supplied by several PWR/GND pin pairs located at different positions inside the ASIC's footprint on the component layer of the board. Each pair represents a port on the board in the cavity model, through which a certain noise-current is drawn. The resulting total noise voltage $V$ at the observation point **r** is the sum of all individual contributions of each pin located at $\mathbf{r}'_i$, i.e.

$$V(\mathbf{r}) = \sum_{i=1}^{N} G(\mathbf{r}, \mathbf{r}'_i)\, I_i \tag{2}$$

The total number of injecting pins of the ASIC is denoted by $N$, $I_i$ are the $N$ individual complex currents associated to the injection points $\mathbf{r}'_i$. In practice, it is not immediate to determine $N$ and $I_i$. Therefore, an approximate lumped-source model was suggested in [6] and validated for the first time by measurements. Based on the total injected current

$$I_{tot} = \sum_{i=1}^{N} I_i \,, \tag{3}$$

concentrated at the center of the ASIC at $\mathbf{r}_0 \equiv (x_0, y_0)$, the voltage $V_0$ produced in **r** by this single source is

$$V_0(\mathbf{r}) = \sum_{i=1}^{N} G(\mathbf{r}, \mathbf{r}_0)\, I_{tot} \,. \tag{4}$$

The question to be answered is how far the lumped-source model given in (4) is valid in comparison to the exact result (2). For this purpose, a rectangular power bus, lid out with to PWR/GND planes adjacent one to another, of length $a = 26.5$ cm and width $b = 20.7$ cm has been considered (Fig.1). The two planes have electrical conductivity of copper $\sigma = 5.65 \cdot 10^7$ S/m and are separated by a dielectric slab with thickness $h = 50\mu$m, $\varepsilon_r = 4.2$, $tg\delta = 0.02$, representing typical FR-4 material. The shaded area in Fig.1 represents the surface covered by an ASIC of squared footprint of side $l = 3.8$ cm, where a number of injecting pins ($N = 50$) was randomly distributed. To each one of the pins is associated an injected current $I_i = |I_i| e^{j\varphi_i}$, whose magnitude and phase are also randomly selected inside the range $0 \le |I_i| \le I_{MAX}/N$ and $0 \le \varphi_i \le 2\pi$ respectively. $I_{MAX}$ is the maximum current drawn by the ASIC and estimated by means of power consumption and thermal data. The noise voltages $V$ and $V_0$ were computed at two locations: "Near" (9.5 cm, 8,5 cm) and "Far" (23.5 cm, 17.7 cm). The ASIC's footprint is centered at $\mathbf{r}_0$ = (6.6 cm,6.6 cm).

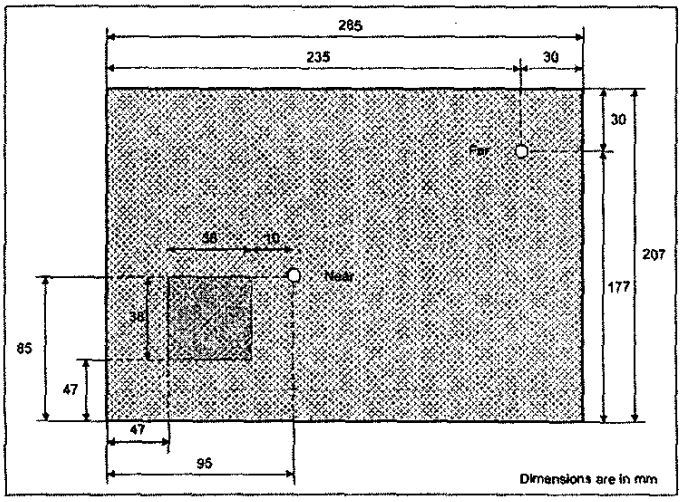


**Fig. 1** - Geometry and dimensions of a test board for validation of the lumped-source approximation for an ASIC (the ASIC's footprint is shadowed).

Figs. 2a and 2b show a comparison among the frequency responses obtained by (2) and (4), for the "Near" and "Far" observation point, respectively. The frequency axis is represented by the ratio between the maximum dimension of the ASIC $d$ (the diagonal in this case) and the wavelength $\lambda$ in the dielectric. From this computational example it is visible that $V_0$ and $V$ correspond quite well, up to $d/\lambda \approx 0.6$, accepting some deviations especially around the nulls of either the

response of V or $V_0$. In this sense, there is no significant different behavior between an observation point located near or far from the ASIC. It is interesting to note that near the resonances the correspondence is much better. This can be explained by the voltage distribution of a resonant mode, which has a much more slower spatial variation in comparison to the superposition of many higher-order modes at non-resonant frequencies.

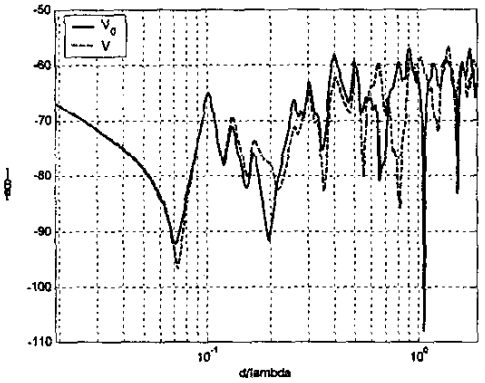


**Fig. 2a** - Example for the noise-voltage frequency response $|V_0|$ of the approximate lumped-source model compared to the exact result $|V|$ at port "Near".

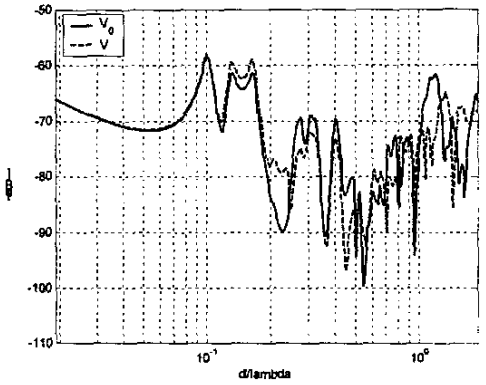


**Fig. 2b** - Example for the noise-voltage frequency response $|V_0|$ of the approximate lumped-source model compared to the exact result $|V|$ at port "Far".

A more statistical evaluation of the approximate lumped-source model is shown in Fig.3a and 3b by the average relative deviation $|V_0/V|$. In each of the two diagrams a number of 50 frequency responses were computed for different and random spatial distribution of 50 injecting pins, each associated to a random current amplitude and phase varying between 0 ... 2 mA and 0 ... $2\pi$ (constant over frequency). The average of $|V_0/V|$ was obtained by calculating the average value of the 50 curves at each frequency point.
Fig. 4a and 4b show the standard deviation, normalized with respect the average at each frequency point, of the curves in Figs. 3. They complete the information needed for a meaningful interpretation of the statistics results.

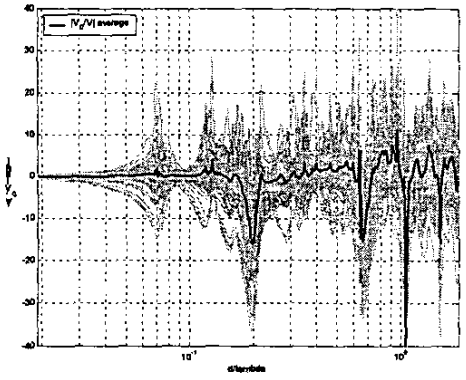


**Fig. 3a** - Average relative deviation of the noise-voltage frequency response of the approximate lumped-source model compared to the exact result at port "Near".

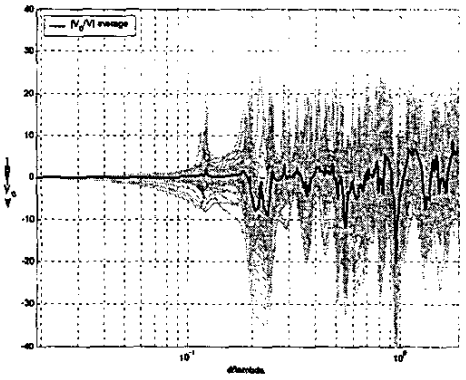


**Fig. 3b** - Average relative deviation of the noise-voltage frequency response of the approximate lumped-source model compared to the exact result at port "Far".

It is visible that the proposed approximate lumped-source model shows relatively small average deviations up to 0.1 ... 0.2 d/λ, corresponding to a frequency range between 250 MHz and 500 MHz for the chosen geometry. Tolerating a maximum average deviation of $|V_0/V|$ up to 10 dB at certain frequencies, the lumped-source model can be even used up to approximately 0.6 d/λ ... 1 d/λ, corresponding to 1.5 GHz to 2.5 GHz. Referring to the observations in Fig.2a and 2b, where the deviations mainly occur near the nulls of the frequency responses, we assume that the above frequency ranges will be higher for smaller power-bus dimensions.

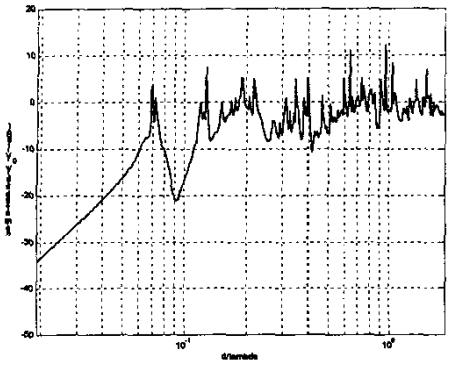

**Fig. 4a** - Normalized standard deviation of the curves in Fig. 3a for port "Near".

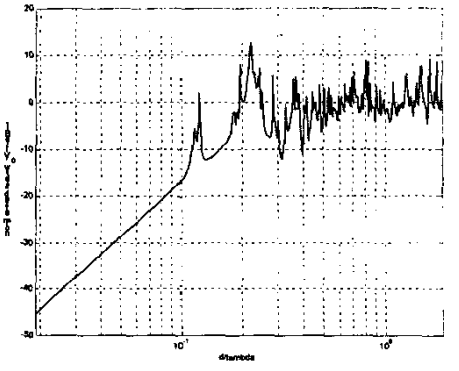

**Fig. 4b** - Normalized standard deviation of the curves in Fig. 3a for port "Far".

## IV. CONCLUSIONS

From the above results (and the other not shown here for sake of brevity) a first conclusion can be drawn and substantiate: for frequencies such as $d/\lambda < 0.1$-$0.2$ the SSN effects of multiple PWR/GND pins can be evaluated with sufficient accuracy by considering a lumped-noise current source placed in the geometric center of the ASIC. Relaxing the deviation of $V_0$ with respect $V$ up to 10 dB the lumped-source model can be used up to 0.6 d/λ ... 1 d/λ, corresponding to frequencies ranging above 1 GHz. This consideration leaves, as only degree of uncertainties, the harmonic content of the lumped current source. Due to the practically unpredictable behavior of each single ASIC supply currents a statistical approach is under development for the assessment of the lumped noise source frequency spectrum.


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