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The Influence of Test Parameters on TEM Cell Measurements of ICs

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Abstract—**The IEC 61967-2 TEM cell standard allows for variations in test parameters which may cause variations in the measured emissions from integrated circuits (ICs). To test the impact of these parameters, two printed circuit boards were designed within the IEC standard using "poor" PCB design strategies and using "good" design strategies. Emissions from three pin-for-pin compatible 8051 microcontrollers were tested. Emissions were measured using both PCBs, changing the PCB configuration, and changing test parameters like the program running on the IC, the rise time of the input clock, and I/O switching. Emissions from the "poor" PCB were about 3-8 dB higher than emissions from the "good" PCB. A change in the program run by the IC, the clock rise-time, and I/O caused a 4-15 dB change in emissions. Emissions differed considerably among the ICs. Possible causes for variations in emissions with the test parameters are discussed**.

Keywords: **Electromagnetic Compatibility, Integrated Circuits, Testing, Emissions, TEM-cell Method**

I. INTRODUCTION

IC manufacturers use standardized testing methods such as IEC 61967 and SAE J1752 for measurement of emissions from ICs [1-3]. One of the procedures described in IEC 61967 uses the TEM cell. Near electric- and magnetic-field emissions are measured with the cell by mounting the IC on a test Printed Circuit Board (PCB), which is then mounted on the wall of a TEM cell with the IC inside the cell. The guidelines given by the TEM cell measurement procedure allow for flexibility in test parameters like the PCB test board design, the input clock edge rate, and others. As a result, tests performed by different companies or engineers using the same guidelines might yield different measurements of emissions for the same IC. This paper studies the variations in TEM cell emissions among test configurations that are allowed by the IEC standard.

To test the influence of variation of PCB design parameters, PCBs which have provisions to vary design parameters (one or many at a time) were developed according to the IEC standard and measurements were made on a typical IC using these boards. PCB design variations that were studied include distance between PCB layers, PCB stack-up, length and width of traces on the IC side of the TEM cell, the amount of decoupling, the placement of decoupling, the decoupling capacitor connection method, and the presence (or absence) of a ground plane below the IC. In addition to the PCB design, other parameters that were studied are the clock edge rate, the use of I/O (i.e. inhibiting I/O from switching), and variations in software. The influence of variation of each of these test parameters was studied individually and is shown in the measurement results section of this paper. Measurements were performed on three pin-for-pin compatible 8051 microcontrollers from three different manufacturers (Atmel, Philips, and Max-Dallas[4-6]), as the emissions are expected to depend on the manufacturer [7, 8]. The design of the test boards, the measurement setup and results, and possible reasons for the change in the emissions from one design to another and from one IC to another are discussed in the following sections.

II. TEST BOARDS

The IEC 61967-2 standard was carefully studied and the design parameters which are not well specified in the standard were determined. Test variations were implemented in two PCBs, which will be called board 1 and board 2. Board 1 has a stack-up GND/PWR/SIG/SIG (starting from the IC side) and board 2 has a stack-up GND/SIG/PWR/SIG. Except for the stack-up, these two PCBs are the same. Pads for the decoupling capacitors were arranged such that capacitors could be placed far away from the IC or very close to the IC, could be connected with long traces to the power and return plane, and so forth, covering many decoupling capacitor arrangements. While traces on the IC-side of the test board are discouraged in the TEM cell standard, some traces are allowed. To allow testing of the effect of the traces on the IC side, each ground pin of the IC was connected to a long trace and these traces could be connected to the return plane either near the IC (short trace) or at the far end of the trace (long trace). Provisions for wide traces were achieved by placing another trace right beside these traces to the return plane (in parallel) and providing pads to connect these traces to the return plane or to each other at both ends. Testing the influence of the presence of a return plane below the IC was achieved by placing a copper fill below the IC, which was not connected to the rest of the return plane. Seven pads were placed around this copper fill which could be used to connect it to the surrounding return plane whenever the return plane was to be extended below the IC; otherwise, the pads were left unconnected. Pads were also provided near the clock input of the board to mount a low pass filter when needed. The

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completed layout of the PCB is shown in Fig. 1. The arrangement of the decoupling capacitors, the traces on the IC side, and the ground fill below the IC are shown in Fig. 2. The finished thickness of the PCB was approximately 62 mils, with the core approximately 42 mils thick. The length and width of the trace used on the IC side was approximately 6 mm and 1 mm respectively. Additional information about the board design can be found in [9].

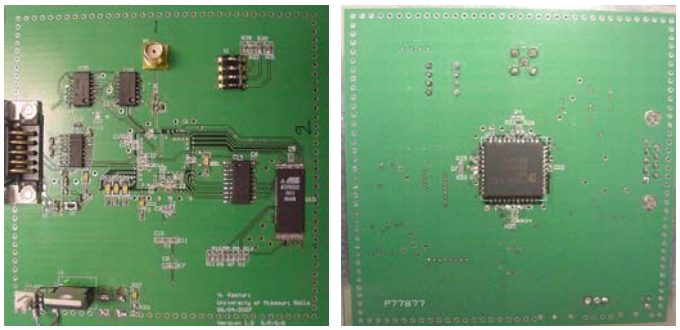

Figure 1. Completed printed circuit board. Top view (left); bottom view (right).

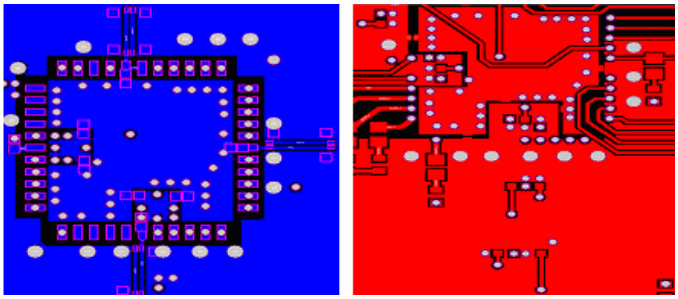

Figure 2. Layout used to modify trace width (left), decoupling capacitor connections (right) and presence of ground pad under the IC.

III. Measurement Set-Up

The measurement set-up included is outlined in Fig. 3. Emissions were measured using a spectrum analyzer (Rohde & Schwarz FSEB) and a 1 GHz TEM cell (FCC-TEM-JM1) One port of the TEM cell was connected to a 50-ohm matched load. The other port was connected to the spectrum analyzer to view the power coupled to the septum of the TEM cell as a function of frequency.

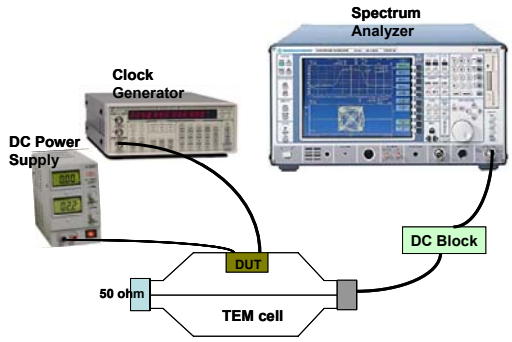

Figure 3. Measurement set-up.

The IC was powered by an external DC power supply. The clock signal for the IC was supplied from an external clock generator. The ICs were clocked at their 33 MHz operating frequency. The spectrum analyzer was set in peak detect mode and for max hold. Resolution bandwidth and video bandwidth were set to 10 KHz and 30 KHz respectively. RF attenuation was set at 10 dB, giving a noise floor of approximately 12 dBμV. Start and stop frequencies were set to 1 MHz and 1 GHz respectively, with 500 points sampled over the total range. The sweep time was 25 sec. Three measurements were taken at different times for each set-up and averaged, with each measurement taken for approximately 7 minutes. Difference in measured values among any two measurements was always less than approximately 2.5 dB. Since, results are presented using the average of three results taken at different times, if error is assumed to be independent and Gaussian distributed, accuracy of the results should generally be better than approximately 1 dB. Measurements were taken for all four orientations of the test PCB within the cell for all test set-ups.

IV. Measurement Results

A. PCB Design Variations

As outlined earlier, the design variations that were studied include the distance between the PCB layers, the decoupling strategy, stack-up, the width and length of traces in the TEM cell, and the presence of a ground plane below the IC. The parameters tested in this section can be divided into two sets. Set 1 includes parameters which dominate the variations in the emissions in the low frequency range (below a few hundred MHz) and set 2 includes parameters which dominate the variations in the emissions in the high frequency range (above a few hundred MHz). Set 1 includes the decoupling strategy as decoupling capacitors are generally only effective up to a few hundred MHz [10]. Set 2 includes the presence of a ground plane under the IC, the presence of wide and long traces to the IC, stack-up, and distance between the layers. These parameters cause variations in the loop area of power return currents, which may increase coupling at high frequencies.

Initially, the idea was to study the variation of each parameter individually. The influence of changing the value, number, and location of decoupling capacitors was studied individually and in combination, but the emissions did not change significantly from one case to another among these combinations [9]. Since emissions varied only slightly among individual parameters, measurements were instead compared between a board using what are typically bad design strategies and a board using typically good design strategies. The boards were called the case 1 and case 2 setups:

• Case 1 uses the GND/PWR/SIG/SIG stack-up, the ground plane is extended under the IC, decoupling capacitors (both local and bulk adds up to 22.2 μF) are present, very short traces on the IC side are used, and an RC low-pass filter (R = 100 Ohm, C = 100 nF) is present in the path of the clock trace.

• Case 2 uses the GND/SIG/PWR/SIG stack-up, uses no decoupling capacitors (both bulk and local), no ground plane

under the IC, long and wide traces on the IC side, and an RC low-pass filter (R = 100 Ohm, C = 100 nF) is present in the path of the clock trace.

Emissions from case 2 would generally be expected to be higher than from case 1. Emission measurements were performed on both these boards while running a program that thoroughly exercised the software, later called program 2 in this paper.

The poor PCB design (case 2) yielded worst emissions than the good PCB design (case 1) for all three ICs. Measurement results for the Atmel and Philips ICs were similar, as shown in Figs. 4 and 5. Below approximately 100 MHz the "poor" case 2 design gave approximately 3-4 dB higher emissions than the "better" case 1 design when the board was oriented at 0 degrees with respect to the TEM cell. Oriented at 90 degrees, the case 2 set-up gave approximately 2 dB higher emissions than the case 1 set-up below 150 MHz. Results at 180 and 270 degree orientations were similar. Above approximately 200 MHz the emissions did not uniformly decrease or increase between the setups. The fact that results differ among orientations indicate that inductive or a combination of inductive and capacitive coupling dominates, though the coupling mechanism was not carefully studied. The Max-Dallas IC has up to 6 dB higher emissions for the "poor" case 2 set-up for all four orientations below approximately 600 MHz, as shown in Fig. 6. Above 600 MHz, both boards produced similarly good or bad emissions.

B. Test Configuration Variations

1) Clock edge rate

While the TEM cell test is intended to only measure emissions related to an IC and not the clock fed to the IC, there is a chance that the clock may couple directly to the TEM cell, independent of the IC. To test this possibility the effect of the input clock edge rate on the measured emissions was studied for the three ICs tested. This test was performed using the setup for case 1, which has the ground plane extended under the IC, uses both local and bulk decoupling capacitors, uses very short traces on the IC side, runs program 2, and uses an RC low-pass filter (R = 100 Ohm, C = 100 nF) in the path of the clock trace on board 1. In one case the clock signal was directly connected to the IC from the clock generator and measurements were performed with this relatively fast rise-time signal (the rise time of the signal directly coming out of the clock generator was approximately 1 ns). In the other case a low-pass filter (R=100 Ohm, C= 100 pF) was placed in the path of the clock trace to increase the rise time of the signal to approximately 22 ns before it was passed inside of the TEM cell to the IC.

Increasing the clock edge rate caused increase in the measured emissions at high frequencies from 5-20 dB for all orientations of the three ICs. One such measurement is shown in Fig. 7. A careful review of all four orientations showed that both capacitive and inductive coupling increased for the three ICs when a clock with fast edge rate was used. Plots for all four orientations and all three ICs tested are shown in [9].

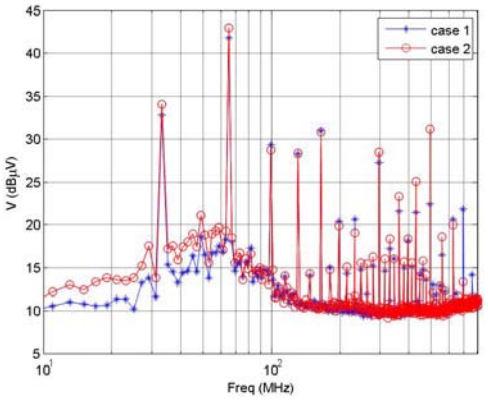

Figure 4. Comparison between TEM cell emissions for case 1 and case 2 (0 degree orientation, Atmel).

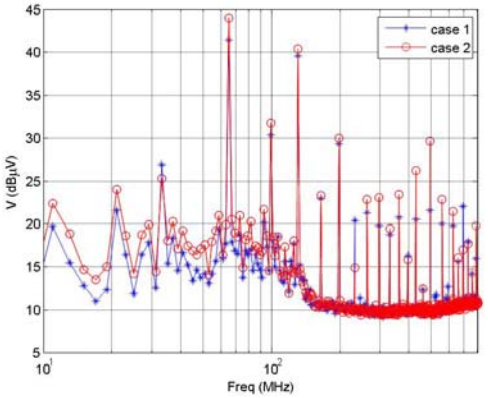

Figure 5. Comparison between TEM cell emissions for case 1 and case 2 (0 degree orientation, Philips).

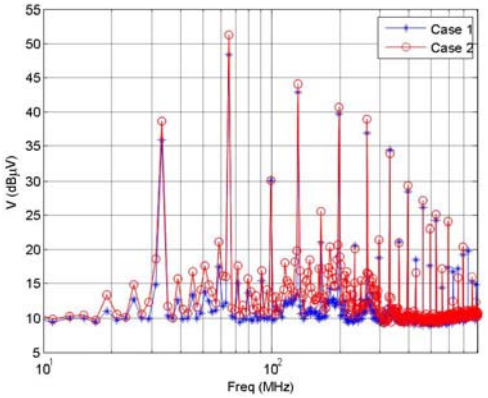

Figure 6. Comparison between TEM cell emissions for case 1 and case 2 (90 degree orientation, Max-Dallas).

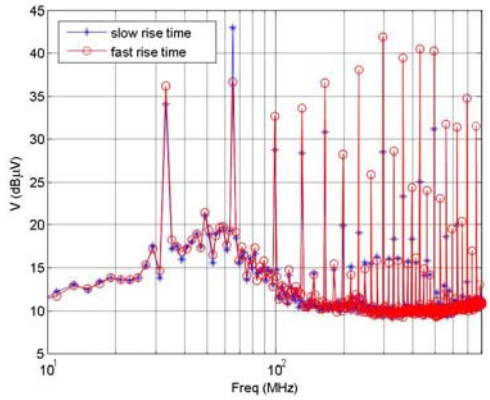

Figure 7. TEM cell emissions when using a fast- and slow- rise-time clock (0 degree orientation, Atmel).

2) Clocking of unused I/O pins

The switching of I/O is also likely to effect emissions and may be particularly important when switching is optional. The effect of switching I/O pins on the measured emissions was studied for the three ICs. This test was performed using the setup from case 1, which has the ground plane extended under the IC, uses both local and bulk decoupling capacitors, uses very short traces on the IC side, runs program 2, and uses an RC low-pass filter (R = 100 Ohm, C = 100 nF) in the path of the clock trace on board 1. The address latch enable (ALE) pin was tested here because this pin is only used when the microcontroller accesses external memory. In the standard 8051 microcontroller, this pin switches at a constant rate close to the clock frequency, even when external memory is not being accessed by the microcontroller. Many microcontroller IC manufacturers provide an option to turn off this ALE pin when the microcontroller is not accessing external memory, by setting a control bit in the software code. Such ICs are often labeled as "low emissions" ICs, a claim which will be validated by this test. Two configurations were tested. In one case the ALE pin was turned OFF so it switches only when the IC accesses external memory or expanded RAM and in the other case the ALE was switching all the time. Since our test setup did not use external memory, the ALE was never required to switch.

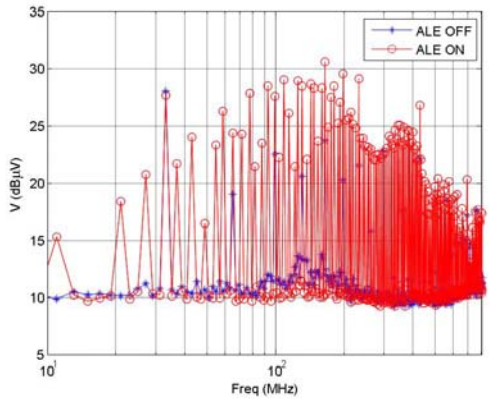

Figure 8. TEM cell emissions with and without ALE switching (90 degree orientation, Atmel).

Switching of the ALE pin (i.e. of unused I/O) caused approximately 5-20 dB increase in the emissions for the three ICs in all four orientations. The frequency range in which the emissions increased depended on the switching rate of the ALE pin. One such measurement is shown in Fig. 8. Additional measurements are shown in [9].

3) Software

As the current drawn by the IC may depend on the instruction or operation performed, the software run by the IC may also influence TEM cell emissions. The effect of software was tested using the setup for case 1, which had the ground plane extended under the IC, used local and bulk decoupling capacitors, used short traces on the IC side, and used an RC low-pass filter (R = 100 Ohm, C = 100 nF) in the path of the clock trace on board 1. Two different programs called program 1 and program 2 were written to perform this test. Program 1 repeatedly blinks four LEDs on the test board in a binary number pattern and does little else. This program does not access different internal memory areas nor exercise many instructions, so there is no significant activity in the core of the microcontroller. Program 2 accesses different internal memory areas, performs arithmetic operations, logical operations, and many other instructions, goes into power-down mode, returns to normal mode through an interrupt, and then blinks the LEDs in a binary pattern. These tasks are done repeatedly in an infinite loop. Emissions were measured when each of these programs was executing in the microcontroller.

Changing the program running in the IC from program 1 to program 2 caused approximately 4-8 dB increase in the emissions at frequencies below 300 MHz for all four orientations of the Atmel and Philips ICs, though the increase was primarily outside of the clock harmonics. At clock harmonics, the emissions were virtually the same. In contrast, for the Max-Dallas IC program 1 had higher emissions than program 2. Fig. 9 and Fig. 10 show two example measurement results. Additional plots are shown in [9][9].

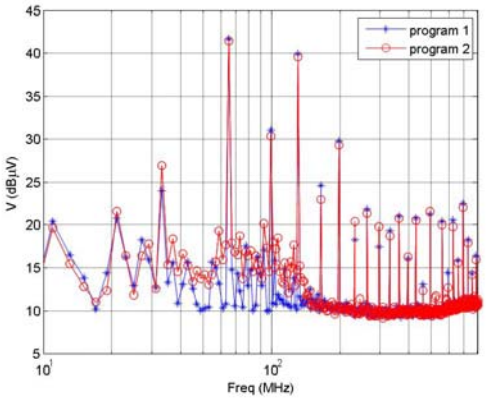

Figure 9. TEM cell emissions using program 1 and program 2 (0 degree orientation, Philips).

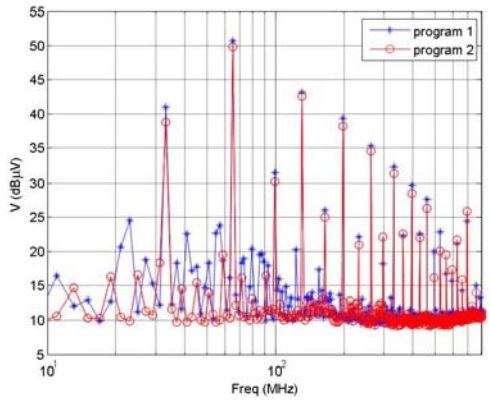

Figure 10. TEM cell emissions using program 1 and program 2 (0 degree orientation, Max-Dallas).

C. *Manufacturer Variations*

While testing variation in IC emissions among manufacturers was not the goal of this study, the results from the previous tests afforded us the opportunity compare emissions among the three tested ICs. The emissions were compared for five different test board setups. The main purpose was to determine which IC performed best (or worst) under which test conditions. The general trend was that the Max-Dallas IC had the highest emissions among the three ICs at the harmonics of the clock frequency for all five test setups. Emissions were generally 5-25 dB higher than the other manufacturer's ICs. Max-Dallas's higher emissions might be due to the fact that the Max-Dallas IC operates approximately twelve times faster than the other two ICs for the same input clock frequency [6]. That is, the Max-Dallas IC completes an instruction in one clock cycle, while the other two ICs complete an instruction in 12, 24 or 48 clock cycles. As a result, the Max-Dallas IC likely has more gates switching in any particular clock. While emissions from the ICs were not generally as large at frequencies that were *not* clock harmonics, at those (non-harmonic) frequencies the general trend was that the Atmel IC caused higher emissions at high frequencies (above a few hundred MHz) and the Philips IC caused higher emissions at low frequencies (below a few hundred MHz). The Atmel IC may have caused higher emissions at high frequencies because this IC had a faster internal rise-time than the Philips IC [8], [11]. The Max-Dallas IC always had low emissions outside of the clock harmonics, since switching always occurs periodically with the clock and not at a sub-harmonic of the clock, as with the other ICs.

V. DISCUSSION

The effect of PCB design variations on TEM cell emissions can be explained better by dividing the total frequency range into two sub ranges: low frequencies (below a few hundred MHz) and high frequencies (above a few hundred MHz). The emissions variations at low frequencies are influenced by the decoupling strategy of the test PCB. Emissions variations at high frequencies are most influenced by PCB design parameters such as the presence or absence of the ground plane under the IC, the width and length of the traces on the IC side, the distance between the layers, and the stack-up of the test PCB. In the ICs tested, the increase in the emissions observed by changing the test PCB design from with decoupling capacitors (both bulk and local) and closely spaced power and ground planes to a test PCB without any decoupling capacitors (local or bulk) and widely spaced power and ground planes was approximately 3-4 dB. Considering the +/-1 dB accuracy of the measurement, there was a measurable but not significant increase in the emissions between these two cases. A more advanced IC with more transistors and higher working frequencies, however, may see a larger change in emissions with decoupling capacitors and power plane spacing, since they require significantly more current, increasing the noise voltage on the power delivery network.

At high frequencies, it was observed that there was a change of approximately 5-8 dB in the emissions when the PCB design was changed from a design with a ground plane under the IC, which used very short traces on the IC side and had closely spaced power and ground planes, to a design which had no ground plane under the IC, which used long wide traces to connect the ground pin to the board ground, and had widely spaced power and ground planes (some orientations saw an increase and some saw a decrease). In the test PCB, the ground pin is the only pin which used a long, wide trace to connect to the PCB ground. ICs with more power and ground pins and/or increased switching current may see a larger or smaller change in emissions with these same variations. More power and ground pins may allow more potential return paths and possibly create loops with opposing flux, potentially reducing the impact of larger traces or a ground plane beneath the IC [12]. Higher switching currents, however, will likely increase the impact of these variations.

Clocking of unused I/O pins - in this case the ALE pin - caused a significant increase in the emissions from all three ICs tested. The ALE pin caused variations either through the entire frequency range, only at low frequencies, or only at high frequencies, depending on the particular IC's ALE pin switching rate. Not surprisingly, switching of unused I/O pins has a large influence on the TEM cell emissions. In the ICs tested, when the ALE pin was off, the emissions were lower by about 10 dB compared to when the ALE pin was on. These results support the manufacturer's typical contention that an 8051 IC with the option to turn off the ALE pin is a "low-emissions" IC. In any case, because of the importance of I/O, an IC should be tested in the configuration it will be used in the end application, as is recommended by the IEC standard. Testing with more I/O switching at a higher speed than in the end application may give artificially high emissions. Similarly, ignoring I/O may ignore potentially significant emissions sources. Different manufacturers should be compared with similar test configurations.

It was observed in all three IC test measurements that there was an increase in the strength of clock frequency harmonics by up to 10 dB at high frequencies when the rise time of the input clock was decreased from 22 nsec to 1 nsec. When using a fast rise-time clock, the emissions from all three ICs were all almost equally bad, indicating that most of the emissions were associated with the clock feeding the IC rather than from the IC itself. If the goal of this test was to measure emissions from the IC, then this test failed to achieve its goal. The clock input

can have a significant influence on emissions, even when connected very well to the IC as it was here, with a via to the clock pin placed directly in the pin-pad. While the influence may not be as large for bigger, faster ICs with more switching current, the effect of the clock input should be accounted for when comparing emissions among different ICs. In general, ICs should be tested and used with as slow a clock edge as is required for operation.

A difference of up to approximately 4-8 dB was observed in the measured TEM cell emissions when changing the software run by the IC. This result supports the IEC's contention that software should be considered when comparing the emissions from different ICs.

For the Max-Dallas IC there was a decrease in the emissions by 10-15 dB at some frequencies when running program 2, compared to program 1. This result was somewhat surprising, since program 1 was expected to have lower emissions. The unexpected result may have been caused by the switching of port pins used to light LEDs. The LEDs were switching very quickly for program 1 and much slower for program 2. If this switching is important to emissions, switching more slowing will reduce overall emissions. Other manufacturers may also see emissions from the switching of the I/O, but that change may be too small to see at the measured frequencies, since instructions are executed at 1/12 the rate or slower. The Max-Dallas switches the LEDs faster than the other two manufacturers, since an instruction is executed in one clock cycle for this IC (12 to 48 times faster than the other ICs). It is also possible that one of the instructions executed by program 1 happens to be a particularly high-energy instruction for the Max-Dallas part, so that program 1, which calls this instruction more often than program 2, has higher emissions.

Emissions variations with software were only seen at low frequencies for the three ICs tested and were generally small at clock harmonics. Other investigators have found that changing the software changed emissions only at high frequencies [7]. The reason we did not see variations at high frequencies for the ICs tested may be the high noise floor of the measurement or the 1 GHz upper frequency limit of the measurement (if the variations occur at even higher frequencies). The change in low-frequency emissions is not unexpected, however, if the energy used by different instructions is expected to vary from one instruction to another, especially if the program is executed in an infinite loop.

VI. CONCLUSIONS

The IEC 61967-2 test standard allows flexibility in the design of the PCB and the selection of other test parameters. Differences in these test parameters can impact the observed EMI performance of the IC. Variations in emissions were seen here with PCB configuration, software, clock driving rate, and I/O usage. The impact of the test configuration on other ICs is uncertain, but it is clear that variations of at least 5 dB are possible even when following similar specifications and adhering to the IEC standard. The most critical element in IC testing, however, is that ICs be compared under the same conditions and that those conditions are as close as possible to the final implementation. Emissions varied here by 5-8 dB depending on the configuration of the PCB. While the decoupling strategy, trace length, and other parameters contributed to this difference, these same parameters will influence how effectively energy associated with the IC will couple to nearby antennas and cause radiated emissions. Similarly, while we found that performing measurements with a fast-edge clock may completely obscure the emissions from the IC, these emissions are still critical to EMI performance in the final application. If a fast-edge clock will be used, then it probably does not matter which IC is selected, since the emissions are primarily from the clock. While this test failed its goal of measuring emissions from the IC (not the input clock), it succeeded in predicting that the IC did not matter in this case. Similar arguments can be made regarding the software and the use of I/O (e.g. a "low-emissions" 8051 that inhibits ALE only has significantly lower emissions if there is no external memory). If these parameters are carefully controlled, the TEM cell test can allow the engineer to extract important comparative information about ICs and their *potential* to cause emissions in the final product. If they are not well controlled, even within the bounds of the IEC standard, the results of the test should be used only with care.

REFERENCES

[1] SAE J1752/3 Measurement of Radiated Emissions from Integrated Circuits- TEM/Wideband TEM (GTEM) Cell Method; TEM Cell (150 kHz to 1 GHz), Wideband TEM Cell (150 kHz to 8 GHz), Jan 2003.

[2] IEC 61967-1, Ed.1, "Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 1: General conditions and definitions," *First edition, Jul. 2001*.

[3] IEC 61967-2, Ed.1, "Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 2: Measurement of radiated emissions, TEM-cell and wideband TEM-cell method," *First edition, Aug. 2002*.

[4] http://atmel.com/dyn/resources/prod_documents/doc4180.pdf, Data sheet of Atmel AT89C51RB2 microcontroller, Oct 2006.

[5] http://www.standardics.nxp.com/products/80c51/datasheet/p89v51rb2.p89v51rc2.p89v51rd2.pdf, Data sheet of P89V51RB2 Philips microcontroller, 1 May 2007.

[6] http://www.maxim-ic.com/quick_view2.cfm/qv_pk/4078, Data sheet of Max-Dallas microcontroller DS89C430, 28 Sep. 2006.

[7] F. Fiori, F. Musolino, "Analysis of EME produced by a microcontroller operations," *Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001. Proceedings 2001, Munich, Germany, March 12-16, 2001 ACM, 2001. page(s): 341-345.*

[8] K. Slattery, J. Muccioli, T. North, "Measuring the radiated emissions from a family of microprocessors using a 1-GHz TEM cell," *IEEE Tran. Electromagnetic Compatibility, Vol. 41, No. 2, May 1999, pp. 146 –152.*

[9] Vijay Kasturi "The influence of printed circuit board design on TEM cell measurements," *Master's Thesis, University of Missouri Rolla, 13 Nov. 2007.*

[10] T. Hubing, J. Drewniak, T. Van Doren, and D. Hockanson, "Power Bus Decoupling on Multilayer Printed Circuit Boards," IEEE Transactions on Electromagnetic Compatibility, Vol. 37, No. 2, pp. 155-166, May 1995.

[11] M.P. Robinson, T.M. Benson, C. Christopoulos, J.F. Dawson, M.D. Ganley, A.C. Marvin, S.J. Porter, D.W.P. Thomas, J.D. Turner, "Effect of logic family on radiated emissions from digital circuits," *IEEE Tran. Electromagnetic Compatibility, vol. 40, no. 3, Aug. 1998, pp.288 –293.*

[12] K. Hu, H. Weng; D. Beetner, D. Pommerenke, J. Drewniak, K. Lavery, J. Whiles, "Application of chip-level EMC in automotive product design," 2006 IEEE Symposium on Electromagentic Compatibility Volume 3,14-18 Aug. 2006 Page(s):842 – 848.