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Distributed Control of Hybrid Motor Drives

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***Abstract* - The hybrid inverter motor drive with two cascaded multilevel inverters is an attractive option for naval ship propulsion systems due to a number of unique features. There is a natural split between a higher-voltage lower-frequency "bulk" inverter and a lower-voltage higher-frequency "conditioning" inverter in the cascaded system which matches the availability of semiconductor devices. Furthermore, the bulk inverter may be a commercial-off-the-shelf (COTS) motor drive meaning that only the conditioning inverter needs be custom made. However, a drive involving a COTS bulk inverter would require a distributed conditioning inverter control which works completely independent of the bulk inverter control. In this paper, a distributed control method is developed for the hybrid inverter drive with cascaded bulk and conditioning inverters. Moreover, a solution to the practical problem of instant synchronization between the two inverters is presented. Laboratory measurements on a 3.7-kW induction motor drive validate the proposed control.**

I. Introduction

The hybrid multilevel inverter has received much attention in the literature during recent years due to advantages of exceptional power quality [1-5]. The general concept of this inverter is to split the power conversion between a "bulk" inverter supplying low-frequency higher-voltage and a "conditioning" inverter supplying high-frequency low-voltage. For many systems (including Naval ship propulsion), there is a desire to distribute the control so that the bulk inverter may be commercial-off-the-shelf with its stock controller and only the conditioning inverter and control, typically an order of magnitude smaller in power, would be custom made [1]. In order for the distributed control to operate properly, the conditioning control needs to provide voltage harmonic compensation and at the same time be synchronized with the bulk inverter. This paper presents recent development of a distributed control where the harmonic compensation and synchronization issues have been thoroughly addressed. Laboratory results of the new control are included for validation.

II. The Hybrid Inverter; Topology and Modulation

Figure 1 shows the topology of the hybrid inverter drive formed by cascading two three-level inverters. Therein, a three-level "bulk" inverter supplies the motor load from the dc source v_{dc}. The neutral point of the machine is opened and the other end of each phase is connected to three-level "conditioning" inverter. This topology has been extensively studied in the literature and previous research has shown that this inverter is capable of operating at maximal distension with nine-level inverter performance if the voltage ratio is set to $v_{dc} = 3v_{dcx}$ [1,4]. For applications such as naval propulsion where only one source is available, the "conditioning" inverter dc source v_{dcx} is supplied by a capacitor bank and its voltage can be regulated using redundant states selection

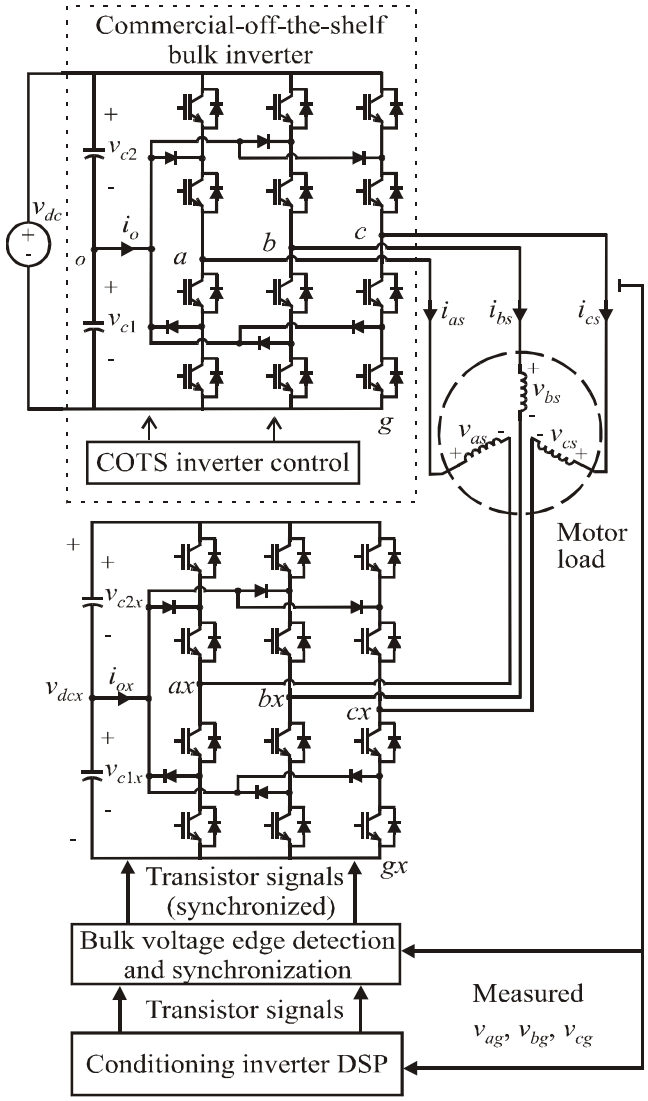

Figure 1. The hybrid multilevel inverter with distributed controller.

(RSS) control [1]. Referring to Figure 1, the line-to-ground voltages of the bulk and conditioning inverter may be expressed as

$$\begin{bmatrix} v_{ag} & v_{bg} & v_{cg} \end{bmatrix}^{\mathrm{T}} = \begin{bmatrix} s_a & s_b & s_c \end{bmatrix}^{\mathrm{T}} \frac{v_{dc}}{2}$$
$$\begin{bmatrix} v_{agx} & v_{bgx} & v_{cgx} \end{bmatrix}^{\mathrm{T}} = \begin{bmatrix} s_{ax} & s_{bx} & s_{cx} \end{bmatrix}^{\mathrm{T}} \frac{v_{dcx}}{2} \quad (1)$$

where (s_a, s_b, s_c)and (s_{ax}, s_{bx}, s_{cx}) are the switching states of bulk inverter and the conditioning inverter. For three-level inverters, the switching states have the option of 0, 1 or 2. Equations (1) are based on the assumption that the capacitors of the bulk and conditioning inverters are regulated to their ideal values [1]. The phase voltages of the load can be expressed in terms of the line-to-ground voltages as [1].

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} - \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{agx} \\ v_{bgx} \\ v_{cgx} \end{bmatrix} \quad (2)$$

The load voltages can be plotted in the *q-d* stationary reference frame for all possible switching states of both the bulk and conditioning inverter resulting in the vector plot shown in Figure 2. The heavily dotted vectors form a 3-level pattern which represents bulk inverter switching states. These will be referred to as "bulk vectors" herein. Each bulk vector is the origin of a smaller 3-level sub-hexagon as marked by dotted line and each vector dot in the sub-hexagon represents one or more switching states of the conditioning inverter. Every dot in the vector plot can be further decomposed into the switching states of the bulk and conditioning inverter. First, each vector dot can be affiliated with a sub-hexagon; the origin of which is it's bulk inverter switching states. For example, in Figure 3 (the zoomed in view of the shaded sub-hexagon in the Figure 2), the vector v_3 can be regarded as the addition of the bulk vector 220 and its conditioning inverter vector with the switching states (210). The conditioning inverter switching states are vector v_3 projections onto the reversed *ax-bx-cx* coordinates (shown as *-ax*, *-bx* and *–cx* axis in Figure 3) with the bulk vector 220 as the origin. The reversed coordinates are used here for convenience since the conditioning inverters phase-to-ground voltages have negative contributions to the load phase voltage according to (2).

In previous research, modulation methods were introduced which take into account the switching states of the bulk and conditioning inverter simultaneously. One example is the space vector modulation (SVM) method [3,4]. Using this modulation method, the nearest vectors to the reference vector are selected and the switching sequence and timing are determined in the vector domain. This method relies on geometric relationships which can be cumbersome.

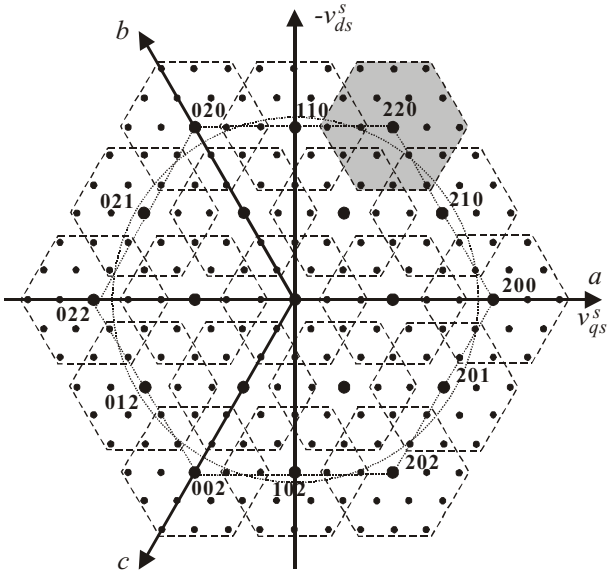

Figure 2. Cascade-3/3 vector plot for DC ratio 1:3.

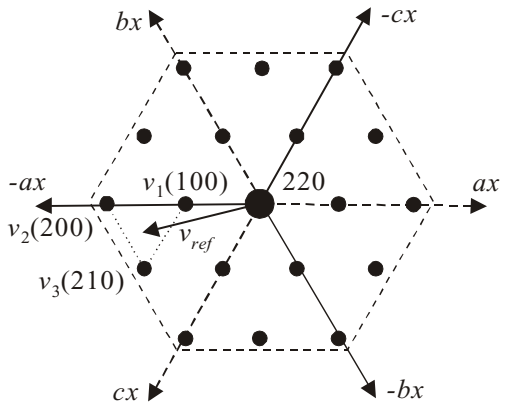

Figure 3. Reversed *ax-bx-cx* coordinates for conditioning inverter switching states.

However, recent research has simplified the SVM method [6-8]. An alternate method is natural sampling which is performed on a per-phase basis in the time domain. This method was recently simplified for programming multilevel modulation in a DSP control [9]. By combining this method with RSS switching, the capacitor voltages can be regulated and the inverter can operate from one voltage source as a seven-level inverter [1].

In this paper, a new distributed modulation is proposed. Using this method, the bulk inverter operates by staircase control (block switching) at the fundamental frequency. The control of the conditioning inverter is independently based on real-time harmonic computation and it operates as an active filter. The resulting load voltage output is equivalent to those created by other two modulation methods. The details of this method will be described in detail in the next section.

III. Distributed Control of the Hybrid Iinverter

The bulk inverter is a commercially available medium-voltage three-level motor drive controlled with its built-in

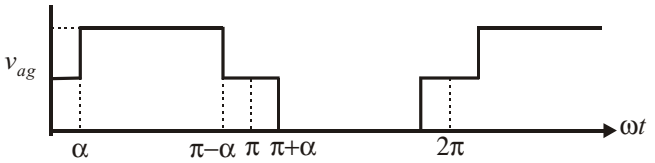

Figure 4. Bulk inverter *a*-phase line-to-ground voltage.

staircase switching. The line-to-ground voltage output is shown in Figure 4 for the *a*-phase. The fundamental component can be adjusted by changing the delay angle α. From Fourier expansion, this is

$$|v_{as}| = \frac{2v_{dc}}{\pi}\cos(\alpha) \tag{3}$$

Although the bulk inverter output has negligible switching losses, large low-frequency harmonics are produced. The conditioning inverter can correct these harmonics by sensing the bulk line-to-ground voltages and computing the required synchronized PWM signals for compensation. The control algorithm used by conditioning inverter is to be introduced in sub-section *A* below. The conditioning control also regulates the dc voltage v_{dcx} through an additional PI term which adjusts the commanded average power flow into the conditioning inverter. In sub-section *B*, the edge detection of the bulk line-to-ground voltages and synchronizing logic is described. Here, the major practical issues in the synchronization are presented and analyzed. The solution to this problem greatly improves the controller performance.

It is insightful to note that the bulk inverter staircase modulation at high modulation index (low α angle) follows the counter clockwise hexagon vector path (as indicated in Figure 2 by dotted line) traversing all the bulk vectors in the perimeter of the three-level hexagon of the bulk inverter. In the proposed hybrid modulation, the combined output voltage command is exactly the fundamental component of bulk inverter voltage and it's circular vector path is also plotted with dotted line in Figure 2. It can be seen from the vector plot that when the bulk inverter switching state is at any bulk vector, the reference (circular locus) is always within a sub-hexagon that originates from the bulk vector. Therefore, it's always possible for the conditioning inverter to synthesize the desired locus of commanded vectors with PWM switching.

In order to determine the switching states and duty cycles of the conditioning inverter for any reference vector along the circular path, the nearest vectors must be located. As an example, the reference v_{ref} in Figure 3 changes to the new origin of bulk vector 220. Then to synthesize the new vector inside the sub-hexagon, it requires the three nearest vectors with certain duty cycles in one PWM cycle. This can be easily accomplished using space vector modulation with non-orthogonal coordinates [6,7] or the vector in *q-d* frame can be transform into reversed *a-b-c* frame and then per-phase duty

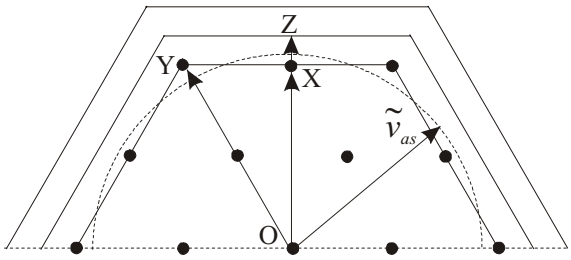

Figure 5. maximum modulation index analysis.

cycles [9] can be defined. However, the major obstacle is that the controls are distributed and the conditioning inverter controller has no information of the combined output voltage command. Before computing the PWM switching commands, it must locate the reference vector which is in phase with the bulk voltage in real-time. Before detailing this control algorithm, it is instructive to discuss the maximal achievable modulation index of hybrid inverter. In Figure 5, the circular vector path is the fundamental component for the maximum modulation index (corresponding to α=0°). As it turns out, this will yield a maximum voltage of $|v_{as}| = 0.637\,\mathrm{V}$. This peak is between the 7th and 8th level hexagon boundaries which are $OX = 0.577\,v_{dc}$ and $OY = 0.667\,v_{dc}$ respectively. This means that the resulting load waveforms will have the performance of an eight-level inverter.

A. Conditioning Inverter Voltage Control

Figure 6 shows the block diagram for the voltage control in the conditioning inverter. The first step in this control is to convert the bulk inverter line-to-ground voltages into line-to-neutral voltages using

$$\begin{bmatrix} v_{as1} \\ v_{bs1} \\ v_{cs1} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \tag{4}$$

The voltages v_{as1}, v_{bs1} and v_{cs1} represent the bulk inverter contribution to the load voltages and have the shape of load voltages of a typical six-step inverter. These voltages are then heavily filtered so that the resulting terms $\tilde{v}_{as1}$, $\tilde{v}_{bs1}$ and $\tilde{v}_{cs1}$ will be sinusoidal and used for synchronous reference frame transformation. In particular, the transformation terms can be calculated by dividing out the magnitude of the filter voltages using

$$\cos(\theta_e) = \sqrt{\frac{3}{2}}\frac{\tilde{v}_{as1}}{\sqrt{\tilde{v}_{as1}^2 + \tilde{v}_{bs1}^2 + \tilde{v}_{cs1}^2}} \tag{5}$$

$$\sin(\theta_e) = \sqrt{\frac{1}{2}}\frac{\tilde{v}_{cs1} - \tilde{v}_{bs1}}{\sqrt{\tilde{v}_{as1}^2 + \tilde{v}_{bs1}^2 + \tilde{v}_{cs1}^2}} \tag{6}$$

These terms can be used to transform the line-to-ground voltages to the q-d synchronous reference frame. Notice that

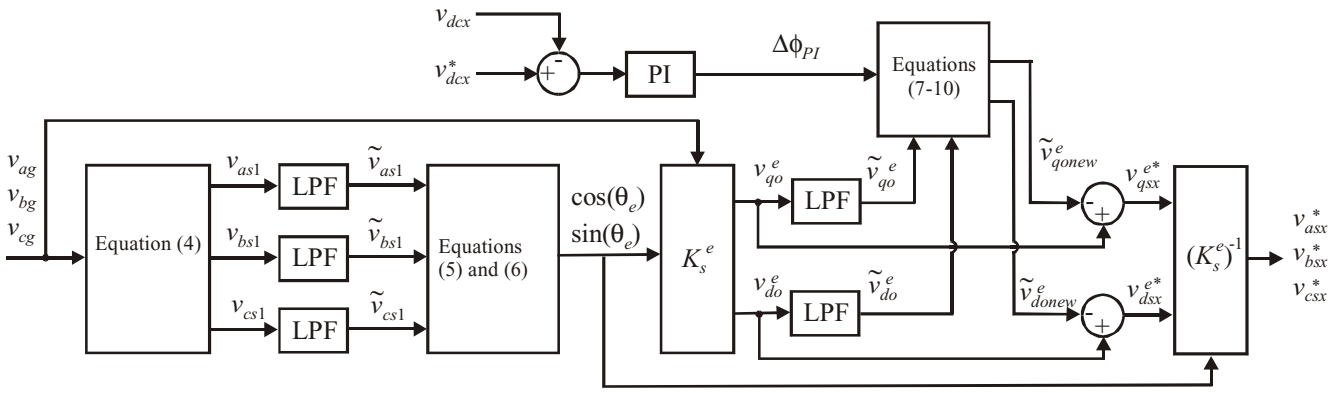

Figure 6. Conditioning inverter voltage controller block diagram.

this is equivalent to transforming the line-to-neutral voltages v_{as1}, v_{bs1}, and v_{cs1} to the synchronous reference frame where they would ideally be dc values. Thus by low-pass filtering (LPF) v^e_{qo} and v^e_{do}, the resulting voltages $v^{\sim e}_{qo}$ and $v^{\sim e}_{do}$ will be ideal (or commanded) values. Note that there will be no attenuation associated with the LPF since the fundamental component is dc in the *q*-*d* reference frame. Next, the commanded conditioning inverter *q*- and *d*-axis synchronous reference frame voltages can be determined by subtracting $v^{\sim e}_{qo}$ and $v^{\sim e}_{do}$ from v^e_{qo} and v^e_{do}. Before this is done, a PI term needs to be added for regulation of the capacitor voltage v_{dcx} (which will be described in detail below). The output of this control is a new set of voltages $\tilde{v}^e_{qo,new}$ and $\tilde{v}^e_{do,new}$ which are subtracted from $v^{\sim e}_{qo}$ and $v^{\sim e}_{do}$. The results can then be transformed back to *a*-*b*-*c* yielding commanded per-phase voltages which will compensate the harmonics from the bulk inverter output. The PWM duty cycles are created using these voltages according to the modulation method described in [9]. Note that the same reference frame transform terms in (5) and (6) are used for the inverse transformation. In this way, the commanded voltages for the conditioning inverter will be in phase with the bulk staircase voltage output, even though a phase delay was introduced by the LPF blocks that formulated the transformation terms.

The vector plot of Figure 7 will be used to gain a more insightful look at the operation of the hybrid modulation control. This plot is the same shaded sub-hexagon in Figure 2, when the bulk inverter stays at the switching states 220. The dotted curve represents the circular vector path taken by the fundamental voltage of the bulk inverter. In each DSP cycle, a certain vector in the circular path (such as v_{ref}) and its projections onto *q*- and *d*-axis in the sub-hexagon will be computed as v^{e*}_{qsx} and $-v^{e*}_{dsx}$ by the algorithm just introduced. Obviously, the origin of v_{ref} is now at vector 220 and for the conditioning inverter, it's switching states and duty cycles within a DSP clock cycle can be determined by first converting the v^{e*}_{qsx} and $-v^{e*}_{dsx}$ into the reversed *a*-*b*-*c* coordinates, then using either space vector modulation or its equivalent per-phase duty cycle modulation [9] to find three nearest vectors in the sub-hexagon which can synthesize v_{ref}.

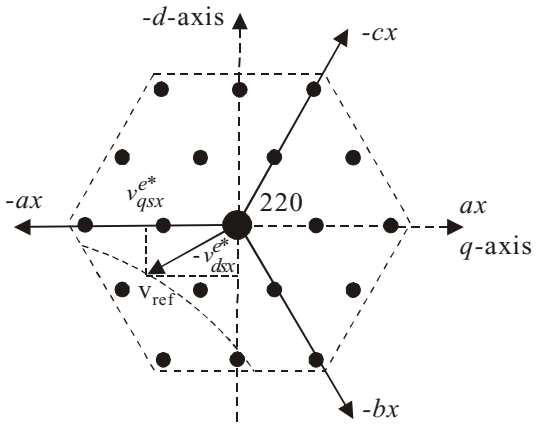

Figure 7. Conditioning inverter reference.

Figure 8 is a graphical representation of the function of the PI control which balances v_{dcx}. Therein, vectors corresponding to the load voltage and current are shown as rotating vectors along with the synchronous reference frame. The effective voltage magnitude and angle from the bulk inverter are first determined using.

$$\left|\hat{v}^e_{qdo}\right| = \sqrt{\left(\tilde{v}^e_{qo}\right)^2 + \left(\tilde{v}^e_{qo}\right)^2} \tag{7}$$

$$\phi_v = \tan^{-1}\left(\frac{-\tilde{v}^e_{do}}{\tilde{v}^e_{qo}}\right) \tag{8}$$

Next, the PI regulator term is added to adjust the voltage angle

$$\phi_{v,new} = \phi_v + \Delta\phi_{PI} \tag{9}$$

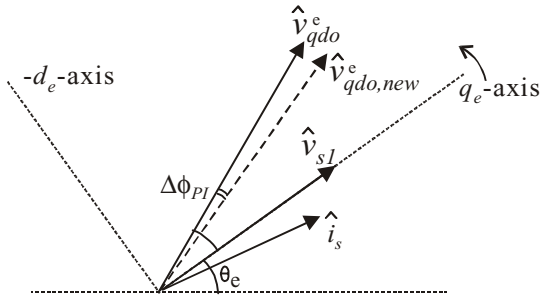

Figure 8. Phasors in synchronous *q-d* frame.

Finally, the *q-d* terms are recombined to form new *q-* and *d-*axis voltages (with the same magnitude but with an altered angle) using,

$$\tilde{v}^{e}_{qo,new} = \left|\hat{v}^{e}_{qdo}\right|\cos\left(\phi_{v,new}\right) \tag{10}$$

$$\tilde{v}^{e}_{do,new} = -\left|\hat{v}^{e}_{qdo}\right|\sin\left(\phi_{v,new}\right) \tag{11}$$

Altering the phase angle as in (9) has the following effect. When the commanded voltage vector $\hat{v}^{e}_{qdo,new}$ is adjusted to slightly lag the bulk inverter fundamental $\hat{v}^{e}_{qdo}$ by $\Delta\phi_{PI}$, the angle between $\hat{v}^{e}_{qdo,new}$ and current vector $\hat{i}_s$ is decreased. Therefore, more real power is commanded from the conditioning inverter than is necessary and the average power flow from the conditioning inverter becomes positive since it not only compensates the harmonics in the bulk inverter output (a process which has zero net power flow) it also attempts to provide the difference between the commanded real power and the real power from the bulk inverter. This tends to discharge the conditioning inverter capacitor bank since it has no dc source. When $\hat{v}^{e}_{qdo,new}$ slightly leads $\hat{v}^{e}_{qdo}$, the commanded load power is less than that provided by the bulk inverter. Hence, the resulting PWM command of the conditioning inverter tends to absorb the extra real power, and charges its capacitor bank. It is also possible to regulate the capacitor by adjusting the magnitude instead of the phase angle of $\hat{v}^{e}_{qdo,new}$ to direct more or less average power flow into and out of the conditioning inverter. Both methods have been verified in simulation and experiment and the phase angle control was proven to be more effective and used in the final prototype.

B. Conditioning Control Synchronization

The above described control and PWM is computed at every clock cycle of the DSP and cannot instantaneously compute the gate signals. In practice, there's always one DSP cycle delay between the bulk output and conditioning inverter

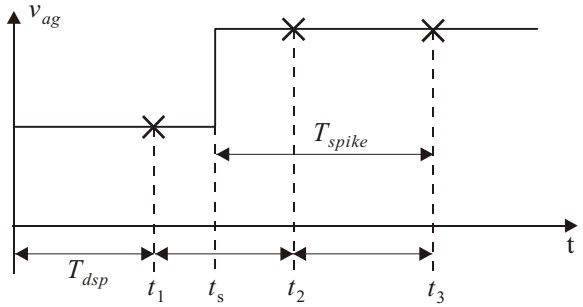

Figure 9. Un-synchronization due to DSP computation delay.

output. While this effect is negligible for most of a fundamental cycle, it poses serious un-synchronization problems at the point where one phase of the bulk inverter voltage steps up or down. The delay time in this case will be between one and two DSP cycles as designated by T_{spike} in Figure 9**.** Therein, the *a*-phase bulk line-to-ground voltage is shown at a time when it steps from the mid-point to the full dc voltage. First, the bulk voltage steps up at time t_s, which is a random position in the middle of a DSP cycle and the time between t_s and the end of the current DSP cycle t_2 is a random number between 0 and a full DSP cycle T_{dsp} (between 0 and 100μs for 10kHz sample period). The other part of the delay is one fixed DSP cycle (100μs) starting from t_2. In this cycle, the DSP samples the new bulk voltage and computes the correct conditioning inverter transistor signals and latches them to be output to the inverter gates in the next DSP cycle starting at t_3.

During T_{spike}, the sudden step up (or down as the case may be) of the bulk inverter voltage at one phase needs to be instantly compensated by synchronized three phase conditioning inverter output; otherwise the per-phase load voltage will have a significant leap to an erroneous value. This problem is analyzed in Figure 10 which is a zoomed-in look at the two neighboring sub-hexagons centering at the bulk vectors 220 and 120. The highlighted triangle region is their overlapped area. The labels in the overlap region are the conditioning inverter switching states of the vectors

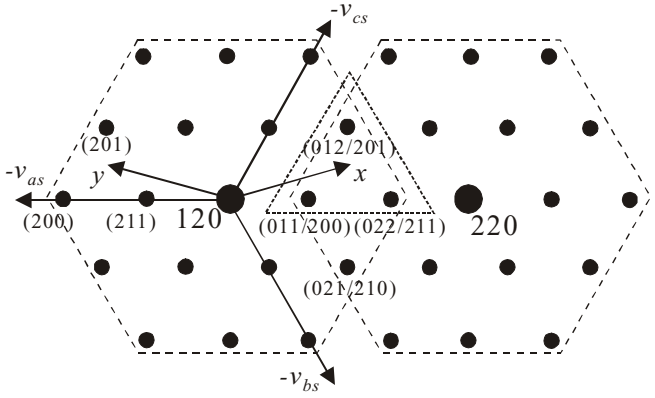

Figure 10. Visualization of un-synchronization problem and the solution.

belonging to both sub-hexagons. It also represents the vector's projection onto the reversed *a*-b-c coordinates in each sub-hexagon as introduced previously. When the reference vector "*x*" of the combined output is inside the triangle, it is synthesized by commanding the bulk inverter at the state 220 and conditioning inverter at the switching states (201), (211), and (200) separately for each vector in the triangle. Then suddenly, the bulk inverter voltage vector jumps to the state 120 (i.e. the voltage v_{ag} steps down from the top voltage level down to the mid-point. Then with the bulk vector 120 as the new origin, the conditioning inverter should use the new set of switching states of (012) ,(022), and (011) to synthesize the combined output vector "*x*". However, during the time T_{spike} following this transition, the new switching states and their switching time is not yet computed and the old states (201), (211) and (200) are still being used. The combined output vector thus created is labeled as "*y*". Obviously, the resulting output vector has a large discrete leap here to an erroneous position which amounts to a large voltage spike with considerable time duration of T_{spike} in the phase voltage of the load. Therefore, the problem is to find the correct switching states immediately following the bulk transition without DSP calculation. The solution lies in the same Figure. For the vectors of the overlapped triangles that originated from bulk vector 220, their *a*-phase conditioning inverter switching states are purely at level 2. For the same set of vectors originated from bulk vector 120, their *a*-phase switching states are all level 0. So immediately after the v_{ag} step down from the state 2 to 1, the correct conditioning inverter switching states must change from all 2 to all 0 in phase *a*. Using a similar argument, the *b*-, *c*- phases need to be increased by one level from those that existed before the bulk step-down occurred. Similar logic can be applied to the other overlapped regions where the bulk voltage step (up or down) occurs in any phase. The solution is summarized for the *a*-phase logic in the flow chart shown in Figure 11.

The discovery above makes instant synchronization between bulk and conditioning inverter possible and practical. Since immediately after the bulk inverter edge, the

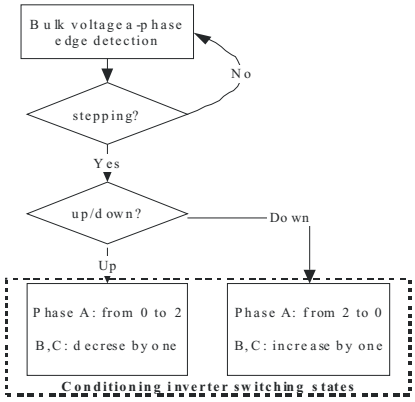

Figure 11. Flow chart of the edge detection synchronization.

conditioning inverter switching states and transistor signals require no DSP calculation and can be programmed into FPGA firmware. Here the only delays of the conditioning inverter output are the propagation delay of FPGA (in the order of nanoseconds) and the dead-time delay in the conditioning inverter PWM which is inherent and not avoidable in the distributed control. However, it will be shown from the lab results that the effect of dead-time can be handily filtered out at the load.

A block diagram of the implementation is presented in Figure 12. At the input side, there is a voltage sensor and edge detection circuitry constructed in hardware. Whenever the bulk inverter output steps, the edge detection circuit outputs digital flags to disable the gate signal output from the DSP and replace them with (correct) signals programmed in firmware. At the same time, the DSP is interrupted and a new cycle is initiated to calculate the conditioning inverter output with the updated bulk inverter voltages. After this new cycle, the edge handling logic will enable the DSP gate signal output again until the occurrence of the next bulk edge.

IV. Laboratory Validation

The bulk and conditioning inverters were constructed in the laboratory for validation of the proposed control. The bulk inverter is controlled by a Cypress CY37128P84 CPLD

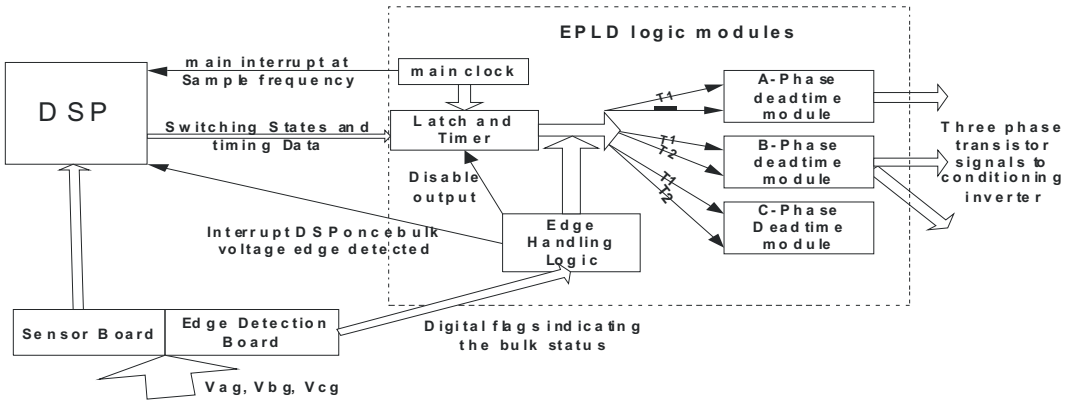

Figure 12. The hardware implementation block diagram.

with staircase modulation. A TI TMS320C32 DSP and Flek-10K EPLD were used for the conditioning inverter control.

For the studies presented herein, the bulk inverter dc voltage applied was 320V. The bulk commanded frequency is 60Hz and the firing angle was set to α=18°. This will produce a peak fundamental phase voltage of 194V according to (1). A 4-pole 3.7-kW induction machine with parameters listed in Table I was used as the load to test the prototype inverter. The induction machine was operated at 186.9-rad/s with an output torque of 20.9-N·m resulting in an output power of 3.9-kW.

Table I. Induction machine parameters.	
$poles = 4$	$M = 64.4\,\text{mH}$
$r_s = 0.4\,\Omega$	$L_{ls} = 5.73\,\text{mH}$
$r_r' = 0.227\,\Omega$	$L_{lr}' = 4.64\,\text{mH}$

Figure 13 shows the laboratory measurements. The first two traces show the bulk and conditioning inverter *a*-phase line-to-ground voltages v_{ag} and v_{agx}. These depict the split between the higher-voltage low-frequency bulk inverter and the lower-voltage high-frequency conditioning inverter. The effect of the conditioning PWM is to compensate the bulk inverter harmonics. To illustrate this, a small PWM filter with a cut-off frequency of 1-kHz was used in the experiment as shown in Figure 14. The resulting filtered voltage v_{asf} was applied to the induction motor and is shown as the fourth trace in Figure 13. As can be seen, the filtered voltage is very smooth. Although the edge detection circuit and EPLD synchronize with the bulk inverter, the transistor dead-time results in some voltage spikes as seen in v_{as}. The dead-time in this circuit was set to 3μs, but the PWM filter also completely removes these spikes. The next trace is the effective line-to-line voltage v_{ab} which is the difference of v_{as} and v_{bs}. This is shown for comparison to a typical multilevel inverter. In this case, the hybrid inverter is operating with eight effective levels. Therefore, the line-to-line voltage will have fifteen distinct levels (seven positive, seven negative, and zero). The fifteen levels can be seen in the v_{ab} waveform. The last two traces are the *a*-phase motor current i_{asf} and the conditioning inverter capacitor voltage v_{dcx}. The capacitor voltage v_{dcx} is well regulated at one-third of the bulk voltage by the PI control and the voltage ripple is very small. The THD values are listed in Table II.

Table II. Measured THD values.	
$THD(v_{as}) = 12.2\%$	$THD(v_{asf}) = 5.5\%$
$THD(v_{ab}) = 11.8\%$	$THD(i_{asf}) = 5.3\%$

The THD of v_{as} and v_{ab} would typically be around 9% for the hybrid inverter [9]. However, they are increased in the

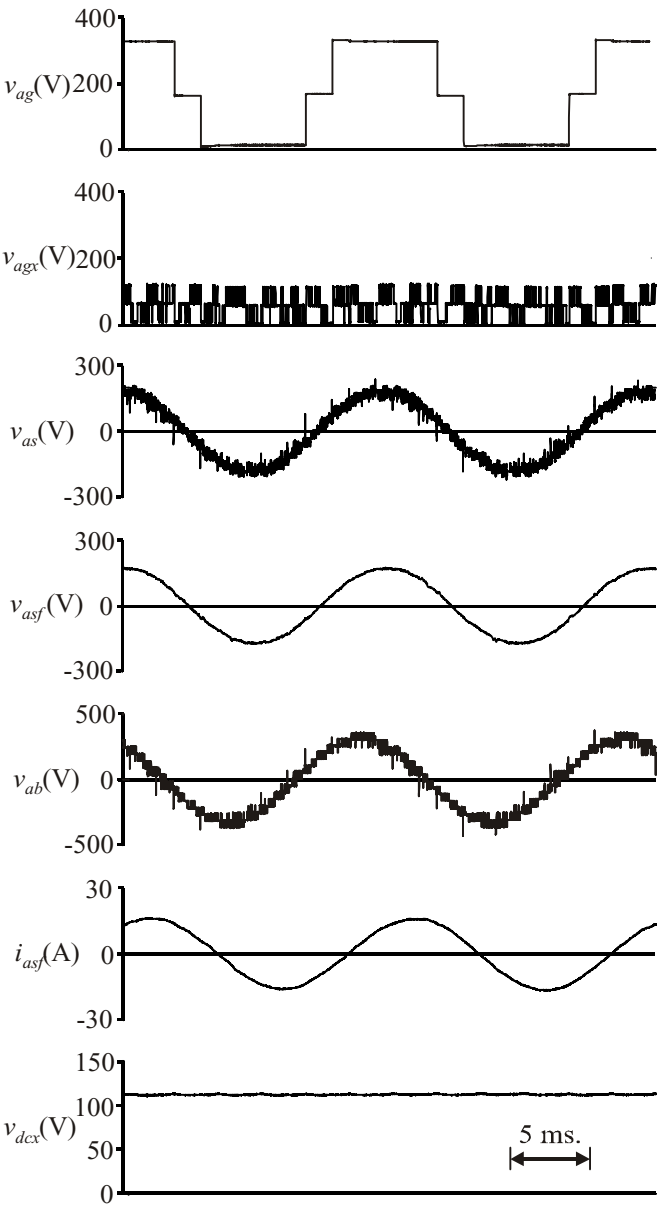

Figure 13. Distributed control laboratory measurements.

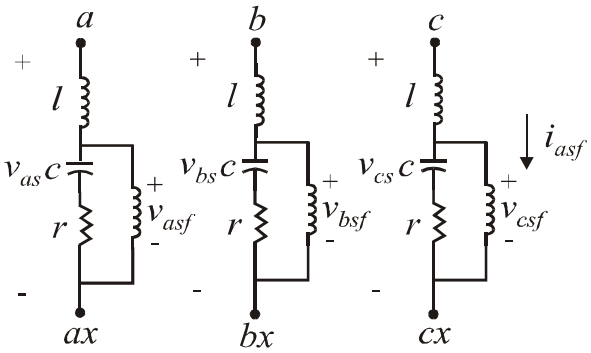

Figure 14. The RLC PWM filter.

distributed control since the conditioning inverter output has a one DSP cycle delay from the bulk inverter output. With a filtered load voltage having a THD of about 5%, one might expect the load current THD to be much less. However, the motor tooth saturation distorts the current waveform resulting in a current THD which is around 5%.

V. CONCLUSION

This paper presented a distributed control for the hybrid inverter. The hybrid inverter is unique in that two three-level inverters are used to drive the motor load. The "bulk" inverter operates at a higher-voltage and low-frequency and provides the power to the machine. The other inverter drives the opposite end of the motor windings with a lower-voltage high-frequency PWM and serves as an active filter or "conditioning" inverter. Since two three-level inverters are used, the resulting waveforms have exceptional power quality. With the proposed distributed control, the bulk inverter can be used with its commercial-off-the-shelf controller. The conditioning inverter senses the bulk voltages in order to compensate the harmonics of the bulk inverter and also synchronize to the bulk inverter steps. This makes the conditioning inverter control independent of the bulk inverter. Furthermore, a component of the conditioning inverter control regulates it's dc voltage so that it can be supplied from a capacitor. This is useful in Naval drive applications where extra voltage sources at high power levels are difficult to create. The proposed control was validated in the laboratory as a 3.7-kW induction motor drive.

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