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The PCB level ESD immunity study by using 3 Dimension ESD Scan System

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Abstract

The use of high-speed logic makes modern electronic systems highly susceptible to electrostatic discharge (ESD). Because of their wider bandwidth, faster digital devices are more susceptible to high frequency ESD transient fields. In the analysis of ESD problems, an exact knowledge of the affected PINs and Nets is essential for an optimal solution. In this paper, a three dimensional ESD scanning system which has been developed to record the ESD susceptibility map for printed circuit board is presented and the mechanisms that the ESD event couples into the digital devices is studied.

Keywords

ESD scan, induced loop voltage, Fast CMOS system, Susceptibility map

I. INTRODUCTION

The high-speed fast CMOS systems are more and more susceptible to electrostatic discharge (ESD) in recent years. The class of problems this paper intended to help solving is system ESD problems, which is also known as ESD soft-errors, such as a reset of a device after discharging to a metallic chassis. The ESD Hard-errors, typically occurring from discharges to connector PINs are excluded as they can be solved by widely known methods such as over-voltage protection.

The general description of a typical ESD soft-error problem is as follows: ESD is discharged to the outside of a system. Upon discharge, the ESD current distributes on the system. It is associated with a strong electromagnetic field that can couple through apertures, cables and slots into the enclosure. There it induces voltages and currents. These voltages or currents lead to bit-errors, wrong instructions or even a system crash. The ESD induced current pulse and involved transient fields have the rise-time in the range of 50 ps to 2ns. The spectral components of these fast pulses are similar to the bandwidth of digital devices that operate at 200 MHz or above. As a result, the interference created by ESD to devices operating in the gigahertz range is of considerable concern.

To improve the robustness of high-speed digital device to the ESD disturbance, it is important to locate the disturbed traces or PINs. In this paper, A specially designed 3D ESD susceptibility scanner is developed that allows the quantification of noise sensitivity of PCBs. Using the knowledge of sensitivity, a cost efficient design of the enclosure will be possible and the chance of product delays due to failed ESD tests will be reduced. In part II, the general ESD debug methodology is described and the 3D ESD scan system is presented in part III. As an example, an ESD susceptibility map for a digital device is shown in part IV.

II. The ESD susceptibility scanning methodology

Debugging ESD problems is not an easy task, which is mainly due to the lag of an easy relationship between applied pulse, characterized by a multitude of parameters and the system response. As each EUT (equipment under test) reacts different to each physical parameter characterizing the ESD event, it is not obvious to define a universal function, which describes the severity of ESD Intuitively. Many different physical parameters should be considered during an ESD robustness test.

- Peak Current: The peak current will determine the maximum voltage drop across a resistive load. The magnetic field near the current is also proportional to the current.
- Discharge current derivative ("smoothness of the waveform"): The current derivative determines the induced voltages.
- Voltage: The voltage determines if a dielectric barrier will break down.
- Energy: Part of the energy stored in the electrostatic field will be dissipated in electronic parts, which may cause thermal damage, parts of it will be radiated and may couple into the circuit somewhere and parts will be transformed into heat, ionized molecules etc. inside the arc.
- Transient fields: Transient fields determine the induced voltages. Their functional dependence on current, derivative, distance etc. is a complex problem.

ESD susceptibility scanning is a method to determine which line is causing a system upset during ESD or other immunity testing. To identify susceptible lines, one can subject only a small area of an electronic system such as a single board, connector, cable or line on a PCB, to transient fields of ESD event. These transient fields will couple into the part of the system and may cause an upset.

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The upset and the phenomena, which causes it, may or may not be the same as the one which has been observed during the standard ESD test. By carefully observing the system performance an educated guess is possible, if an effect, detected during susceptibility scanning is the same as the one seen in the standard test.

In ESD scanning, typically a high voltage square wave pulser is attached to a small loop and the loop is hold in proximity to the board. But it does not have to be a loop, it can be an electric antenna or one can inject a differential signal between e.g., two grounding systems like chassis and digital ground.

II. Three dimensional ESD scanning system

A three dimensional ESD scanning system has been developed to investigate the ESD immunity problem. The aim of the system is to automatically identify the ESD sensitive PINs and Nets of the EUT in non-destructive ESD failure testing. There are four main hardware components in the system.

- Three dimensional positioner
- High voltage pulse generator (transmission line pulse generator)
- Position meter and probe mounting station
- ESD debugging probes

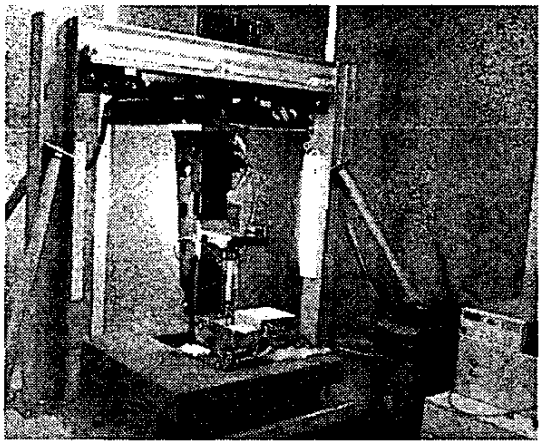

Figure 1: The three Dimensional ESD scanning system.

The ESD pulse is generated by the high voltage source and is coupled into the PCB board through different types of probes. The probe is controlled by the PC to scan over the board and the ESD failure level for each point is recorded to generate the ESD susceptibility map. Since the probe has 20 cm free travel distance in Z direction and the scan resolution is 1 um, the exact ESD sensitive traces and pins can be precisely identified. There are 5 probes used in this system to simulate different coupling process.

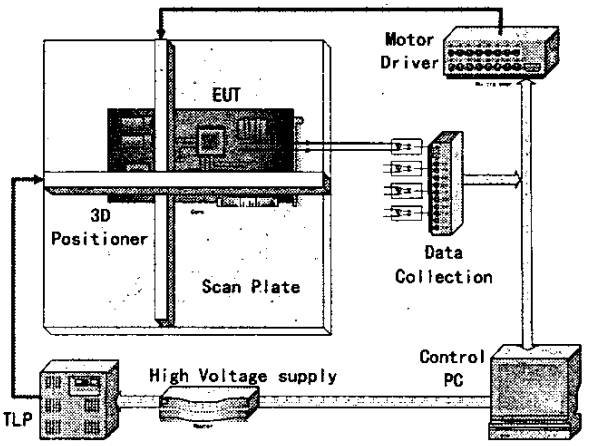

Figure 2: Diagram of the ESD scanning system.

A. Three dimensional positioner

The three dimensional positioner is a cartesian coordinate gantry system, which provide us the ability to move the ESD probes to different test points of the EUT. The positioner is made of three linear step motor traveling stations. The positioner system has 500 mm traveling capability in X and Y axis, and 200 mm in Z axis. The maximum traveling resolution is 1 um in all direction.

B. High voltage pulse generator

The high voltage pulse generator is a transmission line pulse generator, which is connected to a high voltage power supply. It provides a rectangular impulse. Its rise-time is about 200 ps. The pulse length can be changed by adjust the transmission line length and usually a few nanoseconds is sufficient for ESD debugging purpose. The maximum voltage this pulser can provide into a 50 Ohms load is 5000 V, which is the upper limit of the output of the high power supply.

C. Position meter and probe mounting station

The system also has the movement freedom in Phi direction, which allows the system to simulate different H field coupling mechanisms. A hard disk is made to a probe mounting station and a step motor is used to rotate the probes.

To move probes in Z direction, we need to know the topology information of the EUT to avoid the collision between the probes and the surface of the ESD victim board. We use a position meter automatically scan the PCB to measure the surface of the board and get the topology information. The position meter is connected to an AD converter in the PC and the topology of the PCB is generated. Then the topology map is used to move the probes in the Z direction without damaging the board.

Figure 3 shows a topology map example of a computer mother board. It is clearly to find the PCI slots, display card, memory boards and CPU fan.

D. ESD injection probes

As shown in picture 4, ESD injection probes are controlled by the PC to scan over the PCB. The high voltage pulse is applied to the probes to simulate different ESD event scenarioes.

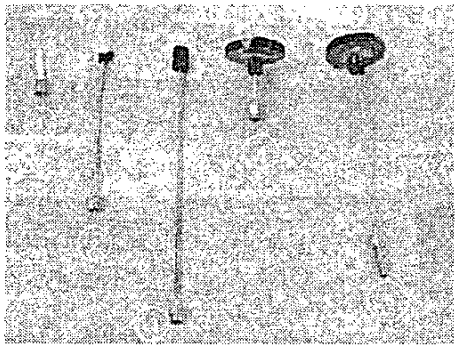

Figure 4: *Different injection probes. 1: Direct injection probe. 2: Loop probe. (Magnetic field probe) 3: E-field small area probe. 4: E-field large area probe. 5: E-field large area probe.*

H-field probes

H field probe is a small loop attached to a semi-rigid cable, which is actually a loop antenna. It simulates the transient ESD magnetic field. H-field probes with different loop antennas sizes are useful to first broadly find the area of sensitivity and later localize it using a very small loop or direct injection.

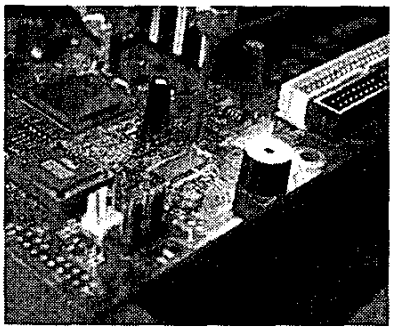

Figure 5: The H-field probe scanning the board.

E-field probes

As not only the magnetic field, but also the transient electric field may cause ESD immunity problems. To test for electric field sensitivities such a probe which is shown in figure 6 is needed. A SMA connector often works fine. Some resistance to ground is needed at its output, otherwise the transmission line will never discharge.

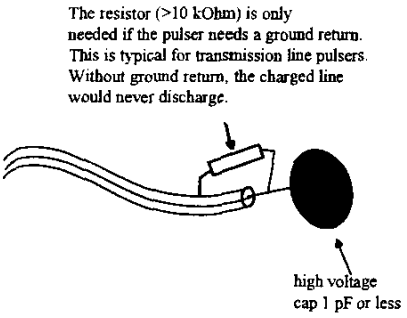

Figure 6: The E-field probe for ESD scanning.

E. ESD scanning software

The flowchart of the ESD scanning software is shown in figure 7. First, the topology map of the EUT is generated by using precision distance meter. Then ESD scanning parameters such as the type of probes, the probe orientation, the scan resolution are setup

The ESD noise comes from the high voltage transmission line pulse generator. The fast rising pulse is applied to the ESD scanning probe and the probe is moved to the surface of the EUT according to the topology map. The working status of the EUT is monitored by the software and any soft-failure of the EUT is recorded to generate the ESD susceptibility map.

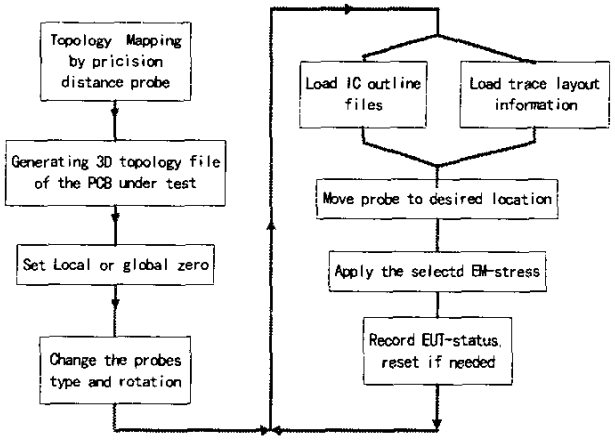

Figure 7: Flowchart of ESD scan software

IV. The ESD Susceptibility Map

The concept of field mapping is widely used for studying electromagnetic emissions from PCB. ESD Susceptibility mapping is similar to an emission map since it also gives an ESD failure level for each point on the board. However, the value on the ESD susceptibility map gives the ESD failure level that if coupled to the PCB at that point would cause the board to malfunction. Peaks in the map indicate the points where are most susceptible to the ESD event.

Figure 8 shows an ESD scanning area and figure 9 is the topology map of the area. A H-field probe is used to scan

the area to find the ESD sensitive trace of the chip that is in the center of the area. The ESD susceptibility map of the scan area is shown in figure 10.

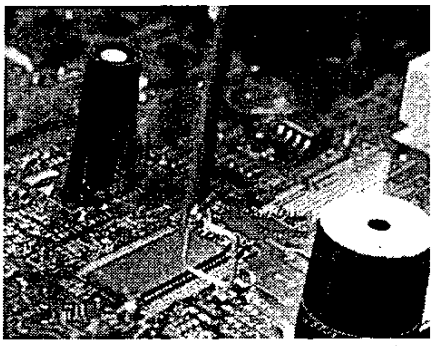

Figure 8: The ESD scanning area

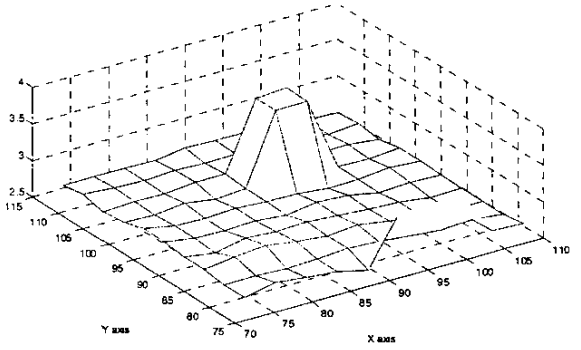

Figure 9: The topology map of the scanning area

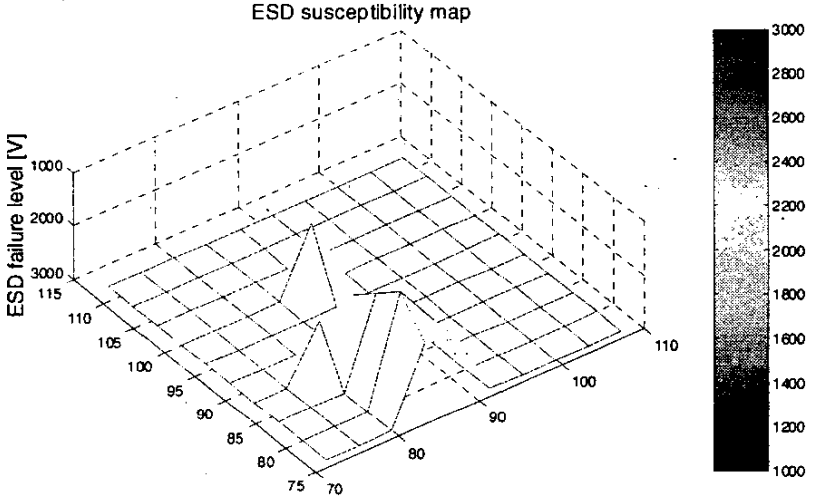

Figure 10: The ESD susceptibility map of the scanning area. Using a small H-field ESD scanning probe

Figure 3 shows the topology map of an EUT, which is a computer mother board. A small H field probe is used to scan the EUT and the ESD suscetibility map of this EUT is shown in figure 11. Each peak in the map represents the ESD sensitive area. The EMC engineer could easily find the sendtive chip or traces in this EUT by the information provided by the susceptibility map.

From our ESD debuging experience, we found that the reset and interrupt lines are more ESD sensitive. The reset and interrupt lines are not treated with the same caution since their logical state will not change often. Reset lines are often routed to many ICs, even via connectors. They react asynchronous making them very sensitive to ESD. They need to be routed with the most possible care.

Conclusion

A three dimensional ESD scan system is developed to test the ESD sensitivity for digital devices. ESD susceptibility maps are recorded for different type of pulse excitations and coupling mechanisms.

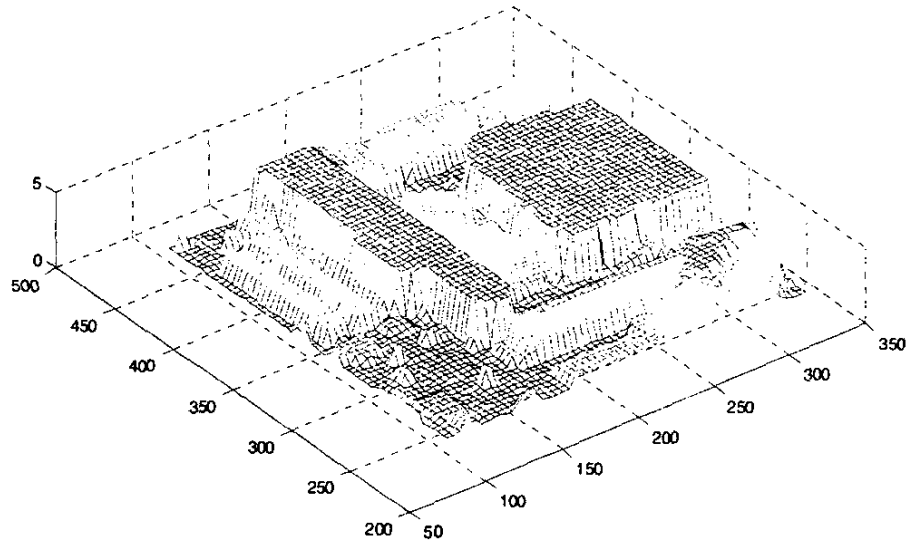

Figure 3: The Topology map of an EUT, a computer mother board.

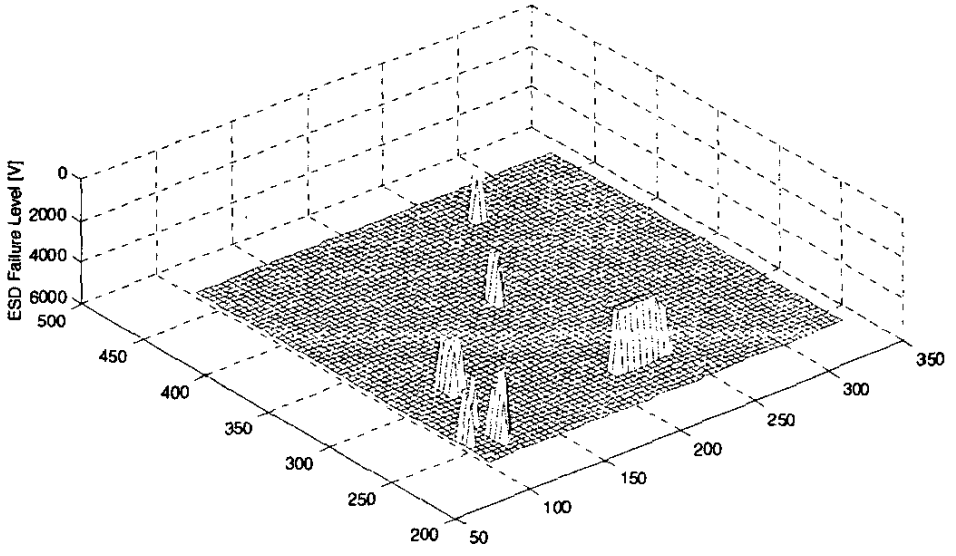

Figure 11: The ESD susceptibility map of the EUT. Using a small H-field ESD scanning probe

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