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Pulse Regulation Control Technique for Flyback Converter

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***Abstract*—Pulse regulation, a fixed frequency control technique, is introduced and applied to flyback converter operating in discontinuous conduction mode (DCM). The control parameters are designed in a way that the converter operates as close as possible to the critical conduction mode. In contrast to the conventional pulsewidth modulation control scheme, the principal idea of pulse regulation is to achieve output voltage regulation using high and low-power pulses. Pulse regulation is simple, cost effective, and enjoys a fast dynamic response. The proposed technique is applicable to any converter operating in DCM. However, this work mainly focuses on flyback topology. In this paper, the main mathematical concept of the new control algorithm is introduced and simulations as well as experimental results are presented.**

***Index Terms*—Critical conduction mode (CCM), dc–dc power converters, discontinuous conduction mode (DCM), flyback converter, switch mode power supplies.**

I. Introduction

DUE to high efficiency and high power density as well as reduced costs, switched mode power supplies (SMPS) are now becoming more popular compared to the linear power supplies [1]. This topology perfectly suits off-line low-cost power supply applications due to the facts that it provides input-output isolation and the number of its semiconductor and magnetic components is less than other SMPS.

Flyback converter has been employed operating both in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) as well as critical conduction mode, i.e., at the boundary between CCM and DCM [2], [3]. Compared with CCM, critical conduction mode enjoys benefits such as zero current turn-on of the switch and zero current turn-off of the freewheeling diode. These soft switching transitions reduce the switching losses as well at the electromagnetic interference (EMI) noise [4]. Critical conduction mode has less current stress than DCM and higher current stress than CCM. Furthermore, the transfer function of the flyback converter operating in critical conduction mode is of order one; thus, the feedback compensation is less complicated than CCM. However, despite the advantageous benefits of critical conduction mode, its major drawback is the variations of the switching frequency of the converter as the output load changes.

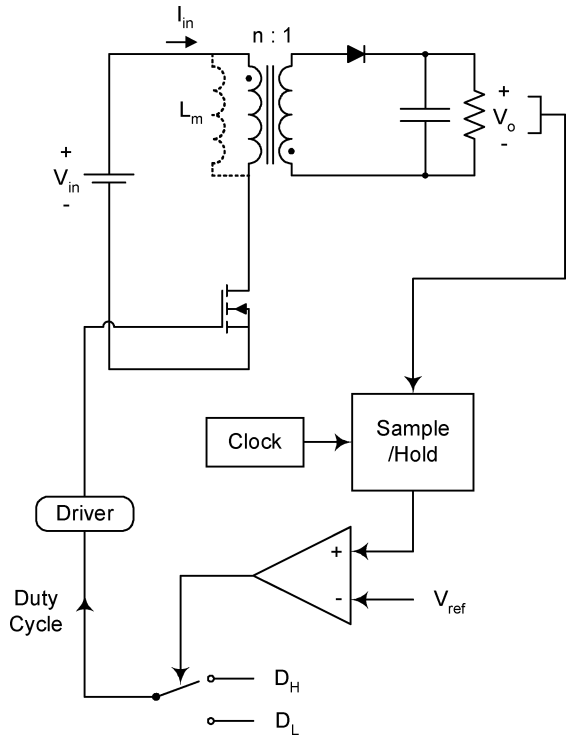

Fig. 1. Block diagram of pulse regulation control scheme.

This paper introduces pulse regulation, a fixed frequency control technique, which regulates the output voltage based on the presence and absence of high-power and low-power pulses and makes the flyback converter operate as close as possible to the critical conduction mode. This control scheme offers a faster dynamic response compared with pulsewidth modulation (PWM) control method [5]–[7]. Pulse regulation is simple, cost effective, and robust against the variations of the parameters of the converter.

In this paper, Section II introduces the basic concepts of the new control algorithm. Section III investigates the stability of the proposed control scheme. In Section IV, a comprehensive analysis of the output voltage ripple is presented. Experimental results of applying Pulse Train technique on a flyback converter are presented in Section V. Finally, Section VI draws conclusions and presents an overall evaluation of this new control technique.

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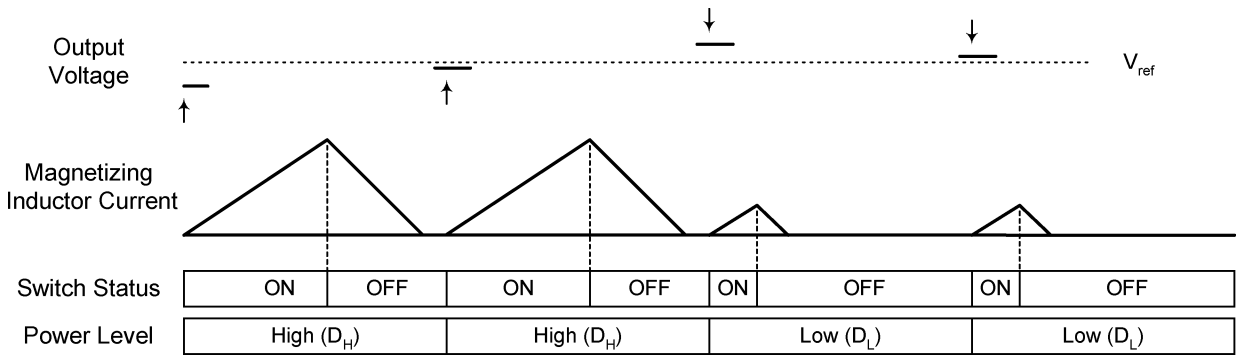

Fig. 2. High and low-power pulse cycles.

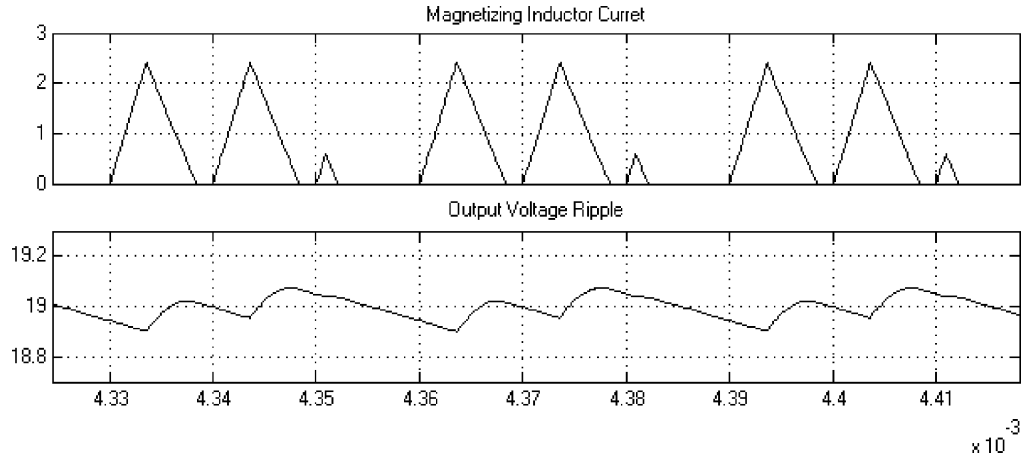

Fig. 3. Simulation results of the pulse regulation control of flyback converter; (top) magnetizing inductor current (A) and (bottom) output voltage ripple (V) versus time (s).

II. Pulse Regulation Control Scheme

Pulse regulation control algorithm achieves output voltage regulation based on generating high and low power pulses, rather than employing PWM control technique. If the output voltage is lower than the desired level, the controller chooses D_H to be the duty ratio and therefore, high-power pulses are generated sequentially until the desired voltage level is reached. On the other hand, if the output voltage is higher than the desired level, instead of generating the high-power pulses, the controller chooses D_L ($D_L < D_H$) to be the duty ratio and hence, low-power pulses are generated to descend the level of the output voltage. Fig. 1 depicts the block diagram of the pulse regulation control technique. Due to the longer on time of the switch during a high-power pulse, compared to a low-power pulse, more power will be delivered to the load. The switching frequency is constant and D_H is chosen in a way that the converter operates in DCM but as close as possible to the critical conduction mode. Critical conduction mode occurs when the input voltage is at its maximum level. k, the ratio between duty cycle of the switch in a high-power cycle D_H and duty cycle of the switch in a low-power cycle D_L, is chosen by making a compromise between the output voltage ripple and the power regulation range from full load to low load.

Considering a flyback converter, Fig. 2 depicts the current waveform of magnetizing inductance of the transformer L_m after pulse regulation is being applied. At the beginning of each switching cycle, output voltage is being sampled and based on the difference of the output voltage with the desired voltage level, pulse regulation controller decides whether a high-power or a low-power cycle needs to be generated. Since the input current ramps linearly with the on-time of the switch, the amount of energy that is drawn from the input power source in a high-power cycle is equal to

$$\Delta E_{in,HP} = \frac{(V_{\text{in}}T)^2}{2L_m} D_H^2 \tag{1}$$

while the amount of energy that is drawn from the input power source in a low-power cycle is equal to

$$\Delta E_{in,LP} = \frac{(V_{\text{in}}T)^2}{2L_m} D_L^2 = \frac{\Delta E_{in,HP}}{k^2}. \tag{2}$$

Therefore a low-power pulse transfers just $1/k^2$ time as much energy as a high-power pulse. Output voltage sampler and the driver of the switch of the converter are synchronized, therefore the switching frequency is constant and the output voltage is being sampled only once during each switching period.

Fig. 3 shows the simulation results of applying this control method on a flyback converter with parameters defined in Table I. For this specific value of the output power demand, the control scheme generates two high-power pulses and one low-power pulse in each regulation cycle. Since the input voltage is not at its maximum level, the current of the magnetizing inductor is slightly operating in DCM.

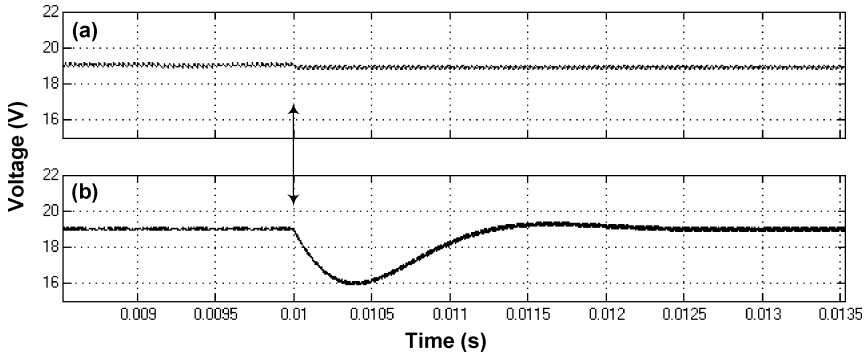

Fig. 4. Simulation results of the output voltage variation after a step load change of 30% to 65% of full-load: (a) pulse regulation and (b) PWM.

TABLE I
DEFINITION OF VARIABLES

Variable	Definition	Value
L_m	Magnetizing inductance	225 μH
C	Output filter Capacitance	100 μF
R	Load resistance	-
V_{in}	Input voltage	150 V
V_{ref}	Output voltage reference	19 V
D_H	Duty cycle of a high-power pulse	-
D_L	Duty cycle of a low power pulse	-
T	Switching period	-
k	D_H / D_L	4
n	Transformer's turn ratio	6

Pulse regulation enjoys on-line waveform analysis and, hence, fast dynamic response. Fig. 4 compares the speed of response of pulse regulation with a typical PWM control to a step load change of 30% to 65% of full load. Arrows in this figure mark the time instant at which the step change has applied. As we can observe, pulse regulation has a much faster speed of response in contrast with PWM.

III. STABILITY ANALYSIS

Considering a general switching period, as shown in Fig. 5, and based on the energy conservation rule, one can write

$$\Delta E_{\text{in}} = \Delta E_{L_m} + \Delta E_C + \Delta E_{\text{Load}} \tag{3}$$

where ΔE_{in} is the amount of energy that has been drawn from the input power source during the considered switching period. ΔE_{Lm} is the difference of the energy stored in the magnetizing inductance of the transformer and is equal to zero since L_m de-energizes at the end of each switching period. ΔE_C is the change of the energy stored in the output capacitor during the same switching period, which can be described as

$$\Delta E_C = E_{C,(n+1)T} - E_{C,nT}. \tag{4}$$

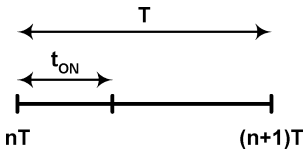

Fig. 5. General switching period.

And finally, ΔE_{Load} is the amount of energy delivered to load R during the same period. Output capacitor C provides the load current; hence, we can write

$$\Delta E_{Load} = \frac{1}{R} \cdot \int_{nT}^{(n+1)T} V_C^2 \cdot dt. \tag{5}$$

In (5), using the trapezoidal rule instead of integration, we can approximate ΔE_{Load} as

$$\Delta E_{\text{Load}} \cong \frac{T}{2R} \left(V_{C,(n+1)T}^2 + V_{C,nT}^2 \right). \tag{6}$$

Moreover, the energy stored in a capacitor at each instant is equal to the squared value of the voltage that appears across the capacitor divided by twice the value of the capacitor; hence, (6) can be rewritten as

$$\Delta E_{Load} \cong \frac{T}{RC} \left(E_{C,(n+1)T} + E_{C,nT} \right). \tag{7}$$

Substituting (4) and (7) into (3) and solving for the energy stored in the output capacitor at the end of the desired switching period, one obtains

$$E_{C,(n+1)T} = M \cdot E_{C,nT} + \frac{1}{1 + \frac{T}{RC}} \Delta E_{\text{in}} \tag{8}$$

where

$$M = \frac{1 - \frac{T}{RC}}{1 + \frac{T}{RC}} < 1. \tag{9}$$

Equation (8) shows the recursive relation of the energy stored in the output capacitor as a function of circuit parameters. In (9), M has been trivially assumed to be positive, due to the design fact that the switching period of converters is much smaller than the time constant of the output *RC* circuit. We need to note

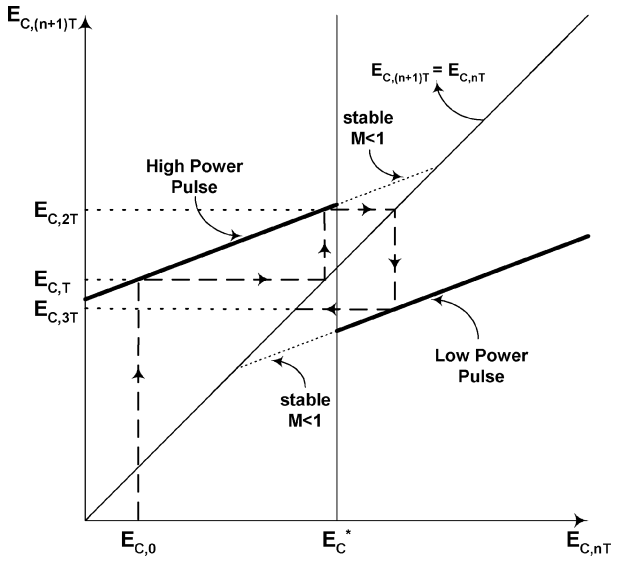

Fig. 6. Sequential evolution of high and low power pulses.

that M is always less than one; therefore, the converter is stable under any pattern of high and low-power pulses in the closed loop system. Using the input current, $\Delta E_{\rm in}$ can be described as

$$\Delta E_{\rm in} = E_{L_m,nT+t_{\rm on}} - E_{L_m,nT} \tag{10}$$

where, for a high-power pulse, we have

$$\Delta E_{\rm in,HP} = \frac{0.5V_{\rm in}^2 (D_H T)^2}{L_m} \tag{11}$$

and for a low-power pulse, we have

$$\Delta E_{\rm in,LP} = \frac{0.5V_{\rm in}^2 (D_L T)^2}{L_m} = \frac{\Delta E_{\rm in,HP}}{k^2}. \tag{12}$$

Therefore, in the closed loop control, the controller makes the decision of generating a high or low-power pulse, such that

$$\begin{aligned} V_{\rm out} < V_{\rm ref} \Rightarrow \Delta E_{\rm in} &= \frac{0.5V_{\rm in}^2 (D_H T)^2}{L_m} \quad \text{high- power pulse} \\ V_{\rm out} > V_{\rm ref} \Rightarrow \Delta E_{\rm in} &= \frac{0.5V_{\rm in}^2 (D_L T)^2}{L_m} \quad \text{low- power pulse.} \end{aligned} \tag{13}$$

An example of the time-evolution of the sequence of high and low power pulses, in a closed loop system and based on (8) and (13), is depicted in Fig. 6. In this figure, based on the initial value of the output voltage, two high-power pulses followed by a low-power pulse are generated. The closed loop system is stable under any conditions of the initial energy stored in the output capacitor. In Fig. 6, the energy level corresponding to $V_{\rm ref}$ is depicted as E_C^* and is equal to

$$E_C^* = 0.5CV_{\rm ref}^2. \tag{14}$$

IV. Output Voltage Ripple

Stability analysis does not determine the output voltage ripple. Hence, the circuit differential equations need to be solved to predict the output voltage ripple. Fig. 7 depicts the switching period of a high power cycle. The new notations that

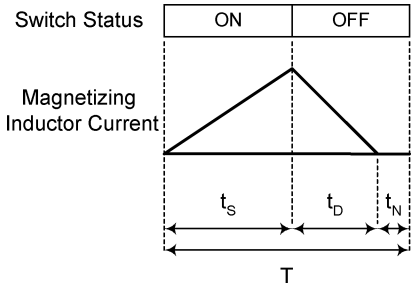

Fig. 7. Switching period of a high power cycle.

will be used are; $t_S = t_{\rm on}$ is the time period in which the switch is on, t_D is the time period during which the diode conducts and $t_N = t_{\rm off} - t_D$ the time period in which both the switch and diode are off.

During time intervals t_S and t_N, diode D is off, hence the output capacitor discharges through the load and the output voltage decreases. In a high-power cycle, assuming that the output voltage is at its desired level $V_o = V_{\rm ref}$, the changes of the output voltage can be written as

$$\Delta v_{C(-)} \cong -\frac{V_{\rm ref}}{RC}(t_S + t_N) = -\frac{V_{\rm ref}}{RC}\left(T - \frac{D_H T}{n}\frac{V_{\rm in}}{V_{\rm ref}}\right). \tag{15}$$

During time interval t_D, diode D conducts and charges the output capacitor, hence the output voltage increases. Assuming that the magnetizing current decreases linearly and the output voltage variation is small, the increase of the output voltage during on time of the diode t_D can be obtained solving the differential equation and is equal to

$$\Delta v_{C(+)} \cong A(e^{-(t_D/RC)} - 1) - \frac{n^2 R}{L_m} V_{\rm ref} t_D \tag{16}$$

where $A = V_{\rm ref} - (nRD_H T/L_m)V_{\rm in} - (n^2R^2C/L_m)V_{\rm ref}$ and $t_D = (D_H T/n)(V_{\rm in}/V_o)$.

The total changes of the output voltage after applying a high-power pulse is the summation of the above two extracted values and can be estimated as

$$\begin{aligned} &\Delta v_{C,HP} \\ &\cong \Delta v_{C(-)} + \Delta v_{C(+)} \\ &\cong \left(V_{\rm ref}\left(1 - \frac{n^2R^2C}{L_m}\right) - V_{\rm in}\frac{nRD_H T}{L_m}\right)\exp\left(-\frac{D_H T V_{\rm in}}{nRCV_o}\right) \\ &\quad + V_{\rm ref}\left(\frac{n^2R^2C}{L_m} - \frac{T}{RC} - 1\right) + V_{\rm in}\frac{D_H T}{nRC}. \end{aligned} \tag{17}$$

Equation (17) depicts how different circuit parameters involve in the generation of output voltage ripple. Fig. 8 sketches $\Delta v_{C,HP}$ as a function of the load for different values of D_H. As a high-power pulse, we expect to have positive values of $\Delta v_{C,HP}$ for the entire load range. Therefore, $D_H > 0.35$ are good choices for the value of the duty cycle in a high-power pulse. As the values of D_H decreases, the functionality of high-power pulses deteriorates and gets similar to a low-power pulse. In order to be in the DCM operating condition, the maximum value of D_H is determined by

$$D_{H,\max} \le \frac{nV_{\rm ref}}{nV_{\rm ref} + V_{in,\max}}. \tag{18}$$

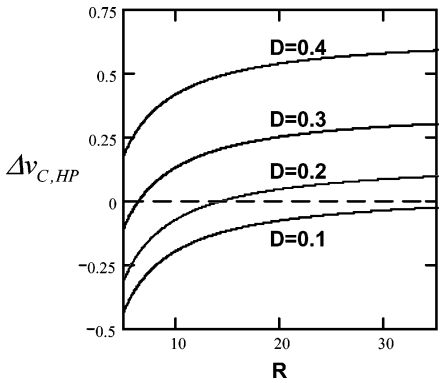

Fig. 8. $\Delta v_{C,HP}$ as a function of load for different values of D_H.

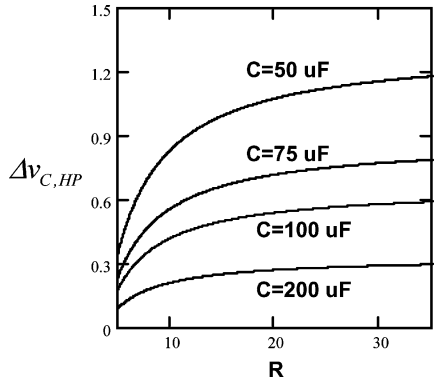

Fig. 9. $\Delta v_{C,HP}$ as a function of load for different values of output capacitor C.

Fig. 9 depicts $\Delta v_{C,HP}$ as a function of load resistance R for different values of output capacitor C. Choosing the right value of output capacitor provides the desired range of output resistance in which output voltage regulation is attainable.

Continuing the same procedure for a low-power cycle, we can easily get that the total changes of the output voltage after applying a low-power pulse is equal to

$$\Delta v_{C,LP} \cong \left(V_{\text{ref}}\left(1-\frac{n^2R^2C}{L_m}\right)-V_{\text{in}}\frac{nRD_LT}{L_m}\right) \cdot\exp\left(-\frac{D_LTV_{\text{in}}}{nRCV_o}\right)+V_{\text{ref}}\left(\frac{n^2R^2C}{L_m}-\frac{T}{RC}-1\right)+V_{\text{in}}\frac{D_LT}{nRC}. \tag{19}$$

$\Delta v_{C,HP}$ and $-\Delta v_{C,LP}$, for the parameters defined in Table I, as functions of the load resistance are sketched in Fig. 10. As we can observe, the control scheme tries to regulate the output voltage by generating the right number of high-power and low-power pulses in each regulation cycle. As the output power increases, $\Delta v_{C,HP}$ decreases; but $-\Delta v_{C,LP}$ increases. This fact implies that, in each regulation cycle at a higher output power level, the control strategy prefers to have more high-power pulses rather than low-power pulses and *vice versa* in light loads. The value of the output load resistance at which the two graphs cross each other is the value of the load, which requires one high-power pulse associated with one low-power pulse in each regulation cycle. $\Delta v_{C,HP}/-\Delta v_{C,LP}$ as a function of load resistance is shown in Fig. 11. As the value of the load increases the ratio of $\Delta v_{C,HP}/-\Delta v_{C,LP}$ increase as well. Using Figs. 10 and 11, the patterns of high and low power pulses in a regulation cycle for a specific value of the load resistance can be extracted. Table II shows some examples of this case.

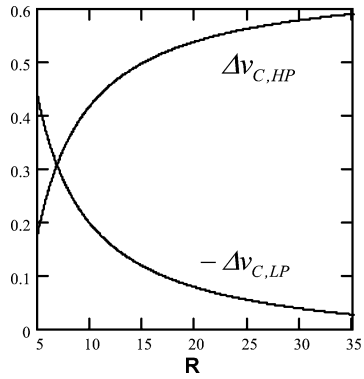

Fig. 10. $\Delta v_{C,HP}$ and $-\Delta v_{C,LP}$ as functions of load resistance.

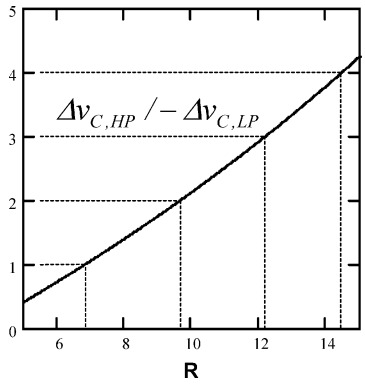

Fig. 11. $\Delta v_{C,HP}/-\Delta v_{C,LP}$ as functions of load resistance.

TABLE II
HIGH AND LOW POWER PATTERN PREDICTION IN ONE REGULATION CYCLE

R	$\Delta v_{C,HP}$	$-\Delta v_{C,LP}$	Predicted Pattern
19.3	0.533	0.082	1*HP - 7*LP - 1*HP - 6*LP
14.5	0.492	0.123	1*HP - 4*LP
12.2	0.461	0.154	1*HP - 3*LP
6.83	0.307	0.307	1*HP - 1*LP
5	0.179	0.434	3*HP - 1*LP - 2*HP - 1*LP

According to Table II, for instance, when $R = 12.2$, we have $\Delta v_{C,HP} \approx 3* - \Delta v_{C,LP}$ which predicts for this value of load, in each regulation cycle, the controller generates three low-power pulses associated with each high-power pulse. Therefore, first we calculate $\Delta v_{C,HP}$ and $-\Delta v_{C,LP}$ ((17) and (19)) associated with each value of R, then we find two integers as this equation holds

$$\alpha*\Delta v_{C,HP} = \beta* - \Delta v_{C,LP}. \tag{20}$$

Where α and β represent the number of high-power and low-power pulses in each regulation period. For any value of $\Delta v_{C,HP}$ and $-\Delta v_{C,LP}$ and with any degree of precision, we would be able to find integer numbers for α and β. However,

the regulation cycle would be very long if α and β do not have a large common multiple. Practically, this doesn't happen due to two reasons, a) the value of load is not absolutely invariant and b) a large regulation cycle can be subdivided to smaller intervals, where instead of (20), this equation $\alpha*\Delta v_{C,HP} \simeq \beta* - \Delta v_{C,LP}$ holds, as can be seen on the first and last row of Table II. In a high-power cycle, we can express the average value of the diode current as

$$\overline{i_{D,HP}} = \frac{V_{\text{in}}^2 D_H^2 T}{2nV_o L_m}. \tag{21}$$

The on time of the switch during a low-power pulse is $1/k^{th}$ of the on time of the switch in a high-power pulse and, hence, for a low-power pulse, we can write

$$\overline{i_{D,LP}} = \frac{\overline{i_{D,H}}}{k^2} = \frac{V_{\text{in}}^2 D_H^2 T}{2nV_o L_m}. \tag{22}$$

In the steady state operation, if there are α high-power pulses associated with β low-power pulses in each regulation cycle, then the average value of the diode current is

$$\overline{i_D} = \frac{\alpha * \overline{i_{D,HP}} + \beta * \overline{i_{D,LP}}}{(\alpha+\beta)T}. \tag{23}$$

By noting that $\overline{i_D} = V_o/R$ and, by solving for the load resistance, one obtains

$$R = \frac{2nL_m k^2}{D_H^2} \frac{V_o^2}{V_{\text{in}}^2} \frac{(\alpha+\beta)}{(\alpha k^2+\beta)}. \tag{24}$$

Equation (24) shows how different parameters like input voltage, output voltage, output load resistance, D_H, and k affect the pattern of high and low power pulses. This equation is being used through the design procedure.

V. Experimental Results

Using the derived formulation in the previous section, a 90-W prototype dc-dc flyback power supply with $V_{\text{in}} = 135 \sim 165$ V, $V_o = 19$ V, and switching frequency of 100 KHz was designed and developed. Using the parameters introduced in Fig. 7, we can write

$$t_D = \frac{V_{\text{in}}}{nV_O} t_S. \tag{25}$$

In order to make the converter operate as close as possible to the critical conduction mode, we need to make sure that $t_S + t_D$ is as close as possible to T, which using (25) leads to

$$D_H + \frac{V_{\text{in}}}{nV_O} D_H \leq 1. \tag{26}$$

Using (26), for the maximum value of the input voltage, gives us an upper limit for the value of D_H.

A TMS320LF2407 digital signal processor was used to implement the suggested control scheme. This DSP has integrated peripherals specifically chosen for embedded control applications. These include analog to digital (A/D) converters, timers, protection circuitry, serial communications, digital to analog (D/A) converters, and other functions. Most instructions for the F240, including multiplication and accumulation (MAC) as one instruction, are single cycle. Therefore, multiple control algorithms can be executed at high speed, thus making it possible to achieve the required high sampling rate for good dynamic response. An external circuitry, using an operational amplifier, has been utilized to bring down the level of the output voltage to the measurable range of the ADC. Duty cycle was presented by an 8-bit binary digit while the resolution of the ADC's was chosen to be 7-bit.

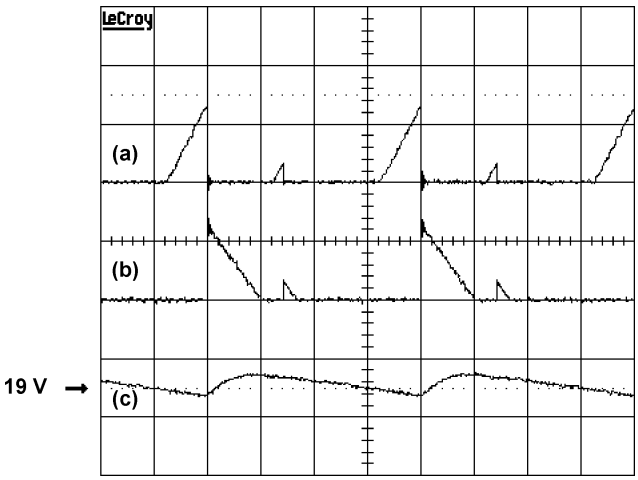

Fig. 12. Experimental results of (a) input current (2 A/div), (b) secondary current of transformer (6 A/div), and (c) output voltage ripple (0.1 V/div) versus time (5 μs/div).

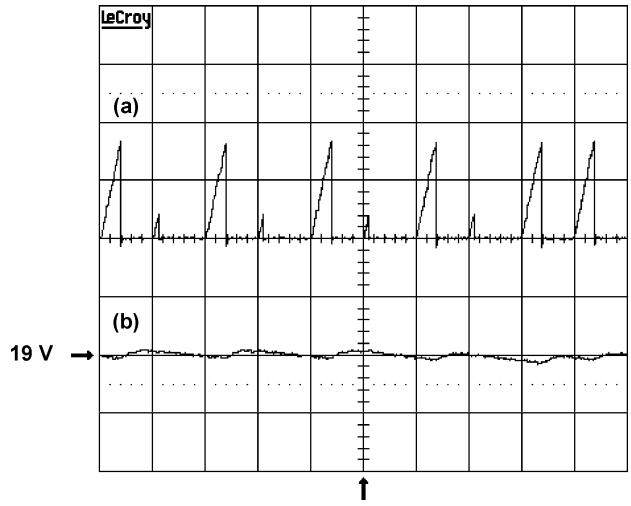

Fig. 13. Experimental results of applying a step load change; (a) input current (2 A/div) and (b) output voltage ripple (0.5 V/div) versus time (10 μs/div).

Fig. 12 depicts the experimental results of the primary and secondary currents of the transformer as well as the output voltage ripple. In this figure, a low-power pulse follows each high-power pulse. Fig. 13 depicts the experimental results of the input current and output voltage ripple for a 30% to 65% step load change. The vertical arrow specifies the instant at which the step change is applied. As we can observe, the pattern of high and low power pulses changes after the step load

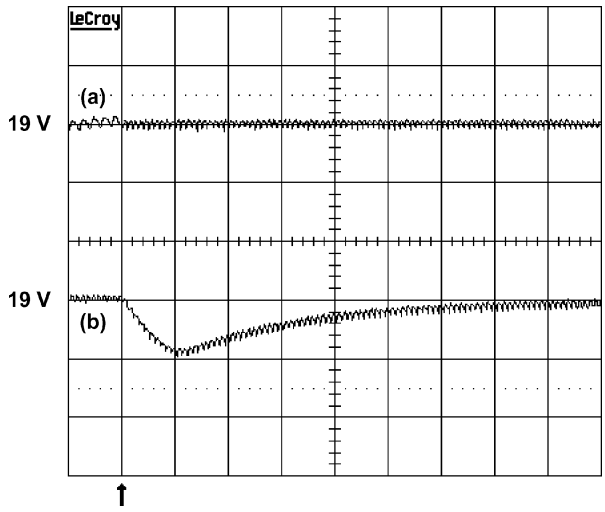

Fig. 14. Experimental results of applying a step load change: (a) pulse regulation (1 V/div) and (b) PWM controller (1 V/div) versus time (200 μs/div).

change and the density of the number of the high power pulses increase upon load demand. The transient response of pulse regulation is so fast that no disturbance at the output voltage can be observed after the load step change. Fig. 14 compares the transient response of pulse regulation with PWM control method.

VI. Conclusion

Flyback power converter has found its way into many applications. To address the challenge of designing a simple controller for this type of converters, this paper introduces the new pulse regulation control technique. This technique is mainly designed for power converters operating in DCM. Pulse regulation enjoys several advantages over conventional control techniques, such as simplicity of design and implementation, accuracy, and fast transient response. Furthermore, pulse regulation makes power converters to operate in fixed switching frequency yet as close as possible to critical conduction mode to reduce the current stress of the elements of the power circuit on one hand and enjoy benefits of DCM operational mode on the other. However, do to using two discrete duty cycles; output voltage ripple might be higher than PWM-based controllers. Simulation and experimental results completely match with the theoretical concept.

References

[1] R. E. Locher, "Introduction to Power Supplies," National Semiconductor, Application Note 556, 1988.

[2] P. Lidak, "Critical Conduction Mode Flyback Switching Power Supply using the MC33364," Motorola Semiconductor, Application Note AN 1594, 2004.

[3] G. Spiazzi, D. Tagliavia, and S. Spampinato, "DC-DC flyback converters in the critical conduction mode: A re-examination," in *Proc. IEEE Industry Applications Soc. Annu. Meeting*, vol. 4, Rome, Italy, Oct. 2000, pp. 2426–2432.

[4] "Critical Conduction GreenLine SMPS Controller," Motorola, Tech. Rep. MC33364/D, 1998.

[5] M. Telefus, A. Collmeyer, D. Wong, and D. Manner, "Switching Power Converter with Gated Oscillator Controller," U.S. Patent 6 275 018, 2004.

[6] M. Telefus, D. Wong, and C. Geber, "Operating a Power Converter at Optimal Efficiency," U.S. Patent 6 304 473, 2004.

[7] M. Telefus, A. Shteynberg, M. Ferdowsi, and A. Emadi, "Pulse train™, a novel digital control method, applied to a discontinuous conduction mode flyback converter," in *Proc. IEEE 34th Power Electronics Specialists Conf.*, vol. 3, Acapulco, Mexico, Jun. 2003, pp. 1141–1146.

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