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Hao Shi

F. Yuan

Fei Sha

James L. Drewniak
Missouri University of Science and Technology, drewniak@mst.edu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1877

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Simulation and Measurement for Decoupling on Multilayer PCB DC Power Buses

H. Shi, F. Yuan†, F. Sha, J. L. Drewniak, T. H. Hubing, and T. P. Van Doren
Electromagnetic Compatibility Laboratory
Department of Electrical Engineering
University of Missouri-Rolla
Rolla, MO 65401
and
†Quad Design Technologies
Camarillo, CA 93010

Abstract

DC power bus decoupling of a multi-layer PCB is modeled by a combination of a lumped circuit model at low frequencies (<200 MHz), and a mixed-potential integral equation approach at high frequencies. In order to determine the lumped parameters of via interconnects, an effective procedure using a network analyzer has been developed to characterize the trace/via inductances/resistances. For an 8"×10" ten-layer test board used in this study, the simulations show good agreement with the measurement. This method can lead to new design strategies of decoupling for multilayer PCB power buses.

1 Introduction

As digital device speeds increase, there is a greater the concern for signal integrity (SI), as well as electromagnetic interference (EMI) problems that result from the delta-I noise caused by device switching. Decoupling capacitors (decaps) are commonly used to mitigate the simultaneous switching noise. However, the PCB board design rules regarding the values and locations of the decaps are based to some degree on experience with single-sided and double-sided PCB technology. In developing new power bus decoupling strategies, the special features of multilayer PCBs should be taken into account. First, there is often at least one set of dedicated Vcc-ground planes. The study presented herein is concerned with high-capacitance low-inductance power planes with layer spacing of 10 mils or less, which differs considerably from the case where the planes are widely spaced with low capacitance [1]. Moreover, the inductance associated with the traces/vias that connect the surface mount technology (SMT) decaps directly to the power bus limits the effectiveness of the decaps to frequencies below several hundred megahertz for low-inductance power planes. Simulations with lumped circuit models and efficient EM solvers are cost effective means in determining: 1) the total value of decaps; 2) the number of SMT decaps; and 3) the locations and connections of the SMTs to the power/ground planes. While these goals require extensive further research to achieve, the present study indicates that the approach taken herein shows considerable promise.

Lumped element models have previously been introduced for the power bus of a multilayer PCB [2]. For these models, determining the SMT interconnect inductances/resistances to the power bus is necessary. In this study, with an 8"×10" ten-layer test board, an easily implementable procedure using a network analyzer is developed to extract these lumped element parameters. However, the lumped model is applicable only for frequencies below the distributed resonances of the board ($\leq$ 200 MHz for this test board). A full-wave analysis is necessary to adequately model the power bus behavior at higher frequencies. Numerical techniques used in reported simulations of the power bus include moment method [3, 4], 3D FDTD [5], and 2D FDTD [6]. Yet, these approaches are computationally intense, and less suitable for design CAD tools. An efficient full-wave EM solver employing a mixed-potential integral formulation has been reported [7], and is used in analyzing the test board in this study. At all frequencies, the $|S_{21}|$ spectrum is chosen as the primary vehicle of investigating the test board. S_{21} can be related to the board impedance seen looking into the power bus at the IC device terminals. At low frequencies where the lumped element model applies, the board

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impedance can be directly related to the noise on the power bus [2]. At higher frequencies, S_{21} measurements are a convenient means of testing the numerical modeling approach, though the model must yield the noise voltage on the power bus, as well as effects on SI. Up to 200 MHz, the $|S_{21}|$ results of the lumped model agree well with the measured data. Above 200 MHz, the full-wave analysis yield the major features of the measured data. Further improvements in the experimental and modeling procedures are necessary, but the approach is promising.

2 Measurement techniques

The 8"×10" test board contains a total of 63 pairs of bonding pads where SMT decaps can be connected to the power planes. The top level configuration is shown in Figure 1. The 63 pairs of bonding pads can

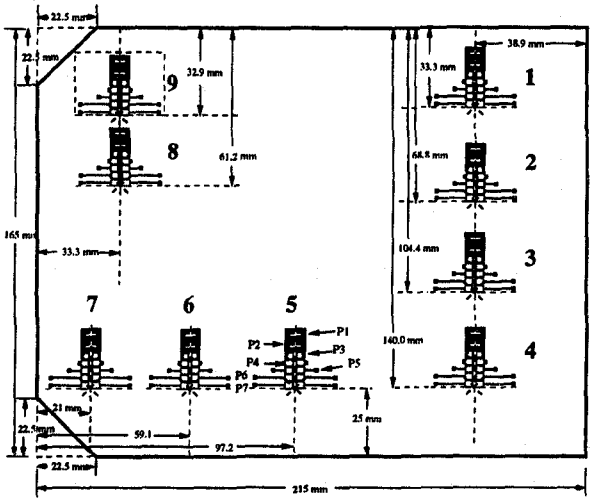

Figure 1: Layout of the top level of the ten-layer test board.

be grouped into 9 identical assemblies (labeled 1–9), with each containing 7 pairs of pads (numbered P1 – P7 from the top down). Then 6P3 specifies the pair of bonding pads that is in Group 6 and 3rd from the top, and so on. A cross-sectional view of the test board is shown in Figure 2. In a typical S-parameter measurement, two sets of the bonding pads are chosen as Port 1 and Port 2. Semi-rigid cables are attached in such a manner to minimize the probe inductance. Any other bonding pads can be used to mount a decap or a wide copper strip for shorting the planes. When the two probe locations are selected with a separation less than 1/4 of the width of the board, the $|S_{21}|$ spectrum exhibits a distributed resonance near 150 MHz, a feature that cannot be

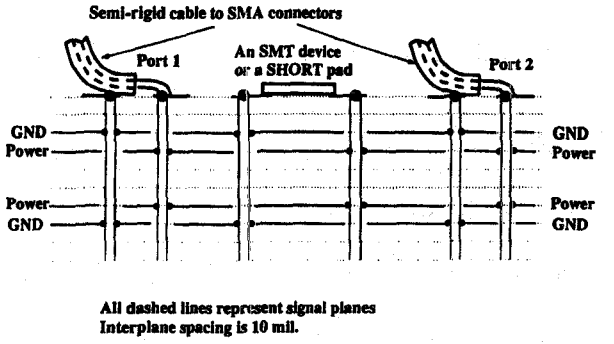

Figure 2: The cross-sectional view of the ten-layer test board.

accounted for by the lumped model, but is exhibited by the full-wave analysis. Increasing this separation, e.g., the two ports on opposite ends of the board, increases the first distributed effects to approximately 200-250 MHz.

A lumped element model of the board is shown in Figure 3 for N connected decaps. At low frequen-

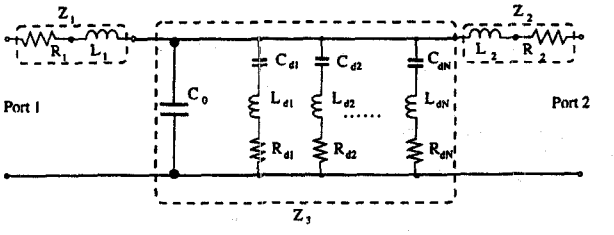

Figure 3: The lumped element model of the test board for a typical two port measurement.

cies, the effect of the internal planes is modeled by a capacitance C_0. $\{R_1, L_1\}$ and $\{R_2, L_2\}$ are the inductances and resistances for the connections from the two probes to the power planes. For the *ith* decap, whose value is C_{di}, there is an inductance L_{di} and a resistance R_{di} due to the traces and vias of the bonding pads. For convenience, the elements are further grouped into three impedances,

$$Z_1 = R_1 + j\omega L_1, \tag{1}$$

$$Z_2 = R_2 + j\omega L_2, \tag{2}$$

and

$$\begin{aligned} Z_3 &= (1/j\omega C_0)//(R_{d1} + j\omega L_{d1} + 1/j\omega C_{d1}) \\ &// \cdots //(R_{dN} + j\omega L_{dN} + 1/j\omega C_{dN}) \end{aligned} \tag{3}$$

The values of the parasitic interconnect inductance and resistance can be determined from S-parameter

measurements. S_{21} is related to Z_1, Z_2, and Z_3 as

$$S_{21} = \frac{2Z_3Z_0}{Z_0^2 + 2Z_3Z_0 + Z_1Z_2 + (Z_1 + Z_2)(Z_0 + Z_3)}, \tag{4}$$

and the input impedance at Port 1

$$Z_{in} = R_{in} + jX_{in} = R_1 + j\omega L_1 + (Z_0 + R_2 + j\omega L_2)//Z_3 \tag{5}$$

can be obtained from the S_{11} measurements, where $Z_0 = 50\ \Omega$. The procedure for determining the lumped element parameters for the test board is comprised of the following steps:

1. Determination of the bare-board interplane capacitance, C_0.
   With no SMT's connected, the values of the input impedance at Port 1 can be read from the Smith Chart display of S_{11} at frequencies f_a and $f_a/2$. The bare board capacitance C_0 can be calculated by first solving

   $$\alpha u^4 - 3u^3 + 5\alpha u^2 + \alpha = 0 \tag{6}$$

   with

   $$\alpha = \frac{X_{in}(f_a) - 2X_{in}(f_a/2)}{Z_0} \tag{7}$$

   for positive solution(s) of u, then

   $$C_0 = \frac{u}{2\pi f_a Z_0}. \tag{8}$$

   $\{R_1, L_1\}$ can also be determined once C_0 is known,

   $$R_1 = R_{in}^{S_{11}}(f_a) - \frac{Z_0}{1 + (2\pi f_a Z_0 C_0)^2} \tag{9}$$

   and

   $$L_1 = \frac{X_{in}^{S_{11}}(f_a)}{2\pi f_a} + \frac{Z_0^2 C_0}{1 + (2\pi f_a Z_0 C_0)^2}. \tag{10}$$

   There may be more than one positive solution for C_0, and only the one leading to positive $\{L_1, R_1\}$ is retained. Likewise, $\{R_2, L_2\}$ can be found if S_{22} is used in place of S_{11}. In general, the choice of f_a will affect the value of C_0 (and consequently, $\{L_1, R_1, L_2, R_2\}$). Typically, the error is within 15% which is mainly caused by the limited sensitivity to the phase information by the network analyzer. If greater precision is pursued, one can utilize a non-linear curve-fitting (data regression) computer routine to fit the $|S_{21}|$ spectrum using the parameters calculated here as the initial guesses.

Table 1: Inductances and resistances associated with traces/vias for the SMT interconnects.

Location	L(nH)	R(mΩ)
6P1	0.69	19.3
6P2	0.64	14.0
6P3	1.41	20.3
6P4	2.17	24.7
6P5	7.23	59.4
6P6	15.5	103
6P7	11.0	70.6

2. Determination of trace/via inductance/resistance of a pair of bonding pads.
   The inductance L and resistance R of the SMT interconnect can be obtained by shorting the bonding pads with a wide copper strip. It can be shown that when

   $$\{R_1,\ R_2,\ R\} << Z_0, \tag{11}$$

   $$\{L_1, L_2, L, RC_0Z_0\} << C_0Z_0^2, \tag{12}$$

   and

   $$2.5R < \eta = \sqrt{L/C_0} < \sqrt{Z_0R} \tag{13}$$

   the peak frequency in the $|S_{21}|$ spectrum is given by

   $$f_0 = \frac{1}{2\pi\sqrt{C_0L}}. \tag{14}$$

   The interconnect inductance L can be determined from Eqn. (14) when the resonance frequency in $|S_{21}|$ is measured with the network analyzer, and C_0 is determined as in the previous step. Once L is calculated, the interconnect resistance R is obtained from S_{11} (Z_{in}) measurements by solving

   $$R_{in}(f_0) = R_1 + Z_0\frac{R^2LC_0 + L^2 + Z_0RC_0}{R^2LC_0 + (L + Z_0RC_0)^2}, \tag{15}$$

   where R_1 is also determined in Step 1.

For the test board shown in Figures 1 and 2, the measured lumped parameters are $C_0 = 14.1\ nF$, and, when 8P4 is used as Port 1, and 2P4 used as Port 2, $R_1 = 0.04\ \Omega$, $L_1 = 2.3\ nH$, $R_2 = 0.04\ \Omega$, $L_2 = 2.3\ nH$. The inductance/resistances associated with traces/vias are listed in Table 1 for Group 6. Assuming the board patterns are manufactured homogeneously, the parameters should be the same for traces/vias belonging to the other groups. The preceding measurement procedures and results are supported by independent precision measurements with

an HP 4291 (1 MHz–1.8GHz) Impedance Analyzer. These results and more extensive details of the method will be presented in a forthcoming paper.

3 Low-frequency modeling of the power bus

The expermentally determined lumped element parameters are used in a lumped element model of the power bus to simulate the decoupling effects with multiple decaps. The lossy X7R SMT decaps employed were modeled as a series RC branch, and the internal resistance was determined by the precision impedance measurements with the HP 4291 model Impedance Analyzer. Three cases were studied with 8P4 as Port 1 and 2P4 as Port 2: (1) The bare-board. (2) A 0.1 μF SMT decap (40 $m\Omega$ internal resistance) is connected at 6P4, and a 0.01 μF decap (110 $m\Omega$ internal resistance) is connected at 5P4. (3) A 0.1 μF decap (40 $m\Omega$ internal resistance) is mounted at 6P4, and four 0.01 μF decaps (100 $m\Omega$ nominal internal resistance) are mounted at 3P4, 4P4, 6P4, and 7P4, respectively (L=2.17 nH for all). The simulated $|S_{21}|$ results, using the lumped element model and independently determined element parameters, are plotted together with the measured data and displayed in Figure 4. For all three cases, the lumped model is

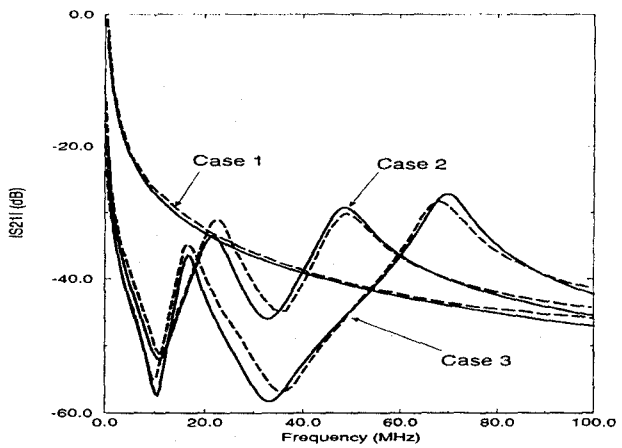

Figure 4: Measured $|S_{21}|_{dB}$ (dashed lines) for three different decoupling cases and simulated results (solid lines) with a lumped model.

able to predict the parallel (maximums in the $|S_{21}|$ spectra) and series (minimum in the $|S_{21}|$ spectra) resonant frequencies with accuracy better than 3%. The differences in levels are well within 5 dB across the range of 0.3 MHz to 200 MHz. Because the major features are toward the lower end, results only up to 100 MHz are displayed. The measured board response is independent of the specific locations of the SMT decaps, indicating that all the decaps affect the board characteristics globally, as long as the decaps are not directly mounted at either Port 1 or 2. This applies only to closely-spaced (10 mils or less) high-capacitance power planes [1].

4 High-frequency modeling of the power bus

A mixed-potential integral equation formulation is employed for modeling the power planes in a multilayer PCB. The potential is retained in this formulation in order to obtain a relation between injected current and the voltage on the planes, and therefore facilitate an equivalent circuit model of the planes [7]. The resulting system of coupled integral equations is then

$$\begin{aligned} & Z_s \hat{\mathbf{n}} \times \bar{\mathbf{J}}_s(\bar{\mathbf{r}}) + \hat{\mathbf{n}} \times \mathbf{j}\omega\mu \int_S d\bar{\mathbf{r}}' \mathbf{G_A}(\bar{\mathbf{r}}, \bar{\mathbf{r}}') \cdot \mathbf{J}(\bar{\mathbf{r}}') \\ & + \hat{\mathbf{n}} \times \nabla \Phi(\bar{\mathbf{r}}) = \mathbf{0} \\ & \nabla \cdot \bar{\mathbf{J}}_s(\bar{\mathbf{r}}) + \mathbf{j}\omega \mathbf{q_s}(\bar{\mathbf{r}}) - \nabla \cdot \bar{\mathbf{J}}^{\mathbf{i}}(\bar{\mathbf{r}}) = \mathbf{0} \\ & \Phi(\bar{\mathbf{r}}) - \frac{\mathbf{1}}{\epsilon} \int_S d\bar{\mathbf{r}}' \mathbf{G}_\phi(\bar{\mathbf{r}}, \bar{\mathbf{r}}') \rho_s(\bar{\mathbf{r}}') = \mathbf{0} \end{aligned} \tag{16}$$

where the injected current $\bar{\mathbf{J}}^i$, surface charge $\rho_s(\bar{\mathbf{r}})$, and surface current $\bar{\mathbf{J}}_s(\bar{\mathbf{r}})$ satisfy a continuity relation, and a surface impedance boundary condition $\hat{\mathbf{n}} \times \bar{\mathbf{E}}(\bar{\mathbf{r}}) = Z_s \ \hat{\mathbf{n}} \times \bar{\mathbf{J}}_s(\bar{\mathbf{r}})$ is employed on the conducting planes. The coupled set of integral equations is discretized using a Galerkin's procedure, and the charge variable is eliminated to give a coupled system of linear equations

$$\begin{aligned} & (\mathbf{Z_s} + \mathbf{j}\omega\mathbf{L})\mathbf{I} - \mathbf{PV} = \mathbf{0} \\ & \mathbf{P^T I} + \mathbf{j}\omega\mathbf{CV} = \mathbf{J^i} \end{aligned} \tag{17}$$

The retarded-potential Green's function in the double integrals for the matrix elements is approximated by the quasi-static Green's function, and analytical techniques are applied for evaluating the integrals to produce a computationally efficient method. The current or voltage can be eliminated in Eqn.(17) to yield an impedance or admittance formulation of the matrix equations, respectively. Further low-frequency approximations are employed, and an equivalent circuit model with reduced rank for the power bus is obtained from the admittance formulation. This approach has been applied for modeling the power planes in an MCM for which experimental results are available in the literature [8].

The mixed-potential integral equation approach is applied to the present test board. To reduce the

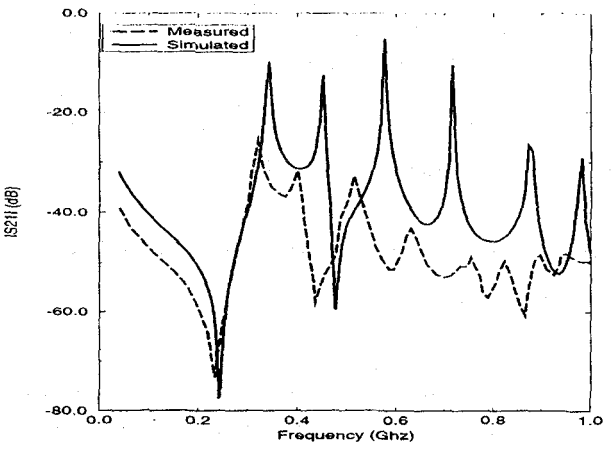

Figure 5: The measured $|S_{21}|_{dB}$ results in comparison with the simulated results by the mixed-potential integral technique. Port 1 is at 2P2, and Port 2 is at 4P2.

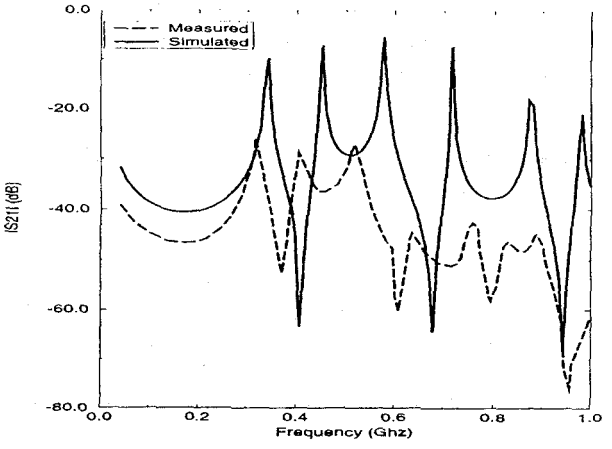

Figure 6: The measured $|S_{21}|_{dB}$ results in comparison with the simulated results by the mixed-potential integral technique. Port 1 is at 4P2, and Port 2 is at 9P2.

computational complexity, only one pair of power and ground planes is modeled in the simulation. Since the loss property of the conducting planes and the dielectric medium were not clearly characterized, the simulation assumes lossless condition. The planes are discretized into approximately 1000 facets in the electromagnetic solution using the method of moment. Through a quasi-static extraction and reduction procedure [7], a 78-node equivalent circuit representing the power/ground planes is obtained and utilized in frequency domain for calculation of the S-parameter. Each port or via on the test board corresponds to a circuit node in the equivalent circuit network. The equivalent RLC circuit, although with frequency independent elements, captures the complex high frequency response of the plane structure up to certain limits. For comparison of the high-frequency simulation with experimental results, $|S_{21}|$ measurements are taken at various port locations and decoupling conditions. The results show that at frequencies greater than 250 MHz, the impact of SMT decaps are negligible, and the response is a function of the port locations. For the 8"$\times$10" board under study, a resonance (minimum in $|S_{21}|$) occurs at about 150 MHz when the two ports are less than 2" apart. If the distance between the two ports is greater than 2", the bare board behaves capacitively up to approximately 200 MHz. The full-wave simulations of two typical cases are shown in Figure 5 and 6.

While there are considerable discrepancies in the measured and the simulated results, the agreement of trends and broad features are very encouraging. The resonant features are consistently shifted toward higher frequencies in the simulations. There are several possibilities for the discrepancies. First, due to the complexity of the geometry involved, only one set of Vcc-ground planes are simulated in the numerical computations. Further, the simulations do not include the effects of the probes connected to the power bus for the measurements. While the electrical length of the probes was calibrated out, compensation for the series inductance and resistance of the probes was not done. These probes are a likely contributor toward the decrease in $|S_{21}|$ at higher frequencies. Finally, the dielectric constant of FR4 was assumed to be constant up to 1 GHz.

5 Summary and Conclusion

A measurement technique for obtaining parameters for a low-frequency lumped element model of a multilayer PCB power bus has been presented. The lumped element model of the power bus for a closely spaced (10 mils or less) high-capacitance board is different from that for a widely spaced low-capacitance board. This study focused on power buses with high interplane capacitance. The lumped element model applied to two cases with SMT decaps agreed well with measurements. At low frequencies, this study shows: (1) the capacitance for SMT decaps attached to the power planes is global below the distributed resonance of the board, hence, the decaps when connected directly to the planes can be located anywhere; and, (2) the effectiveness of the decaps connected directly to the planes is limited in frequency by the via inductance. At high frequencies, results of the numerical simulation based on the mixed-potential

integral equation approach agreed in the broad trends, showing very promising characteristics. Further improvement in both the experiment and modeling procedures is being pursued. The equivalent circuit model extracted from the high-frequency modeling can be employed with circuit simulators to yield noise voltage on the power bus, and to determine the effects of simultaneous switching noise on SI.

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