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***Abstract*—Recently, the full binary combination schema (FBCS) method has been introduced to control the flying capacitor multilevel inverter. This method has the primary advantage that the number of voltage levels can be increased for a given number of semiconductor devices when compared to the conventional control methods. However, due to the difficulty of balancing the capacitors, the new schema requires fixed floating sources to provide the dc voltages. This paper reveals an approach onf balancing the capacitors, thus expanding the application fields of FBCS inverters to the family of the flying capacitor multilevel inverters under the condition of choosing a suitable modulation index. Simulation results demonstrate the proposed voltage balancing control.**

***Index Terms*—Active filters, capacitor voltage balancing, flying capacitor, medium-voltage drives, multilevel inverters.**

I. Introduction

In recent years, the multilevel inverter has become popular due to its advantages which include higher power quality, lower switching losses, higher voltage capability, and better electromagnetic compatibility [1]–[3]. One popular multilevel structure is the flying capacitor topology [1]. Recent research has shown that by changing the dc voltage ratios, a higher number of levels can be obtained for a given number of transistors [2]. This method, referred to as full binary combination schema (FBCS), relies on using floating sources instead of flying capacitors. In this paper, a capacitor voltage balancing method is introduced which allows FBCS operation with flying capacitors; within a certain modulation index limit.

II. Two-Cell FCMI Inverter Topology

Fig. 1 shows the per-phase structure of a two-cell flying capacitor multilevel inverter (FCMI) topology. The relationship between line-to-ground voltages and phase voltages in a three-phase implementation of the topology can be calculated from

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \quad (1)$$

The conventional FCMI inverter schema sets the dc voltage ratio as $v_{cx} : v_{dc} = 1 : 2$ [1], which yields a three-level inverter operation. Herein phase "x" represents phase a, phase b or phase c. Table I shows the inverter switching states (with a dc voltage of $v_{dc} = E$). It can be seen that "01" and "10" switching states both refer to the same switch level $s_x = 1$ which leads to the same voltage level of v_{xg}. The redundant switching combinations provide the possibility for conventional topology to use capacitors as the dc voltage sources [1]. When $s_x = 0$ and $s_x = 2$, the inner capacitor voltage is not involved in generating the line-to-ground voltage v_{xg} so these states do not affect capacitor voltage balance. When $s_x = 1$, the inner capacitor voltage will contribute to v_{xg} and, thus, has capacitor balance concerns. The capacitor voltages can be balanced by selecting a suitable switching combination from the redundant v_{xg} table according to the current flowing through the capacitor. Let F_{vx} denote the capacitor voltage flag, which equals to 1 when v_{cx} is greater than $0.5E$ or equals to 0 when v_{cx} is less than $0.5E$. Let F_{ix} denote the capacitor branch current flag, which equals to 1 when i_{xs} is greater than 0 and equals 0 when i_{xs} is less than 0. When $F_{vx} = F_{ix}$, $T_{x1} = 1$ and $T_{x2} = 0$ are desired. When $F_{vx} \neq F_{ix}$, $T_{x1} = 0$ and $T_{x2} = 1$ are desired for balancing.

A four-level FBCS inverter can use the same topology shown in Fig. 1, except that the voltage ratio should be set to $v_{cx} : v_{dc} = 1 : 3$ according to FBCS 1 or $v_{cx} : v_{dc} = 2 : 3$ according to FBCS 2 [2]. As can be seen from Table II, no re-

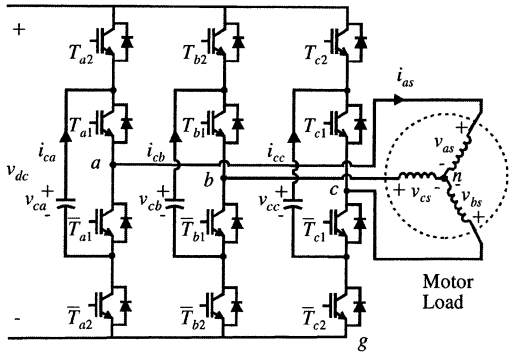

Fig. 1. Two-cell flying capacitor inverter topology.

TABLE I
Conventional Two-Cell Three-Level Inverter States

T_{x2}	T_{x1}	s_x	v_{xg}
0	0	0	0
0	1	1	*E*/2
1	0	1	*E*/2
1	1	2	*E*

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TABLE II
TWO-CELL FOUR-LEVEL FBCS INVERTER STATES

	T_{x2}	T_{x1}	s_x	v_{xg}
FBCS 1,2	0	0	0	0
FBCS 1	0	1	1	$E/3$
FBCS 2	1	0		
FBCS 1	1	0	2	$2E/3$
FBCS 2	0	1		
FBCS 1,2	1	1	3	E

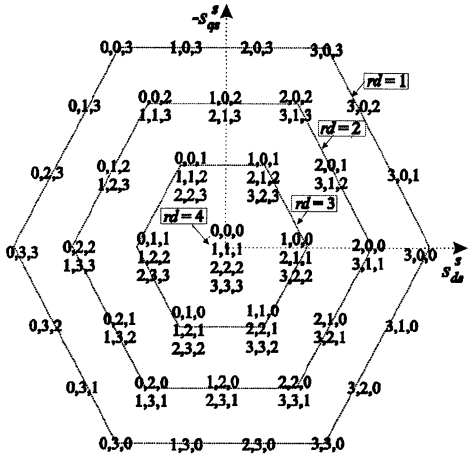

Fig. 2. Space vector plot of the two-cell four-level FBCS inverter.

dundant switching combinations are available in terms of v_{xg}, so if capacitors are used to form the dc voltages, there is no direct approach to balancing the capacitor voltages on a per-phase basis as in the conventional two-cell flying capacitor topology. Generally, FBCS requires fixed floating sources instead of capacitors. However, an approach will be described herein, which achieves capacitor balancing by utilizing information from all three phases.

III. CAPACITOR BALANCING METHOD FOR FOUR-LEVEL FBCS INVERTER

A. Three-Phase Joint Redundancy

Although no redundant switch state in terms of s_x (or v_{xg}) separately is available to balance the capacitors for the two-cell four-level FBCS inverter topology on a per phase base, three-phase joint switching state redundancy does exist in the same way as it does in the diode clamped inverter [3]. For example, according to (1), both $s_a s_b s_c = 002$ and $s_a s_b s_c = 113$ refer to the same v_{as}, v_{bs}, v_{cs} combination, which is $-2E/3$, $-2E/3$, and $4E/3$ respectively. The space vector plot as shown in Fig. 2 clearly demonstrates the distribution of the three-phase joint redundancies. This fact reveals the possibility of utilizing these redundant combinations to balance the capacitors. Because s_x ranges from 0 to 3, the total joint switching combination numbers of $s_a s_b s_c$ are $4^3 = 64$. The term, redundant degree (rd), is used to represent the number of the redundant joint switching states $s_a s_b s_c$, which refer to the same $v_{as} v_{bs} v_{cs}$ voltage value group.

$$rd = nl - [\mathrm{MAX}(s_a, s_b, s_c) - \mathrm{MIN}(s_a, s_b, s_c)] \qquad (2)$$

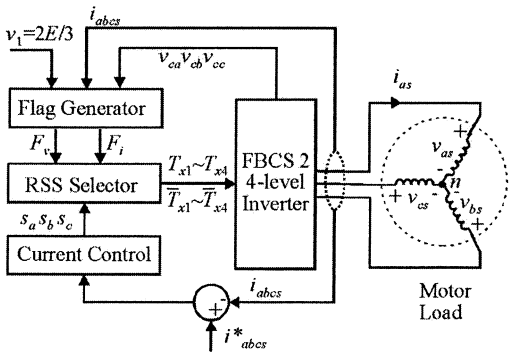

Fig. 3. Current control illustration.

where nl represents the number of v_{xg} levels of the FBCS inverter. For the 4-level FBCS inverter, $nl = 4$ and rd ranges from 1 to 4. Take the case of $rd = 4$ as an example, where four joint switching states of $s_a s_b s_c$ (000 111 222 333) refer to the same v_{as}, v_{bs}, v_{cs} voltage value group (0, 0, 0), which also means that each joint switching state has three other redundant joint switching states available. The rd of those 18 three-phase joint switching states located at the outer loop of the space vector plot is 1, which indicates the absence of the redundant state.

B. Capacitor Balancing Approach

Different current source or voltage source methods are available to control the switching states for the power semiconductors. Fig. 3 shows a current control example. It is not the aim of this paper to discuss the current control or voltage control schema. This paper will focus on the redundant state selector (RSS), which is the key component for balancing the capacitor voltages shown in Fig. 3. Therein the current control can generate the original switching states of $s_a s_b$ and s_c. As mentioned above, these switching states cannot be used individually to balance the capacitor voltages. However, Fig. 2 shows the fact that some of the joint switching combination of $s_a s_b s_c$ have redundancy in terms of v_{as}, v_{bs}, and v_{cs}. The RSS selector can be used to select a suitable joint switching state $s_a s_b s_c$ from the related redundancy group so as to keep the capacitor voltages balanced. Assuming FBCS 1 is used in Fig. 1, the reasons for capacitor voltage v_{cx} imbalance lie in two aspects. 1) When the capacitor voltage v_{ca} is higher than $E/3$, it is desired to discharge the capacitor, and this also implies that the i_{ca} should be greater than 0. 2) When the capacitor voltage is less than $E/3$, it is desired to charge the capacitor, and this implies that the i_{ca} should be less than 0. If not, then the capacitor voltage would become even lower. Therefore, the RSS selector should be able to adjust the switching states based on the capacitor voltage flags Fv_x and the capacitor current flags Fi_x. For phase x, the Flag Generator is used to provide the information of Fv_x and Fi_x. The capacitor current i_{cx} might equal i_{xs} or $-i_{xs}$, depending on the switching states. The RSS selector takes the voltage and current flag information as the condition for the balance situation. It uses the following principles for selecting the best joint combination state of $s_a s_b s_c$ from a redundancy group to minimize the unbalanced phases at the related point in time:

Principle A: If the $rd = 4$, it is always possible to select a $s_a s_b s_c$ from the redundancy group so that all the phases can be

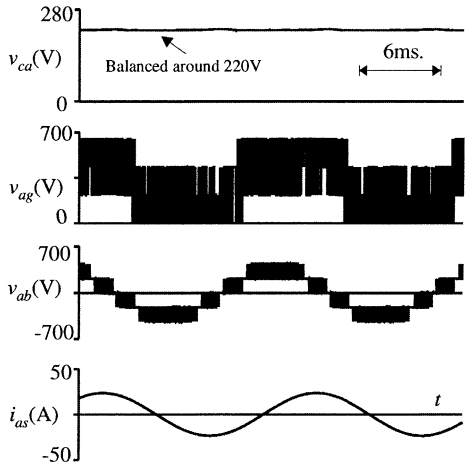

Fig. 4. Two-cell four-level FBCS 1 inverter waveforms. (modulation index $= 0.65$, power factor $= 0.763$).

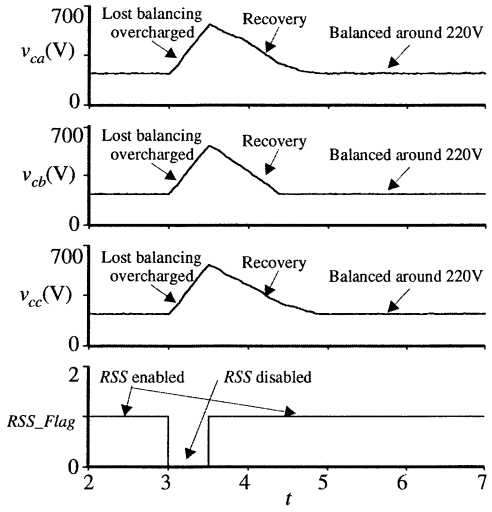

Fig. 5. Capacitor voltage transient study.

balanced at the related time point. Note that this is in contrast to the diode-clamped topology [3], where the redundant zero states do not affect the capacitor voltages! If several $s_a s_b s_c$ are in a good balancing situation, then RSS gives priority to the selection of the original $s_a s_b s_c$ generated by the current control.

Principle B: If $rd = 2$ or 3, it may be possible to select a $s_a s_b s_c$ from a redundant group so that all phases can be balanced at the related time point. If not, it is always possible to select a $s_a s_b s_c$ from its redundancy group so that only one phase can not be balanced at the related time point. If several of the switching state combinations work under the same balancing situation, RSS gives priority to the selection of the original $s_a s_b s_c$ generated by the current control.

Principle C: If $rd = 1$, no redundant switching combinations are available, so the RSS can only use the original $s_a s_b s_c$ generated by the current control.

IV. Simulation Studies

Based on Figs. 1 and 3, a two-cell four-level FBCS 1 inverter computer simulation model that follows principles A, B, and C has been created to verify the capacitor balancing approach. Three 6.86-Ω resistors and three 15.43-mH inductors were used to emulate the motor load. The outer dc link voltage v_{dc} is 660 V, and three 3,300 μF capacitors are used to form the dc link voltage v_{cx} for each phase. The commanded fundamental frequency was 60 Hz. Fig. 4 shows the voltage and current waveforms. It can be seen that the 2-cell flying capacitor inverter as shown in Fig. 1 can yield 4 line-to-ground converting levels using FBCS 1 since capacitor voltage balance is achieved. The RSS selector affects the shape of the line-to-ground voltage, but not the line-to-line voltage. Fig. 5 shows a capacitor voltage balancing transient study. RSS_Flag is used to represent the active state of RSS selector. When RSS_Flag is active high, the RSS Selector is enabled. When RSS_Flag is active low, the RSS selector is disabled and the switching states generated by the current control are fed back to the converter directly. In the simulation of Fig. 5, the RSS selector was disabled when $t = 3$ s and enabled again when t $= 3.5$ s. From the capacitor voltage plots, it is clear that the capacitor can maintain balance when the RSS selector is enabled. When the RSS selector is disabled, FBCS 1 tends to overcharge the capacitors; thus it loses balance. The reason for this phenomenon is that the average currents flowing out of the floating sources are negative for FBCS 1, but positive for FBCS 2 [2]. This simulation verified that the capacitor balancing approach could guarantee the use of capacitors as the dc voltages in FBCS multilevel inverters. The modulation index used in the above two studies is 0.65. Extensive simulation studies showed that for a load condition with a power factor of 0.8, one can set the modulation index value up to 0.7 and maintain balanced capacitor voltages. If the FBCS Inverter is used in highly inductive load applications, such as active filters, one can apply a modulation index up to the physical limit of 1.15. Fig. 6 shows a simulation study with a highly inductive load where $R = 1.0\ \Omega$ and $L = 66$ mH. The modulation index is set to 1.13 (close to the upper limit considering third harmonic injection). It can be seen from Fig. 6 that one can still achieve balanced capacitor voltages.

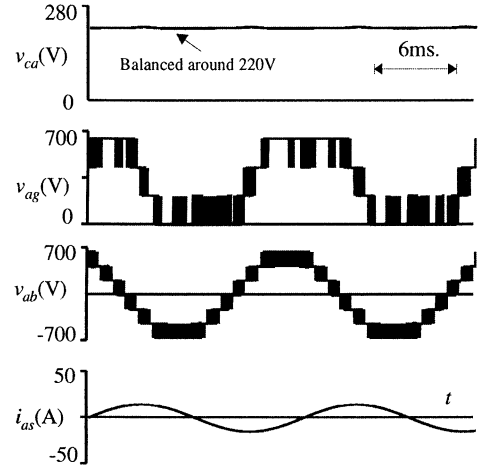

Fig. 6. Two-cell four-level FBCS 1 inverter waveforms. (modulation index $= 1.13$, power factor $= 0.11$).

V. Conclusion

In this paper, a capacitor voltage balancing method for the flying capacitor multilevel inverter was introduced. The balancing method applies to the FBCS control, introduced in prior research, which results in more voltage levels for a given number of semiconductor devices in the flying capacitor topology. The proposed method is based on joint-phase redundancy and will successfully balance the capacitor voltages within a given modulation index limit. Detailed simulations demonstrated the operation of the proposed method.

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