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# Control of Cascaded Multilevel Inverters

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***Abstract*—A new type of multilevel inverter is introduced which is created by cascading two three-phase three-level inverters using the load connection, but requires only one dc voltage source. This new inverter can operate as a seven-level inverter and naturally splits the power conversion into a higher-voltage lower-frequency inverter and a lower-voltage higher-frequency inverter. This type of system presents particular advantages to Naval ship propulsion systems which rely on high power quality, survivable drives. New control methods are described involving both joint and separate control of the individual three-level inverters. Simulation results demonstrate the effectiveness of both controls. A laboratory set-up at the Naval Surface Warfare Center power electronics laboratory was used to validate the proposed joint-inverter control. Due to the effect of compounding levels in the cascaded inverter, a high number of levels are available resulting in a voltage THD of 9% (without filtering).**

***Index Terms*—Cascaded inverter, multilevel inverter, three-level inverter.**

## I. Introduction

THE CONCEPT OF multilevel inverters, introduced about 20 years ago [1], [2], entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. Considering these advantages, multilevel converters have been gaining considerable popularity in recent years [3]–[18]. The benefits are especially clear for medium-voltage drives in industrial applications [7], [9] and are being considered for future Naval ship propulsion systems. In fact, several IEEE conferences now hold entire sessions on multilevel power conversion.

Several topologies for multilevel inverters have been proposed over the years; the most popular being the diode-clamped [3], [4], flying capacitor [5], [6] and cascaded H-bridge [7]–[10] structures. One aspect which sets the cascaded H-bridge apart from other multilevel inverters is the capability of utilizing different dc voltages on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher-frequency inverters [9], [10]. An alternate method of cascading inverters involves series connection of two three-phase inverters through the neutral point of the load. Past research has shown this concept for cascading two-level inverters [11]–[15] and multilevel inverters [16]–[18]. An advantage of this approach is that isolated sources are not required for each phase. It should be noted that cascaded inverter systems can be considered from a number of different viewpoints. Considering the cascaded inverter to be one unit, it can be seen that a higher number of voltage levels are available for a given number of semiconductor devices. Considering the system as separate inverters, the cascaded design can be regarded as a combination of a bulk power (higher-voltage) inverter and a conditioning (lower-power) inverter. An alternate viewpoint is to consider the conditioning inverter as an active filter and the bulk inverter as the drive inverter. In any case, the cascaded multilevel inverter has several advantages for Naval ship propulsion systems. One advantage is that cascaded inverters provide a compounding of voltage levels leading to extremely low harmonics. Another advantage is that the bulk inverter may be commercial-off-the-shelf; requiring that only the lower-power condition inverter to be custom made. Yet another advantage is that the cascaded design avoids a large number of isolated voltage sources which would be cumbersome in shipboard power systems. An additional advantage is that the dual inverter structure may be useful for redundancy providing remedial operation for survivability. Furthermore, in Naval applications, the propulsion motor is typically custom built and can be readily made to have access to both ends of each winding.

This paper reports the development of new control methods for cascaded multilevel inverters. In particular, capacitor voltage regulation methods are introduced resulting in a cascaded inverter which only requires one dc source. The new control methods are applied to a topology where two three-level inverters are cascaded. Simulation and laboratory measurements are presented which demonstrate the effectiveness of the proposed control.

## II. Cascaded Multilevel Inverters

The cascade-3/3 inverter is shown in Fig. 1. This topology is constructed by connecting a three-level inverter to both sides of the motor windings. As a practical matter, the inverters may have any number of voltage levels as described in the literature [17]. Herein, a control will be developed to regulate the dc voltage so that only one dc source voltage is required. This provides some unique advantages for Naval propulsion systems which typically operate from a single source, but also leads to other aspects which should be pointed out. Since the conditioning inverter is supplied by a capacitor bank, the bulk inverter must be rated for the entire amount of the load power. Under these conditions, the conditioning inverter becomes an added expense which is justified by the higher power quality. An alternate approach to reducing harmonics would be to add passive filter components to the bulk inverter which would also increase the cost. However,

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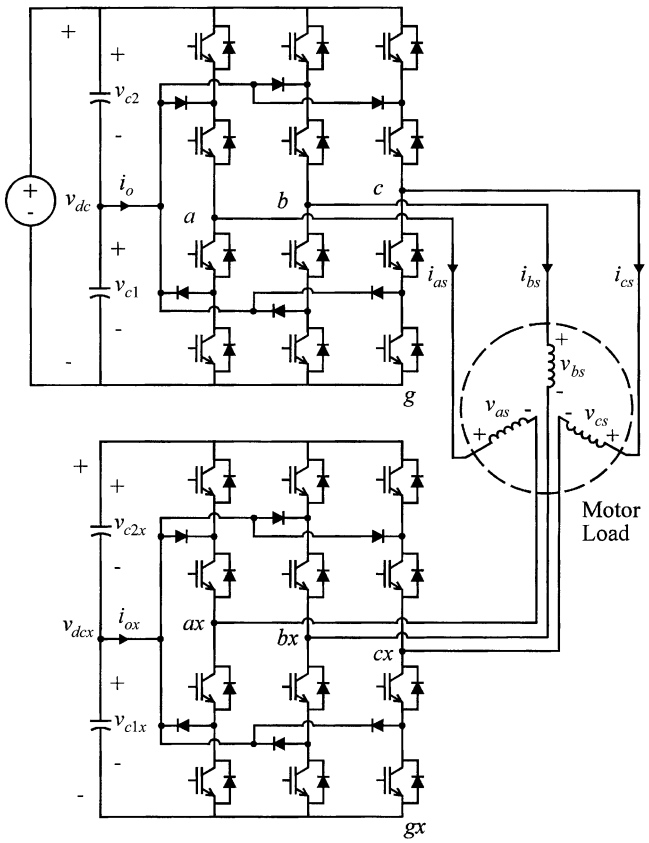


Fig. 1. Cascade-3/3 multilevel inverter.

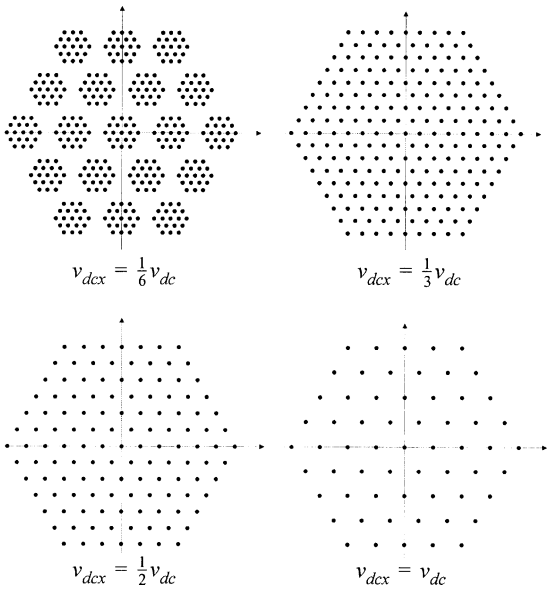


Fig. 2. Cascade-3/3 inverter vector plots.

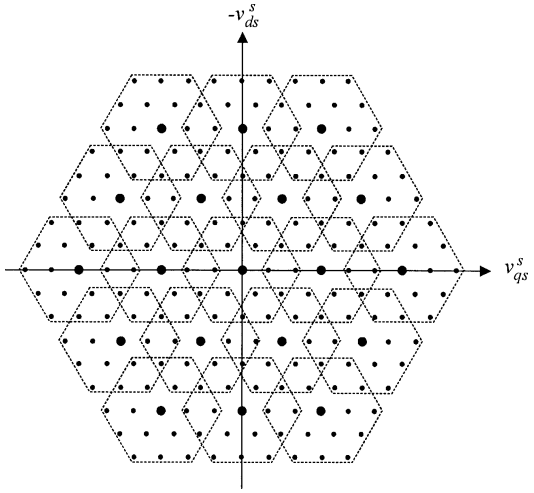


Fig. 3. Cascade-3/3 vector plot for maximal distention.

the passive components will change their effect on the system harmonics as the drive operating point is varied. Another aspect of eliminating the voltage source for the conditioning inverter is that it is no longer available for driving the motor in situations where there is a fault in the bulk inverter. In those cases, a dc source would need to be switched in to the conditioning inverter. One good feature about fault operation of ship propulsion loads is that a relatively low amount of power is needed to operate in a survivable situation. Since propulsion load power typically varies as the speed cubed, only 12% of full power is necessary to operate at half-rated speed.

Referring to Fig. 1 and assuming that the capacitors are charged to half of their respective dc bus voltage, the line-to-ground voltages of the upper and lower voltage may be expressed as

$$[v_{ag} \quad v_{bg} \quad v_{cg}]^{\mathrm{T}} = [s_a \quad s_b \quad s_c]^{\mathrm{T}} \frac{v_{dc}}{2} \tag{1}$$

$$[v_{agx} \quad v_{bgx} \quad v_{cgx}]^{\mathrm{T}} = [s_{ax} \quad s_{bx} \quad s_{cx}]^{\mathrm{T}} \frac{v_{dcx}}{2} \tag{2}$$

where $s_a$, $s_b$, and $s_c$ are the switching states for the upper inverter and $s_{ax}$, $s_{bx}$, and $s_{cx}$ are the switching states for the lower inverter. For three-level inverters, the switching states corresponding to the line-to-ground voltage levels and can have the values 0, 1 or 2. The phase voltages of the load may be expressed in terms of the line-to-ground voltages as [19]

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} - v_{agx} \\ v_{bg} - v_{bgx} \\ v_{cg} - v_{cgx} \end{bmatrix}. \tag{3}$$

The effective line-to-line load voltages may be expressed in terms of the phase voltages as

$$\begin{bmatrix} v_{abs} \\ v_{bcs} \\ v_{cas} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix}. \tag{4}$$

It is often insightful to look at the voltage vector plot of a multilevel inverter which can be accomplished by plotting the phase voltages in the $d-q$ stationary reference frame for all possible combinations of switching states [11]. In the case of the cascaded multilevel inverter, vector plots vary widely depending on the ratio of the dc voltages. Fig. 2 shows the voltage vector plots for the cascade-3/3 inverter for several dc voltage ratios. Therein, the axes of each subplot are the same as those shown in Fig. 3. When the voltage ratio is set to $v_{dcx} = v_{dc}/6$, the vector plot appears as that of several three-level vector plots arranged in a three-level pattern. This is to be expected when cascading two three-level inverters as the amplitude of the small vector patterns depends on the dc voltage $v_{dcx}$. Incidentally, if $v_{dcx}$ is set to zero, the amplitude of its vectors goes to zero and the overall

vector plot is that of a three-level inverter (the lower inverter turns into a neutral connection). The next ratio is $v_{dcx} = v_{dc}/3$ where there is some overlap of the voltage vectors and the vector plot is the same as that of a nine-level inverter. As it turns out, nine levels is the largest number of voltage levels that the cascade-3/3 inverter is capable of emulating. For this reason, this mode of operation is referred to as maximal distention [11], [17]. In general, the voltage ratio which yields maximal distention for an arbitrary number of voltage levels is [17]

$$\frac{v_{dcx}}{v_{dc}} = \frac{n_x - 1}{nn_x - n_x} \tag{5}$$

where $n$ and $n_x$ are the voltage levels of the upper and lower inverter, respectively. As shown in Fig. 2, if the voltage ratio is increased further to $v_{dcx} = v_{dc}/2$ and $v_{dcx} = v_{dc}$, the cascade-3/3 inverter can operate as a seven-level and five-level inverter, respectively. However, these mo des of operation are not as desirable as that of maximal distention which yields the highest power quality through lower voltage steps.

## III. Cascade-3/3 Inverter Control

Before considering specific modulation and capacitor voltage regulation strategies, it is instructive to examine the cascade-3/3 inverter vector plot shown in Fig. 3 in detail. Therein, the vectors produced by the upper inverter are denoted as being slightly larger than the other vectors. The small three-level vector plots produced by the lower inverter are indicated by the dashed hexagons. One of the significant features of the controls developed herein is the ability to regulate the dc voltage $v_{dcx}$ so that only one dc source is required. This can be accomplished through redundant selection of inverter switching states. Fig. 3 shows overlap amongst the smaller hexagons and where this overlap occurs there is a choice as to the realization of the voltage vectors. This choice can be made with regard to the power flow in the lower inverter [14] so that the dc voltage $v_{dcx}$ remains at one-third of $v_{dc}$. As can be seen form Fig. 3, a considerable amount of overlap occurs for vectors toward the inside of the vector plot and the full dc voltage $v_{dc}$ may be utilized while regulating the lower inverter capacitor voltage. Toward the outside of the vector plot, the overlap is not present for many vectors and in this case, the power flow can not be used to maintain $v_{dcx}$. This results in a limitation of operating region within the upper inverter vectors (larger vectors in Fig. 3). Considering the number of lower inverter vectors in-between the upper inverter vectors, it can be seen that this limitation will result in seven-level operation. However, only one dc source is required and that dc voltage can be fully utilized.

### A. Joint-Inverter Control

The method of joint inverter control proposed herein utilized nine-level modulation followed by a redundant state selection (RSS) table for capacitor voltage balancing. The process of nine-level modulation is shown for the a-phase in Fig. 4 where a modified duty cycle $d_{am}$ is compared to eight triangle waveforms to produce the $a$-phase commanded switching state $s^*_{am}$. The comparison rules assert that the switching state be equal to

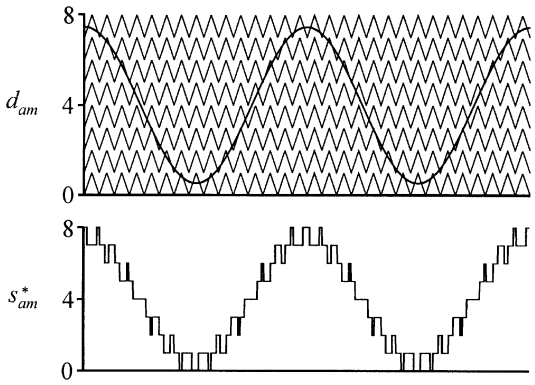


Fig. 4. Nine-level triangle modulation.

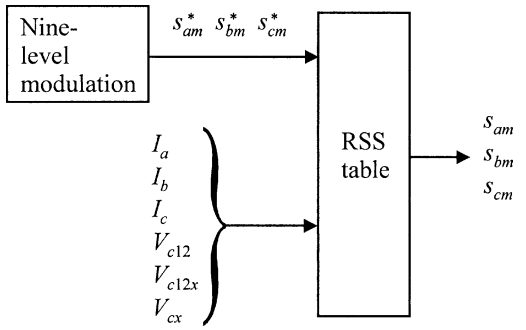


Fig. 5. Redundant state selection implementation.

the number of triangle waveforms that the modified duty cycle is greater than. The modified duty cycle is calculated as

$$d_{am} = 4\left[1 + \frac{3\hat{m}}{4}\cos(\theta_e)\right] \tag{6}$$

where the duty cycle has been modified from the traditional definition so that it ranges from 0 to 8 (the number of levels minus 1) and the modulation index $\hat{m}$ represents the percent of voltage utilization of $v_{dc}$ and ranges from 0 to 1. The angle is the electrical angle which corresponds to the commanded frequency. The duty cycles of the $b$- and $c$-phase are similar to that of (6) with 120° and 240° offset in the electrical angle, respectively. Typically, all three duty cycles are compared to the same set of triangle waveforms. To produce commanded switching states $s^*_{am}$, $s^*_{bm}$, and $s^*_{cm}$.

The modulation is typically programmed in a digital signal processor (DSP) and may be followed by an RSS table located in either the DSP or in a programmable logic device (PLD). Fig. 5 shows the RSS table structure for this system. The inputs (address) of the table are the commanded switching states from the modulator as well as digital flags which represent the state of the system. The flags $I_a$, $I_b$, and $I_c$ indicate the current direction and are 1 for positive and 0 for negative vales of $i_{as}$, $i_{bs}$. and $i_{cs}$, respectively. The capacitor voltage flags represent voltage balance and are defined by

$$V_{c12} = \begin{cases} 1 & v_{c1} \geq v_{c2} \\ 0 & v_{c1} < v_{c2} \end{cases} \tag{7}$$

$$V_{c12x} = \begin{cases} 1 & v_{c1x} \geq v_{c2x} \\ 0 & v_{c1x} < v_{c2x} \end{cases} \tag{8}$$

$$V_{cx} = \begin{cases} 1 & v_{dcx} \geq \frac{1}{3}v_{dc} \\ 0 & v_{dcx} < \frac{1}{3}v_{dc} \end{cases}. \tag{9}$$

The RSS table output is the switching state for each phase. This can be related to the switching states of the individual inverters by consideration of the line-to-ground voltages [16]. Table I shows this relationship for the $a$-phase.

Identical relationships apply for determining the $b$- and $c$-phase inverter switching states.

The final consideration for this control is the method of generating the RSS table. For this, a program was written to evaluate the redundant states for all possible combinations of the RSS table inputs. Each combination of inputs was evaluated in the following way. First the number of redundant switching states was identified by

$$n_{RSS} = n \cdot n_x - (s_{max} - s_{min}) \tag{10}$$

where $s_{max}$ and $s_{min}$ are the maximum switching states from the modulator or

$$s_{max} = \mathrm{MAX}\,(s^*_{am}, s^*_{bm}, s^*_{cm}) \tag{11}$$

$$s_{min} = \mathrm{MIN}\,(s^*_{am}, s^*_{bm}, s^*_{cm})\,. \tag{12}$$

To obtain the first redundant state, $s_{min}$ is subtracted from the switching states of all three phases. The other states are obtained by adding 1 to all three phases (changing the common-mode or zero sequence term) until all redundant states are evaluated. For each redundant state, the contribution to power from the lower inverter is found by first deterring the switching states corresponding to that inverter from Table I. Next, the contribution to the line-to-ground voltages can be evaluated using

$$\begin{bmatrix} v_{asx} \\ v_{bsx} \\ v_{csx} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{agx} \\ v_{bg} \\ v_{cgx} \end{bmatrix}. \tag{13}$$

Finally, the contribution of the lower inverter power may be expressed as

$$p_x = v_{asx}(1 - 2I_a) + v_{bsx}(1 - 2I_b) + v_{csx}(1 - 2I_c). \tag{14}$$

It should be noted that (14) can not calculate the exact power since the current flags only represent the current direction. however, for high power factors (14) can be used to determine the direction of power flow. If the direction is positive (out of the inverter) and the capacitor is overcharged (or $V_{cx} = 1$) the redundant state will help regulate the capacitor voltage. Similarly, if the power direction is negative and the capacitor is undercharged, the redundant state will help regulate the capacitor voltage. Any redundant states which help the balance situation are given a priority of 4. The reason for this is that some priority will be added to the redundant states which also help the capacitor voltage balancing within the inverters. Evaluating this voltage balance amounts to determining the direction of the current in each inverter which flows out of the capacitor junction (currents $i_o$ and $i_{ox}$ in Fig. 1). For each redundant state, the junction current is determined by using Table I to determine which phases are connected to the junction and then adding the current depending on the current direction flags. The direction of the junction currents can be used with the capacitor balance information ($V_{c12}$ and $V_{c12x}$) to determine if the redundant state helps the voltage balance. For the upper inverter, cases which help the balance have their priority increased by 1. For the lower inverter, cases which help the balance have their priority increased by 2.

TABLE I
RELATION OF A-PHASE SWITCHING STATES

| $s_{am}$ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| $s_a$ | 0 | 0 | 0 | 1 | 1 | 1 | 2 | 2 | 2 |
| $s_{ax}$ | 2 | 1 | 0 | 2 | 1 | 0 | 2 | 1 | 0 |

This choice is arbitrary, but was made based on simulation results. After evaluating all of the redundant states, the one with the highest priority is selected for the RSS table data.

The cascade-3/3 inverter was simulated using the proposed control. In the simulation, the dc voltage was set to $v_{dc} = 601.8$ V. The controller modulation index was $\hat{m} = 1$ with a commanded frequency of 60 Hz. The load was a resistive-inductive load with $R = 11\ \Omega$ and $L = 17.5$ mH. Fig. 6 shows the simulation results. Therein, the $a$-phase upper and lower line-to-ground voltages $v_{ag}$ and $v_{agx}$ are shown followed by the load voltage $v_{as}$, the line-to-line voltage $v_{abs}$ as defined by (4), and the phase current $i_{as}$. From the line-to-ground voltages, it can be seen that there is a natural split between higher-voltage lower-frequency and lower-voltage higher-frequency. The line-to-ground voltages also demonstrate the effectiveness of the capacitor voltage balancing control. From the line-to-line voltage, the effective seven-level operation can be seen (six positive levels, six negative levels, and zero). For this simulation, the output power was 23 kW and the THD of the phase and line-to-line voltages were $\mathrm{THD}(v_{as}) = 9.42\%$ and $\mathrm{THD}(v_{abs}) = 9.34\%$. Further simulations were performed to evaluate the proposed control and it was shown that the capacitor voltage balancing control works over a range of modulation indices and varying power factors from 0.0125 lagging to 0.997 lagging.

### *B. Separate Inverter Control*

The above described joint-inverter control algorithm treats both (the bulk and the lower-power) inverter bridges as one unit and has to be implemented by one consolidated DSP/PLD control board. As mentioned above, one advantage of the proposed cascade inverter system is that the bulk inverter may be commercial-off-the-shelf; requiring that only the lower-power condition inverter to be custom. In order to achieve this, a separate inverter control with minimal or no communication to the bulk inverter control is required. In addition, the dual inverter structure with separate control may be useful for redundancy and reliability improvement. The inverter system becomes more reliable and flexible for future system change and maintenance.

Unlike the joint-inverter control, the proposed separate inverter control utilizes isolated algorithms for the bulk and conditioning inverter. The bulk inverter is controlled by the staircase or low-frequency PWM method to provide power needed to drive the motor, whereas the conditioning inverter utilizes high-frequency PWM to shape motor voltage and current and achieve high performance drive with low current and torque ripple. One advantage of the separate inverter control is that no communication is needed between the two inverters, thus making it possible to use commercial-off-the-shelf motor

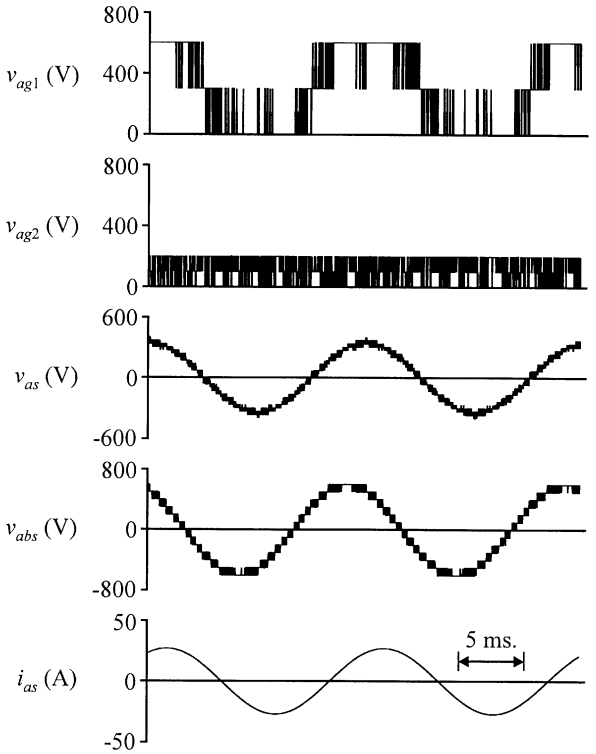


Fig. 6. Cascade-3/3 inverter simulation results.

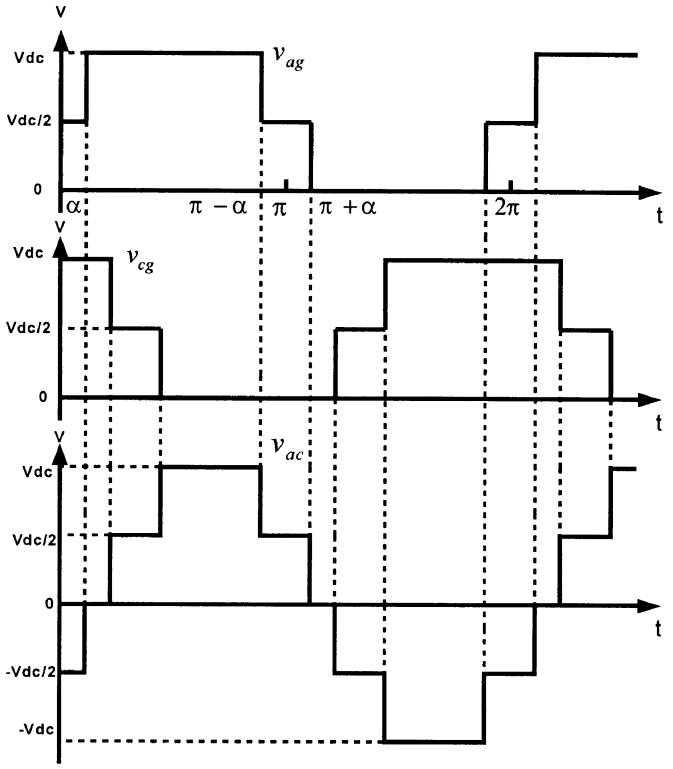


Fig. 7. Staircase control of the bulk inverter.

drive inverters. It should be noted that, as with the joint-inverter control the conditioning inverter does not need a power supply, thus acting like an active filter.

The process of the staircase control of the bulk inverter is shown in Fig. 7, where the angle $\alpha$ is controlled to produce the staircase voltage waveform. Therein, the phase voltages $v_{ag}$ and $v_{cg}$ and the line-to-line voltage $v_{ac}$ are shown. The amplitude of any odd $n^{th}$ harmonic of the phase voltage can be expressed as

$$v_n = \frac{2v_{dc}}{n\pi}\cos(\alpha) \tag{15}$$

where $n$ is an odd harmonic order; the amplitudes of all even harmonics being zero. The amplitude of the fundamental component in the phase voltage can be calculated as

$$v_f = \frac{2v_{dc}}{\pi}\cos(\alpha). \tag{16}$$

According to Fig. 7, $\alpha$ must satisfy $0 < \alpha < (\phi/2)$.

The conditioning inverter functions like a series active power filter to compensate the harmonic voltage produced by the bulk inverter. In the time-domain, this harmonic can be computed for the $a$-phase as

$$v_{ag,h} = v_{ag} - v_{ag,f} \tag{17}$$

where $v_{ag,f}$ is the fundamental component of $v_{ag}$. The fundamental component $v_{ag,f}$ can be obtained simply through a low pass filter. However, it should be noted that a three-phase vector PLL circuit [20], [21] based on the line-to-line voltages gives better performance because the three-phase line-to-line voltages contain no triplens and their lowest harmonic is the fifth. Once the phase angle information is obtained by the PLL circuit, the synchronous frame method can be used to extract the fundamental component [22].

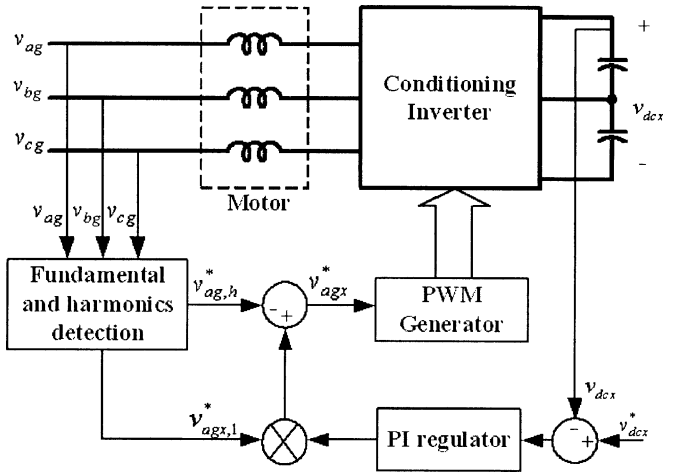


Fig. 8. Conditioning inverter control diagram.

Another consideration of the separate inverter control is the dc voltage control of the conditioning inverter. In order to maintain maximal distention, the dc capacitor voltage on the conditioning inverter should be kept at one third of the dc voltage of the bulk inverter. To achieve this, a straightforward PI control is adopted to regulate active power flow into the conditioning inverter. The control scheme of the conditioning inverter is shown in Fig. 8 for the $a$-phase. Therein, $v^*_{dcx}$ is the dc voltage reference, which is set to one third of $v_{dc}$. The voltage $v^*_{ag,1}$ is a unit sine wave in phase with the phase voltage $v_{ag,f}$ and can be directly obtained from the vector PLL circuit [20], [21]. The voltage $v^*_{ag,1}$ is a unit sinusoidal

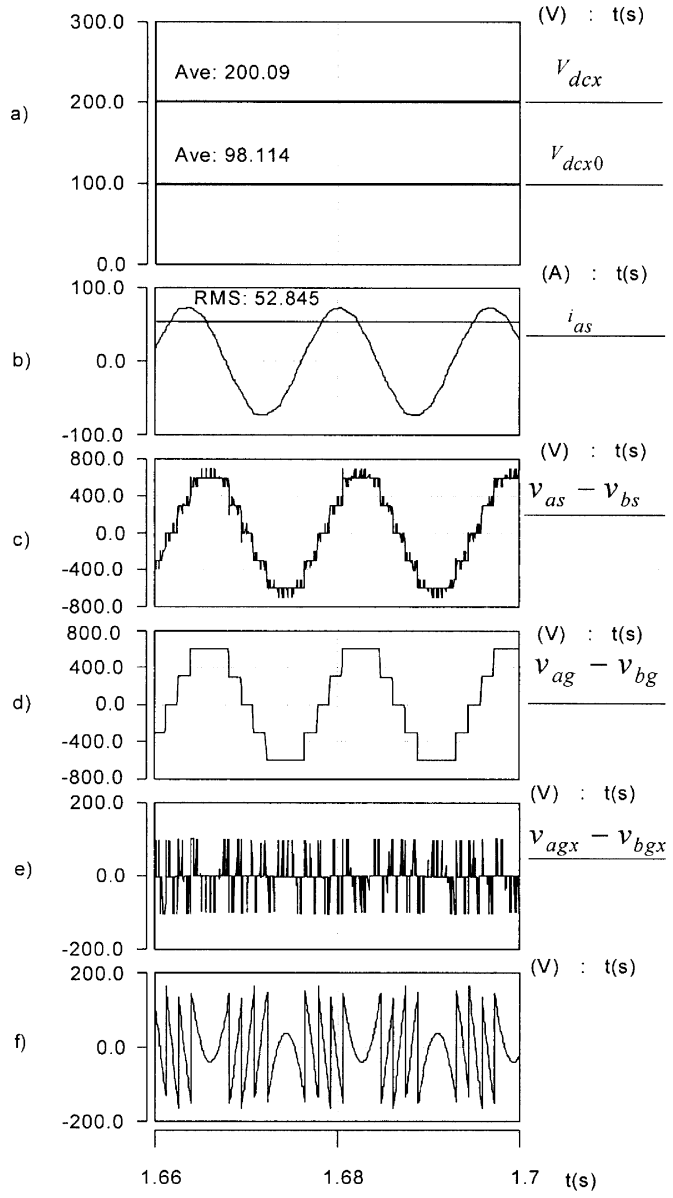


Fig. 9. Separate control simulation results.

wave, which has the same phase angle with the phase voltage $v_{ag,f}$. The resulting reference voltage is used as an input for a PWM modulator for the conditioning inverter. Similar control channels are used for the $b$- and $c$-phase.

Fig. 9 shows simulation results of the cascade multilevel converter using the separate control, in which

a) is the dc voltage of the conditioning inverter;
b) is the motor current;
c) is the total motor line-line voltage;
d) is the bulk inverter line-line voltage;
e) is the conditioning inverter line-line voltage;
f) is the harmonics in the line-line voltage of the bulk inverter.

In simulation, $v_{dc}$ was set to 600 V and $\alpha$ was set to 15°. It can be seen that the dc link voltage of the conditioning inverter is kept at one third of the dc voltage of the bulk inverter. The total line-to-line voltage is improved from the bulk inverter five-level waveform by the conditioning inverter and the maximal distention of the cascaded inverter is realized.

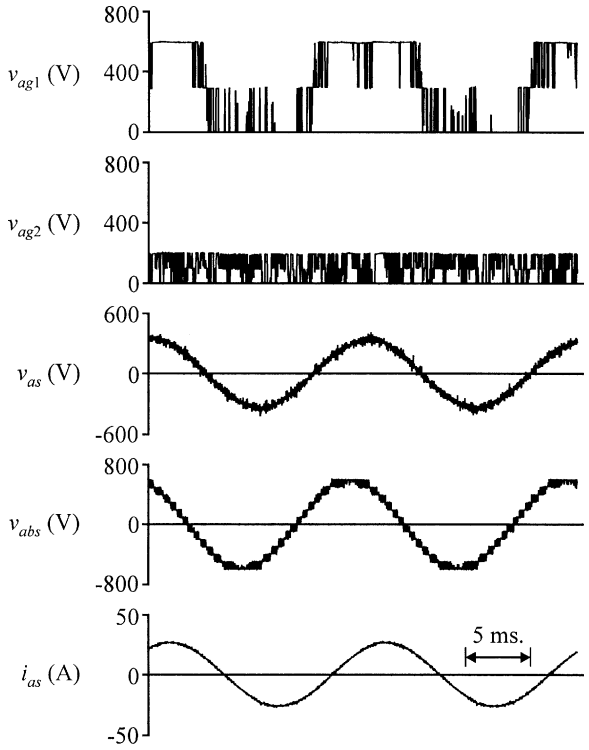


Fig. 10. Cascade-3/3 inverter measurements.

## IV. Laboratory Validation

The cascade-3/3 inverter was constructed in the power electronics laboratory at the Naval Surface Warfare Center (NSWC), Philadelphia, PA. Joint inverter control was used and the operating conditions were the same as those described in the simulation in Section III-A. Fig. 10 shows the laboratory measurements displaying the same system variables as Fig. 6. As can be seen, the measurements are nearly the same as the simulation with the exception of the ripple in the phase current which is higher in lab measurements due to high-frequency effects which were not included in the simulation. From the measured data, the THDs were $\mathrm{THD}(v_{as}) = 9.00\%$ and $\mathrm{THD}(v_{abs}) = 8.14\%$.

## V. Conclusion

This paper has studied a new type of multilevel inverter which consists of two three-phase three-level inverters cascaded through the load connections. Two types of control were developed for this inverter. One relies on controlling the two three-level inverters jointly and the other uses separate controls. Both controls included capacitor voltage balancing so that a dc source was needed for only one three-level inverter. Simulation results demonstrate the effectiveness of each control. The joint control was validated with laboratory measurements on a 23-kW inverter system.

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