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***Abstract*—In this paper, a four-level dc/dc buck converter is introduced. The primary application for this converter is to regulate the center capacitor voltage in a four-level inverter system. The steady-sate and average-value models for the proposed converter are developed and compared in simulation. The converter was constructed in the laboratory and verified on a four-level motor drive system. It was shown that the four-level dc/dc converter provides capacitor voltage balancing and allows higher output voltage utilization from the inverter.**

***Index Terms*—Average-value modeling, dc/dc converters, four-level converters, multilevel converters.**

I. Introduction

THE general trend in power electronics devices has been to switch power semiconductors at increasingly high frequencies in order to minimize harmonics and reduce passive component sizes. However, the increase in switching frequency increases the switching losses, which become especially significant at high power levels. Several methods for decreasing switching losses have been proposed including constructing resonant inverters and multilevel inverters [1].

Resonant inverters avoid switching losses by adding an *LC* resonant circuit to the hard-switched inverter topology. The inverter transistors can be switched when their voltage or current is zero, thus mitigating switching losses. Examples of this type of inverter include the resonant dc link [2], and the auxiliary resonant commutated-pole inverter (ARCP) [3], [4]. One disadvantage of resonant inverters is that the added resonant circuitry will increase the complexity and cost of the inverter control. Furthermore, high insulated gate bipolar transistor (IGBT) switching edge rates can create switch-level control problems.

Multilevel inverters offer another approach to reducing switching losses. In particular, these converters offer a high number of switching states so that the inverter output voltage can be "stepped" in smaller increments [5]–[11]. This allows mitigation of harmonics at low switching frequencies, thereby reducing switching losses. In addition, electromagnetic compatibility EMC concerns are reduced through the lower common-mode current facilitated by lower dv/dt's produced by the smaller voltage steps. One disadvantage of these techniques are that they require a high number of switching devices. The primary disadvantage of a multilevel inverter is that they must be supplied from isolated dc voltage sources or a bank of series capacitors with balanced voltages. In systems where isolated dc sources are not practical, capacitor voltage balancing becomes the principal limitation for multilevel inverters.

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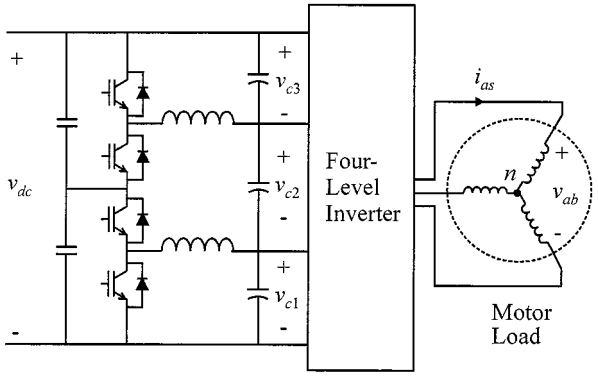

Fig. 1. Proposed four-level two-quadrant dc/dc converter.

One of the most popular industrial multilevel inverters is the diode-clamped three-level inverter [5], [7], [8], [10]. It has been well established that the dc capacitor voltages can be readily balanced through the use of straightforward selection of redundant inverter switching states [10]. However, for inverters with a higher number of levels, the voltage balancing through redundant state selection limits the output voltage to 50% of the maximum [12], [13]. For this reason, some systems incorporate auxiliary dc/dc converters for capacitor voltage balancing [14]–[17]. Three-level boost dc/dc converters have been proposed for systems that are powered from a low-voltage source such as a battery, fuel cell, or superconducting magnetic energy storage (SMES) [18]–[21]. A four-level dc/dc boost converter has been recently introduced for supplying a four-level inverter [22]. In this paper, a novel four-level dc/dc buck/boost converter is presented. For unidirectional power flow motor drive applications, such as naval ship propulsion, the buck operation is of primary interest. Steady-state and average-value models are developed for buck operation and compared in simulation. The buck converter is constructed in the laboratory and validated on a four-level motor drive system.

II. Proposed Four-Level Dc/Dc Converter

Fig. 1 shows the proposed two-quadrant dc/dc converter connected to a four-level motor drive. This converter is capable of operation in buck or boost mode depending on whether the $v_{\rm dc}$ is supplying or absorbing power respectively. It should be pointed out that the series IGBTs in Fig. 1 are included for voltage sharing. Using this structure, each dc/dc converter IGBT will be required to block half of the dc-link voltage. In practice, snubber capacitors can be connected to the junction of the series IGBTs as shown in Fig. 1. This is necessary so that adequate inductor current switching can be ensured. These capacitors are

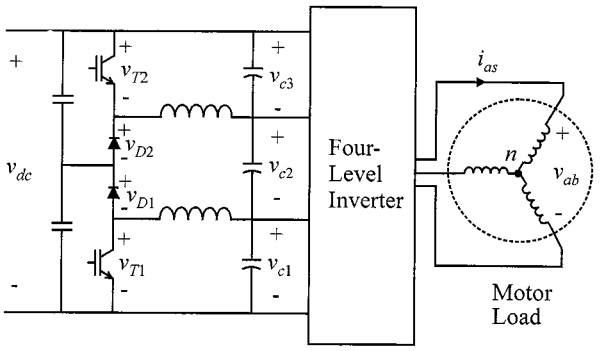

Fig. 2. Proposed four-level one-quadrant boost converter.

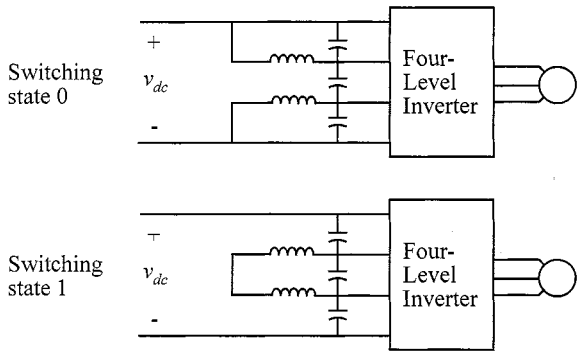

Fig. 3. Four-level dc/dc converter switching states.

small-microfarad high-frequency (polypropylene) types. As an example of how they assist commutation, consider the circuit of Fig. 1 where the upper and lower IGBTs are gated on. If there is a slight difference in the inductor currents (perhaps due to slightly different inductances) then the difference in current can flow into the capacitor junction when entering the next state where the outer IGBTs are gated off and the inner IGBTs are gated on. Low-wattage resistors can also be connected in parallel with the snubber capacitors to ensure steady-state voltage sharing.

In many systems, such as naval propulsion systems, bidirectional power flow is not necessary and the topology may be reduced to the one-quadrant version shown in Fig. 2. It should be pointed out that this specific topology was first introduced in [17]. The study herein expands on this concept by providing mathematical modeling and laboratory verification under load. As will be described herein, this converter regulates the center capacitor voltage v_{c2} by performing a buck operation from the supplied dc voltage $v_{\rm dc}$. This is significant since the four-level inverter will tend to discharge the center capacitor from its ideal value of $(1/3)v_{\rm dc}$. It will also be shown that the buck converter does not regulate the upper and lower capacitor voltages v_{c1} and v_{c3}. These voltages will be balanced through redundant state selection (RSS) from the inverter.

Fig. 3 shows the two reasonable switching states for the buck converter. State 0 is achieved by gating both transistor switches on. As can be seen, this will increase the charge on the center capacitor through the converter inductors. When the transistors are gated off, the inductor current continues to flow in the diodes resulting in state 1. In this switching state, the inductor current

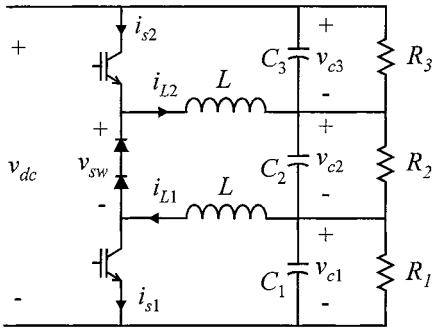

Fig. 4. Four-level converter with resistive load.

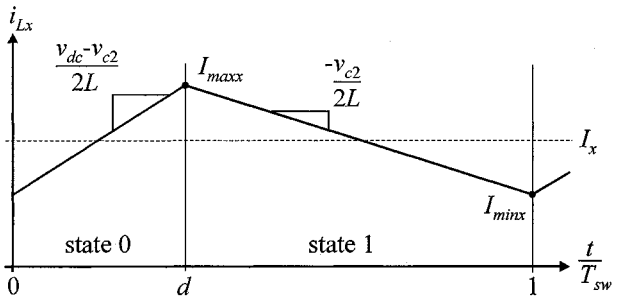

Fig. 5. Steady-state inductor current waveform.

is again charging the center capacitor. Switching between the states is performed at a constant clock rate with a duty cycle according to

$$\text{state} = \begin{cases} 0, & 0 \le t < dT_{\rm sw} \\ 1, & dT_{\rm sw} \le t \le T_{\rm sw} \end{cases} \tag{1}$$

where $T_{\rm sw}$ is the switching period and d is the duty cycle.

III. Steady-State Modeling

As with other types of dc/dc converters, it is instructive to perform a steady-state analysis of the converter driving a resistive load [18]–[20], [23]. Fig. 4 shows the topology for this analysis. If continuous current operation is assumed, the inductor current waveform will appear as shown in Fig. 5. Therein, the current i_{Lx} represents the current in either inductor (x may be 1 or 2). This is done since the current in both inductors is identical if the inductors are matched and the load is symmetrical. The current slopes are depicted in Fig. 5, which represent the inductor voltage divided by L. The average current I_{Lx} as well as the maximum current $I_{\max x}$ and minimum current $I_{\min x}$ are also defined. The analysis begins by setting the average inductor voltage to zero, resulting in

$$v_{c2} = dv_{\rm dc}. \tag{2}$$

From (2), it can be determined that it is optimal to set $d = 1/3$ since that will result in $v_{c2} = (1/3)v_{\rm dc}$ and that will be utilized in the studies to follow. However, a regulating control may be added to determine d in order to maintain good capacitor balancing under transient conditions or provide control in the discontinuous current mode.

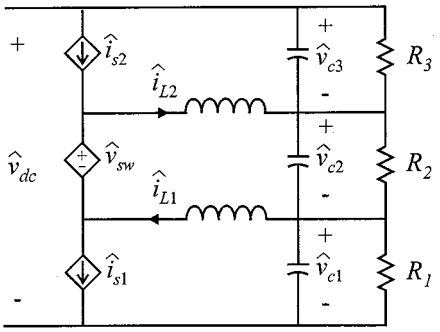

Fig. 6. Four-level buck converter NLAM structure.

From the inductor current slope and the definition of the average current I_{Lx}, it may be shown that the maximum and minimum current are

$$I_{\max x} = I_{Lx} + \frac{(1-d)T_{\rm sw}v_{c2}}{4L} \tag{3}$$

$$I_{\min x} = I_{Lx} - \frac{(1-d)T_{\rm sw}v_{c2}}{4L}. \tag{4}$$

The average current depends on the load and may be expressed for inductors 1 and 2 as

$$I_{L2} = \frac{v_{c2}}{R_2} - \frac{v_{c3}}{R_3} \tag{5}$$

$$I_{L1} = \frac{v_{c2}}{R_2} - \frac{v_{c1}}{R_1}. \tag{6}$$

It can be seen from (5) and (6) that the average currents in both inductors will be equal if $v_{c1} = v_{c3}$ and $R_1 = R_3$. This 1–3 symmetry is typical of inverter loads and by assuming such symmetry, and setting $I_{\min} = 0$, it can be shown that

$$L \geq \frac{T_{\rm sw}R_1R_2}{6(R_1 - R_2)} \tag{7}$$

in order to avoid discontinuous current operation. If the inductance is fixed, the switching period may be set to

$$T_{\rm sw} \leq \frac{6L(R_1 - R_2)}{R_1R_2} \tag{8}$$

in order to avoid discontinuous current operation.

IV. Non-Linear Average-Value Modeling

The general concept of nonlinear average-value models (NLAMs) is that the high-frequency switching of the power converter is represented on an average-value basis. These models provide insight into the operation of switching converters as well as suggest control strategies. Another advantage of NLAMs is that some simulation packages can linearize these models about an operating point and determine the state-space matrices. From this information, classical control theory can be applied [24], [25].

Fig. 6 shows the general structure of the NLAM where the converter switches have been replaced by dependent voltage and current sources. Therein, the $\hat{}$ symbol denotes the fast average which is the average value of the quantity over one switching cycle of the converter $T_{\rm sw}$. The converter waveforms used for determining the dependant source equations are shown in Fig. 7.

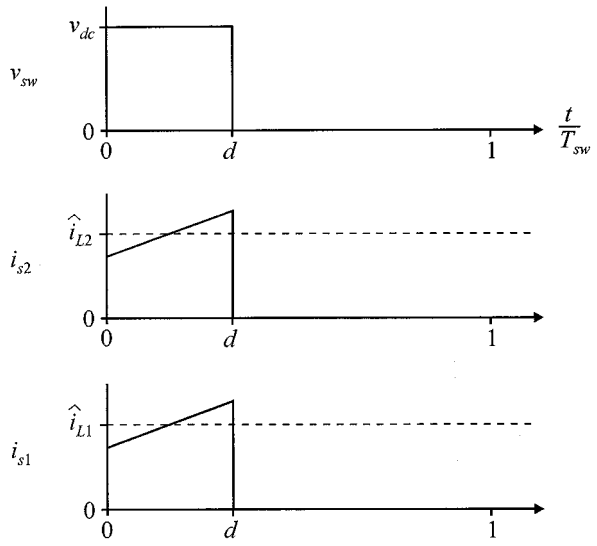

Fig. 7. Converter switching waveforms.

If the inductor current ripple is neglected, the average-value equations are

$$\hat{v}_{\rm sw} = d\hat{v}_{\rm dc} \tag{9}$$

$$\hat{i}_{s1} = d\hat{i}_{L1} \tag{10}$$

$$\hat{i}_{s2} = d\hat{i}_{L2}. \tag{11}$$

It is instructive to consider the insights into converter operation that the NLAM model provides. From the steady-state operation of the equivalent circuit, the relationship given in (1) can be directly seen. Furthermore, it can be seen that the voltages v_{c1} and v_{c3} are not directly determined by the converter, but instead depend on the load resistors.

V. DC/DC Converter Simulation Studies

Detailed and NLAM-based simulations were performed on the buck converter circuits shown in Fig. 4. For the detailed simulation, the switching period was set to $T_{\rm sw}95.2$ μs. The dc input voltage was $v_{\rm dc} = 648$ V. The converter inductance was $L = 2.9$ mH and the capacitor values were $C_1 = C_2 = C_3 = 3100$ μF. The upper and lower resistor values were set to $R_1 = R_3 = 20\ \Omega$ and the center resistor was stepped from $R_2 = 11.6\ \Omega$ to $R_2 = 3.7\ \Omega$.

Figs. 8 and 9 show the simulation results for the detailed and NLAM models, respectively. As can be seen, the center capacitor voltage drops when the load is stepped, but then settles back to its original value. The inductor current increases as the power to the load increases. As can be seen, the NLAM predicts the dynamic performance of the converter but neglects the high-frequency switching. As a result, the NLAM simulation ran four times faster than the detailed model.

VI. Four-Level Inverter

Fig. 10 illustrates a four-level diode-clamped inverter [6]–[8], [12], [13]. The general theory of this inverter is that each phase (a, b, or c) can be electrically connected to the junctions d_0,

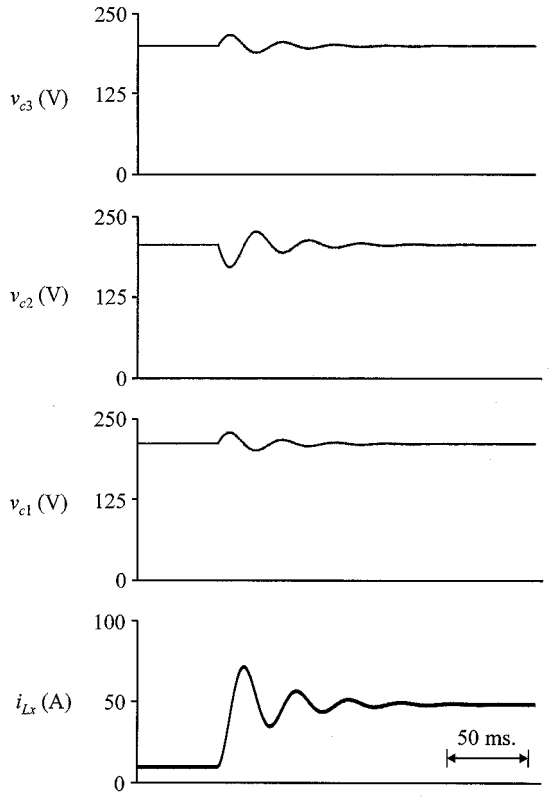

Fig. 8. Converter detailed model performance prediction.

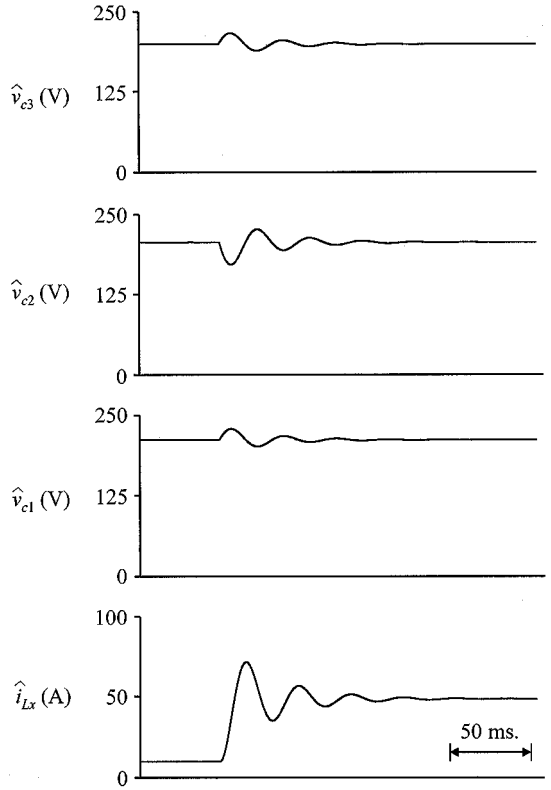

Fig. 9. Average-value model performance prediction.

d_1, d_2, and d_3 by appropriate switching of the inverter transistors. By pulsewidth modulation (PWM), the inverter line-to-ground voltages v_{ag}, v_{bg}, and v_{cg} can be directly controlled.

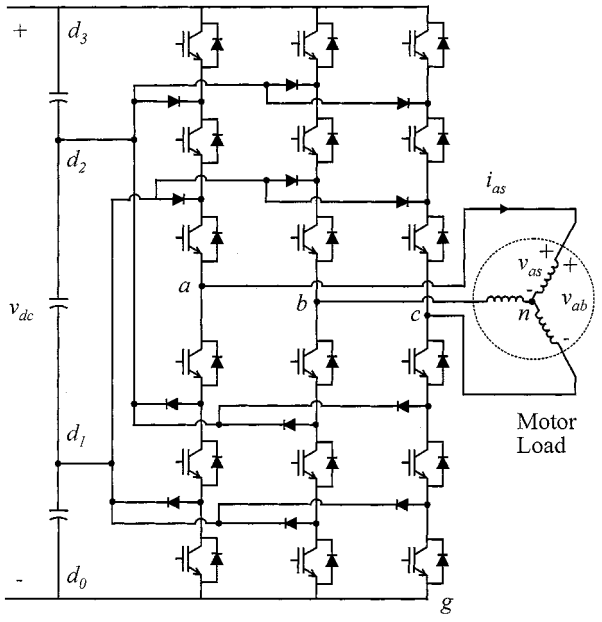

Fig. 10. Four-level inverter topology.

The motor line-to-neutral voltages can be calculated from the line-to-ground voltages by [26]

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \tag{12}$$

Modulation of the line-to-ground voltages may be accomplished with time-domain-based voltage-source methods such as sine-triangle modulation [11], [12] or duty-cycle modulation [22]. These methods rely on a three-phase set of duty cycles, which may be expressed as

$$d_a = \frac{1}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \tag{13}$$

$$d_b = \frac{1}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{14}$$

$$d_c = \frac{1}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{15}$$

where θ_c is the inverter electrical angle and m is the modulation index which ranges from 0 to 1.15 [22]. For constant-frequency operation, the electrical angle may be related to the commanded frequency by

$$\theta_c = 2\pi f^* t. \tag{16}$$

If the duty cycles of (13)–(15) are used in the modulation, then the line-to-ground voltages will contain the same offset, fundamental, and third harmonic terms [22]. From (12), it can be seen that only the fundamental terms will appear on the motor windings resulting in a three-phase sinusoidal set of voltages.

VII. Four-Level System Laboratory Studies

The system shown in Fig. 2 was constructed in the laboratory. The motor load was an 18-kW induction motor loaded by a synchronous generator. For the studies that follow, the dc voltage was $v_{\rm dc} = 648$ V and the modulation parameters were

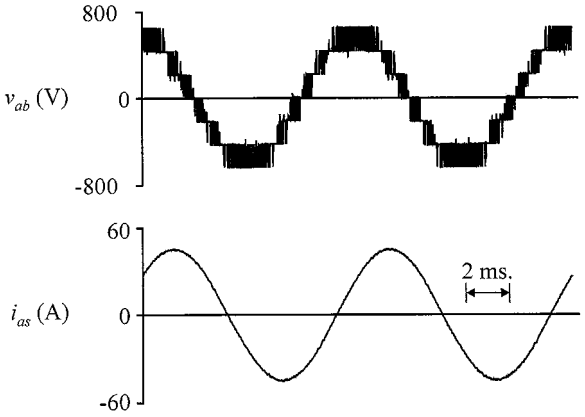

Fig. 11. Measured inverter output waveforms.

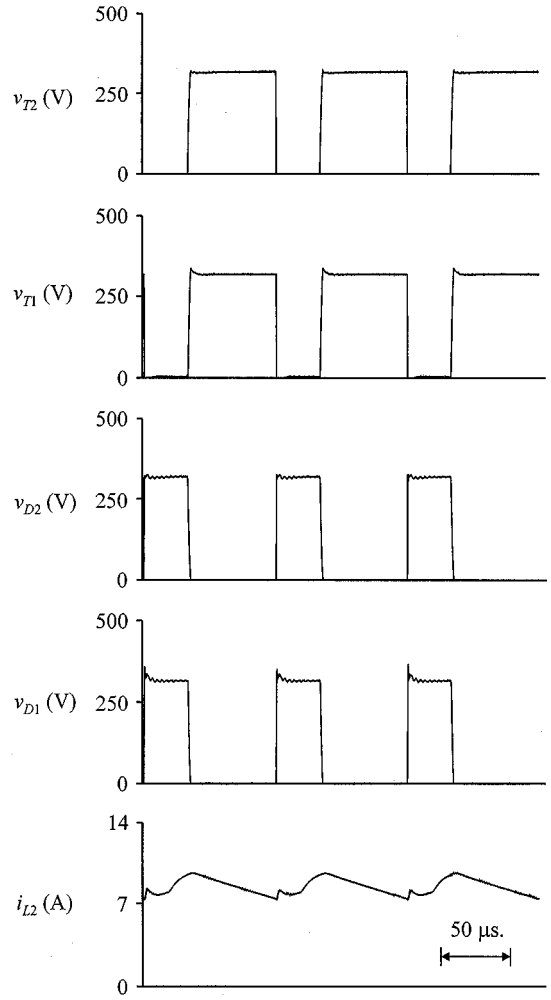

Fig. 12. Measured converter waveforms.

$f^* = 100$ Hz and $m = 1.04$. The buck converter inductance, capacitance, and switching period were the same as with the simulation studies. The system control scheme for the converter was a fairly straightforward triangle comparison circuit to produce PWM signals with a duty cycle of 1/3.

Fig. 11 shows the motor line-to-line voltage and the a-phase current. As can be seen, the voltage waveform exhibits the typical four-level inverter shape [8]. In this case, the fundamental component of the voltage and current waveforms were $v_{ab1} = 636$ V and $i_{as1} = 28.4$ A. The voltage and current total harmonic distortions (THDs) were $\mathrm{THD}(v_{ab}) = 18.3\%$ and $\mathrm{THD}(i_{as}) = 2.22\%$. Measured values for the machine input power and power factor were 13.6 kW and 0.882 lagging, respectively. As stated before, the buck converter regulated the center capacitor and the upper and lower capacitors were balanced by redundant state selection within the inverter [13]. In this study, the capacitor voltages measured $v_{c1} = v_{c2} = v_{c3} = 216$ V. Fig. 12 shows the buck converter semiconductor voltages and inductor current as labeled in Fig. 2. This figure demonstrates the voltage sharing of the IGBTs and diodes. Fig. 13 demonstrates a transient study where the motor drive system is operating at rated power and the dc/dc converter is turned off. Although capacitor voltage balancing is incorporated in the inverter-switching algorithm, it is not effective at this modulation index and the center capacitor voltage discharges to zero.

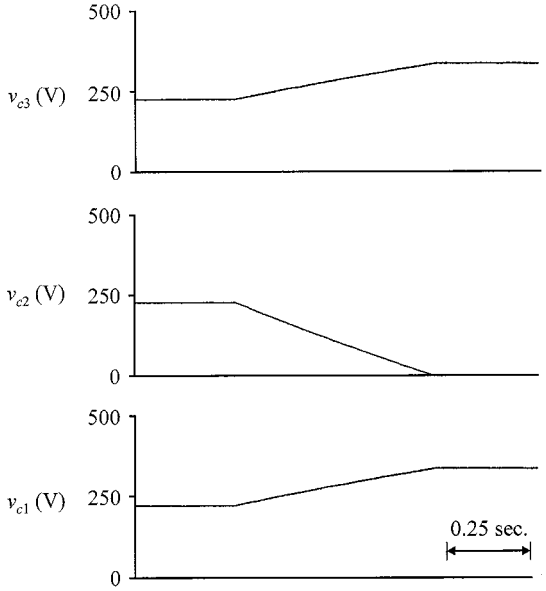

Fig. 13. Measured capacitor voltages in transient state.

VIII. Conclusion

This paper has presented an analysis of a four-level dc/dc buck converter, which is designed to supply a four-level inverter. Detailed and average-value models were developed. A computer simulation showed that the average-value model accurately predicted the dynamics of the buck converter when compared to the detailed model. The new converter was constructed in the laboratory and tested on a four-level motor drive. It was demonstrated that the buck converter was necessary for regulating the capacitor voltages at a high modulation index.

Acknowledgment

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