01 Jan 2007

Experimental Investigation of the ESD Sensitivity of an 8-Bit Microcontroller

Lijun Han

Jayong Koo

David Pommerenke
Missouri University of Science and Technology, davidjp@mst.edu

Daryl G. Beetner
Missouri University of Science and Technology, daryl@mst.edu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1613

Recommended Citation

L. Han et al., "Experimental Investigation of the ESD Sensitivity of an 8-Bit Microcontroller," *Proceedings of the 2007 IEEE International Symposium on Electromagnetic Compatibility (2007, Honolulu, HI)*, Institute of Electrical and Electronics Engineers (IEEE), Jan 2007.
The definitive version is available at https://doi.org/10.1109/ISEMC.2007.173

Experimental Investigation of the ESD Sensitivity of an 8-Bit Microcontroller

Lijun Han, Jayong Koo, David Pommerenke and Daryl Beetner
ECE Department, University of Missouri-Rolla
Rolla, MO, USA 65401
davidjp@umr.edu

Ross Carlton
Freescale semiconductor Inc.
6501 WM. Cannon Dr. West,
Austin, Texas 78735
Ross.Carlton@freescale.com

***Abstract*—In this paper, the susceptibility of an 8-bit microcontroller to electrostatic discharge (ESD) and electrically fast transients was tested by injecting currents through a capacitive probe into the microcontroller package pins. The reaction of the microcontroller to discharges with different rise times and polarities were investigated by measuring the voltage on the tested pins and by observing the microcontroller's clock output. Susceptibility varied significantly when injecting to one pin compared to another. Interestingly, the clock was more sensitive to currents injected into I/O pins than into pins directly related to the clock (e.g. EXTAL). Further work is underway to explain the causes of susceptibility inside the IC.**

***Keywords:* electrostatic discharge, sensitivity, microcontroller, immunity, testing;**

I. INTRODUCTION

Low-cost microcontroller-based embedded applications are particularly sensitive to performance degradation during electrostatic discharge (ESD) or electrically fast transient (EFT) events. This sensitivity to fast transients is to be expected, even for those microcontrollers running at relatively low clock frequencies, due to the process technologies used to fabricate the chips. Modern microcontrollers are implemented with technologies using transistor gate lengths in the 0.65 µm to 90 nm range. These gate lengths are capable of generating and responding to signals with a rise time in the sub-nanosecond range. Integrated circuits (ICs) based on submicron process technologies are capable of responding to fast transients injected onto its pins. Controlling ESD/EFT events at the IC level is particularly important for microcontrollers, since these ICs are used in very cost-sensitive safety-critical applications, where it may not be practical to solve ESD/EFT problems at the board level and where IC failure can have much more significant consequences than simply needing to reboot your computer.

In order to quantify the sensitivity of a modern 8-bit microcontroller to ESD/EFT events, an 8-bit microcontroller fabricated with a commercially available 0.25 µm, 4-layer metal process technology was selected for analysis. General I/O pins, power and ground pins, and three standard microcontroller pins that are typically most susceptible to fast transients (i.e. the reset pin, the interrupt request pin, and the external clock reference input pin) were tested by injecting fast rise-time pulses onto the pins through a capacitive probe. The pin voltages were recorded during injection and the reactions of the microcontroller to these injections were analyzed.

II. METHODS

The basic measurement setup is shown in Fig. 1. The IC under test is an 8-bit microcontroller in a QFP 64-pin package using a 5 V supply voltage. The microcontroller can run under four different operating modes plus an off mode which can be used for programming and debugging. Depending on the CPU mode and on the internal clock configuration, the CPU clock may run at speeds from 32 kHz to 40 MHz. In the tests, the microcontroller was set to run at from 4 to 40 MHz.

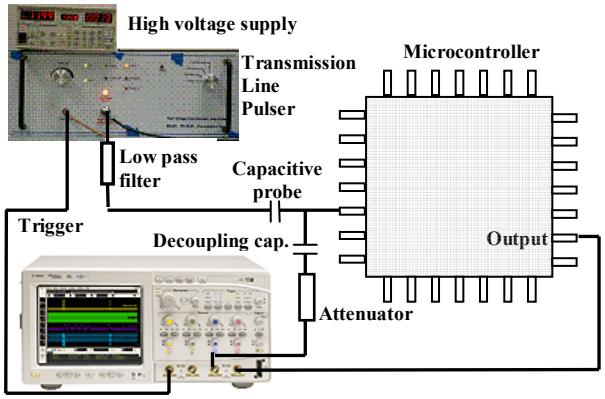

Figure 1. Measurement setup.

The fast rise-time pulses used in our tests were generated by a transmission line pulser (TLP) built by our lab. In the tests, the TLP was connected to a high voltage supply such that the pulse amplitudes can be up to 5 kV. The rise times of the pulses were typically around 200~400 ps. The current injected into a package pin through the capacitive probe is a function of the derivative of the injected voltage with time. Without filtering, this current has a rise time comparable to an ESD event. By placing a high-voltage low-pass filter at the output of the TLP, the rise time can be increased to 5.4 ns, which is suitable for simulating electrically fast transients (EFTs). An example of the TLP voltage waveform with and without a low-pass filter (LPF) added is shown in Fig. 2. The TLP supply voltage was

1-4244-1350-8/07/$25.00 ©2007 IEEE

set to 500 V and a 40-dB attenuator was placed in series with the input of the oscilloscope. The corresponding voltage measured on a 50-ohm trace when the trace and TLP were coupled with a capacitive probe is shown in Fig. 3. A 20-dB attenuator was placed in series with the input of the oscilloscope in this case. The capacitive probe used in this and other experiments presented in this manuscript was made from a coaxial cable by soldering the center conductor of one cable to the shield of another as shown in Fig. 4. The resulting capacitance is around 1~2 pF. The coaxial cable connection was also glued with epoxy to provide additional support to the probe tip.

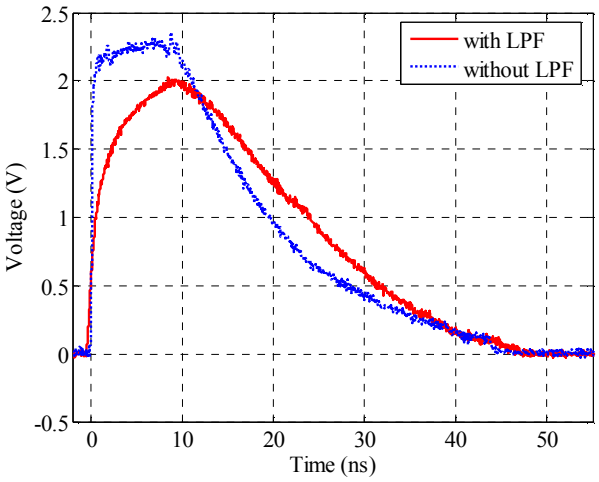

Figure 2. Voltage waveform from the TLP under normal conditions and when using a low-pass filter (LPF).

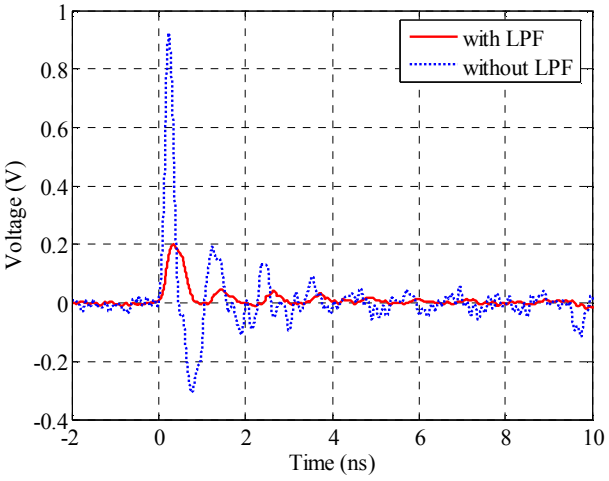

Figure 3. Voltage induced on a 50-ohm trace by the TLP through a capacitive probe.

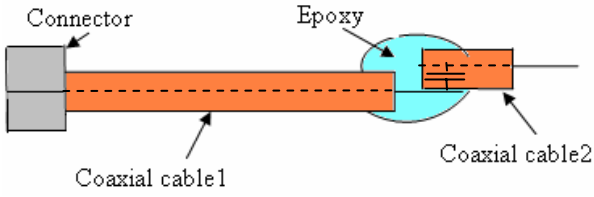

Figure 4. The capacitive probe.

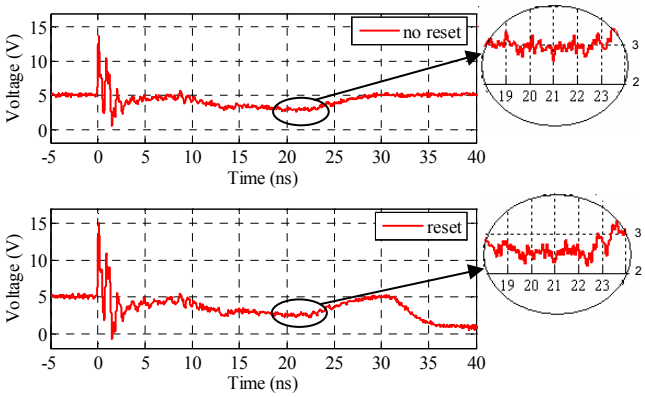

Figure 5. Voltage waveform on the reset pin using a positive injection pulse without a low-pass filter. The top plot was produced with a TLP voltage of 300 V. The bottom plot with a TLP voltage of 350 V.

III. RESULTS

A. *Reset pin*

Reset can be triggered from either an external signal or from a request internal to the processor. The processor is reset when the reset pin voltage is driven lower than V_{IL}. Fig. 5 shows the voltage waveform on the reset pin when a positive pulse was injected onto the reset pin through the capacitive probe. The low-pass filter was not used in the measurement. The top waveform was generated when the TLP voltage was 300 V. This waveform did not trigger a reset. The bottom waveform was generated when the TLP voltage was 350 V and did trigger a reset. In the second waveform, the pin voltage dropped below V_{IL} (approximately 2.5 V) about 20 ns after the pulse was applied. 12 ns later, the microcontroller pulled the reset pin low internally in response to the detected low level on the reset pin. This response is part of the microcontroller design. Both pulses cause the reset pin to fall below V_{IL} during the first few nanoseconds of the pulse; however, the voltage only goes low for a very short time during this period. A filter internal to the microcontroller prevents it from reacting to a low-level that occurs for only a very short time.

In addition to a fast rise-time positive pulse, negative polarity pulses and pulses with long rise time were also tested. Fig. 6 shows voltage waveforms measured at the reset pin when a pulse was injected using TLP supply voltages of 450 V, -150 V and -200 V, when using and not using a low-pass filter. These were the minimum TLP voltage magnitudes that triggered a reset. Not surprisingly, the negative pulse quickly caused the reset pin voltage to drop and was able to induce a reset with a lower magnitude TLP voltage than a positive pulse. Using the low-pass filter resulted in a smaller change in the reset pin voltage for the same applied voltage level at the TLP and also smoothed oscillations in reset pin voltage after the initial pulse.

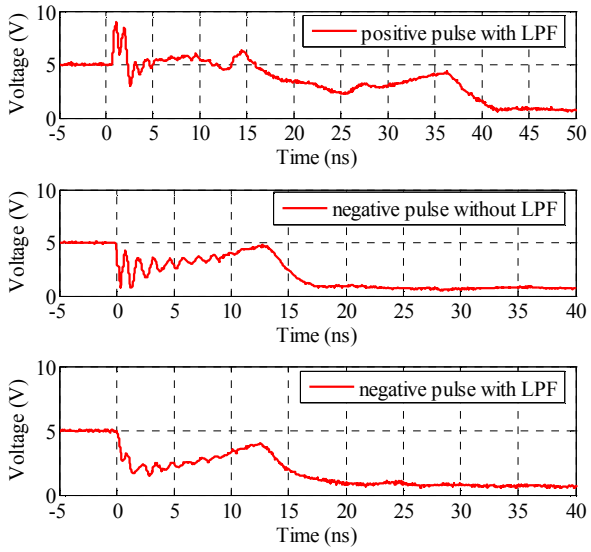

Figure 6. Reset pin voltage waveform. Top: waveform with a 450 V TLP voltage and a low-pass filter. Middle: waveform with a -150 V TLP voltage and no low-pass filter. Bottom: : waveform with a -200 V TLP voltage and with a low-pass filter

B. *General I/O pins*

The microcontroller under test has 54 general I/O pins. These pins may be configured by the user as input or output. As inputs, user may select the pull-up, if any, used by the port As outputs, the user may select slew rate and drive strength. Results of testing only a single I/O pin are presented here, as the behavior of the other I/O pins was similar.

When testing the general I/O pins, the criteria for determining a fault was a repeatable disturbance in the bus clock output pin – that is, a temporary suspension or disappearance of the clock signal. Figs. 7 and 8 show the I/O pin voltage waveform responsible for a fault in the clock output. The waveforms only show the high-frequency portion of the signal since the DC voltage is dependent on the state of the pin (e.g. output high compared to output low). The voltage on the I/O pin causing a fault when the pulse was injected without the low-pass filter was 50 V. The pin voltage causing a fault with the low-pass filter was 40 V. Interestingly, the microcontroller was more sensitive to the slower rise-time pulse. There was no apparent difference in sensitivity to negative or positive polarity pulses. The cause of this sensitivity is under investigation.

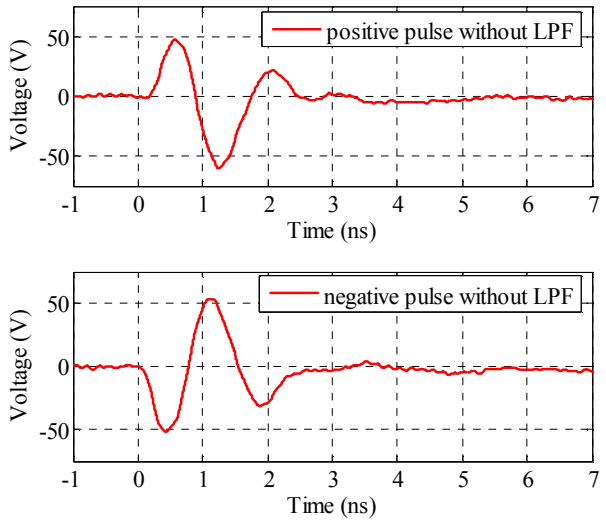

Figure 7. Voltage waveform on I/O pin when a 50 V pulse was injected without using a low-pass filter.

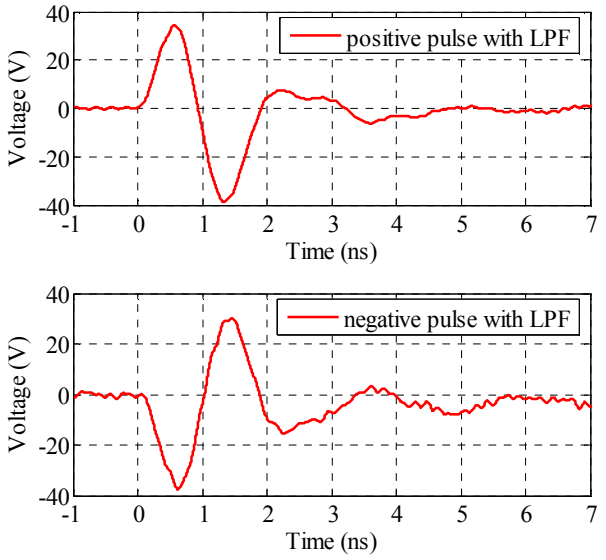

Figure 8. Voltage waveform on I/O pin when a 40 V pulse was injected while using a low-pass filter.

Injecting TLP pulse onto the I/O pins may also interfere the transmitting signals on the I/O pins. To test the sensitivity of the I/O pins, 16 I/O pins were selected and every pin was connected to another directly. The data were sent out from 8 I/O pins and received by the other 8 I/O pins while the TLP pulses were injected onto the I/O pins. By comparing the data transmitted and received, it can be determined if the signal was interfered. Test results shown that the I/O pins will not be able to recognize the signal correctly when the TLP supply voltage increase to around 1 kV. In addition, the microcontroller did not exhibit apparent difference in the sensitivity to the pulse polarities.

C. *External clock reference pin*

The external clock reference pin (EXTAL) connects to a crystal oscillator as shown in Fig. 9. The output of the crystal oscillator can be used directly by the microcontroller as the clock or can be used as a reference clock for an on-board frequency locked loop (FLL). There are two microcontroller running modes which need the external clock reference input. One is the FLL Bypassed External (FBE) mode, which uses the oscillator waveform on the EXTAL pin to directly clock the IC. When testing the FLL bypass mode, the CPU clock was set to run at 4 MHz and the bus clock ran at 2 MHz. The other mode is the FLL Engaged External (FEE) mode, which uses the signal on the EXTAL pin as a reference to the internal frequency locked loop. The frequency locked loop can generate a range of CPU clock frequencies from this reference. When testing the FLL engaged mode, the CPU clock was set to run at 16 MHz and the bus clock ran at 8 MHz. Measurements were performed at the bus clock output pin. The bus clock output pin (MCLK) can be programmed to generate a frequency from $f_{bus}/2$ to $f_{bus}/14$. In both tests, the output frequency was set to $f_{bus}/2$ resulting in a 1 MHz signal on the bus clock output pin while in FLL bypass mode and a 4 MHz signal while in FLL engaged mode. The slew rate control on the MCLK output was disabled to get good clock waveform.

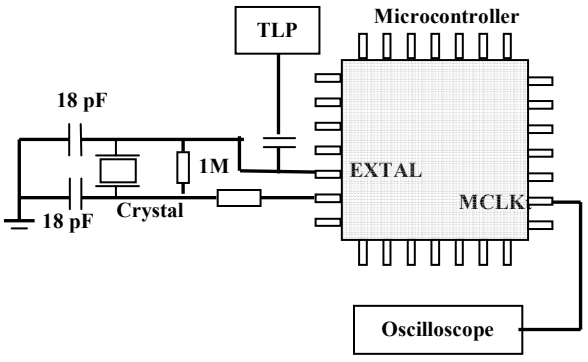

Figure 9. Measurement of the EXTAL pin.

A program was written to monitor two microcontroller register bits: one is the FLL loss of lock status, and the other is the loss of clock status. Both status flags were set to zero on power up or reset. If the FLL has an unexpected loss of lock, the FLL loss of lock status register bit will be set to one. The loss of clock status register bit will be set to one if the internal clock generator loses the clock unexpectedly. The microcontroller was configured to shine one of two LEDs for either event. As before, a fault was defined as a repeatable disturbance in the bus clock as monitored on the bus clock output pin.

At TLP voltages less than 1 kV, abnormal waveforms were only captured during FLL bypass external mode. Although both the FLL bypass external mode and the FLL engaged external modes will initiate self-clocking of the device from an internal reference after the external oscillator input is disturbed (i.e. a loss of the external reference clock is detected), the FLL engaged external mode always uses the internal digitally-controlled oscillator (DCO) to maintain the internal clock while the FLL bypass external mode does not. The digitally controlled oscillator will maintain the operating frequency during a loss or removal of the reference clock and is apparently undisturbed by small, momentary pulses injected on to the external clock reference pin. Even in the FLL bypass external mode, the disruption of the clock was only momentary and the clock was soon recovered. In both modes, the microcontroller detected the loss of the external clock and loss of lock, and the corresponding register bits were set to one. Increasing the disturbance voltage levels above 1 kV, it becomes possible to observe a sustained disturbance to the clock signal in either mode.

Figs. 10 and 11 show measured clock output waveforms recorded while applying a fast rise-time pulse to the clock reference pin in FLL bypass external and in FLL engaged external mode, respectively. Noise and a slight delay in the clock can be seen in Fig. 10 when applying a +100 V TLP voltage pulse in FLL bypass external mode. A -100 V TLP voltage pulse caused a suspension of the clock for approximately 2 clock periods. Small distortions in the clock first begin to appear at a 50 V TLP voltage (for example, the distortion seen at 0 uS in Fig. 10 taken with a 100 V TLP voltage). During low voltage tests, the clock waveform quickly recovered after the stress was removed.

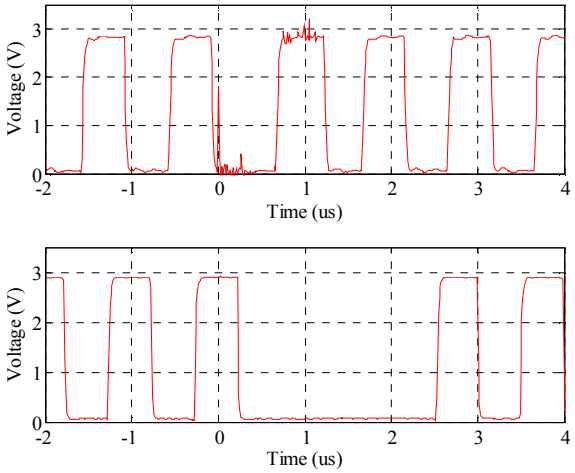

Figure 10. Disturbed bus clock waveforms measured while applying a fast rise-time pulse to the EXTAL pin while in FBE mode. Top: waveform with a 100 V TLP voltage. Bottom: waveform with a -100 V TLP voltage.

Disturbances in the clock could only be observed in FLL engaged external mode when large voltages were used by the TLP. Fig. 11 shows the disturbed clock when a 2250 V TLP voltage fast rise-time pulse and a -1200 V TLP voltage fast rise-time pulse were applied to the clock reference pin. While the voltage necessary to disturb the clock is now relatively high, the time to recover the clock is also now quite long, almost 200 us as shown in Fig. 12. Interestingly, the sensitivity of the pin to positive or negative pulses depended on rise time. Figs 13 and 14 show the clock reference pin voltage waveforms when not using and when using a low-pass filter, respectively. The waveforms were recorded when applying the minimum positive or negative TLP voltage that would cause a disturbance in the clock. When using a fast rise-time pulse, the microcontroller was more sensitive to a negative pulse. When using a slow rise-time pulse, the microcontroller was more sensitive to a positive pulse.

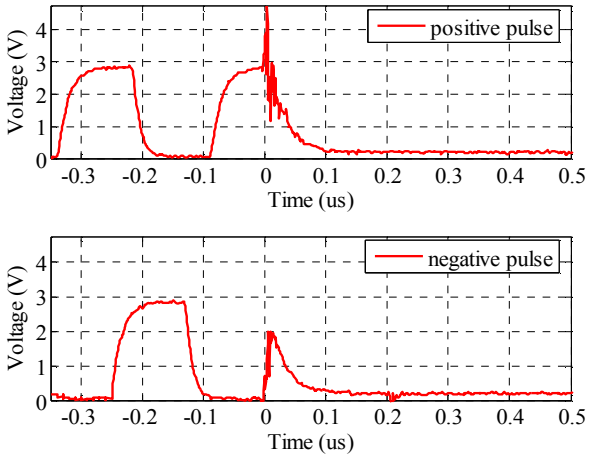

Figure 11. Disturbed bus clock waveforms measured while applying a fast rise-time pulse to the EXTAL pin while in FEE mode. Top: waveform with a 2250 V TLP voltage. Bottom: waveform with a -1200 V TLP voltage.

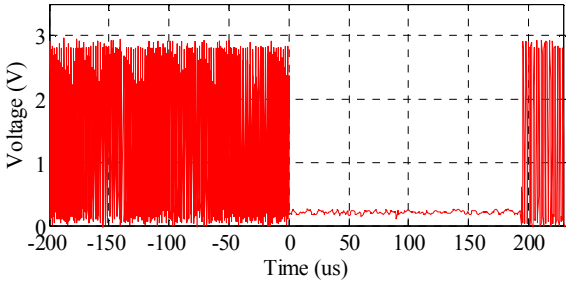

Figure 12. The disturbed bus clock waveform after applying a pulse to the clock reference pin while in FEE mode.

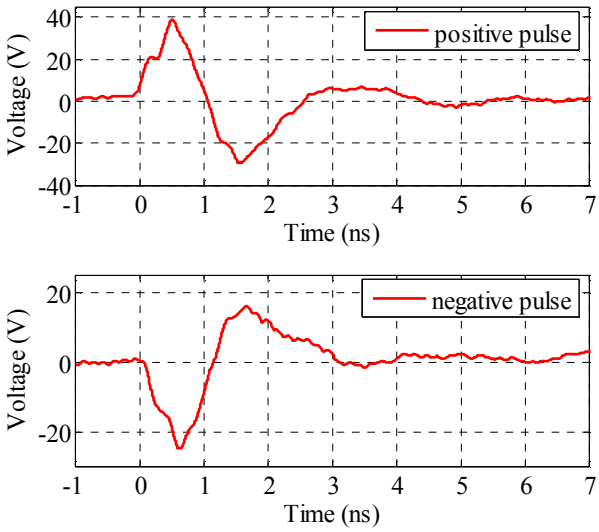

Figure 13. Voltage waveforms on the EXTAL pin when applying a TLP pulse without a low-pass filter.

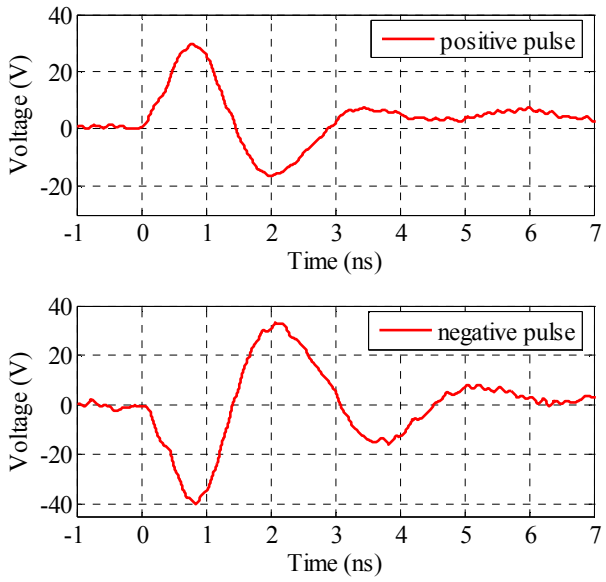

Figure 14. Voltage waveforms on the EXTAL pin when applying a TLP pulse with a low-pass filter.

D. Other package pins

Another pin of interest is the Interrupt Request pin (IRQ). After applying a fast rise-time pulse with a 200 V TLP supply voltage, an interrupt was caused and detected by the software. The IRQ-pin voltage levels that cause the soft error are close for negative and positive polarity pulses.

Power and ground pins were also tested. The power and ground pins have stronger immunity to fast rise-time pulses than other pins, because of the much greater internal decoupling capacitance that is available to them.

IV. CONCLUSION

This paper describes the methodology used to test an 8-bit microcontroller for sensitivity to ESD and electrically fast transient events. Electrically fast transients were simulated with a transmission line pulser using a low-pass filter. Both positive and negative pulses caused a reset event to be detected on the reset pin. Disturbances in the clock could be observed when injecting directly to the clock reference pin. The microcontroller clock was observed to be highly resistant to ESD or transient events when in FLL engaged external mode. The clock was most sensitive when in FLL bypass external mode. In either case, the microcontroller recovered the clock within 200 us of the injected pulse. The most sensitive pins were the general I/O pins. Disturbances in the system clock were observed for pin voltages as low as 40 V when injecting to general I/O pins. These pins were most sensitive to slow rise-time pulses. Interestingly, it was easier to cause a disturbance to the clock by injecting noise on general I/O pins than through pins directly associated with the clock, like the EXTAL pin. This sensitivity of the clock to transients on I/O pins is under investigation.

REFERENCES

[1] International Electro-technical Commision, "IEC 61000-4-2, Testing and Measurement Techniques – Section 2: Electrostatic Discharge Immunity Test," *IEC standard*, 2002, www.ied.ch.

[2] International Electro-technical Commision, "IEC 61000-4-4, Testing and Measurement Techniques – section 4: Electrical Fast Transient/Burst Immunity Test," *IEC standard*, 2002, www.ied.ch.

[3] R. Carlton, G. Racino and J. Suchyta, "Improving the transient immunity performance of microcontroller-based applications," Freescale Semiconductor Inc. application note AN2764.

[4] S. B. Dhia, M. Ramdani and E. Sicard, "Electromagetic Compatibility of Integrated Circuits", Springer 2006.

[5] E. Lamoureux, A. Boyer, S. Dhia and E. Sicard, "Investigations on a conducted agrresion insider a digital integrated circuit", 5th International EMC Compo 05 (EMC Compo 2005) Munich, Allemagne (November 2005)