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Performance of a Quaternary Logic Design

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Abstract—This paper analyzes the performance of a quaternary logic circuit and its components. The multi-valued logic design consisting of two drivers and a transistor matrix is simulated using Mentor Graphic software. Functional operation of the circuit is shown and propagation delay and power consumption are determined. The design is dependent on the voltage values for the multi-valued logic. Three logic cases are investigated. The performance of the logic circuit as a quaternary difference calculator is described.

Index Terms—Multi-valued logic circuits, inverters, memory architecture, circuit simulation

I. INTRODUCTION

Current digital electronics technologies are mainly based upon binary systems. The logic has two truth values which are zeros and ones. Multi-valued logic design has more than two truth values. Multi-valued systems are usually proposed to provide advantages by decreasing the number of data interconnect lines and processing components. Such logic circuits can represent numbers with fewer bits than binary, e.g. the decimal number 255 is represented as 11111111 in binary and 3333 in quaternary. As the circuits become less complicated, the data processing may be faster and more reliable [1,2]. However, multi-valued logic designs are challenging due to difficulties in implementation [3].

The idea of the multi-valued logic, or “fuzzy logic,” opened a vast research area. In 1920, Jan Lukasiewicz began to create a system of many-valued logic [4]. Later, Jan Łukasiewicz and Alfred Tarski together formulated logic on “n” truth values where “n” was equal to or more than two [5]. In 1973, Lotfi A. Zadeh proposed his theory of fuzzy logic [6]. Research continues with the objective of faster and more reliable logic systems [7]. Four-level or quaternary approaches offer improvements in interconnects and pinouts while minimizing implementation problems. The performance of various quaternary implementations must be evaluated [8,9,10].

This paper introduces a quaternary logic circuit and its components. The performance is investigated using Mentor Graphics software. The circuit consists of two drivers that get

inputs and one transistor matrix which yields to a quaternary output. Functional simulations of a driver and the matrix are performed. Applications include use as a quaternary difference calculator. Also, propagation delays and power consumption are determined.

II. OVERVIEW

A. Multi-Valued Logic and Research Issues

The logical circuitry that works with two truth values is called a binary system. In binary calculus, logic is either true, which is represented by 1 or false which is represented by 0. By contrast, quaternary logic uses four truth values. A number in a quaternary system is represented by digits 0, 1, 2, and 3. As a result, operators such as AND, NAND, OR, etc., used for binary logics, cannot be used for quaternary systems.

The research seeks to verify the functional operation of the proposed circuit. In particular, performance as a function of specific quaternary voltage schemes is investigated along with timing and power characteristics.

B. Architecture

A logic circuit is proposed that uses quaternary logic. The components are two drivers that receive the quaternary inputs and a transistor matrix that selects the overall output. Figure 1 shows the schematic of the overall logic circuit. Figures 2 and 3 show the driver and transistor matrix, respectively.

The driver input expects a signal voltage with four levels corresponding to the quaternary values of 0, 1, 2, and 3. Depending on the values of the inputs and the associated logic levels, the driver output corresponding to the logic value will be high and will be selected. The driver outputs are connected to the transistor matrix. The vertical driver selects a row in the transistor matrix and the horizontal driver selects a column. The transistor at the row-column intersection provides a quaternary output. Hence, the circuit performs a quaternary difference calculation.

Driver circuitry, shown in Figure 2, is built from four series inverters, one for each quaternary level. Three lines provide power for the driver. Depending on the three line values, each inverter in the series will trigger at different voltages. For example, an input of logic 2 would ripple through the second series of inverters, but it would not be sufficient for the third or fourth series to turn on. Therefore, output2 of the driver is going to be high and other three outputs will be low.

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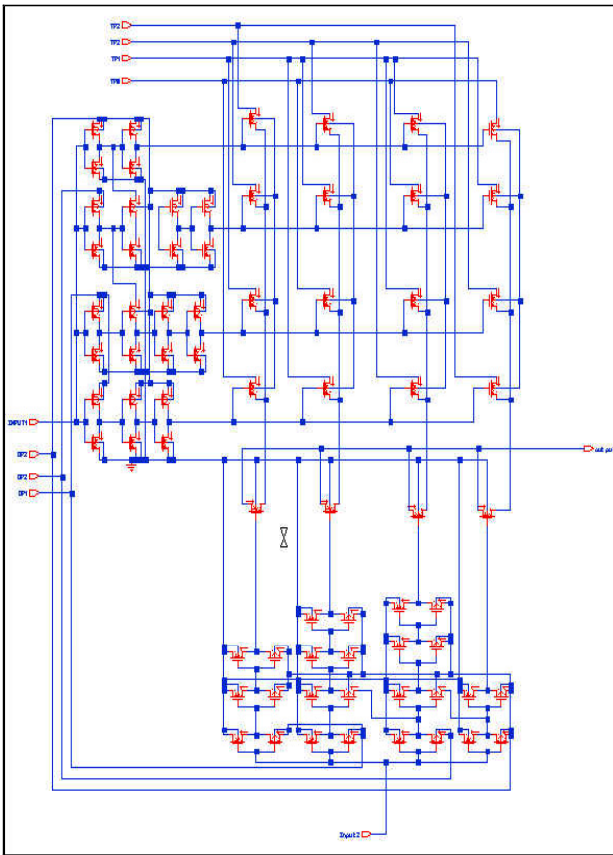


Fig.1 The complete quaternary circuit with two driver components and a transistor matrix component.

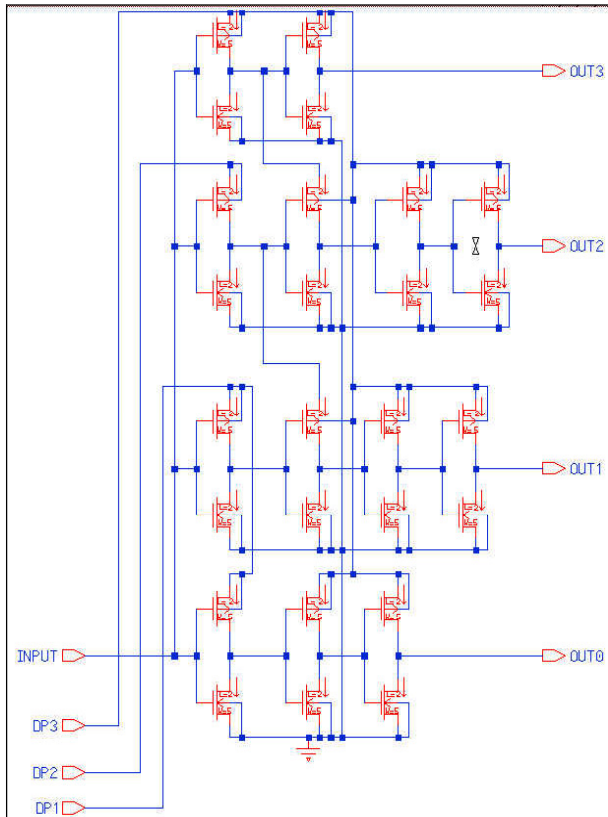


Fig. 2 Schematic of the driver circuit.

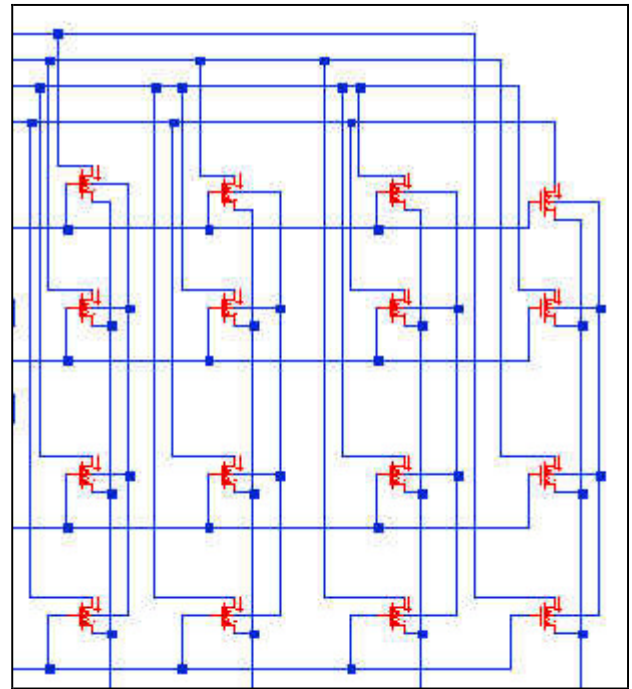


Fig. 3 Schematic of the transistor matrix.

III. CIRCUIT PERFORMANCE

Mentor Graphics' Design Architect and Accusim were used for designing and simulating the proposed circuits. Figures 1, 2, and 3 are taken from Design Architect and the rest of the figures show simulations done in Accusim. In order to observe the functionality of the driver, three voltage discretization schemes for logic levels were tested. Table 1 shows these three logic cases. Table 2 shows all possible combinations of the input voltage pulses to the driver in logic case 1.

Table 1: Three logic cases

Cases	Input Voltage (V)			
Case 1	0	1.00	1.63	2.50
Case 2	0	0.75	1.00	2.25
Case 3	0	1.00	2.00	3.00

Table 2: Six possible sets for logic 1

Sets	input pulse (V)	
	minimum Value	maximum value
Set 1	0	1.00
Set 2	0	1.63
Set 3	0	2.50
Set 4	1.00	1.63
Set 5	1.00	2.50
Set 6	1.63	2.50

A. Functional Simulation

The power for the transistors is provided by the voltages in Table 3. These voltages for the driver power lines determine the transition points. Table 4 shows the applied input voltages to the driver and the corresponding output in logic case 1. Figure 4 shows the simulation of the driver for the first set of

case 1. The last trace on the bottom of Figure 4 shows the input voltage. The input voltage is a pulse with a maximum value of 1.00 volt and a minimum value of zero volts. The third and fourth traces show output2 and output3, respectively, which are zeros. The second trace shows output1 which stays zero while the input is at zero level and goes high as soon as the input is logic level 1. The first trace, output0, is high when input is zero and goes back to zero when the input is 1.00 volt.

Table 3: Power Voltages

Signal	Voltage (V)
DrivePower1	2.00
DrivePower2	3.75
DrivePower3	5.00

Table 4: Logic case 1

Input Voltage	Output 0	Output 1	Output 2	Output 3
0 V	1	0	0	0
1.00 V	0	1	0	0
1.63 V	0	0	1	0
2.50 V	0	0	0	1

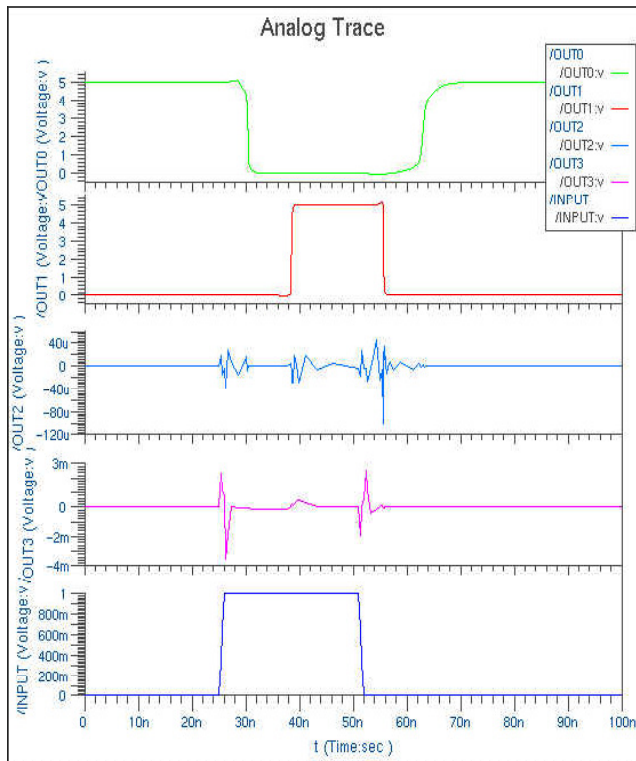


Fig. 4 Simulation of driver for the first set of case 1.

The second set in case 1 is an input pulse with a minimum value of zero and a maximum value of 1.63 volts. When the input is zero, output0 will be high and when the input is 1.63 volts as logic 2, output2 will be high as in Figure 5. In the third set of case 1, Figure 6, the input is 0 to 2.50 volts. Zero input again makes output0 high and 2.50 volts makes output3 high. Hence, 2.50 volts is recognized as logic 3.

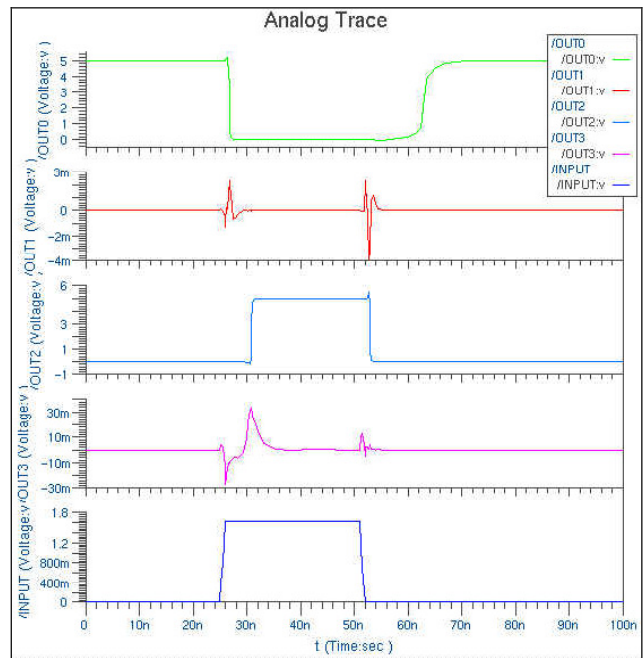


Fig. 5 Simulation of driver for the second set of case 1.

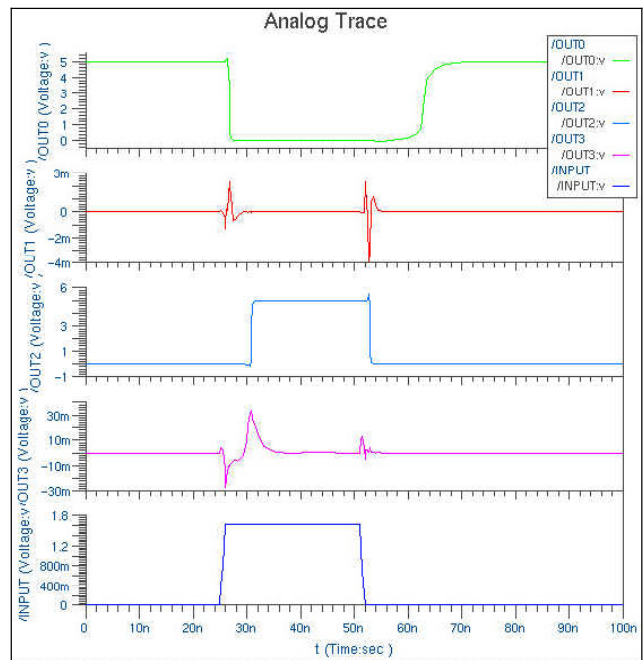


Fig. 6 Simulation of driver for the third set of case 1.

The remaining sets show the desired behavior as specified in Table 4. The fourth set of case1 is a pulse from 1.00 to 1.63 volts. For the 1.00-volt input, output1, which shows logic 1, will be high. And, when the input is 1.63 volts, output2 will be high. In the fifth set of the case 1, the maximum value of the applied pulse signal is 2.50 volts and the minimum value is 1.00 volt. As in the previous case, the 1.00-volt level is logic 1 and output1 is high and the 2.50-volt level makes output3 high. The last set of the first case is an input pulse with a maximum value of 2.50 volts and a minimum value of 1.63 volts. The 2.50-volt input will make output3 high, i.e. logic 3, and 1.63-volt input will make the output2 high, i.e. logic 2.

Two other voltage schemes were applied to the driver to analyze the output (Tables 5 and 6). As shown in Table 5, all outputs in case 2 work properly except for output1. When the input is 0.75 volts, output0 is high, whereas 0.75 volts is logic 1 and output1 should be high. Hence, the functional operation is sensitive to the voltage scheme.

Table 5: Logic case 2

Input Voltage	Output 0	Output 1	Output 2	Output 3
0 V	1	0	0	0
0.75 V	1	0	0	0
1.00 V	0	1	0	0
2.25 V	0	0	1	0

Table 6: Logic case 3

Input Voltage	Output 0	Output 1	Output 2	Output 3
0 V	1	0	0	0
1 V	0	1	0	0
2 V	0	0	0	1
3 V	0	0	0	1

Table 6 shows the operation for the third voltage scheme, i.e. logic case 3. Again, one output does not work properly. When the input is 2.00 volts, or logic 2, output2 should be high, but output3 is high, instead. Further studies are needed on driver voltages to achieve proper results for any logic case.

B. Matrix Simulation

Figure 7 shows the simulation for the matrix component, i.e. providing operation as a difference calculator. Input1 is a pulse from 1.00 volt to 2.50 volts. Input2 for the circuit is a pulse from 1.00 to 1.63 volts. Input1 at logic 1 will select row 2 of the transistor matrix and input2 will select column 2 of the transistor matrix. The transistor at the intersection has its source tied to a voltage representing logic 0, which has now channeled to the output. Table 7 shows the power voltages that provide sufficient separation between logic levels for the circuit to function properly.

Table 7: Power Voltage

Signal	Voltage
TriggerPower0	0 V
TriggerPower1	1 V
TriggerPower2	2 V
TriggerPower3	3 V

When input1 is set to 2.50 volts and input2 to 1.63 volts, row 4 and column 3 of the transistor matrix are selected. The transistor at that intersection has its source tied to a 1.00-volt power supply; hence the output is high and represents logic 1. When input1 and input2 are both 1.00 volt, the output shows zero volts. The transistor at the intersection of the row 2 and the column 2 has its source tied to a zero volts power supply; therefore, the output of the circuit shows zero volts.

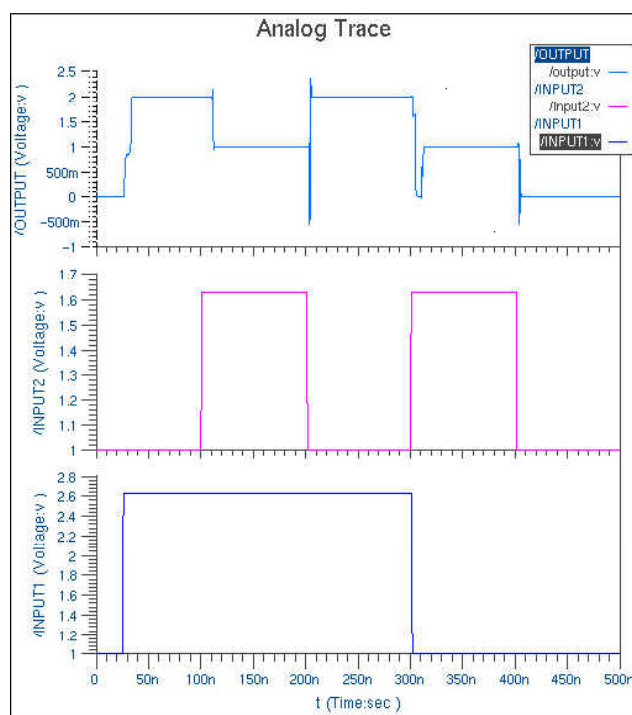


Fig. 7 Simulation of the circuit.

The circuit acts as a quaternary difference calculator. For example, when input1 is at 2.50 volts (logic 3) and input2 is at 1.63 volts (logic 2), the difference between two input signals is 0.87 volts. Hence, the output of the circuit shows 1.00 volt, or logic 1. In the situation with input1 and input2 both at 1.00 volt, the output of the circuit shows zero volts. This quaternary difference configuration is expected to provide fast operation, but it may not be optimal with regard to power.

IV. PARAMETER TESTS

Parameters that are reported in this paper are propagation delays and power consumption. The propagation delays of the driver with different inputs as well as the propagation delay of the matrix are analyzed. The power consumption of the driver is another aspect that is calculated in the steady-state situation.

A. Power Consumption

Power consumption for these electrical circuits is the amount of energy needed for the circuits to continue their performance. The calculated power is in the steady-state situation for the driver. The power consumption is calculated by multiplying driver voltages and currents in each branch attached to the input voltages.

$$P = \sum V_{\text{driver}} I_{\text{driver}}$$

$$P = 5 * 110\mu\text{A} + 3.75 * 60\mu\text{A} + 2 * 15\mu\text{A}$$

$$P = 1.675 \text{ mW}$$

Eq.1

B. Propagation Delay of the Driver

The digital propagation delay measures the time difference between a change in the input to the logic gate and settling of the gate output to a stable level. The smaller the propagation delay of a digital circuit, the faster the data processing. By knowing the propagation delay of the individual gates, more information about the overall propagation delay of the circuit with multiple logic gates can be found. Table 8 shows the signal delays of the circuit in the first set of case1 and Figure 8 shows the simulation for the driver by which the values have been taken. In the rising edge of the input, output0 has a 4.479 ns delay with respect to input and output1 has a 13.177 ns delay with respect to input. A time of 8.360 ns is required for the output1 to rise when output0 goes zero. In the falling edge of the input, output0 has an 11.268 ns delay and output1 has a 4.268 ns delay with respect to the input. Input1 has a 7.548 ns delay with respect to output1. Therefore, for the steady-state condition, the propagation delay of the circuit in the first set of case 1 is 13.177 ns in the rising edge of the input and 11.263 ns in the falling edge of the input.

Table 8: Signal delays for the first set of case 1

Delay (ns)	Input Voltage (V)	
	0 to 1.00 V	1.00 to 0 V
output0 wrt input	4.479 ns	11.263 ns
output1 wrt input	13.177 ns	4.268 ns
output0 wrt output1	8.360 ns	7.548 ns

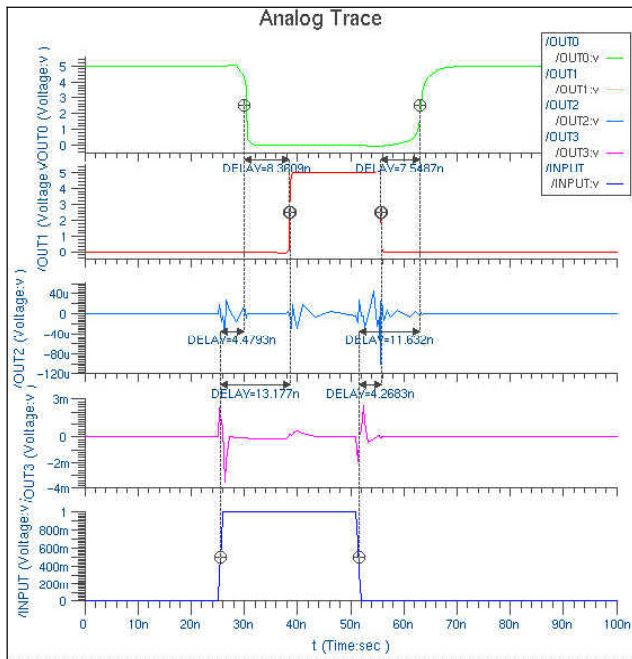


Fig. 8 Calculated signal delays in the first set of case 1.

Table 9 shows the signal delays of the circuit in the second set of the logic case1, in which the input is a pulse with a minimum value of zero and a maximum value of 1.63 volts. In this case, the propagation delay of the circuit is 5.277 ns in the rising edge of the input and 11.520 ns in the falling edge.

Table 9: Signal delays for the second set of case 1

Delay (ns)	Input Voltage (V)	
	0 to 1.63 V	1.63 to 0 V
output0 wrt input	1.018 ns	11.526 ns
output2 wrt input	5.277 ns	1.406 ns
output0 wrt output2	3.862 ns	10.119 ns

Tables 10 and 11 show outputs signal delays with respect to input for the third and fourth sets in case 1, respectively. For the input pulse with a minimum value of zero and a maximum value of 2.50 volts, the delay is 1.039 ns in the rising edge and 11.713 ns in the falling edge. For the input pulse with a minimum value of 1.00 volt and a maximum value of 1.63 volts, the propagation delay is 11.269 ns in the rising edge of the input and 2.922 ns in the falling edge of the input.

Table 10: Signal delays for the third set of case 1

Delay (ns)	Input Voltage (V)	
	0 to 2.50 V	0 to 2.50 V
output0 wrt input	0.579 ns	11.647 ns
output3 wrt input	1.039 ns	0.571 ns
output0 wrt output3	0.613 ns	11.713 ns

Table 11: Signal delays for the fourth set of case 1

Delay (ns)	Input Voltage (V)	
	1.00 to 1.63 V	1.63 to 1.00 V
output1 wrt input	0.839 ns	1.923 ns
output2 wrt input	11.269 ns	0.999 ns
output1 wrt output2	10.429 ns	2.922 ns

Tables 12 and 13 are for the fifth and sixth sets of the case 1, respectively. When the input of the driver is a pulse from 1.00 to 2.50 volts, the total of a 6.278 ns delay in the rising edge of the input and a 2.815 ns delay in the falling edge of the input makes the driver work in the steady-state condition. Therefore, the propagation delay of the driver is 6.278 in the rising edge of the input and 2.815 in the falling edge of the input. With a pulse of 1.63 volts as minimum value and 2.50 volts as maximum value, it has a 7.880 ns propagation delay in the rising edge of the input and 3.490 ns in the falling edge.

Table 12: Signal delays for the fifth set of case 1

Delay (ns)	Input Voltage (V)	
	1.00 to 2.50 V	2.50 to 1.00 V
output1 wrt input	6.278 ns	2.815 ns
output3 wrt input	1.437 ns	0.460 ns
output1 wrt output3	4.278 ns	2.354 ns

Table 13: Signal delays for the sixth set of case 1

Delay (ns)	Input Voltage (V)	
	1.63 to 2.50 V	2.50 to 1.63 V
output2 wrt input	7.888 ns	3.49 ns
output3 wrt input	1.592 ns	1.206 ns
output2 wrt output3	6.296 ns	2.284 ns

C. Propagation Delay of the Matrix

Figure 9 shows the performance of the matrix component the determination of signal delays. Typically, a delay of 8 ns is needed for the output to respond to the changes in the rising edge of the inputs and 3 ns in the falling edge of the input. Therefore, for the quaternary difference calculator, the propagation delay is 8 ns in rising edge of the input and 3 ns in the falling edge of the input.

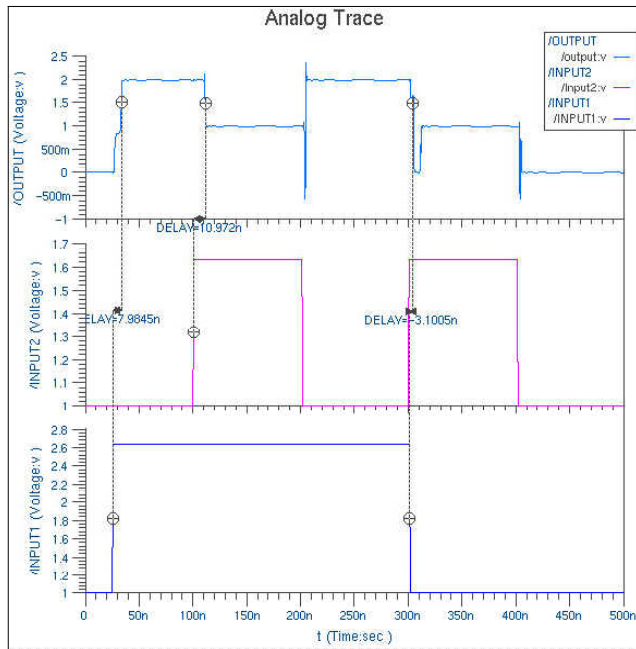


Fig. 9 Calculated delays in the matrix

V. SUMMARY

As electronics technology advances, faster and less complicated designs are desired. Multi-valued logic approaches offer advantages, but the performance of specific circuit implementations must be analyzed. Multi-valued logic inputs or outputs can be defined as any n-valued truth values where “n” is greater than 2. A four-level, or quaternary, approach was the subject of this paper.

A quaternary circuit was proposed and a functional simulation of its components has been performed. It was observed that driver circuitry can be used to represent the quaternary logic of the input. One case worked properly, but additional cases had isolated errors. The sensitivity of the performance to the voltage levels will require more analysis. The circuitry of the matrix can be used as a quaternary difference calculator. The circuit receives two inputs and presents the difference between the inputs in four-level logic. The propagation delay of the driver and matrix was analyzed. A typical delay of 8 ns is needed for the circuit to respond to the changes of the input and act in a steady-state situation. The calculated power consumption of the driver was 1.675 mW in the steady-state situation.

Future research is required on the proposed circuits. The power inputs to the driver need to be completely characterized for the range of possible inputs. After refinements, the circuit can be implemented in a specific semiconductor technology. Applications such as processing of sensor signals may use the driver design and take the advantages of its potential for fast and reliable response [11]. Furthermore, the circuitry acting as a difference calculator can be used in preprocessors.

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