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### Recommended Citation

M. A. Cracraft et al., "Modeling Issues for Full-Wave Numerical EMI Simulation," *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility (2003, Boston, MA)*, vol. 1, pp. 335-340, Institute of Electrical and Electronics Engineers (IEEE), Aug 2003.

The definitive version is available at <https://doi.org/10.1109/ISEMC.2003.1236617>

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# Modeling Issues for Full-Wave Numerical EMI Simulation

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**Abstract**—In electromagnetic modeling, agreement between modeling and measurements is a common goal. There are questions that define every model. What is to be modeled? How is it going to be modeled? At what scale is it to be modeled? Through sample results and discussion, this paper addresses some general and some specific elements of model veracity. Through determination, numerical models can certainly be pushed to match any measured results. However, in the end the question that this paper addresses is not necessarily “How good can this model be?” as it is “Is this model good enough?”

## I. INTRODUCTION

A common goal in electromagnetic compatibility is matching a numerical model to a measurement. When developing a numerical model, there are three questions that need to be answered.

- 1) What will be modeled?
- 2) How will it be modeled?
- 3) At what scale will it be modeled?

These questions are not independent nor are their answers unique. Further, the answers to these questions are often full of more questions.

### A. What will be modeled?

The focus of the model may be a shielding enclosure, a printed circuit board (PCB), an antenna, or any number of other structures. Even with the few examples just given, the relevant geometric and temporal scales may differ by several orders of magnitude. Thus, there is no one way to model every possibility in a practical time frame.

### B. How will it be modeled?

Each class of problems should be considered separately to make sure that physics are being applied properly. This consideration includes using a proper equation of motion and defining and enforcing the boundary conditions. Specifically how the fields or circuit parameters are calculated and how the boundary conditions are enforced depend on the method. The Finite-Difference Time-Domain (FDTD) method, which is developed well in [1], was used almost exclusively for the models presented here. However, the ideas presented can be applied to any method.

### C. At what scale will it be modeled?

Defining the numerical model depends on the scale of the details of the structure. An integrated circuit chip has detail on a totally different detail level than a shield chamber. The same contrast exists in a temporal sense.

Again relating the model to the measurement, if the variable of interest can only be measured to a certain level with a certain sensitivity, modeling the same problem to a greater precision is unnecessary.

### D. What is good enough?

In addition to the questions posed, there is yet another question: “What is good enough?” That one question influences the answers to each of the prior questions. The only perfect model for an object is the object itself. The rest of this paper gives specific problems and the models that were good enough for them, as well as suggestions on how the models could be made better if needed.

## II. MEASURING THE INDUCED CURRENTS ON A MONOPOLE WITH A CURRENT PROBE

The common-mode current on external cables of a device under test (DUT) is a good indicator of the electromagnetic interference (EMI) that will be radiated by the DUT. In [2] a measurement technique was introduced to measure the common-mode current induced by a signal current. A variation on that test setup, shown in Figure 1 from [2], was constructed to gauge the effective frequency range of the technique.

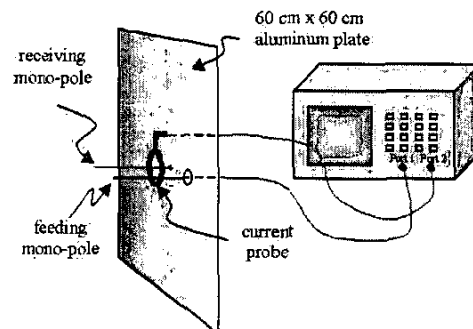


Fig. 1. Current probe setup for measuring the EMI from a monopole

### A. The Construction and the Measurement

For the measurement, an HP8753D network analyzer was used along with a Fischer F-2000 clamp-on current probe. In addition to a standard open-short-load calibration, the transfer characteristics of the current probe were compensated for in a calibration procedure described in [3].

The measurement structure consists of a wide aluminum ground plane, one monopole connected to an SMA bulkhead connector fixed to the ground plane, and one monopole shorted to the ground plane. Port 1 of the network analyzer was used to drive the first monopole with the SMA connector. Port 2 was connected to the current probe, which was clamped around the shorted monopole. All of these components affect the fields around the structure. However, modeling every tiny detail would result in an extremely long computation time.

### B. The Numerical Modeling

When applying the FDTD method to the structure, it is the smallest details that determine the cell size for the model. It is possible to create a graded mesh where the cell size can vary. However, the smallest cell still defines the largest time step that can be used in this multistep algorithm. The discussion of the specific relation between the spatial and time steps is beyond the scope of this paper. See Chapters 2 and 4 of [1] for reference. For this paper, it is sufficient to say that as the spatial step decreases so must the time step. Thus, modeling very small details relative to a wavelength requires an impractical amount of time. Subcell algorithms are introduced to allow for more coarse meshes.

The essential objects that are included in this model are each characterized by a form of subcell algorithm. The aluminum plane is modeled as an infinitely thin perfect electric conductor (PEC), a fairly straightforward practice. The  $E_{tan} = 0$  boundary condition is applied over the PEC. The monopole connected to Port 1 is modeled by a thin wire algorithm with a  $50\text{-}\Omega$  voltage source at its base (Figure 2). The shorted

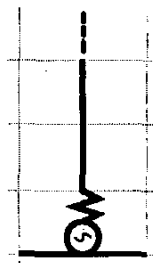


Fig. 2. FDTD model for a monopole antenna

monopole is modeled nearly identical to the Port 1 monopole except that the  $50\text{-}\Omega$  source is replaced by a  $50\text{-}\Omega$  termination. The thin wire algorithm enforces the tangential electric field to be zero. In addition, the thin wire algorithm enforces the adjacent magnetic field components to match that of the quasi-static magnetic field around a wire of a declared radius carrying a specific current density. In this model that condition

is also enforced on the fields around the source of the Port 1 monopole and around the termination of the shorted monopole.

There are alternative ways that the monopole source could be modeled. Figures 3 and 4 are two alternatives. It is possible to calculate either the electric field or the rotating magnetic field that would produce a current distribution on the wire matching that of the  $50\text{-}\Omega$  source feeding the wire. Once either the electric field or the magnetic field is known, it is just a matter of enforcing these field components in the model. The resulting calculation better resembles the physics in the test device and should produce superior modeling agreement.

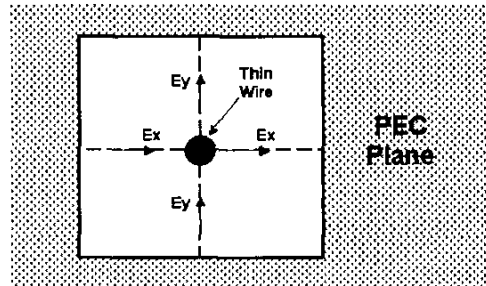


Fig. 3. An alternative method for enforcing the source through the electric fields in the via aperture

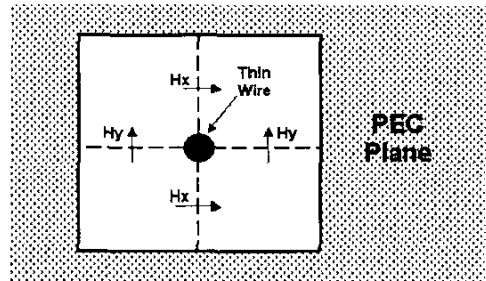


Fig. 4. An alternative method for enforcing the source through the magnetic fields in the via aperture

There are discrepancies between the physical structure and the numerical model. Most notably, the current probe is not mentioned anywhere above. The current probe is a physical object with boundary conditions, but its curved geometry and nonhomogenous construction are difficult to handle in the rectangular mesh of the FDTD model. The current probe is worked into the problem by way of the  $50\text{-}\Omega$  termination in the shorted monopole. This approach is appropriate for circuit theory, since the calibration removes the probe influence, but the boundary conditions of the probe are not correctly included. The influence of the physical presence of the current probe is still evident in the fields due to the capacitive coupling to the monopole and the plane. A comparison of the modeled and measured results from [2] are shown in Figure 5. The agreement breaks down for frequencies greater than 1.5 GHz, where the probe influence becomes important.

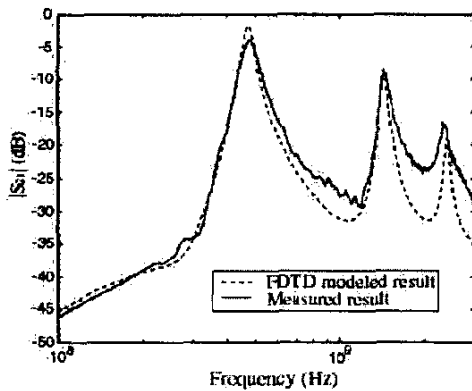


Fig. 5. Agreement between measured and modeled results for the current probe setup

Figure 6 from [2] shows a similar structure where the current probe and shorted monopole are replaced with another monopole port for Port 2. This structure is closer to what the model defines, and the results in Figure 6 show that the agreement is quite good up to 2 GHz and above.

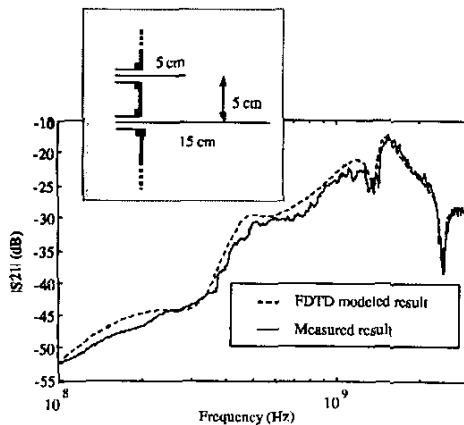


Fig. 6. Agreement between measured and modeled results for the monopole setup

Neglected in the previous model are the physical structures of the SMA bulkhead adaptors. Their effect is much smaller than the presence of the current probe. A similar structure is discussed in Section III, where this issue is covered in more detail.

### III. DC POWER BUS DESIGN WITH DISPERSIVE DIELECTRICS

As integrated circuits have become faster, the importance of providing low-parasitic current paths in DC power bus structures has grown. The problem is quite common in EMC. Both local and global decoupling capacitors are used to provide those low-parasitic paths. Modeling the surface-mount

(SMT) capacitors and their parasitics is required for good agreement. The connections to the board, like the SMA adaptors mentioned at the end of the last section, are also an issue for modeling. Last, but perhaps most important, is the issue of dispersive dielectrics.

#### A. The Construction and the Measurement

The test board and results discussed here were presented in [4] and [5]. Figure 7 from [4] and [5] shows the test board configuration. The lossy board dielectric in the test device is FR-4, 65 mil thick. The upper and lower planes are both copper, and an array of sixteen global decoupling capacitors connects to the power plane by wires passing through square via holes.

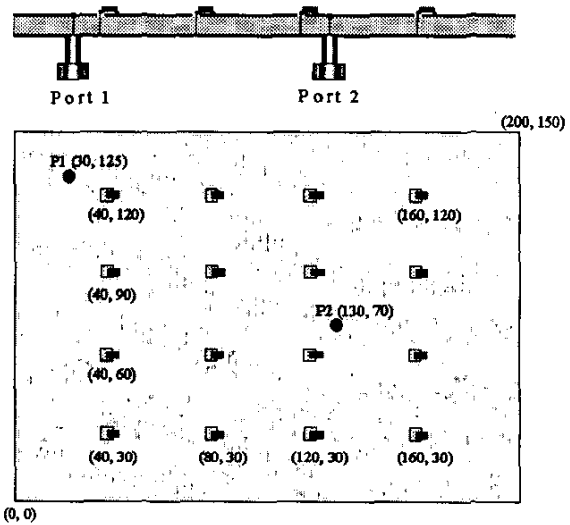


Fig. 7. Two-layer DC power bus using an array of decoupling capacitors

An HP8753D network analyzer was used to measure  $S_{21}$  between two arbitrary port positions on the board. The connections to the board were made with 85-mil semi-rigid coax. A combination of calibrations and port extensions put the measurement plane at the ground layer surface. The measurement plane location is important in the discussion of the port model.

#### B. The Numerical Modeling

The FDTD method is used to model the power bus structure. In this structure it is the square via holes for the SMT capacitor interconnects that define the minimum cell dimension in  $x$  and  $y$ . Normally, it is possible to apply aperture subcell algorithms to holes like this. Then, the cell size could be made larger. However, there is a wire passing through the middle of the hole, which precludes the use of an aperture subcell. The subcell model does not account for the additional boundary conditions of the wire. A sufficient model for the hole is four cells arranged in a square across the surface of the hole, like the arrangement shown in Figure 3. So, in  $x$  and  $y$  there are two field components across the width of the cell to account

for the field variation. When a voltage is applied to the wire at the center of the hole, the electric field on either side of the wire will be roughly equal in opposite directions. A single cell does not have enough variables to model that difference, and if the structure were perfectly symmetric, that field value would be zero.

The cell size in the  $z$  direction is a little more arbitrary. The fields between the planes are similar to a parallel plate capacitor in that the variation in the  $z$  direction is negligible. Thus, there is not a great need to make the  $z$  cell dimension very small. *As a general rule, it is prudent to keep the cell dimensions such that the ratio between the largest and smallest is no more than five.* For the model presented in [4], three cells were used making the  $z$  dimension 0.55 mm. This makes the  $z$  dimension on the same order as the  $x$  and  $y$  dimensions, which are both 1 mm. (The via holes are 2 mm by 2 mm.)

In reality the sixteen SMT capacitors with their connections to the power and ground planes also have parasitic inductances and effective series resistances (ESR). Figure 8 from [4] shows how the FDTD cells are distributed to form the capacitor connections. The capacitance and the ESR were experimentally determined, and capacitive and resistive cell models were included to account for the affect of each. A reference for lumped element FDTD models is Chapter 15 of [1]. In the

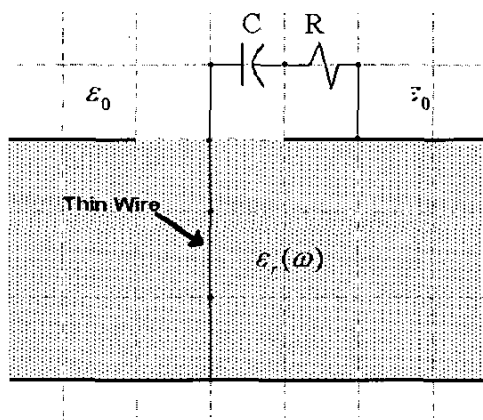


Fig. 8. FDTD model for a SMT Capacitor

model, the lumped elements are placed in adjacent cells, although the resistance and capacitance attributed to those cells is actually distributed in the body of the capacitor. It is unlikely that the fields immediate to the SMT part match what is calculated in this model, but since that is not the objective, the model is sufficient. The  $S_{21}$  calculated matches the measured results well. For the parasitic inductance, a lumped element is inadequate, since the inductance is a property of not only the capacitor but also the connections to the planes and the current path across the planes. The parasitic inductance associated with the decoupling capacitor interconnect to the power and ground planes is included in the model through the thin wire connections. In this way, both the circuit properties of

the inductance and the scattering properties of the wire are included in the model.

A thin wire algorithm is also used for the measurement ports and their plane connections. The model used is illustrated in Figure 9. On the board there is an aperture where the outer

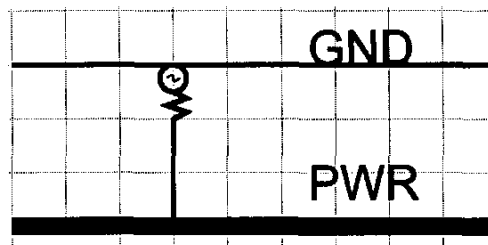


Fig. 9. FDTD model for an SMA port

conductor of the coax connects to the plane. The measurement plane is also at the ground plane, and this level is where the boundary condition, that of a  $50\text{-}\Omega$  source or termination, should be applied. The situation here is the same as was discussed in Section II-B. In order for the fields around the via to accurately reflect the real fields in the test device, the correct current distribution must be enforced on the wire. The calculated fields be correct once that current distribution is there. In the model in Figure 9, however, the boundary condition is enforced by the  $50\text{-}\Omega$  source just below the plane rather than at plane. There is little likelihood that this would cause a major difference in  $S_{21}$  over the frequency range of interest. The agreement achieved with the present model is sufficient despite this discrepancy.

The last piece of the model is the dispersive dielectric. Without loss, a dielectric is rather straightforward to model; simply adjust the relative permittivity and enforce the field continuity at the boundaries. Dispersive dielectrics require a more complex implementation. The Debye model is a function of the complex permittivity varying continuously with frequency [5]. When Maxwell's equations are transformed through a Fourier transform to the frequency domain, there is a convolution between the permittivity and the electric field. Two ways to handle the convolution are to approximate the permittivity as constant or to do a recursive convolution with the continuous permittivity and the electric field. With the constant permittivity method the medium is modeled with a relative permittivity and an effective conductance such that the medium behaves approximately correct over a narrow band of frequencies. A lot more computation time is required for the Debye method, due to the recursive convolution, than is required by the effective conductance method. However, the Debye method produces good agreement over a large frequency range, while the first method is only good for the narrow frequency band over which the effective conductance is calculated. Figure 10, presented in [4], shows the results of two calculations with the constant permittivity method over two frequency ranges. Reasonable agreement is attained over each frequency range. Figure 11 from [5] shows the agreement

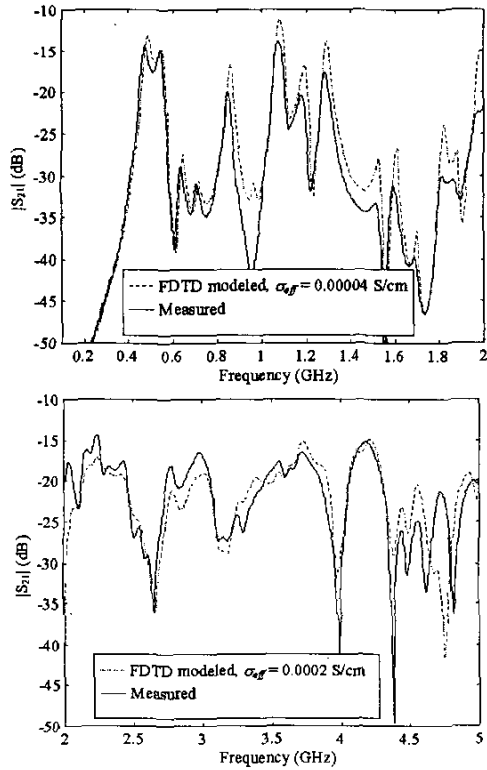


Fig. 10.  $|S_{21}|$  calculated using two effective conductances over their appropriate frequency ranges

attained with a Debye calculation covering the frequency range of both the effective conductance calculations.

#### IV. ROUTING TRACES OVER A GAPPED GROUND PLANE

In the two previous examples, FDTD, a full-wave modeling technique, has been applied to predict the behavior of their structures. Full-wave modeling is not always the best choice for modeling though. It is time consuming and sometimes unnecessary for the task. For example, there is no reason to model field behavior in an infinite section of a rectangular waveguide with a full-wave method. The analytical solution is easily solved. Therefore, two different models are compared in this example: a full-wave model (FDTD) and a transmission line model using HSPICE.

Routing traces across gaps in ground planes is generally not a good design practice. Potential differences between the two sides of the gaps produce EMI. Two designs are tested in this example: a trace over a partially slit ground plane and a trace over a fully slit ground plane. Both are shown in Figure 12.

The FDTD model for the boards in Figure 12 is similar to what was discussed in Sections II and III. The plane conductors, including the traces, are represented as planar conductors. The vias use thin wire models. The FR-4 is modeled with a Debye model.

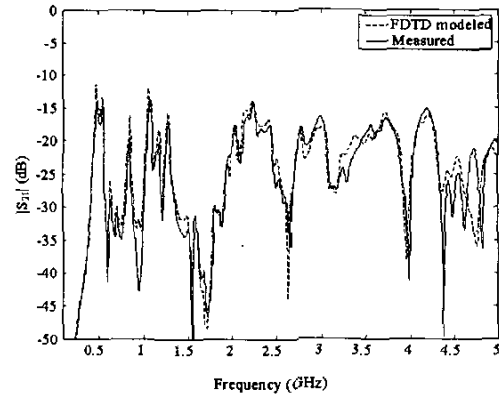


Fig. 11.  $|S_{21}|$  calculated using the Debye model for dispersive dielectrics

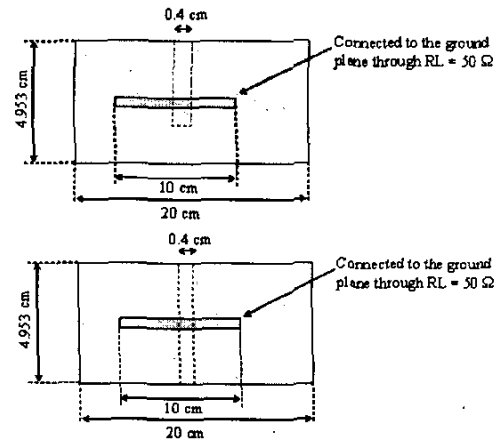


Fig. 12. Trace over a partially and fully slit ground plane

The transmission line model in Figure 13 treats the trace like two lossy transmission lines with a discontinuity between them. This particular model does not include radiation losses. Transmission lines by nature do not include radiation losses, but it might be possible to add them to the model. If the radiation loss is reasonably small, the transmission line model will be sufficient even without the extra loss.  $Z_{slot}$  might be

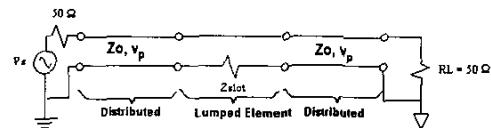


Fig. 13. Transmission line model including  $Z_{slot}$

modeled by two parallel slot lines, one shorted and one open in the case of the partially slit line as shown in Figure 14.  $Z_{slot}$  can also be determined using FDTD by inducing a voltage across the gap and recording the current for both cases. The model is slightly different. The trace is not present for the de-

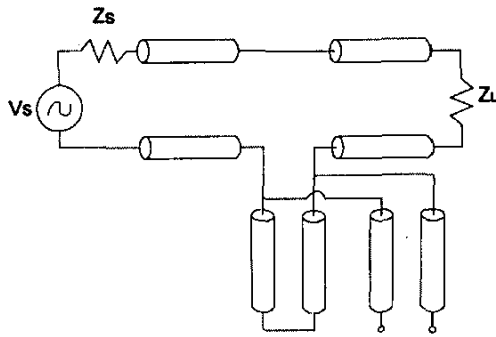


Fig. 14. Schematic for a trace over a partially slit ground plane

termination, making the process identical to disconnecting part of a network and finding the Thevenin equivalent impedance. The results for  $Z_{slot}$  are shown in Figure 15.

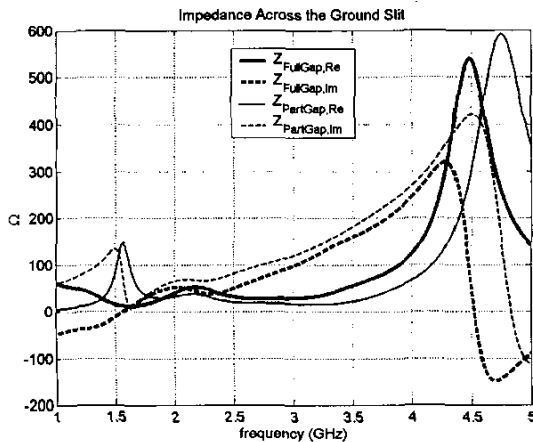


Fig. 15. The impedance across the ground slit calculated by EZFDTD

The transmission line model was calculated using HSPICE, which is capable of handling the dispersive transmission line calculations, and the FDTD models were calculated using EZFDTD. The gap voltage amplitudes calculated are shown in Figure 16. Figure 16 shows that the two methods agree fairly well up to 5 GHz. The real importance in this example is not so much the modeling technique as it is to show that similar results can be achieved by much simpler methods than a full-wave approach.

## V. SUMMARY

In each of the three examples, the three questions posted in the introduction were encountered. In each there was a decision about what to model, how to model it, and at what scale to model it. That decision was influenced by the test structure and the variables of interest. In the Sections II and III,  $S_{21}$  was calculated by full-wave modeling, and while the local field structure was not modeled perfectly everywhere, the

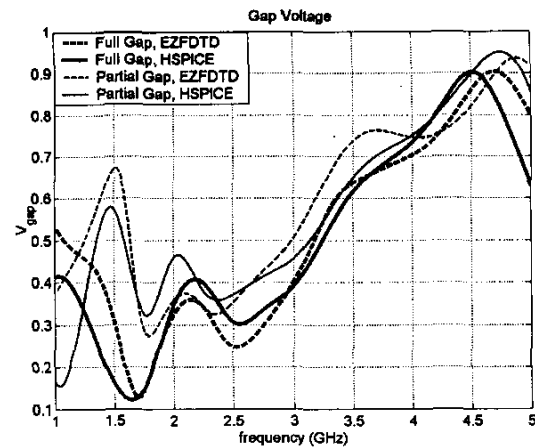


Fig. 16. Voltage calculated for the two designs

overall result agreed well with measurements. In Section IV, the voltage across a ground slit was calculated, and the results show that a simple transmission line method can achieve very good results in much less time than with a full-wave model.

In the end these models could be made better if need be. Check that all of the boundary conditions are applied correctly. Make sure the equations of motion model the proper movement of waves in the media. And, the modeled results can be pushed closer to the measurement results, provided the measurement is correct. However, if the model is good enough, there may be no need to go further.

## REFERENCES

- [1] Computational Electrodynamics: the Finite-Difference Time-Domain Method, *Allen Taflov and Susan C. Hagness*, 2nd ed. Boston: Artech House, 2000.
- [2] X. Ye, J. L. Drewniak, J. Nadołny, and D. M. Hockanson, "High-performance inter-pcb connectors: Analysis of emi characteristics," *IEEE Transactions on Electromagnetic Compatibility*, vol. 44, no. 1, pp. 165–174, Feb. 2002.
- [3] X. Ye, J. Nadołny, J. L. Drewniak, T. H. Hubing, T. P. Van Doren, and R. E. DuBroff, "EMI associated with inter-board connection for module-on-backplane and stacked-card configurations," in *IEEE International Symposium on Electromagnetic Compatibility*, 1999, pp. 797–802.
- [4] X. Ye, D. M. Hockanson, M. Li, Y. Ren, W. Cui, J. L. Drewniak, and R. E. Dubroff, "EMI mitigation with multilayer power-bus stacks and via stitching of reference planes," *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 4, pp. 538–548, Nov. 2001.
- [5] X. Ye, M. Y. Koledintseva, M. Li, and J. L. Drewniak, "DC power-bus design using FDTD modeling with dispersive media and surface mount technology components," *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 4, pp. 579–587, Nov. 2001.