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Voltage Balancing Control of Diode-Clamped Multilevel Rectifier/Inverter Systems

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***Abstract*—This paper presents a new voltage balancing control for the diode-clamped multilevel rectifier/inverter system. A complete analysis of the voltage balance theory for a five-level back-to-back system is given. The analysis is based on fundamental frequency switching control and then extended to pulsewidth modulation (PWM). The method involves obtaining optimal switching angles; a process that is described in detail herein. The proposed control strategy regulates the dc bus voltage, balances the capacitors, and decreases the harmonic components of the voltage and current. Simulation and experimental results demonstrate the validity of the optimizing method and control theory.**

***Index Terms*—Multilevel converter, total harmonic distortion, voltage balancing.**

I. Introduction

AT THIS TIME, several researchers are familiar with the diode-clamped multilevel power converter. Although this concept was introduced over 20 years ago [1], [2], there has been considerable recent research in this area [3]–[14], especially for medium-voltage applications [3], [4], [13]. Primarily, the recent interest stems from advantages over traditional "two-level" power converters that come about since the power conversion is performed in smaller voltage steps. Specifically, these advantages are higher power quality, better electromagnetic compatibility, lower switching losses, and higher voltage capability.

One of the original diode-clamped topologies was the three-level or "neutral-point-clamped" [2] structure for which the balancing of dc capacitor bank voltages is fairly straightforward. However, it has long been recognized that when a number of levels greater than three is used, capacitor voltage balancing is only achievable if the modulation index is limited to about 60% of its maximum value for loads with a typical 0.8 power factor [5]. For inverter applications, if the modulation index is set beyond this limit, the center capacitors tend to discharge and eventually the converter converges to a three level [6]. To address this limitation, isolated dc sources can be used for multilevel inverter systems [4]. Alternatively, auxiliary dc/dc converters can be added for capacitor voltage balancing [7], [8]. Another option is to use an active rectifier as a front-end to a multilevel inverter system. Recent research in this area has focused on four-level [9], [10], five-level [6], [11], [12], and six-level [13] systems.

In this paper, a voltage balancing control theory for the multilevel "back-to-back" rectifier/inverter system is presented. The method relies on coordination between rectifier and inverter switching angles to achieve capacitor charge balance and at the same time minimize the switching harmonics of both rectifier and inverter. The method differs from that presented in [9]–[11] in that a voltage-source control is implemented on both rectifier and inverter circuits. This yields good harmonic performance and is readily implemented on a digital signal processor (DSP). The proposed method is different from that presented in [10] and [12] since it does not utilize redundant switching states. Instead, the capacitor voltage balancing is built into the modulation control and a balancing theory is formulated to generate switching angles. Finally, the proposed method differs from that of [6] and [13] in that it is extended to include pulsewidth modulation (PWM), which reduces the total harmonic distortion (THD). Some features of the proposed control are as follows:

1) balance of the capacitor bank dc voltages;
2) unity power factor operation (or desired leading or lagging power factor);
3) low harmonic content (even with fundamental frequency switching);
4) nearly sinusoidal current with PWM control.

After introducing the proposed control, the voltage balancing theory for a five-level "back-to-back" system is analyzed. The principle of the proposed theory is derived from fundamental frequency switching and then extended to PWM control. A five-level experimental system has been constructed and used to substantiate the theory.

II. Voltage Balancing Theory

Fig. 1 shows a three-phase five-level rectifier/inverter back-to-back system that can generate a nine-level line-to-line voltage waveform. The system consists of two identical five-level converters with shared dc buses. The left half-side is

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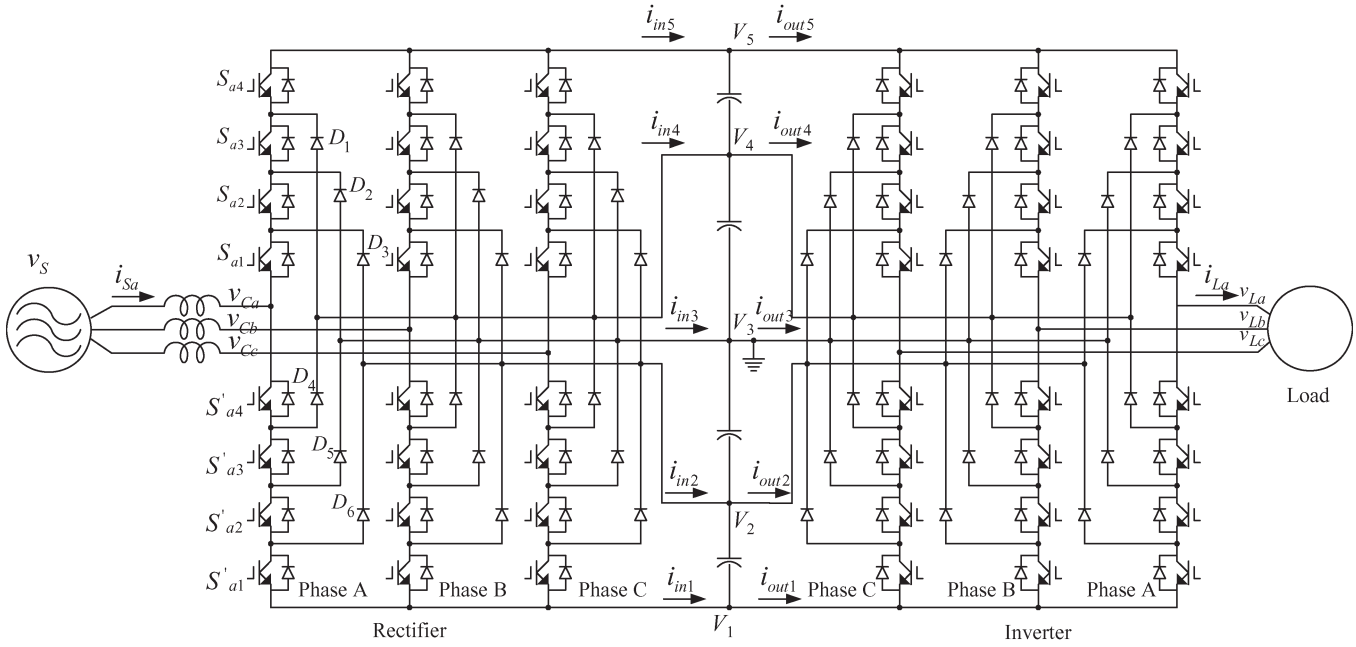

Fig. 1. Schematic of a three-phase five-level rectifier/inverter system.

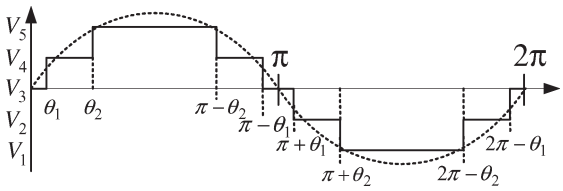

Fig. 2. Fundamental frequency switching of a five-level converter.

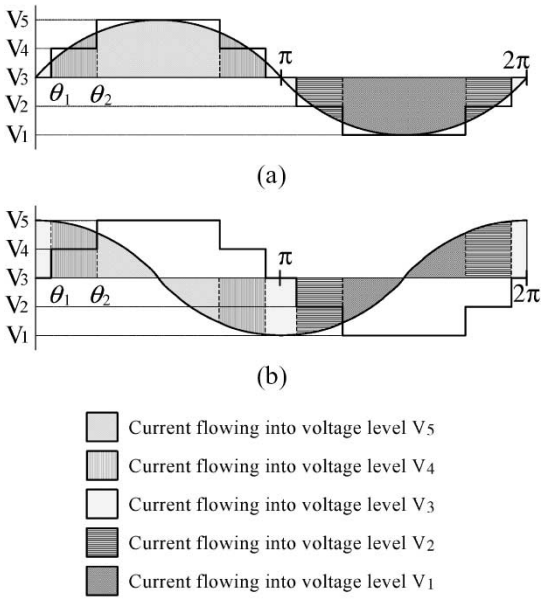

Fig. 3. Current flowing into the capacitor junctions. (a) Current flowing into each level when the current is in phase with the phase voltage. (b) Current flowing into each level when the current is 90° leading from the phase voltage.

connected to the utility and acts as a rectifier; the right half-side is connected to load and acts as an inverter.

The simplest way to control a multilevel converter is to use a fundamental frequency switching control wherein the switching devices generate an N-level staircase waveform that tracks a sinusoidal waveform. In this control, each switching device only needs to switch one time per fundamental cycle, which results in low switching losses and low electromagnetic interference. Fig. 2 shows a five-level staircase waveform. Considering the symmetry of the waveform, there are only two switching angles that need to be determined in this control strategy: θ_1 and θ_2.

From the topology of the multilevel inverter, it can be seen that the current flowing into each voltage level is determined by the input current and the switching status of each phase leg of the inverter side. When considering only the A phase leg, the current flowing into junction labeled V_5 is

$$i_{in5} = \begin{cases} i_{Sa} & \text{for } v_{Ca} = V_5 \\ 0 & \text{for } v_{Ca} \neq V_5. \end{cases} \tag{1}$$

In general, the current flowing into junction V_x is

$$i_{inx} = \begin{cases} i_{Sa} & \text{for } v_{Ca} = V_x \\ 0 & \text{for } v_{Ca} \neq V_x \end{cases} \tag{2}$$

where x equals 1, 2, 3, 4, or 5.

Fig. 3 illustrates the waveforms of the phase voltage of the rectifier v_{Ca} (relative to the ground in Fig. 2) and the input current i_{Sa}, in which it is assumed that the input current is sinusoidal. Fig. 3(a) shows the case when the input current is in phase with the voltage. The input current will flow into different voltage levels V_1, V_2, V_3, V_4, or V_5 according to the switching status of the rectifier.

The different shaded areas shown in Fig. 3(a) express the charge flowing into each voltage level over one period. It is obvious that the currents flowing into voltage levels V_4 and V_5

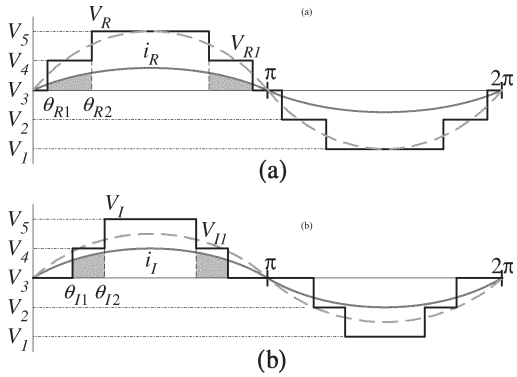

Fig. 4. Rectifier and inverter voltage and current waveforms. (a) Rectifier side. (b) Inverter side.

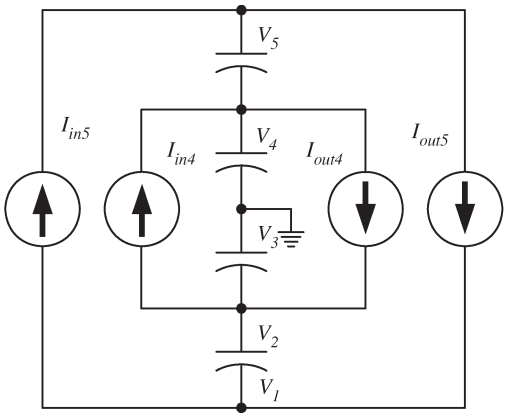

Fig. 5. Capacitor junction equivalent circuit.

(i_{in4} and i_{in5}) are always positive. Likewise, i_{in1} and i_{in2} are always negative. The average current flowing into the junction V_3 (i_{in3}) is zero on average because of the symmetry of the current waveform.

Fig. 3(b) shows the case where the line current is 90° leading from the phase voltage. It is obvious that the average current flowing into each voltage level over one period is always zero, which means that reactive currents have no effect on each level's average voltage.

From the above analysis, if only the rectifier side is considered, the levels of V_4 and V_5 have the tendency to increase because there is always positive current flowing into these levels, and the levels of V_1 and V_2 have the tendency to decrease. In the back-to-back structure, due to the symmetry of the system, the unbalance tendencies of both sides have a potential to compensate each other. With a proper control strategy, net current flowing into each level can be regulated to zero.

Since the reactive components of the current for both rectifier and inverter have no effect on the voltage balance, only the active components of the currents need to be considered. The voltage and active current waveforms are illustrated in Fig. 4. Fig. 4(a) shows the voltage and current waveforms of the rectifier, where v_R and v_{R1} are the output staircase voltage waveform and its fundamental component, respectively. The variable i_R is the active current waveform. Fig. 4(b) illustrates the waveforms of the inverter. The average current flowing into each voltage level can be expressed as

$$I_{in1} = \frac{1}{T}\int_{\pi+\theta_2}^{2\pi-\theta_2} I_R \sin\theta \mathrm{d}\theta \tag{3}$$

$$I_{in2} = \frac{1}{T}\left(\int_{\pi+\theta_1}^{\pi+\theta_2} I_R \sin\theta \mathrm{d}\theta + \int_{2\pi-\theta_2}^{2\pi-\theta_1} I_R \sin\theta \mathrm{d}\theta\right) \tag{4}$$

$$I_{in3} = \frac{1}{T}\left(\int_{-\theta_1}^{\theta_1} I_R \sin\theta \mathrm{d}\theta + \int_{\pi-\theta_1}^{\pi+\theta_1} I_R \sin\theta \mathrm{d}\theta\right) \tag{5}$$

$$I_{in4} = \frac{1}{T}\left(\int_{\theta_1}^{\theta_2} I_R \sin\theta \mathrm{d}\theta + \int_{\pi-\theta_2}^{\pi-\theta_1} I_R \sin\theta \mathrm{d}\theta\right) \tag{6}$$

$$I_{in5} = \frac{1}{T}\int_{\theta_2}^{\pi-\theta_2} I_R \sin\theta \mathrm{d}\theta \tag{7}$$

where I_R is the peak value of the input current.

From the symmetry of the sinusoidal waveform, it can be concluded that $I_{in1} = -I_{in5}$, $I_{in2} = -I_{in4}$, and $I_{in3} = 0$. Accordingly, the simplified equivalent circuit can be drawn as that in Fig. 5. In order to balance the dc capacitor voltage, the average net charge following into the inner level V_4 should be zero, i.e.,

$$\sum_{abc}\int_{\theta_{R1}}^{\theta_{R2}} i_R \mathrm{d}\theta = \sum_{abc}\int_{\theta_{I1}}^{\theta_{I2}} i_I \mathrm{d}\theta. \tag{8}$$

Also, the input and output active power to the dc link capacitors has to be balanced, which is also the charge balance equation for level V_5

$$\sum_{abc} V_R I_R = \sum_{abc} V_I I_I. \tag{9}$$

Assuming that the three-phase currents are balanced and sinusoidal, only the fundamental components in (8) and (9) need to be considered, i.e.,

$$V_{R1} I_{R1} = V_{I1} I_{I1} \tag{10}$$

and

$$I_{R1}(\cos\theta_{R2} - \cos\theta_{R1}) = I_{I1}(\cos\theta_{I2} - \cos\theta_{I1}) \tag{11}$$

where V_{R1}, V_{I1}, I_{R1}, and I_{I1} are the fundamental components.

On the other hand, the fundamental voltages can be obtained from Fourier series analysis of the waveform shown in Fig. 4 and expressed as functions of the switching angles and the dc link voltage by

$$V_{R1} = M_R \cdot V_{\max} = f(\theta_{R1}, \theta_{R2}, V_{dc}) \tag{12}$$

and

$$V_{I1} = M_I \cdot V_{\max} = f(\theta_{I1}, \theta_{I2}, V_{dc}) \tag{13}$$

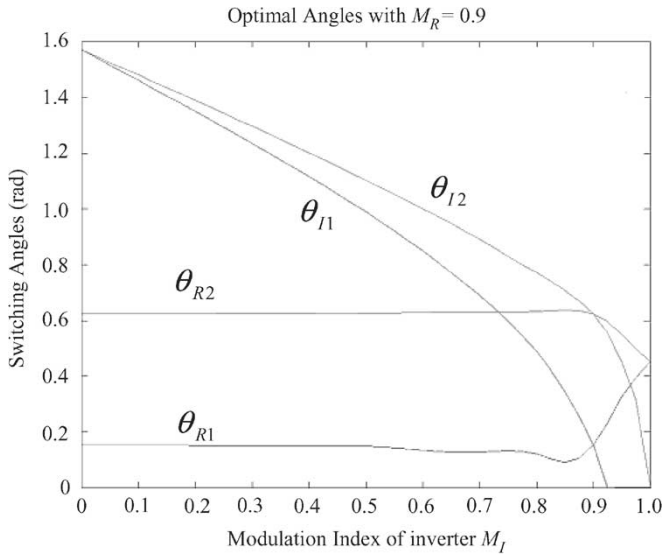

Fig. 6. Optimal switching angles for $M_R = 0.9$.

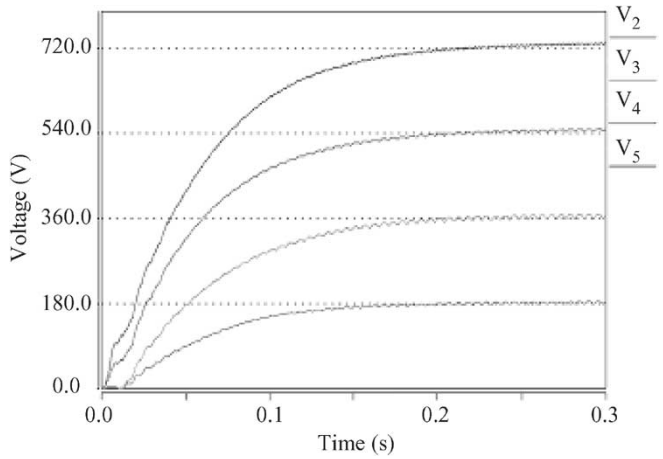

Fig. 7. Junction voltages for $M_R = 0.9$.

where M_R and M_I are modulation indices for the rectifier and inverter, respectively, and $V_{\max}$ is the maximum obtainable output voltage when both θ_1 and θ_2 are zero.

Eliminating the variables I_{R1} and I_{I1} from (8) and (9) results in the constraint condition for the four switching angles to balance both active power and charge, i.e.,

$$V_{I1}(\cos\theta_{R2} - \cos\theta_{R1}) = V_{R1}(\cos\theta_{I2} - \cos\theta_{I1}). \quad (14)$$

In addition to this power and charge balance constraint, the optimal switching angles can be determined by minimizing the THD or fifth and seventh harmonic components, e.g.,

$$\min\left(V_{R5}^2 + V_{R7}^2 + V_{I5}^2 + V_{I7}^2\right) \quad (15)$$

where each harmonic component can be expressed as functions of the switching angles and the dc link voltage by Fourier series expansion.

For given modulation indices on the rectifier side and inverter side M_R and M_I, the four switching angles of various inverter modulation indices can be obtained by an iterative method.

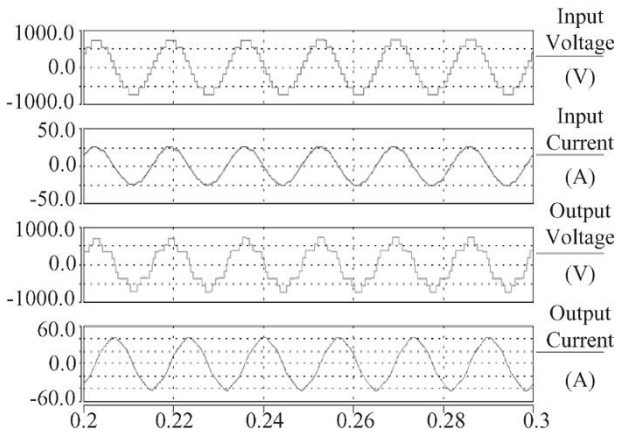

Fig. 8. AC waveform for $M_R = 0.9$ and $M_I = 0.8$.

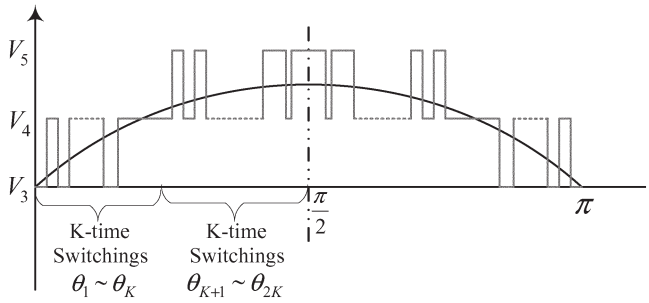

Fig. 9. Extension of the proposed method to PWM.

Fig. 6 shows the results when M_R is set to 0.9. For a given modulation index of the inverter M_I, the switching angles of both rectifier side and inverter side can be obtained from the figure.

III. Simulation Results

Using the optimal switching angles calculated above, simulations have been conducted to verify the dc link voltage balance. The former results and discussion are based on some idealized assumptions that may not be guaranteed in the actual system due to control errors and tolerances. This will result in a voltage error of each level. Therefore, a closed-loop feedback control is introduced to improve the performance of the voltage balance strategy. A small corrective component will be added to each switching angle to compensate the changing tendency of each voltage level.

Figs. 7 and 8 show the simulation result of the control when the modulation indices of rectifier and inverter are 0.9 and 0.8, respectively. Fig. 7 shows the voltage of each level relative to V_1. It can be seen that the voltages are well balanced in steady-state operation. Fig. 8 shows the line-to-line voltage and phase current of the rectifier (input) and inverter (output). It can be seen that the input and output currents are quite sinusoidal even with fundamental frequency switching.

IV. Voltage Balancing for PWM Control

Although fundamental frequency switching can achieve high control performance and low harmonics at high modulation

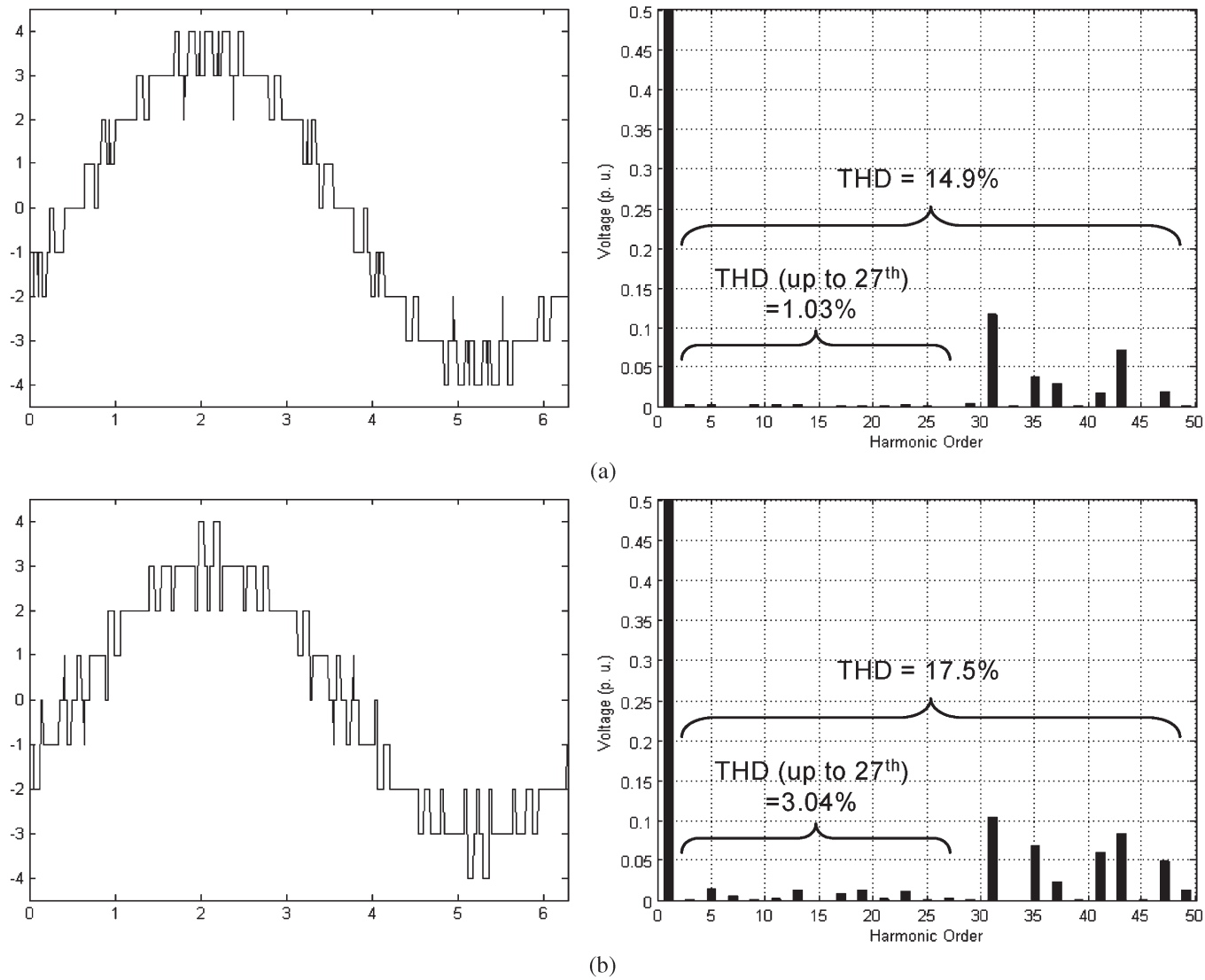

Fig. 10. Line-to-line voltage waveforms and their spectrum when $M_I = 0.7$. (a) Rectifier THD (up to 27th) is 1.03% and total THD is 14.9%. (b) Inverter THD (up to 27th) is 3.04% and total THD is 17.5%.

index, it still needs to be improved to be suitable for low modulation index operation. One of easiest ways to improve control performance is to extend the above voltage balancing control theory to PWM control. Fig. 9 illustrates the voltage waveform of the proposed PWM strategy. There are K transitions for each change from one voltage level to another. Obviously, fundamental frequency switching is the special case of this PWM strategy where $K = 1$.

Using the same theory as with fundamental frequency switching, optimized switching angles can be obtained by minimizing the phase voltage THD with the constraint equations of charge balance. In the following calculation, the number of switches is set to $K = 9$ as an example. The optimizing program will try to minimize the lower harmonics up to 27th. Higher harmonics in the voltage have less effect on the current waveform because of the filtering of line and load inductances. The lower harmonics can be further reduced with larger K. The modulation index of the rectifier M_R is set to 0.8, and the modulation index of the inverter changes from 0.3 to 0.95. Fig. 10 illustrates the line-to-line voltage waveforms and the harmonic spectra of the rectifier and inverter when the modulation index of the inverter M_I is 0.7, which shows that the lower harmonic components have been effectively eliminated. Even when M_I is low, the proposed strategy can still obtain satisfactory results. As a drawback, the switching loss of the PWM is much higher than the fundamental frequency switching. Fig. 11 shows the output voltage waveform and its spectrum when M_I is 0.25. Table I shows the THD of the output voltage for 2nd–27th of the proposed PWM strategy, which shows a tremendous reduction compared with the THD of fundamental frequency switching.

The simulation result of this proposed PWM strategy with voltage balance control when M_I is 0.7 is shown in Figs. 12 and 13. Fig. 12 shows the voltage waveform of each voltage level, and Fig. 13 shows the detailed voltage and current waveforms. As can be seen, the capacitor voltages remain balanced and the voltage waveforms exhibit typical five-level PWM shapes.

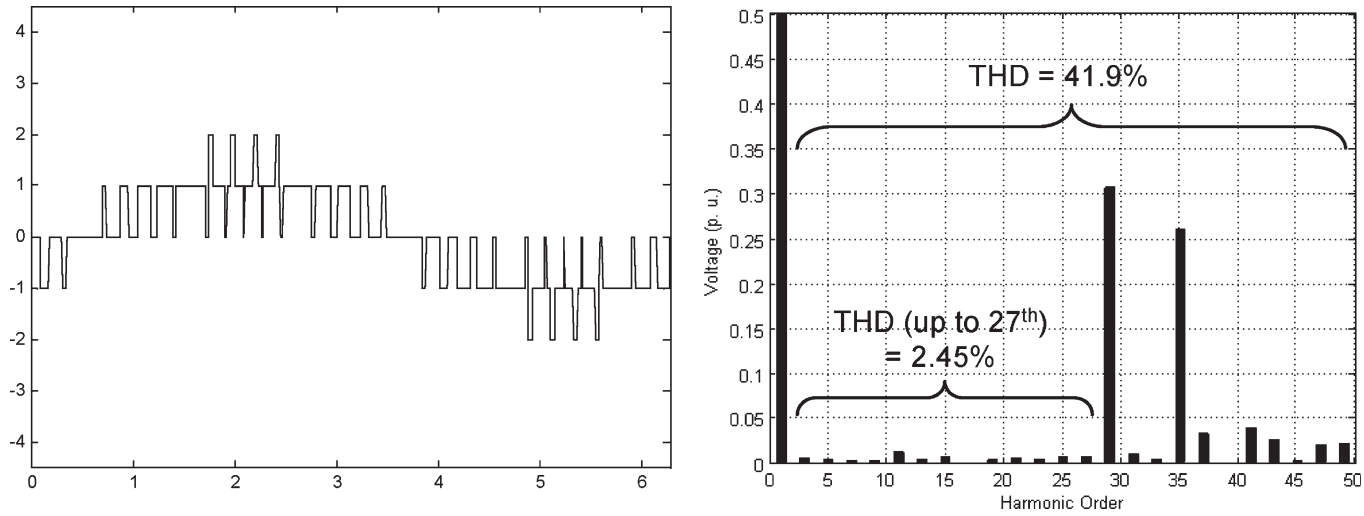

Fig. 11. Line-to-line voltage waveform of the inverter and its spectrum when $M_I = 0.25$.

TABLE I
OUTPUT LINE VOLTAGE THD COMPARISON FOR 2ND–27TH HARMONICS OF FUNDAMENTAL FREQUENCY SWITCHING VERSUS PWM

Control Method	Modulation index of inverter									
	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	0.95
PWM (N=9)	17.3%	8.92%	6.60%	6.77%	10.1%	1.91%	3.04%	2.52%	3.52%	5.29%
Fundamental Freq.			74.7%	43.2%	20.8%	16.2%	16.5%	13.2%	12.7%	11.5%

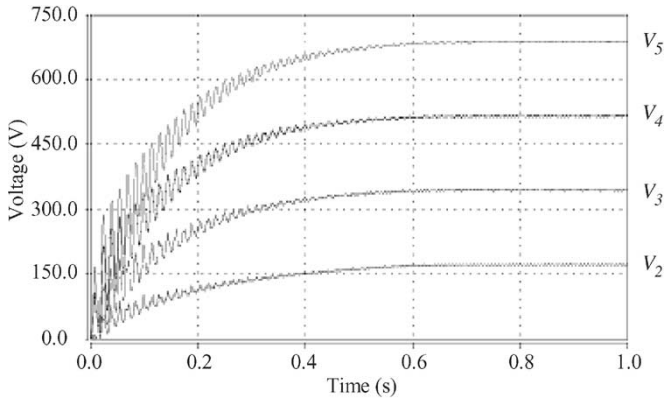

Fig. 12. Simulated voltage of each capacitor junction.

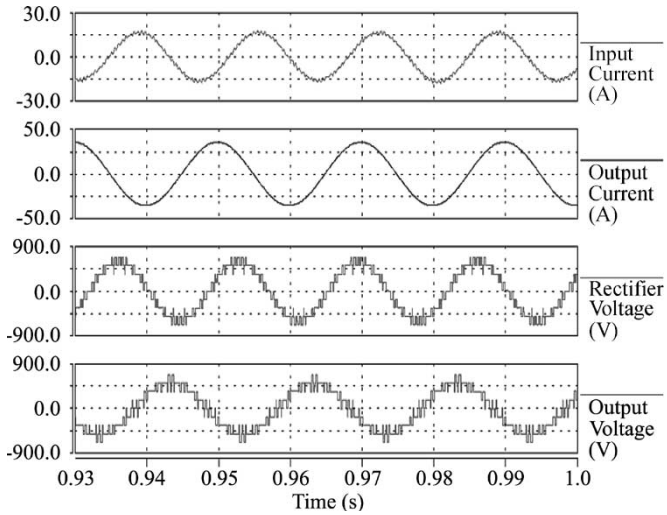

Fig. 13. Simulated ac voltage and current waveforms.

V. EXPERIMENTAL RESULTS

A five-level three-phase back-to-back 10-kW rectifier/inverter prototype was constructed for laboratory validation of the proposed control. Fig. 14 shows the control block diagram for the rectifier, where V_{dc}^* is the reference of the dc voltage, δ is the phase shift of the rectifier, and I_{SQ}^* is the reference of the reactive component of source current i_s. The reactive power can be directly controlled in this system. For example, choosing $I_{SQ}^* = 0$ will result in unity power factor. Also, this system can generate either leading or lagging reactive power to compensate the power system. The dc link voltage is controlled by changing the phase difference δ between rectifier voltage and input voltage.

Fig. 15 illustrates the layout of the prototype system. The control strategy is implemented by a DSP board based on ADSP-21065L by Analog Devices. There are four dc voltage sensors to sense the voltage on each capacitor. Two ac voltage sensors are used to detect ac line voltage, which will be used in phase detecting. Two current sensors are used to measure the input currents in order to calculate the phase difference between the voltage and the current. The load used is an induction motor with a resistance–inductance (*RL*) load to achieve 10-kW rating.

Since the converter has six phase legs and each of them has eight switching devices, there are 48 switching devices in total. The gate drive signals of these 48 switching devices were sent to the converters by optical fibers. The fault signal for each phase leg is transmitted into the DSP board. All gate drive

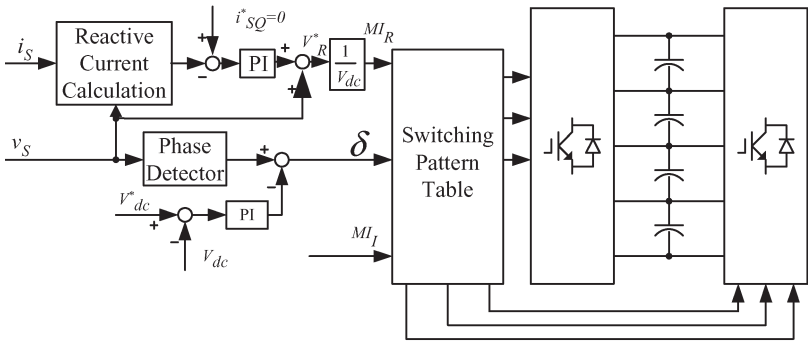

Fig. 14. Prototype system control block diagram.

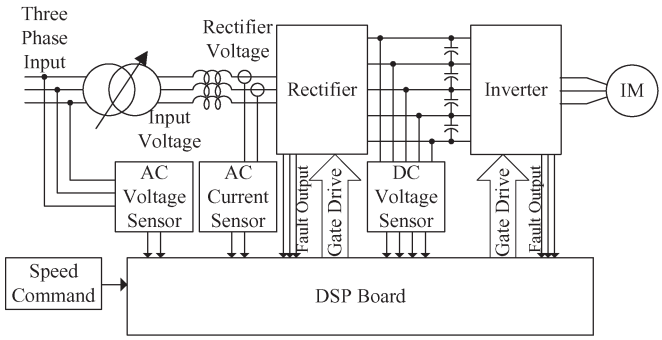

Fig. 15. Prototype system schematic diagram.

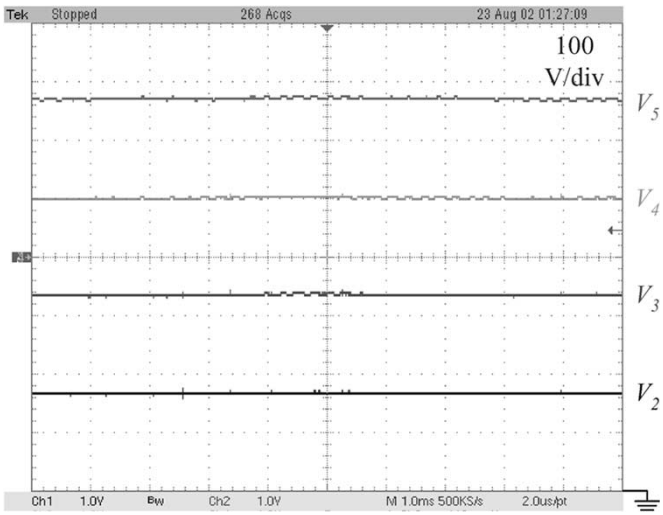

Fig. 16. Experimental waveforms showing each voltage level (100 V/division; time 100 ms/division).

signals were set to shut off for protection if a fault signal is detected. The speed command was sent to DSP by an external potentiometer.

Fig. 16 shows the voltage waveforms of each voltage level during steady-state operation. Therein, the vertical axis ranges from 0 to 800 V. It can be seen that the voltage of the dc bus is stabilized at 720 V and all voltage levels are well balanced. Fig. 17 illustrates the detail of the ripple voltage on each capacitor. It is shown that the capacitor voltage ripple is only 2 V out of the 720-V dc bus, which shows the voltage balance strategy is very effective.

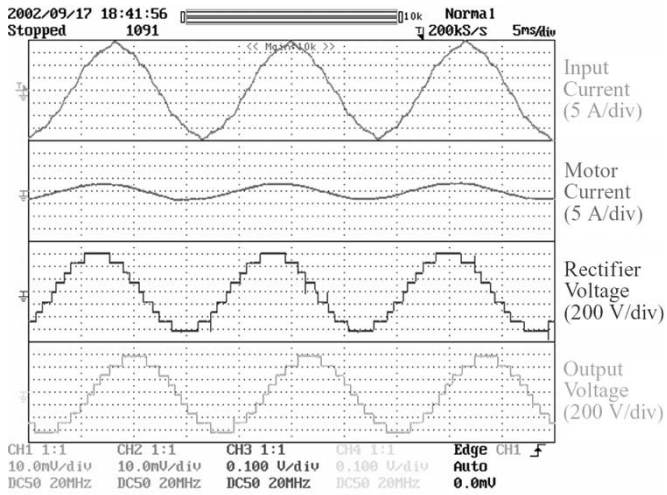

Fig. 17. Input and output waveforms for $M_I = 0.9$.

Fig. 17 illustrates the detailed waveforms when the modulation index of the inverter is 0.9 and the output frequency is 60 Hz. Therein, Ch1 is the input current, Ch2 is the motor current, which is much smaller than the input current because *RL* load current is excluded, and Ch3 and Ch4 are the staircase line-to-line voltage waveforms of rectifier and inverter, respectively. The scale of the voltage is 200 V/division, and the scale of the current is 5 A/division.

From Fig. 17, it can be seen that the input current is almost sinusoidal. To get the THD of the waveform, a fast Fourier transform (FFT) is applied to obtain the spectrum of the input current, which is shown in Fig. 18. The THD of the input current is 6.1%. Similarly, the THDs of other waveforms were obtained and are shown in Table II.

Figs. 19 and 20 show the comparison of fundamental frequency switching and PWM control when the modulation index of the inverter drops to 0.7. It can be seen that the harmonic component of the fundamental frequency switching has increased, while PWM can still create nearly sinusoidal current waveforms. The THDs of the waveforms in both control methods have been calculated and shown in Table III.

VI. Conclusion

In this paper, a control theory for the charge balancing of the diode-clamped multilevel rectifier/inverter system has been

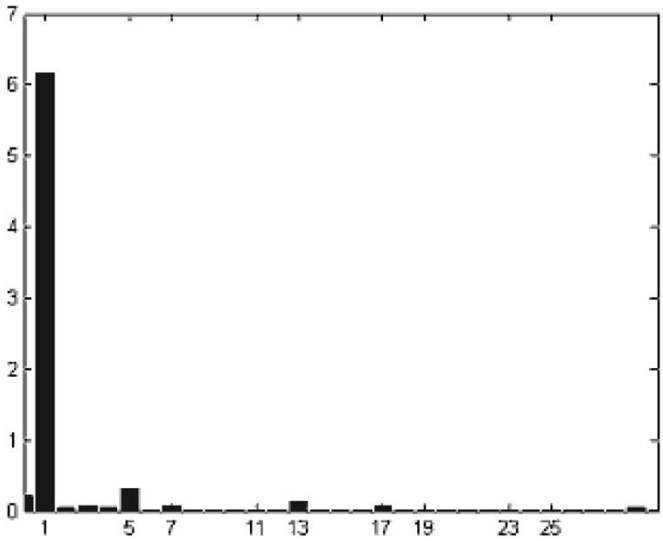

Fig. 18. Spectrum of the input current.

TABLE II
THD OF THE WAVEFORM (FUNDAMENTAL FREQUENCY SWITCHING AND $M_I = 0.9$)

	THD
Input Current	6.1%
Motor Current	5.0%
Rectifier Voltage	14.6%
Output Voltage	9.5%

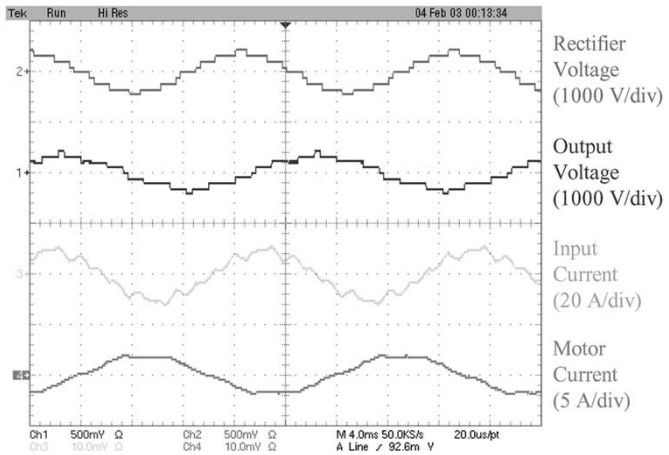

Fig. 19. Fundamental frequency switching waveform measurements.

presented. Simulation and experimental results were shown to verify the analysis and to demonstrate the following advantages of the proposed control.

1) Since it can generate a nine-level line-to-line staircase waveform, the five-level converter generates almost sinusoidal voltage and current waveforms even at fundamental switching frequency.
2) The voltages on the dc link capacitors are well balanced with very small ripple.
3) The system has low harmonics in the input current. The total harmonic distortion (THD) of input current was as low as 6.1% at full load with fundamental frequency switching and 4.6% with pulsewidth modulation (PWM) control.
4) Each switch in the converter can swtich only once per cycle when performing fundamental frequency switcing; this results in high efficiency.

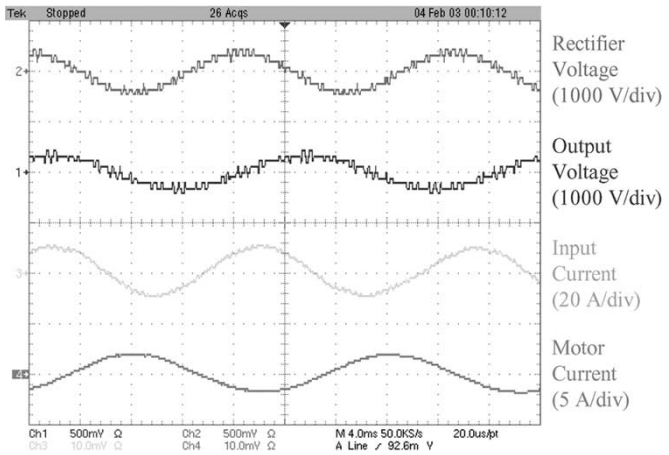

Fig. 20. PWM waveform measurements.

TABLE III
COMPARISON OF THD OF FUNDAMENTAL FREQUENCY SWITCHING AND PWM CONTROL ($M_I = 0.7$)

	Fundamental Frequency Switching	PWM
Input Current	15.3%	4.6%
Motor Current	8.9%	2.2%
Rectifier Voltage	13.0%	11.8%
Output Voltage	15.1%	12.9%

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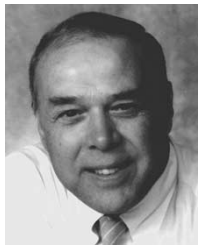

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