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TID and SEE Testing Results of Altera Cyclone Field Programmable Gate Array

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Abstract*— TID and SEE testing was performed on Altera Cyclone FPGAs. The devices exhibit slight performance degradation to a TID of 1 Mrad (Si), but also exhibited SEL at a low LET.*)

Keywords-FPGA, Altera Cyclone, radiation, TID, SEE, SEU, SEL

I. INTRODUCTION

Altera is a large commercial Field Programmable Gate Array (FPGA) supplier, but little is known about the suitability of their parts for space applications. The objective of this experiment was to establish a baseline tolerance to total ionizing dose (TID) effects and single event effects (SEE) for an Altera commercial FPGA device. The device selected was representative of the current state of the art for commercial FPGAs. These tests exposed the devices to radiation levels seen space applications. These tests were established to determine the viability of using these devices in current and future designs, and to highlight the susceptible elements of the FPGA for possible re-design using design hardening approaches.

The selected device is Altera Cyclone Part # EP1C6-Q240C8. This device was chosen to represent the current device family of the manufacturer. A small device was chosen to reduce testing complexity. The Altera Cyclone FPGA family is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities up to 20,060 logic elements (LEs) and up to 288 kbits of RAM. The version chosen for this test contains 5,980 LEs and 80 kbits of RAM. It includes two phase-locked loops (PLLs) for clocking and a dedicated double data rate (DDR) interface to meet DDR SDRAM and fast cycle RAM (FCRAM) memory requirements. The Cyclone device also contains a cyclic redundancy check (CRC) error checking of the configuration memory. The device is packaged in a cavity up 240-pin plastic quad flat pack. The Cyclone is a reduced feature-set version of the Altera Stratix FPGA. The Cyclone and Stratix devices are manufactured in the same process, which allows the results for the Cyclone to be extrapolated to the Stratix.

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II. TEST METHODOLOGY

A. TID Tests

1. The first test will look at the configuration memory of the device. Using an alternating pattern (checkerboard), the device will be irradiated to a predetermined level. Once at that level the device will be tested to determine if the programmed configuration is still valid. If it is not valid, the device will be considered to have failed functionally. If the configuration is valid, the device will be configured with the inverted pattern (checkerboard not). If the device can be configured it will undergo the next level of irradiation. If the device cannot be configured, it will be considered a functional failure. This test sequence will continue until there is a functional failure. Any parametric failure will be noted and the testing resumed.
2. The second test will measure the speed of the device versus the supply current at the specified radiation levels. It is expected that the speed will decrease as the radiation level increases. The supply current will be incremented from the minimum supply voltage to the maximum supply voltage in predetermined steps. The frequency will be increased from 100 kHz to the point where the output does not match the input in specified increments. The configuration will use a simple shift register of 1024 bits that utilizes a significant number of logic elements, where the term significant is defined as greater than 50 percent of the useable logic elements. A single input and single output will be used for this test.
3. The third test will evaluate the input and output parameters of the device under increasing radiation levels. Parameters include input leakage current, output drive current, etc. Pre-radiation measurements will be taken to determine the baseline measurements. The device will undergo irradiation at predetermined increments. At the specified levels, parametric measurements will be taken. These measurements will be compared with the baseline measurements and those defined in the data sheet [1]. These steps will be

repeated until the measurements fall outside the limits. This point will be noted and the testing continued until a functional failure occurs.

B. SEE Tests

1. The first test will watch for power supply excess current or single event latchup (SEL). Configure the part with a static pattern and don't clock it. Expose the part to the beam while another FPGA monitors core and I/O currents for a sudden large increase. Continue to monitor the part for 60 seconds to determine if it's going to latch up. If the part latches-up, command the crowbar transistors "ON" to protect the part from excess dissipation. If latch-up occurs, shut-off power, re-establish power and go back to A. If no latch-up occurs, move on to test 2.
2. The second test will measure configuration upsets. Configure parts and allow them to remain static. Increase the dose rate until configuration CRC errors occur. Reconfigure and repeat until the dose rate is adjusted to get an average of one error every 30 seconds.
3. The third test will measure register and flip-flop upsets. Configure eight 512 bit shifters in the device. Clock in data to fill all registers and turn clock off when all are full. Irradiate the part for a specified time. Shift all data out of the shifters and record all errors.
4. The fourth test will measure RAM upsets. Load a configuration to initialize a specific pattern in the RAM. Allow the RAM to remain static. Radiate the part for a specific period of time. Read the RAM and record number of errors and position in RAM for each error.
5. The last test will measure combinatorial logic transient upsets. Configure a serial cloud of combinatorial logic using almost all LUT logic in the device. Connect the output of the combinatorial logic to a D flip-flop, D input. Connect the input to the cloud to a static "0" (low) source. Clock the flip-flop at a frequency just below a frequency corresponding to the propagation delay of the cloud and record the errors.

III. TID Test Results

The Altera Cyclone device was tested for TID irradiation effects at two sources. The first source was the Low Energy X-Ray (LEXR) source at AFRL/VSSE, Kirtland AFB, New Mexico. One part was tested at this facility, Part #1, as a check of the test set-up and system. This site was also used to correlate data between the two types of sources. The second source was the Cobalt-60 source, also located at AFRL/VSSE, Kirtland AFB, New Mexico. Two parts, Part #9 and Part #10, were tested at this facility. Measurements were taken on several parameters of the target FPGA. The last part irradiated, Part #10, was placed in an oven under bias and annealed at 100°C for 168 hours.

The device configurations were the same for all three tests. The 4000-shift register chain with PLL was used. The device was held under constant bias throughout the duration of the tests and exercised at the intervals indicated. The device irradiated at the LEXR was de-capped to expose the bare die. The devices irradiated at the Co-60 were fully packaged.

The results of the three tests follow:

1. No functional failures of the configuration of the memory were observed to 1 Mrad (Si) and after annealing.
2. Fig. 1 shows the degradation of maximum frequency versus TID with various conditions placed on device #10. The data demonstrates the functionality of the device to 1 Mrad (Si) as long as some margin is incorporated into the maximum operating frequency.
3. Fig. 2 shows the core current and I/O current for the three devices as the radiation levels were increased. There was no noticeable effect on the I/O current. This may be due to the fact that we weren't using a large number of the I/O resources. The core current begins to increase rapidly around 120 krad (Si) under irradiation from the Cobalt-60 source and around 250 krad (Si) under irradiation from the LEXR source. Device number 10 had its bias maintained following the test and was placed in an oven at 100°C. After 120 hours the device was removed and tested. The device recovered fully from the radiation effects with the core and I/O currents returning to normal. Parametric test results remained the same.

IV. SEE Test Results

Latchup testing was first to be attempted. The beam was set using gold with an LET of 96 and was turned on, and the device immediately latched-up on both core and I/O supplies. The FPGA on the motherboard sensed the latched conditions within about 0.5 seconds. Manual reconfiguration of the device was attempted, but failed. After the beam was shut off and the power recycled on the device, the device resumed normal functioning with core and I/O currents returning to the normal levels cited above. Test 1 was repeated three times with identical results.

The beam species was changed to nickel, allowing the LET level to be dialed down to 26.6 MeVcm^2/mg. Application of the ion beam produced immediate (<0.5 second) core supply latch-up, but no I/O latchup was produced. Manual reconfiguration was attempted, but was unsuccessful while the beam remained on. Power cycling resulted in the DUT core latching-up every time while the beam remained on. No I/O latchup was evident during repeated supply cycling. The DUT came out of latch-up and reconfigured successfully after a final power supply cycle with the ion beam turned off. Core and I/O current levels returned to the normal levels as cited above.

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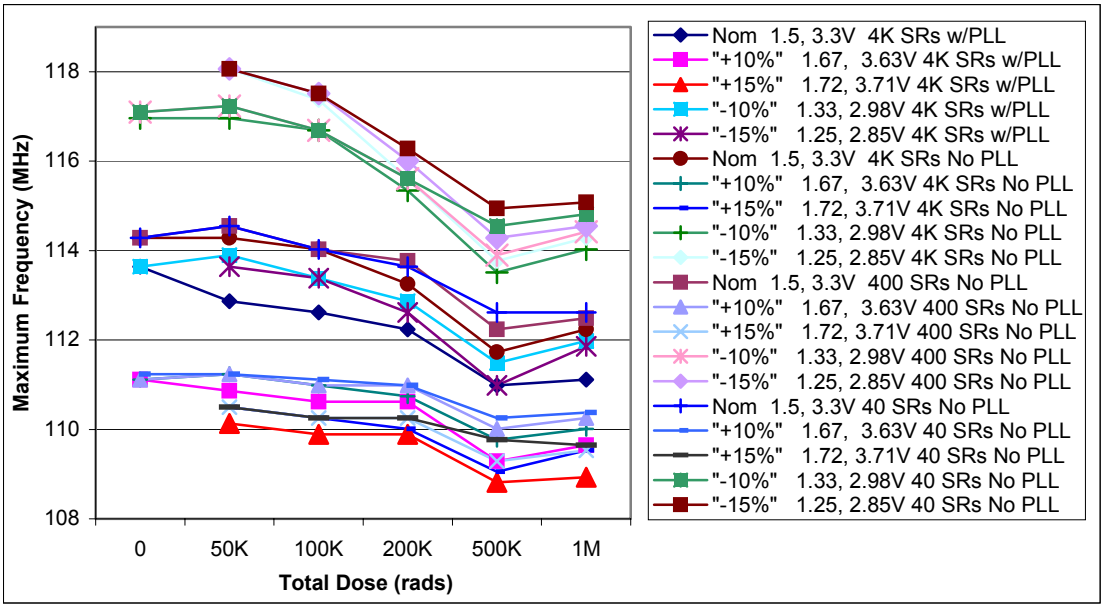

Figure 1. Maximum Frequency vs. TID.

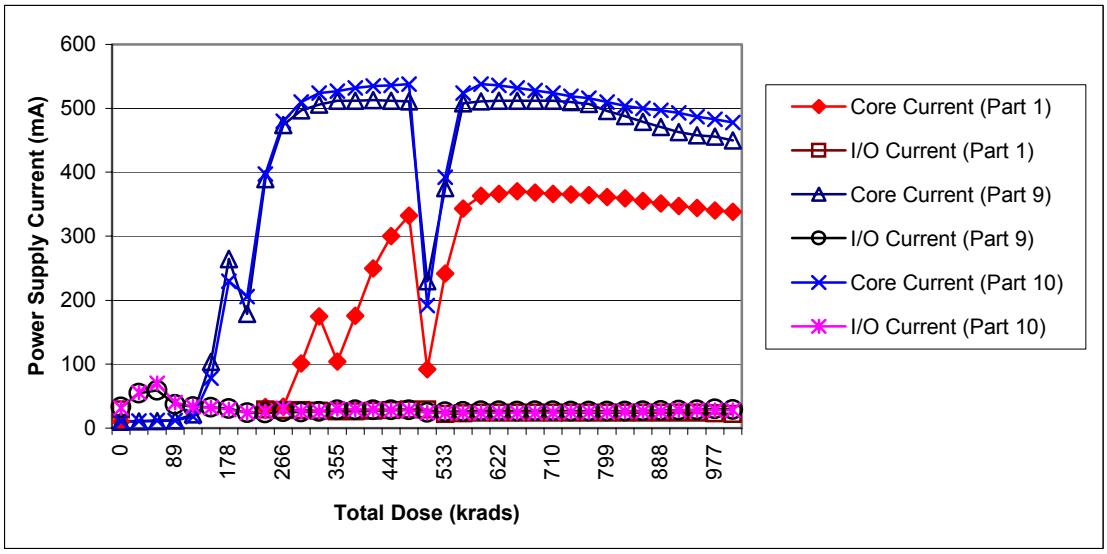

Figure 2. Supply Currents vs. TID.

V. CONCLUSION

The Altera Cyclone device exhibited latchup at LET levels below 35 MeVcm^2/mg. As a result, the part is deemed unusable in space applications, as it currently exists. If future versions of the Cyclone or the Stratix family do not exhibit this latchup problem, then the remainder of the SEE evaluations can be completed.

The TID results of the Cyclone devices demonstrated the potential of 130 nm bulk CMOS technology. Without any attempt to harden the part, the devices survived to at least 1 Mrad (Si) with little performance degradation. This shows that standard commercial design methodologies are capable of producing devices resistant to TID at the 130 nm technology node.

VI. REFERENCES

[1] Cyclone FPGA Family Data Sheet; Altera Corporation, 101 Innovation Drive, San Jose, CA 95134

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