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On-die transient event sensors and system-level ESD testing

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ON-DIE TRANSIENT EVENT SENSORS AND SYSTEM-LEVEL ESD TESTING

by

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This dissertation consists of the following five articles which have been submitted for publication, or will be submitted for publication as follows:

Paper I: Pages 3-20; Systematic Evaluation of Soft-Failures in System Level ESD Transient Events, has been accepted in IEEE Transactions on Electromagnetic Compatibility.

Paper II: Pages 21-43; An On-Chip Detector of Transient Stress Events, has been accepted in IEEE Transactions on Electromagnetic Compatibility.

Paper III: Pages 44-67; Transient Peak Voltage Level Sensors, will be submitted in IEEE Transactions on Device and Material Reliability.

Paper IV: Pages 68-81; Characterizing ESD Stress Currents in Human Wearable Devices, has been accepted in Proceedings of the 39th Electrical Overstress/Electrostatic Discharge Symposium.

Paper V: Pages 82-106; A Transient Event Sensor for Efficient System Level ESD Testing, has been accepted in IEEE Transactions on Electromagnetic Compatibility.

ABSTRACT

System level electrostatic discharge (ESD) testing of electronic products is a critical part of product certification. Test methods were investigated to develop system level ESD simulation models to predict soft-failures in a system with multiple sensors. These methods rely completely on measurements. The model developed was valid only for the linear operation range of devices within the system. These methods were applied to a commercial product and used to rapidly determine when a soft failure would occur. Attaching cables and probes to determine stress voltages and currents within a system, as in the previous study, is time-consuming and can alter the test results. On-chip sensors have been developed which allow the user to avoid using cables and probes and can detect an event along with the level, polarity, and location of a transient event seen at the I/O pad. The sensors were implemented with minimum area consumption and can be implemented within the spacer cell of an I/O pad. Some of the proposed sensors were implemented in a commercial test microcontroller and have been tested to successfully record the event occurrence, location, level, and polarity on that test microcontroller. System level tests were then performed on a pseudo-wearable device using the on-chip sensors. The measurements were successful in capturing the peak disturbance and counting the number of ESD events without the addition of any external measurement equipment. A modification of the sensors was also designed to measure the peak voltage on a trace or pin inside a complex electronic product. The peak current can also be found when the sensor is placed across a transient voltage suppressor with a known I-V curve. The peak level is transmitted wirelessly to a receiver outside the system using frequency-modulated magnetic or electric fields, thus allowing multiple measurements to be made without opening the enclosure or otherwise modifying the system. Simulations demonstrate the sensors can accurately detect the peak transient voltage and transmit the level to an external receiver.

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TABLE OF CONTENTS

Page

LIST OF ILLUSTRATIONS

PAPER V

LIST OF TABLES

SECTION

1. INTRODUCTION

System resets and failures can occur due to many reasons. Fast transient events such as an electrostatic discharge (ESD) can cause complex electronic systems to undergo system resets and in extreme cases permanent failure. Electronic devices are generally tested for immunity under different test conditions. Immunity tests involve stressing the system with different peak transient levels and performing a failure analysis if and when needed. When the system fails in the immunity test, further investigation is needed in order to ensure the system is ready to handle field operating conditions. For determining the exact cause of failure, many probes and measurement instruments need to be added to the system to monitor the current paths and determine the failure mechanism. The system level ESD testing is challenging and has many uncertainties in determining the exact current path as well as determining the devices which are impacted within a system. Gathering information about transient events effecting an IC without altering the system can be difficult. Intrusive hardware methods or sophisticated simulations may be required to determine if and how a particular integrated circuit (IC) was affected. Hardware modifications to measure the event can alter the way the transient event propagates through the system, causing different results during the measurement compared to the unaltered system.

Adding detection and sensing capabilities to different ICs in a system would enable the engineer to understand the different current paths better. These ICs would add non intrusive measurement capabilities to a system. Once an event is detected, preventive measures could be taken by the IC itself. This is the first step towards an intelligent system. Once the sensors are embedded into the ICs, they can relay the information to the user after system level tests. In the case of field failures, they can record the number of events and

determine and notify the user for maintenance of the system. However, all the above is limited to integration of the sensors within an IC. Alternatively, a sensor is designed which can be added during testing. These sensors are designed to be economical and small in size so as to be easily added to the system under test. The sensor has the capability to wirelessly transmit the level of the event detected to a measurement probe external to the system. Having the additional information related to the transient event can assist the engineer to understand the protection methodologies better and thus reduce time and cost in the process of system design.

PAPER

I. SYSTEMATIC EVALUATION OF SOFT-FAILURES IN SYSTEM LEVEL ESD TRANSIENT EVENTS

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ABSTRACT

A system such as a human assisting robot consists of many sub-systems such as sensors, display, motors, and control. When an electrostatic discharge (ESD) occurs, it can disrupt the normal operation of any sub-system. The paper analyzes such events beginning at the the tribo-charging down to the sensor disruption. The rolling wheels charge the robot, and a discharge occurs when it reaches the charging station. Based on the charge voltage, the discharge current is simulated using a simple switch model along with the loop impedance which limits the current. In multiple steps, the discharge current couples to the sensor. This coupling is represented as S-parameters obtaining the noise voltage at the sensor. This noise voltage is compared to the sensor's noise sensitivity threshold to reproduce the disruptive event. The model is validated with measurements. The simulation model can help system designers assess ESD risks without damaging hardware as well as efficiently design filtering components and effective on-board ESD protection.

Keywords: Electrostatic Discharge (ESD, Soft failure, Electromagnetic Interference (EMI), Robot, Tribo-charging, Coupling path.

1. INTRODUCTION

Electrostatic discharge (ESD) can cause hard failures or recoverable soft failures in a system (Standard, 2007). Soft failure related issues are increasing with the increase in system complexity. A complex system will have many subsystems which can experience soft failures during a transient event. Understanding which system fails and developing methods to prevent this failure is a challenging task and is critically important for designing a system which is robust to a high level of ESD risks.

If an ESD injects current into a system, strong electromagnetic fields (a 5 kV ESD will cause about 10 kV/m pulses at 0.1 m distance) are generated. The fields couple into different wires and traces (Cerri *et al.*, 1994, 1996) inducing noise voltages and currents. These noise voltages and induced currents can cause error bits in a data stream, transient latchup, etc. To optimize robustness of a system it is important to understand the source of the transient event, the coupling path as well as the impact on the system operation. This work provides a systematic methodology to model and understand the impact of an ESD event. The methodology is illustrated by the analysis of a human assisting robot which suffers soft failures upon reaching its charging station. Due to an ESD event, sensors in the robot are disabled. As the system recovers by reboot, these upsets are considered to be a soft failure problem.

At first, the charge voltage the robot can reach is analyzed by tribo-charging measurements in a climate chamber. The charge voltage is used to simulate the discharge current with a simple contact switch representing the contact action. This simple switch model can be improved to use the non linear arc resistance modeled by the arc resistance law of Rompe and Weizel (Rompe and Weizel, 1944). As the spark resistance is a function of the voltage and the surrounding impedance where the impedance is obtained by measurements.

In combination with the charge voltage, the discharge current is obtained. The discharge current couples in multiple steps to the sensor. Each of these steps is described by measured S-parameters to obtain the noise voltage at the sensor. This noise voltage is compared to the experimentally obtained sensor robustness threshold to predict the charge voltage at which the sensor will fail. Once the system has been modeled into a simulation environment, different filter options can be evaluated to reduce the soft failures for a certain level of transient event.

The methodology has been developed and validated for the detection of soft failures. An introduction to the important blocks of the system has been discussed in (Patnaik *et al.*, -to appear). This article describes in greater detail the characterization along with the validation of the different blocks. Here the simulation model is validated with measurements on the real system. This was achieved by enforcing a certain pre-charge voltage on the system; in measurement and in simulation and observing which sensors get disabled. The failure thresholds for different sensors need to be determined on the system and when used with the simulation model can predict which sensors will fail and for what peak pre-charge voltage. The simulation model was able to successfully determine the failure of the sensors.

2. METHODOLOGY

The methodology outlined allows to create a simulation model which predicts the impact of an ESD to the system. The system is divided into multiple blocks, modeled and then validated with measurements. Different blocks are then combined in a SPICE simulation to predict the noise voltage on a critical signal line. Comparing the noise voltage against the failure threshold voltage of the particular sensor will tell if the sensor will fail for a given charge voltage. In order to understand the worst case voltage the robot can charge up to, tribo-charging studies were performed on the robot. The tribo-charging study of the robot is discussed in subsection A. The modeling of the robot and charging station's electrical parameters is discussed in subsection B. Subsections C, D and E discuss:

the coupling of energy from the transient event location to common mode (CM) noise on different sensor wire systems, CM noise conversion to a noise voltage on the enable net, and failure threshold identification respectively. Section III discusses the application and testing of the complete SPICE model along with correlation to hardware followed by Section IV for discussion and conclusions.

2.1. Tribo-Charging Study. Tribo-charging is caused by friction between different bodies (Allen, 2000). The polarity and maximum charge developed on the bodies depends on many factors such as: material combination, temperature (T), relative humidity (RH), etc. The polarity of the surfaces in contact can be estimated based on the tribo-electric series (AlphaLab, 2009). The chart identifies the material combinations which can be used to minimize tribo-charging between bodies in contact. Using materials that are on the extremes of the chart enhances the chance of building up high level of charges. Studies (Pommerenke and Aidam, 1996; Ryser, 1990; Seng, 2000; Swenson *et al.*, 1995) have been performed to estimate the maximum and typical voltage a human can charge up to under different actions and flooring conditions. Similar studies have also been performed to understand the impact of climatic conditions in (Moradian *et al.*, 2014; Talebzadeh *et al.*, 2015a,b). The robot wheels make contact with the floor. When in motion, there is friction between them and the robot charges up. The same factors (material combination, climatic conditions, actions) influence the charge up of the robot.

The net voltage the robot can build up under different conditions is investigated. A contact less voltmeter (field mill sensor) was used for measuring the peak voltage on the robot. The test setup to measure the voltage on the robot is shown in Fig. 1a. The tests were performed in a climate controlled chamber where the humidity and temperature can be controlled. The flooring material over which the robot moved was changed to study the impact for different flooring types. The robot was made to follow different controlled motion patterns as illustrated in Fig. 1b. An example of the transient recorded voltage for the circular pattern movement is shown in Fig. 2. The voltage increased when the robot

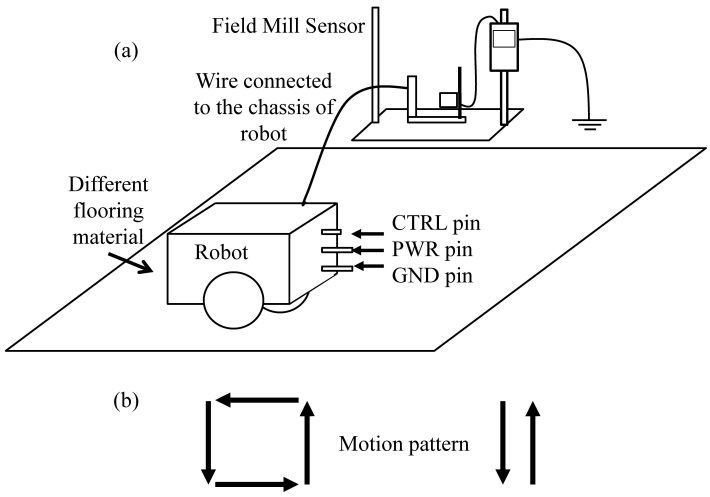

Figure 1. (a) Test setup for measurement of charge voltage on a robot, (b) Equivalent loop impedance model of robot and charging station.

was in motion and it discharges after it stopped. The decay can be attributed to the surface charge leakage due to the conductivity of the surfaces in contact and neutralization caused by ions in the air. The peak voltage recorded for different flooring materials under different climatic conditions is tabulated in Table 1. Tribo-charging studies give an estimate on the peak voltage the robot can charge up to. The assumption here is that the robot charges up to a certain peak voltage when approaching the charging station and an ESD occurs once the charging station is reached. The peak voltage recorded is used in the simulation models to estimate the currents and the voltages the sensors are exposed to. If the sensor's soft failure thresholds are known, it can be predicted if a soft failure occurs.

2.2. Loop Impedance and Primary Discharge Current. A discharge event occurs when the charged robot approaches the charging station and makes initial contact with it. A current loop is set up between the robot and the charging station due to charge sharing between the two bodies. The robot and the charging station have three pins which mate: the power (PWR), return (GND), and detect (CTRL) pin as shown in Fig. 1. By design, the GND and PWR pin have equal probability of making first contact. These two pins

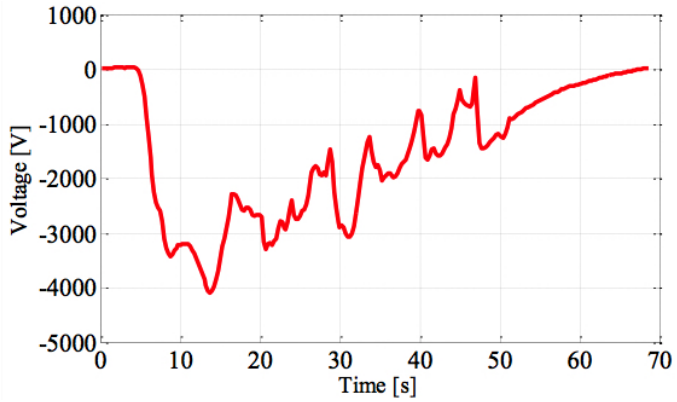

Figure 2. Transient voltage measured on the robot.

protrude out beyond the CTRL pin. To study the ESD event in a system, it is important to identify the location of the discharge. The following methodology has been applied under the assumption the GND pin makes first contact, but other tests have shown not much difference in the outcome with the selection of the PWR pin. The discharge current flows through the pins making first contact between the robot and the charging station. This current is referred as the primary discharge current. The primary discharge current has a very fast changing amplitude per unit time ($\frac{dI}{dT}$). The fast time changing discharge current can cause electric and magnetic field coupling to nearby sensor wire bundles, disrupting the normal operation of the system.

A loop is defined along the following path: Docking station contact, docking station to ground via the capacitance to ground or the wall adapter, via ground to the robot, from ground capacitively to the robot and back to the pins that contact the charging station. The robot impedance and charging station impedance forms the two halves of the loop. When the robot makes contact with the charging station, the loop for the current is established. The impedance of the robot and the charging station together form the loop impedance. The setup for measuring the loop impedance is shown in Fig. 3. Ports for input impedance measurements were defined between the contact pin and a large reference plane. A vector network analyzer (VNA) was used to measure the input impedance looking into the device.

Table 1. Charge voltage for different material and environmental conditions.

Material	Condition	Charge voltage
White-cotton	RH = 24%, T = 66°F	-1.7 KV
Poly vinyl chloride	RH = 24%, T = 66°F	-1.0 KV
Nylon on foam spacer	RH = 24%, T = 66°F	-4.0 KV
Styrofoam	RH = 31%, T = 66°F	-2 KV
Vinyl	RH = 31%, T = 66°F	-0.5 KV
Polyester	RH = 40%, T = 66°F	-2.6 KV
Polyethylene without anti-static coating	RH = 40%, T = 66°F	-2.5 KV
Polyethylene without anti-static coating	RH = 40%, T = 66°F	2.1 KV
Non-ESD protection	RH = 40%, T = 66°F	-2.0 KV
Teflon film on foam spacer	RH = 40%, T = 66°F	3 KV
Teflon film	RH = 40%, T = 66°F	1.5 KV
Ultra-high-molecular-weight polyethylene	RH = 40%, T = 66°F	0.43 KV

The details of the measurement are discussed in (Patnaik *et al.*, -to appear). Fig. 4. shows the measured impedance parameters. At low frequencies, the robot and charging station have a capacitive impedance profile. The capacitance was calculated from the measured input impedance. The robot has a capacitance of 47 pF while the charging station has a capacitance of 54 pF. The measured impedances are used in the SPICE simulation along with a HV (high-voltage) source on the robot side to replicate the system and simulate for the primary discharge current as shown in Fig. 3b. The HV source represents the voltage the robot has charged up to as a result of tribo-charging. The switch represents the docking action which initiates the fast transient event in the system. When the capacitance associated with the robot gets charged and makes contact with the charging station capacitance, charge sharing takes place and drives a loop current from the charged robot into the charging station.

The simulation model was validated by measuring the primary discharge current in a controlled setup. The current on the GND pin was measured using a current clamp (FCC F-65) on the charging station wire as shown in Fig. 5. The robot was charged to a pre-defined

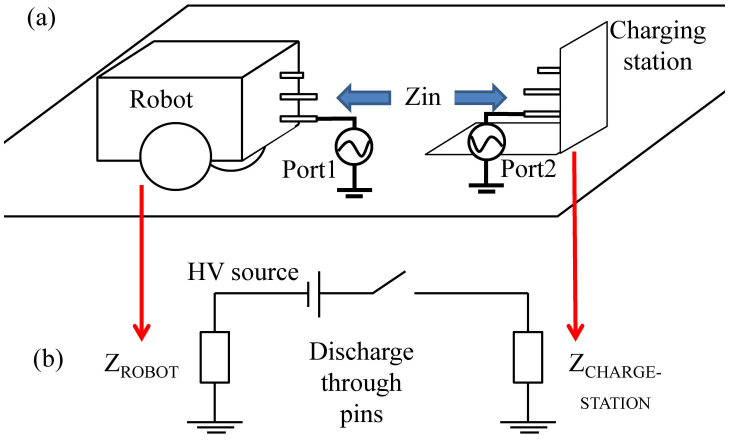

Figure 3. (a) Test setup to measure the loop impedance in the robot - charging station structure. (b) Equivalent SPICE representation using the measured loop impedances of the robot - charging station.

voltage using a HV source through a current limiting resistor. This configuration ensured a known voltage on the robot while docking. The SPICE simulation was configured with the HV source set at 1 kV and the currents were observed in the loop. The comparison of the measured and simulated loop current for a pre-defined voltage of 1 kV is shown in Fig. 6 where the loop current has a rise time in the order of 100's of pico-seconds. This fast rising edge transient current with a high magnitude is responsible for the noise disturbance in the system. The pulse width of 10 ns was observed for the initial peak. The peak values between measurement and simulations show agreement within 200 mA accuracy. This validates the model for the primary discharge current. The loop impedance model can similarly predict the primary discharge current through the PWR pins when using the PWR pin impedance models.

2.3. Coupling to Shields of Different Wire Bundles. After accurately identifying the origin and modeling of the fast transient current, it is important to capture the coupling path which couples energy from the discharge location to the enable signal net of the sensors causing a disturbance. The robot has many wire bundles connecting different sub-systems

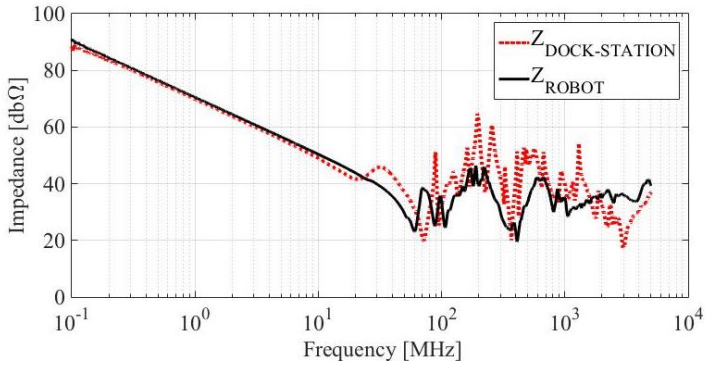

Figure 4. Measured input impedance for robot and charging station. Capacitance associated with the robot and charging station is calculated to be approximately 47 pF and 54 pF respectively.

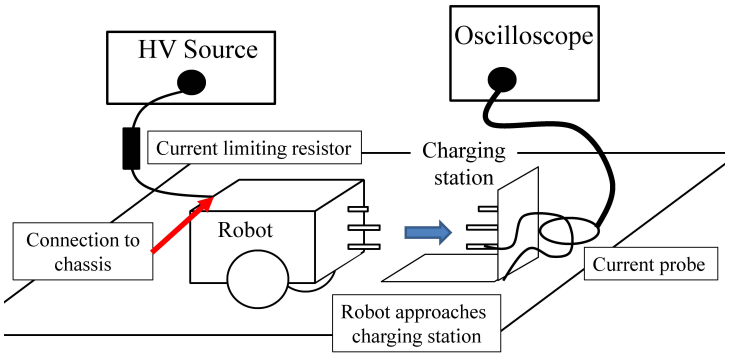

Figure 5. Test setup for measuring the primary discharge current during the docking action between the charged robot and charging station. The robot is charged to a known voltage using an external HV source through a current limiting resistor.

together. The wire bundles have signal wires which connect to the sensor modules. The electric and magnetic fields which arise due to the fast time changing, high amplitude current, couple onto these wire bundles. The nature of the coupling is not investigated as this article focuses on the methodology and application to model fast transient events and soft-failures in a system. The coupled noise current, is expressed in terms of a common mode (CM) current - $I_{CM,NOISE}$ which can further couple into the internal wires and cause disturbances. The source location of the primary discharge current was identified in the previous section to be the first contact location between the robot and the charging station,

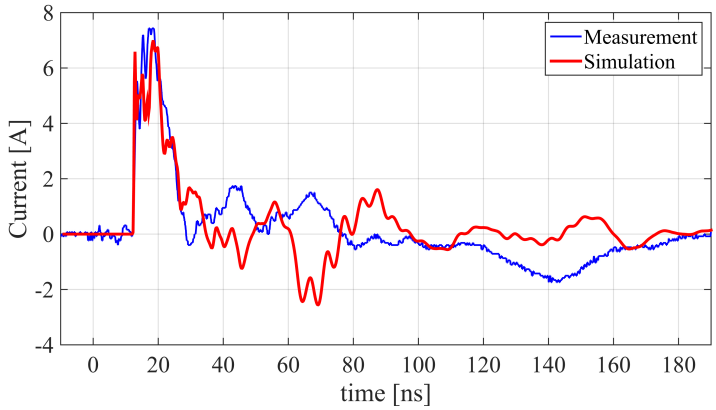

Figure 6. Comparison of measured and simulated primary discharge current on the GND wire of the docking station when the HV source is set at 1 kV.

the GND pin in this case. The coupling from the discharge location to the CM noise on the wire bundle is captured in terms of S-parameters. The measurement setup to measure the coupling is shown in Fig. 7. Port 1 of the VNA is defined at the aggressor location - between the GND pin of the robot and the GND pin of the charging-station while Port 2 is defined at the victim location using a current probe (FCC F-65) on different wire bundles. The measured network parameters were used in Block II in the simulation model shown in Fig. 8. The input to this model is the fast transient current from the current loop simulation. It is coupled into the simulation using a current controlled current source. The output of the block is the CM current on the wire bundle. The current is compensated with the probe factor of the current probe to compare to measurements. Coupling to different sensor bundles were measured and different S-parameter blocks were implemented representing the coupling to the different wire bundles.

The CM noise current model was validated using a controlled setup similar to Fig. 7, where port 1 was connected to a TLP source. The TLP has a fast rising edge (< 500 ps) with similar bandwidth as the primary discharge current. $I_{CM,NOISE}$ was measured at the same location (where port-2 for the S-Parameters was defined) on different sensor wire bundles using the current clamp. The CM noise current was measured using an oscilloscope and

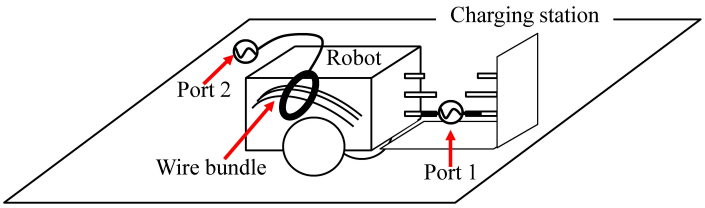

Figure 7. Test setup to measure the coupling from the primary discharge location to different sensor wire bundles.

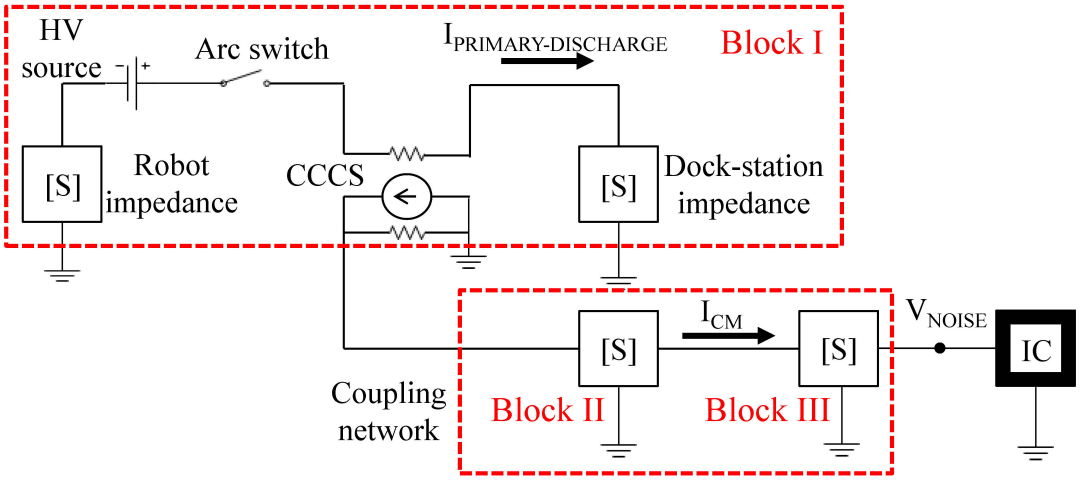

Figure 8. Complete simulation model. Block I represents the loop model which estimates the primary current. Block II represents the coupling between the primary current at the discharge location to the CM noise on wire bundles. Block III represents the conversion from CM noise to the noise voltage on the enable signal net.

a current clamp. In the simulation, Block II was excited in isolation using a TLP like source. The comparison between measurement and simulation for $I_{CM,NOISE}$ with a 1 kV TLP source voltage at port 1 is shown in Fig. 9. The peak, pulse width and frequency of the common mode current align well between measurement and simulations. The disturbance in system operation is primarily due to the peak current which the simulations predict well. The peak current for a 1 kV HV source setting on different sensor bundles is shown in Fig. 10. The CM peak current scales approximately linearly with the HV source. Though

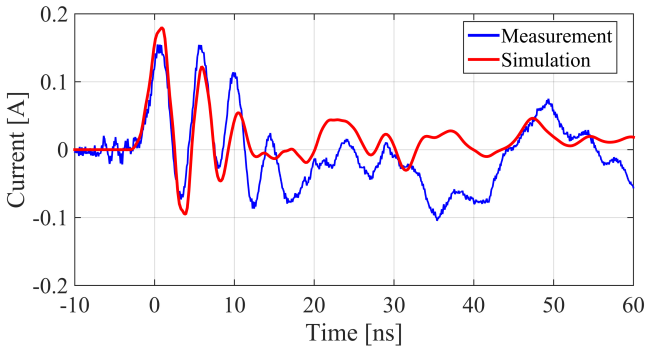

Figure 9. Comparison of measured and simulated CM current on sensor bundle 3 when the HV source is set at 1 kV.

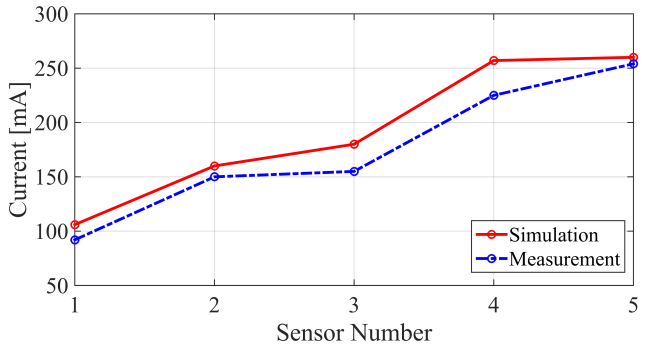

Figure 10. Comparison of peak measured and simulated CM current on all five sensor bundles when the HV source is set at 1 kV.

sensors 4 and 5 have the highest coupling from the injection port, they may not be the sensors which are most susceptible to failure. The sensor failure threshold determined later in the article determines which sensor is most susceptible.

2.4. Noise Voltage Measurement on Sensor Detect Line. The CM current on the shield of the sensor wire bundle can further couple into the individual wires and upset the signal integrity. The critical net identified here was the sensor enable signal. The perturbations on the enable signal net causes the obstacle sensor IC's logic to invert. Here the coupling path under investigation is from the CM current on the sensor wire bundles

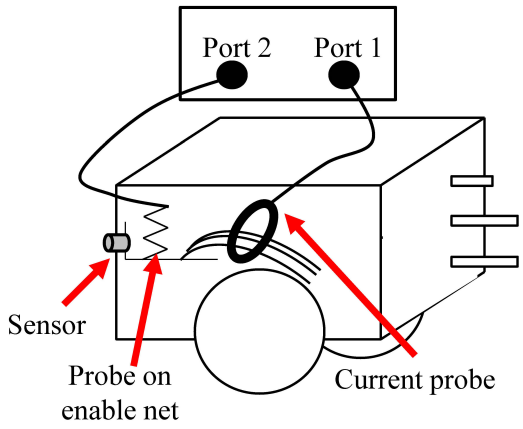

Figure 11. Test setup for noise characterizing the noise from the CM current on sensor wire bundles to noise voltage on the enable signal net. Similar setup is used for soft failure threshold measurements.

to the noise voltage on the enable net of the sensor IC. The coupling was measured using S-parameters and the measured parameters were then used in the simulation model (Block III of Fig. 8) for estimating the noise voltage on the enable line of the sensor IC's.

The coupling was measured as CM on the sensor bundle (Port-1) to the noise voltage on the enable signal line (Port-2) probed using a 1 kΩ resistor in order to avoid loading effects on the signal. CM current was induced on the sensor bundle using a current clamp (Port-1). The S-parameters from Port 1 to Port 2 were measured using a VNA for different sensor wire bundles and sensor modules as shown in Fig. 11. The S-parameters measured were used in Block III of Fig. 8. to determine the noise voltage on the enable signal. The validation of the noise voltage measurement is performed with the complete simulation model demonstrated later.

2.5. Soft-Failure Threshold Measurement. The threshold voltage on the enable net to cause a soft-failure (disabling of sensor) was determined. The test setup for determining the noise voltage for sensor failure is shown in Fig. 11. with a slight modification - the injection Port 1 was connected to a TLP while Port 2 was connected to an oscilloscope

Table 2. Simulation and testing results for different HV source settings.

		Peak voltage from simulation				
	HV source	Sensor 1	Sensor 2	Sensor 3	Sensor 4	Sensor 5
case 1	0. 1 kV	0.60 V	0.55 V	0.70 V	1.2 V	1.3 V
case 2	0.2 kV	1.15 V	1.20 V	1.40 V	2.10 V	2.40 V
case 3	0.3 kV	1.85 V	1.95 V	2.00 V	3.40 V	3.90 V
case 4	0.4 kV	2.40 V	2.45 V	2.60 V	4.80 V	5.00 V
case 5	0.5 kV	2.90 V	3.00 V	3.10 V	5.90 V	6.00 V

	Observations	
	Expectation from simulation	Measurement outcome
case 1	No sensor failure	No sensor failed
case 2	Sensor 4 and 5 will fail	Sensor 5 failed
case 3	Sensor 3, 4 and 5 will fail	Sensor 4 and 5 failed
case 4	All sensors will fail	All sensors failed
case 5	All sensors will fail	All sensors failed

to measure the noise voltage. The disturbance in CM was injected by a current probe using the TLP. The noise voltage on the sensor enable pin was monitored using a resistive pickup (to avoid any signal loading). A software application which monitors the status of every sensor in the system was used to monitor when the sensors get disabled.

The TLP source induces a CM current on the sensor wire bundle through the current probe. The TLP voltage was incremented and the noise voltage along with the status of the sensors was monitored. The noise voltage for which the sensor would fail was recorded. This is termed as the failure threshold voltage. All the sensors demonstrated a threshold voltage of approximately 2 V. The threshold voltage measurement was checked for repeatability. An alternative approach could be to use dedicated noise sensors embedded in the IC capable of detection of an over- or under-voltage on a signal line as shown in (Patnaik *et al.*, 2018) (Patnaik *et al.*, 2017). These sensors could store the peak noise voltage without addition of any external probes in the system.

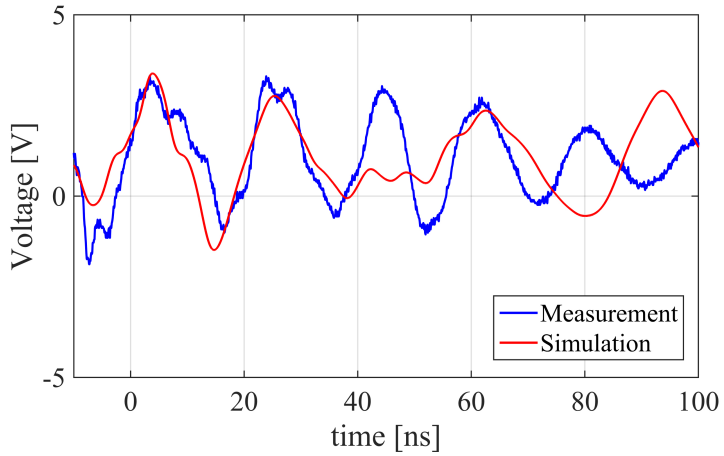

Figure 12. Comparison of measured and simulated noise voltage on the enable signal line for sensor 3 for a pre-charge voltage of 500 V.

3. APPLICATION AND TESTING

The simulation is performed with all the measured network parameters as shown in Fig. 8. The input to the simulation model is the peak voltage the robot can charge up-to while approaching the charging station. The output is the noise voltage at the enable pin of the sensor. Simulations were performed for different charge up voltages and the noise voltage was monitored. A validation of the noise voltage is shown in Fig. 12. The robot was charged using a HV source at 0.5 kV and the noise voltage on the enable signal was monitored while docking. The simulation was performed under the same conditions.

The simulation model predicts the correct frequency and peak for the noise on the enable signal net. The oscillation frequency was observed to be approximately 45 MHz with a peak voltage of nearly 3 V. This noise voltage is higher than the failure threshold and will cause the sensor to fail. The measurements confirmed the failure of the sensor which was simulated. Simulations were performed with different HV source settings from 0.1 kV to 0.5 kV. The noise voltages were monitored for all the sensors enable pin. Table II lists the peak voltages identifying the sensors which would fail based on the simulations. Measurements were similarly performed with different HV source settings and observing

the status of the sensors when the robot docked. The simulations were able to predict which sensor would fail for which pre-charge voltage setting within ± 20%. From simulations it was determined that the sensor 5 starts failing at a pre-charge voltage of 0.2 kV. All the sensors fail above 0.4 kV. This correlated well with measurements.

4. DISCUSSION AND CONCLUSIONS

A method to characterize system level soft failures is discussed. In this study a robot with many sensors is under study. The cause of the soft failures was identified experimentally. The system is separated into important blocks and the blocks are characterized in isolation to create a multi-step simulation model. The blocks are then validated with measurements. The study covers the charge up of the robot, the ESD event, the coupling and the sensor soft failures. The simulation model is developed for different sensors in the system as each network parameter block measured is different for each of the sensor systems. This type of simulation model is limited by the assumption of linearity of the system. The characterization is performed using a small signal model powered by the VNA. When transient events having significant amplitudes occur, non linear devices, such as internal ESD protection devices can turn on. The simulation models would fail to predict the non-linear response as the system was characterized at much lower current levels. Only at the spark, and at the sensor response it is possible to include non linear effects. The coupling path, described by S-parameters needs to be linear.

The simulation models can be used to evaluate the effectiveness of certain filters and ESD protection devices. By adding filters on the enable net, the noise can be filtered. The optimal filter design can be achieved by simulation methods rather than performing tests on the actual hardware. Having system level simulation models at hand for ESD robustness testing to evaluate different protection devices prevents having many hardware failures during the testing phase. This is both cost effective and time efficient.

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II. AN ON-CHIP DETECTOR OF TRANSIENT STRESS EVENTS

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ABSTRACT

Testing and debugging of electrostatic discharge (ESD) or electrical fast transient (EFT) issues in modern electronic systems can be challenging. The following paper describes the design of an on-chip circuit which detects and stores the occurrence of a fast transient stress event at the ESD protection structures in an I/O pad. Measurements and simulations of a test chip in 90 nm technology show that this circuit can accurately detect and record the presence of a transient stress event with a peak current as low as 0.9 A or a duration as short as 1 ns, and that the detector works well across typical temperature and process variations. The small size of the detector allows it to be used effectively in low-cost commercial ICs. The detector was tested in a system level environment and successfully records transient events. The importance of simulating with intelligent approximations of the system parasitics is described and demonstrated in measurements. An improved detector is discussed which performs better in terms of process variations.

Keywords: Electrostatic discharge (ESD); Electrical fast transient (EFT); System level ESD; On-chip measurements; ESD detectors.

1. INTRODUCTION

Electromagnetic immunity to transient electrical events can be a major problem for electronic systems. While electrostatic discharge (ESD) or electrical fast transient (EFT) events can cause permanent damage, soft errors are often more challenging, as it is difficult to determine how the soft error occurred, and it is not always possible to detect all soft errors in a typical test procedure. Debugging of immunity problems is a time intensive task which is becoming increasingly difficult with the shrinking size and growing complexity of electronic systems.

Isolating which integrated circuits (ICs) are affected by a transient electrical event is difficult. Intrusive hardware measurements or sophisticated simulations are often required to determine where design changes are needed. An alternative to adding hardware or relying on simulations is to provide on-chip circuitry, which detects transient events at input/output (I/O) pins and provides these measurements to the user through on-chip software. There are many challenges to this approach. The scheme must be area, cost, and power efficient; it must function accurately during the transient event; it should not be triggered by normal signals at the I/O; and more.

Circuits that can be used to detect on-chip transient events have been proposed by others, but do not give information about events at individual I/O pads - a necessary capability for effective debugging and analysis. The circuit proposed in (Ker *et al.*, 2008) (Thomson *et al.*, 2017) capacitively couples energy from the on-chip power delivery network to the input of a static latch, so that a rapid change in the power supply voltage from a transient event causes the latch output to switch state. A modification where multiple copies of the circuit with different RC time constants are connected in parallel allows determination of the level of the transient power supply disturbance (Ker and Yen, 2009). A sample-and-hold circuit was proposed in (Chow and Hor, 2008) providing a measure of the power supply noise. A similar circuit was proposed in (Sehgal *et al.*, 2006) for detecting power supply over- and under-shoot. While these circuits were not explicitly designed to detect transient

stress events, it is one possible application of the circuits. The circuit in (Gerdemann *et al.*, 2007) and (Jack and Rosenbaum, 2011) was designed to detect the peak voltage at an I/O pad during a fast transient event, but has limited capability and is only appropriate for use in the lab.

These circuits either do not give information about which I/O pins were affected by a transient stress event or are not suitable for use in the field. The goal of the work presented here is to develop a small, inexpensive circuit which can be used in low-cost commercial ICs to detect fast transients which stress the ESD protection structures at individual I/O pins. Application software can then read information about when and on which pin an event has occurred. The following article describes the design and testing of the proposed fast transient stress detector, its performance across process variation and temperature, and measurements of circuit performance on a microcontroller-based product test chip.

2. EVENT DETECTOR

A typical IC ESD protection scheme with I/O protection diodes, a power clamp, a trigger block for the power clamp, and an ESD-boost bus is shown in Fig. 1 (Stockinger *et al.*, 2013). When the I/O pad is subjected to a transient stress event, the voltage on the I/O pad either goes higher than V_{DD} and current is injected into the VDD rail (i.e. during a positive event), or the voltage on the I/O pad goes below V_{SS} and current is drawn from the VSS rail (i.e. during a negative event). Fast transient stress detectors were designed to sense the voltage drop across the I/O ESD protection structures during the event. While Fig. 1 and the following development assumes the use of diode-based ESD protection, the detectors can be used with other protection schemes as well.

2.1. Circuit Design. Detection is enabled by placing a MOSFET across the ESD protection diodes as shown in Fig. 2. The diode, D1, in this figure is the same as the diode D1 in Fig. 1. For the positive detector (Fig. 2a), the gate of PMOS transistor M1 is connected to VDD and the source is connected to the pad. The negative detector (Fig. 2b)

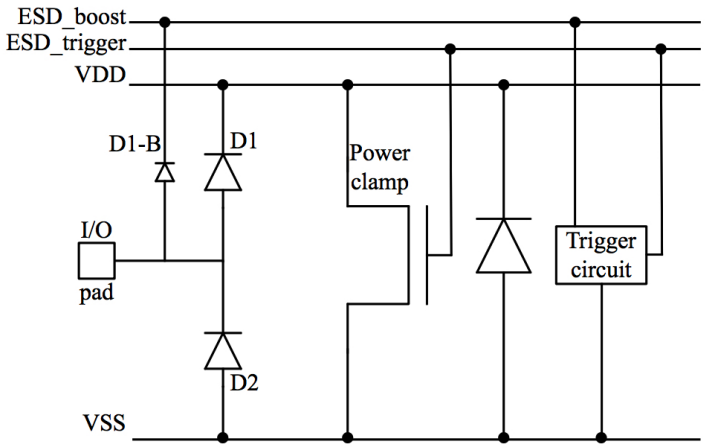

Figure 1. A typical IC ESD protection scheme showing the ESD protection diodes and power clamp network.

is connected similarly, with the gate of the NMOS transistor M10 connected to VSS while the source is connected to the pad. The MOSFETs M1 and M10 add less than a few tens of femtofarads of capacitance to the I/O pad and have negligible impact on signal integrity. Sense transistor M1 will be turned on if the voltage drop across the ESD protection diode from the pad to VDD is more than a PMOS threshold voltage. M10 is similarly turned on if the voltage from VSS to the pad is greater than an NMOS threshold voltage. The current driven by the FETs is directly related to the diode voltages, which depend on the transient stress currents.

The drains of M1 and M10 connect to latches, as shown in Fig. 2. Under normal conditions, the output of the latches are in a reset state. The user places the latches in the reset state by briefly turning on transistors M2 and M11 and turning off M6 and M14. A transient stress event of sufficient size will turn on the sense FETs and cause the latch outputs to switch state. In the case of the positive event detector, node ‘A’ is normally low and the output (‘Out-p’) is pulled high. When the pad is subjected to a positive transient stress event, M1 turns on, drawing node ‘A’ high, which switches the output low and flips the state of the latch. The latch output remains low as long as the power supply voltage

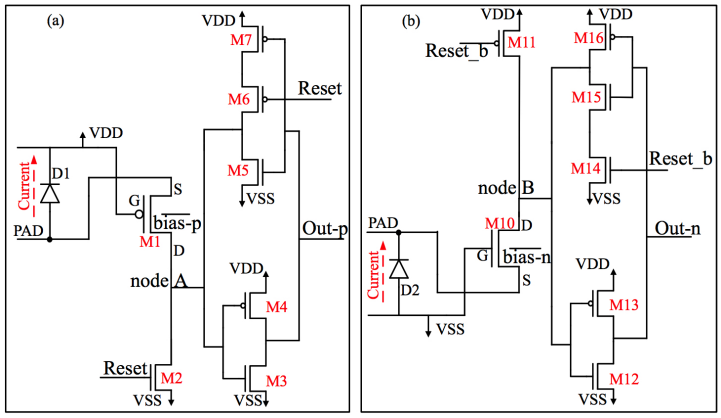

Figure 2. Event detector circuits - (a) Positive detector (b) Negative detector.

stays above a FET threshold level, so the occurrence of a transient stress event can be read from the latch long after the event has passed, even if there is a significant droop in V_{DD} caused by the event. The negative detector works in a similar manner. The latch states are not affected by a power-on reset of the IC, allowing the IC to know if a stress event has occurred even after a transient induced reset. This may aid in the forensic analysis of the cause of the reset.

2.2. Switching Threshold of the Latch. A sufficient voltage must be developed across the ESD protection structure during a transient stress event to switch the latch state. The switching threshold voltage of the positive detector is primarily determined by the sizes of MOS devices M1 and M5, the switching threshold of inverter M3/M4, and the MOS device characteristics. At the moment of switching, the current through M1 equals the current through M5:

$$k_p'\left(\frac{w}{L}\right)_{M1}\left[\left(-V_D - V_{t,p}\right)V_{d,satp} - \frac{V_{d,satp}^2}{2}\right] = k_n'\left(\frac{w}{L}\right)_{M5}\left[V_{OP} - V_{SS} - V_{t,N}\left(V_A - V_{SS}\right) - \frac{\left(V_A - V_{SS}\right)}{2}\right] \tag{1}$$

where $k_p^{'}$ and $k_n^{'}$ are the process trans-conductances for the PMOS and NMOS devices, respectively, $(\frac{w}{L})_{M1}$ and $(\frac{w}{L})_{M5}$ are the width-to-length ratios of M1 and M5, V_A is the voltage at node 'A' (shown in Fig. 2), V_{OP} is the voltage at the output node 'Out-p', V_D is the voltage drop across the diode, $V_{t,P}$ and $V_{t,N}$ are the threshold voltages for the PMOS and NMOS devices, and $V_{d,satp}$ is the velocity saturation voltage of the PMOS device. Solving (1), the V_D required to switch the latch is given approximately by

$$V_D = V_{t,P} + \frac{V_{d,satp}}{2} + \left\{ \frac{k_n^{'}}{k_p^{'}} \left(\frac{w}{L}\right)_{M5} \left(\frac{w}{L}\right)_{M1} \frac{1}{V_{d,satp}} \left[(V_{OP} - V_{SS} - V_{t,N}) \left(V_{A,SW} - V_{SS}\right) - \frac{\left(V_{A,SW} - V_{SS}\right)}{2} \right] \right\}, \tag{2}$$

where $V_{A,SW}$ is the switching threshold of inverter M3/M4. The transient stress current required to reach this voltage depends on the diode characteristics. The diode voltage is primarily dependent on the stress current level, though it may also depend on the rise time and pulse width of the current pulse, due to overshoot and transient self-heating effects, respectively.

As indicated in (2), the latch threshold voltage can be controlled by changing the sizes of M1 and M5. It should be noted that the switching threshold of the detector is not strongly dependent on the power supply voltage. This independence allows the circuit to work effectively even when there is a large disturbance of the power supply during a transient stress event.

2.3. Setting Body Bias of the Sense MOS Device. The sense transistors form parasitic lateral BJTs. In the positive detector, for example, PMOS transistor M1 forms a PNP device Q1 with its collector tied to node 'A' and its emitter connected to the pad, as illustrated in Fig. 3. The body of M1 forms the base region of Q1. If the body terminal of M1 were connected directly to VDD (dashed line in Fig. 3), the emitter-base junction of Q1 would be in parallel with the ESD protection diode D1 and would be forward-biased during

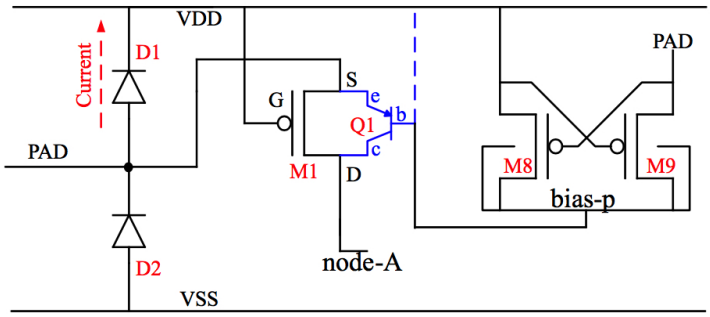

Figure 3. Body biasing circuit for PMOS M1, the sense MOS device in the positive detector. Parasitic BJT Q1 could be turned on if the body of MOSFTET M1 were connected to VDD (dashed line). The biasing circuit M8/M9 helps prevent Q1 from turning on during a positive transient event.

a positive stress event at the pad. This would activate Q1 and cause substantial PNP current flowing from the emitter (pad) to the collector (node 'A'), in parallel with the MOS channel current of M1. The additional PNP current would make the detector more sensitive to stress events and may be leveraged for this purpose in some designs. However, while the electrical behavior of PMOS M1 may be modeled quite accurately, the PNP Q1 may not, due to the parasitic nature of the device and its dependence on a specific layout implementation. The lack of an accurate PNP model made us choose a different approach, where a body-biasing circuit was used to prevent the emitter-base junction of Q1 from turning on.

The body-biasing circuit shown in Fig. 3 ensures that the body of M1 is biased at the higher of the pad voltage and V_{DD}. When the pad voltage is at least a PMOS threshold voltage higher than V_{DD}, PMOS M9 is turned on and M8 is turned off, coupling the shared body of M1, M8, and M9 to the pad. When V_{DD} is at least a PMOS threshold voltage higher than the pad, the body is coupled to V_{DD}. This circuit therefore prevents activation of the parasitic PNP device Q1.

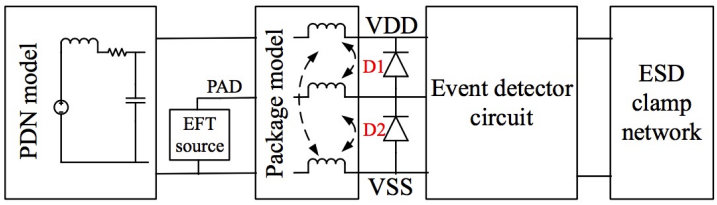

Figure 4. Test bench for characterizing detector performance.

A similar biasing circuit is used in the negative event detector. The sense NMOS device is implemented in an isolated P-well. Here the isolated P-well is biased at the lower of the pad voltage and V_{SS} to prevent the parasitic NPN device from turning on during a negative stress event on the pad.

3. SIMULATION

The transient event detectors were included in a 90 nm technology microcontroller test chip and were simulated using SPICE. A block diagram of the simulation setup is shown in Fig. 4. This test bench represents a full transient immunity test environment including the printed circuit board (PCB) power delivery network (PDN), the package, the EFT source, the ESD protection structures, the on-die power delivery network, and the I/O pad cell. This setup was designed to reflect the physical setup used later to test the detectors in hardware.

The PCB PDN model was extracted from measurements on an existing test board. An IC package model was used which takes into account all parasitic self and mutual inductances and capacitances and parasitic resistances that are part of the bond wire and lead frame. Results shown later in this paper demonstrate the full package model is required for accurate system level simulation. The ESD diodes were characterized for this technology and SPICE models were developed that capture the I-V curve responses, the transient overshoot, and the impact of self heating, all with good accuracy (Stockinger *et al.*, 2009).

In addition to the ESD protection diodes, the ESD protection network includes power clamps and dedicated trigger cells which use a boost bus architecture, as illustrated in Fig. 1 (Stockinger *et al.*, 2003). This protection network uses a boost bus to provide a large gate voltage to the power clamp and uses a proportional triggering scheme which turns the power clamps on in regulation mode as opposed to a strict 'on' or 'off' mode (Stockinger *et al.*, 2013). Using the clamps in regulation mode prevents V_{DD} from collapsing during a transient event and thus minimizes the occurrence of system upsets. Because the power supply voltage will not be lost during the event, the event detectors should be able to retain the detector latch state throughout the transient event. The power clamp network consists of distributed power clamps located within each I/O cell which are triggered by a signal on the common trigger bus.

The simulation model takes into account the presence of 100 I/O pads along with the distributed trigger and power clamp network associated with these I/Os. The trigger circuits are repeated at regular intervals among the I/Os to ensure uniform triggering across the I/O pad ring. The detectors were tested using transmission line pulse (TLP) and powered ESD (PESD) gun-type stress events as specified by IEC 61000-4-2. The source was applied between an I/O and VSS. Figures 5 and 6 show the simulation results for a 4 kV PESD source and a 5 A TLP source, respectively. These levels are sufficient to significantly disturb the power delivery network and show if the detector output will remain stable. During the rising edge of the event, the power delivery network voltage nearly doubles over its normal value. The supply voltage similarly drops during the falling edge of the TLP event. The waveforms show that the detectors successfully detect and record the presence of the transient events.

Simulations were performed when the I/O pad was stressed with TLP injections with peak currents ranging from 0.5 A to 3.5 A and with pulse widths varying from 1 ns to 50 ns. Figure 7 shows the switching threshold of the detector (in terms of the ESD current) as a function of the pulse width and of device process corners. The switching threshold current was determined by the current level which caused the detector to latch onto the

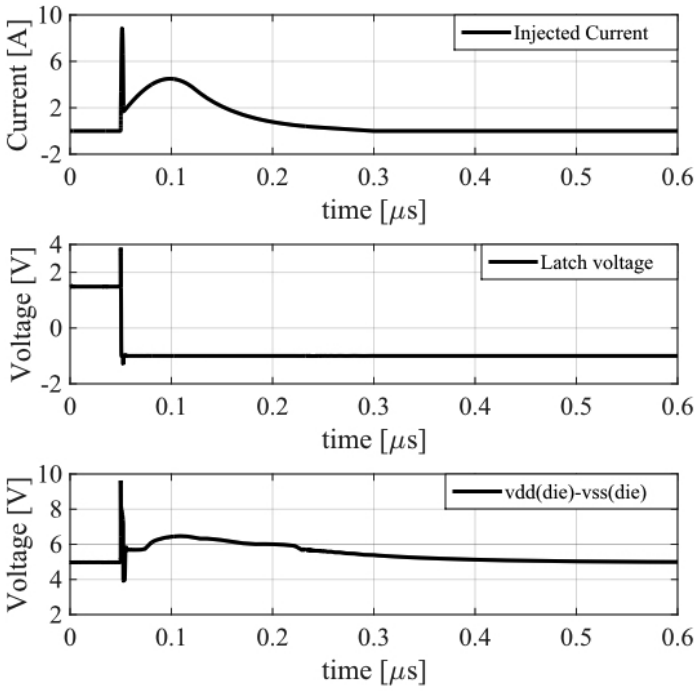

Figure 5. Simulated transient waveforms for a 4 kV IEC-61000-4-2 type PESD event between an I/O and VSS.

event. Simulations were performed for 'typical,' 'slow,' and 'fast' process corners. In the legend in Fig. 7, a 't' represents a typical process, an 's' represents a slow process, and an 'f' represents a fast process. The process corner used for the NMOS device is given first in the legend and the corner for the PMOS device second. For example, the curve labeled 'sf' shows a simulation for a 'slow' NMOS device and a 'fast' PMOS device.

As shown in Fig. 7, short events (e.g. less than 5 ns for the 'tt' case) require higher transient current levels to trigger the latch than long events. The switching threshold does not change for pulse-lengths longer than 10-20 ns. The threshold current varies by nearly 2 A between 'sf' and 'fs' process corners, or about -55% to 145% from the 'tt' case. This variation is expected due to the changing drive strength of the opposing FETs M1/M5 and M10/M16 in the latch, as shown in Fig. 2 and in (2). In the worst case (the 'fs' corner),

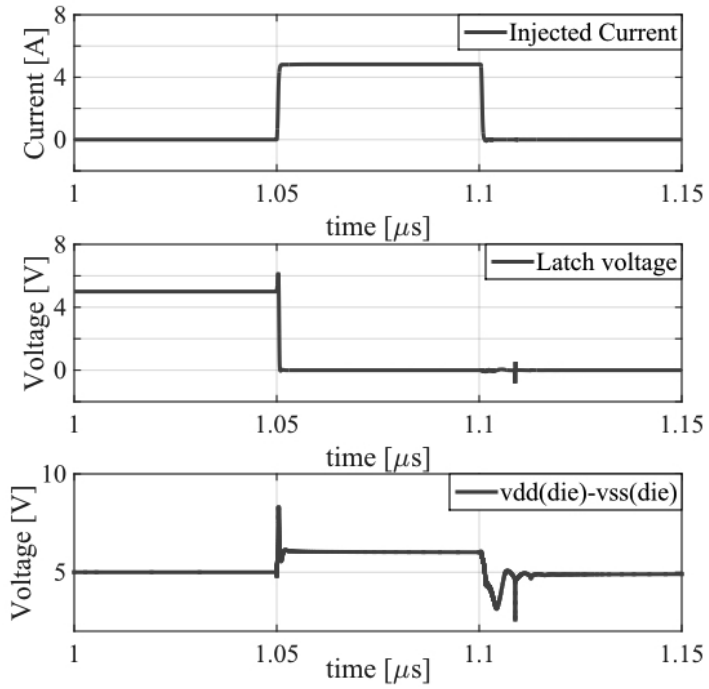

Figure 6. Simulated transient waveforms for a 5 A TLP event between an I/O and VSS.

the detection is limited to events larger than 2.25 A, or roughly a 4 kV PESD event. The worst-case current detection level could be reduced by changing the relative size of M1/M5 and M10/M16 if required.

Figure 8 shows the detector response for IC temperatures ranging from 10°C to 45°C. Reducing the temperature increases the switching threshold current for longer pulses (i.e. longer than 5-20 ns). The switching threshold current for longer pulses varied by about 0.2 A, or about ±12% from the typical case.

4. IMPLEMENTATION AND MEASUREMENT

Positive and negative event detection circuits were implemented and tested in hardware. The circuits were implemented on a microcontroller product test IC manufactured using the same 90 nm technology as was used in simulations. Event detectors were added

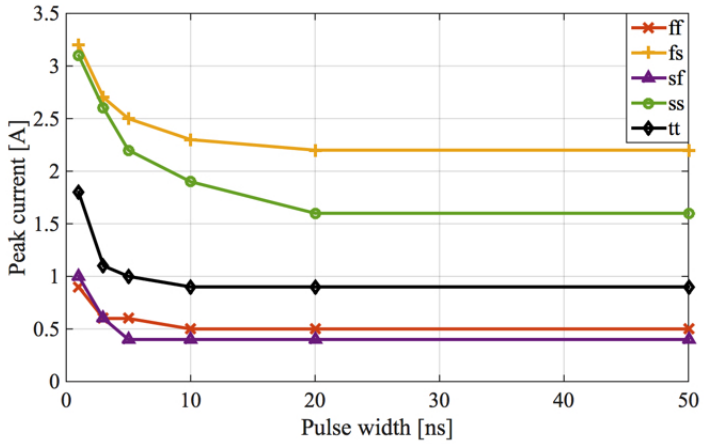

Figure 7. Simulated ESD current switching threshold for the positive detector as a function of transient event pulse width and process corners.

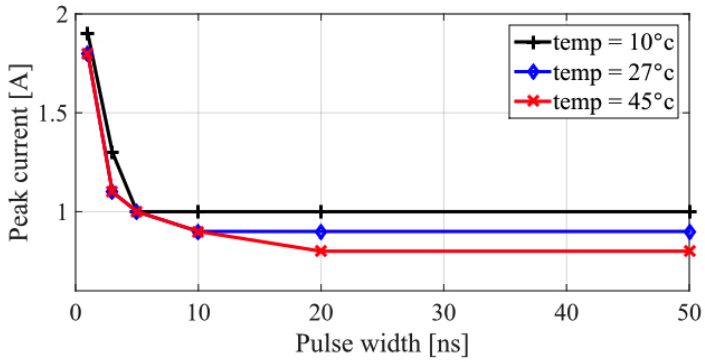

Figure 8. Simulated ESD current switching threshold for the positive detector as a function of transient event pulse width and IC temperature.

to 72 out of 100 I/O pad cells on the IC using abutment cells. In this chip implementation, the abutment cells contained additional circuitry that was not part of the detectors. If the detector circuits were added to an I/O pad cell, we estimate that the total area of the cell would increase by approximately 7%. Therefore, the area required for the detectors is relatively small. The addition of these event detectors does not impact the normal operation of the microcontroller.

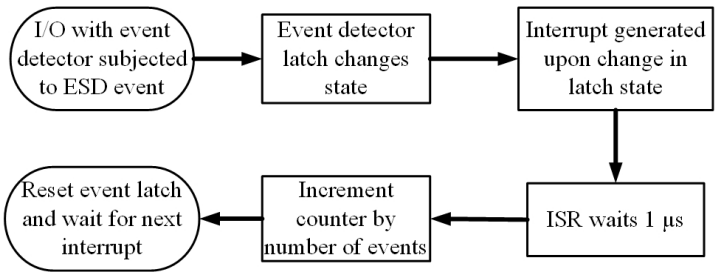

Figure 9. Flow chart for detecting and reporting stress events in the microcontroller test IC.

To provide the microcontroller with access to the detector data, the latch outputs were converted to the core voltage level and then routed to addressable registers within the chip core. By accessing these registers, the microcontroller can see the state of the positive and negative detector outputs at each of the 72 I/O cells. Hardware was also provided to generate a software interrupt when a transient event is detected. The output of all the event detect latch registers are logically OR'ed to generate the interrupt request flag (Patnaik *et al.*, 2017c).

A flowchart for the microcontroller software used during testing is shown in Fig. 9. Upon power-up of the microcontroller, the event latches are reset and brought to their normal "ready" state. When a transient event is detected, an interrupt service routine (ISR) is called. The ISR waits 1 μs before reading the event detect registers to ensure the on-die power supply voltage has stabilized after the event. After the delay, the ISR reads the event detect registers, stores the values of the registers in memory, increments the value of a counter, resets the latches to their "ready" state for detection of the next event, and then exits, allowing the normal microcontroller code to resume execution. The stored values of the event detection registers and the count of the number of events are later read from the microcontroller through a serial port.

4.1. Measurement of Standalone Detectors. The event detectors were tested with a TLP using the setup shown in Fig. 10. A contact probe was used to apply a transient stress between I/O pads and VSS (Patnaik *et al.*, 2017c). Spring loaded pogo-pins were used to

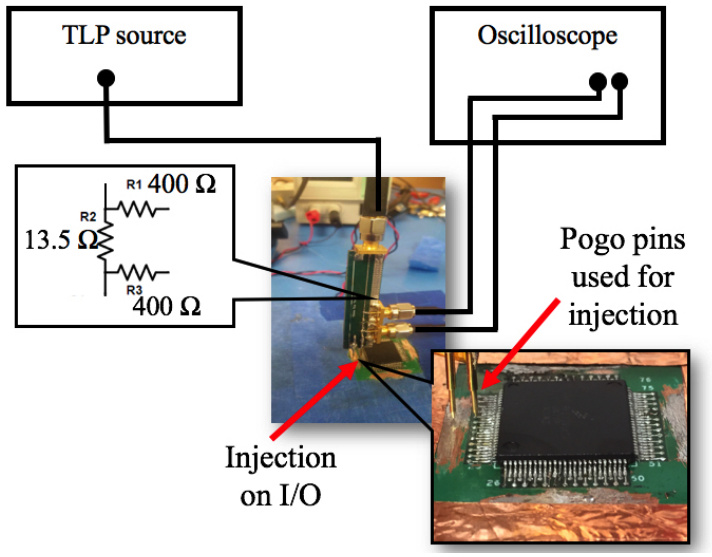

Figure 10. Test setup for characterizing the event detector on the test IC. A resistive pi-network on the injection probe is used to measure the injected current by measuring the voltage across a known resistor.

ensure good contact to the PCB. The TLP pulse had a rise time of 300 ps and a variable pulse width between 1.5 ns and 40 ns. The TLP voltage was varied to determine the detector switching threshold current for each pulse width. The probe allowed precise determination of the injected current by measuring the voltage across a resistor placed in series with the pad. The values of components used in this measurement circuit were selected to ensure a well-matched 50-ohm system impedance.

Figure 11 shows the measured switching threshold current for the positive detector as a function of pulse width. The measured values are compared to the simulated thresholds for a 'tt' corner case simulated at room temperature. Measured detector thresholds matched the shape of the simulated thresholds and were well within the limits predicted with process variation.

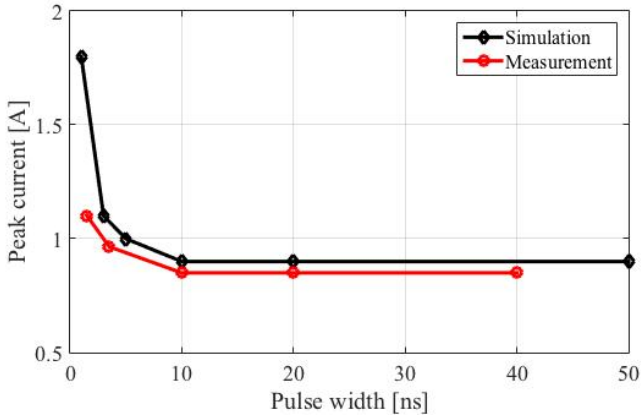

Figure 11. Comparison of measured and simulated threshold currents for the positive detector.

Another test was performed where the I/O pad was stressed with ten consecutive 40 ns wide pulses of the same magnitude spaced more than 100 ms apart. The number of detected events was then read from chip memory. The microcontroller was able to reliably detect all 10 pulses when the pulse-magnitude was above 0.9 A. This result is in-line with simulations.

Mutual inductance can allow coupling between package pins. To demonstrate the effect of mutual inductance, a positive injection was performed on one I/O pin (I/O-1) while an adjacent pin (I/O-2) was shorted to the on-board VSS. A positive current (into the IC) induces a current in the opposite direction on the adjacent pin due to the mutual inductance between the two pins. For I/O-2, the current can be significant, since there is a low-impedance path to VSS on the board. This coupled current can trigger the I/O-2 negative detector. Similarly, a negative injection on I/O-1 may trigger the positive detector in I/O-2. It is easier to trigger a positive event when I/O-2 is connected to VDD than to VSS, though either connection may allow a positive stress event. Table 1 compares the minimum injected current on I/O-1 required to trigger a detection on I/O-2 as found in measurement

Table 1. Minimum current to trigger detector on adjacent pins.

	Simulation	Measurement
Positive injection on I/O-1, I/O-2 shorted to VSS.	2.1 A	1.65 A
Negative injection on I/O-1, I/O-2 shorted to VDD.	-1.7 A	-1.7 A

and simulation. This measurement was repeated on multiple pin pairs around the IC and found a variation of about 150 mA in the threshold between pins. Only the average values are listed in the table.

These results demonstrate that a transient event on a single pin may trigger multiple detectors. A full package model is important when simulating the impact of transient events, as the mutual inductance between pins must be included in the model to determine the impact on neighboring pins. While the neighboring pin was shorted for the results shown in Table 1, a short to VDD or VSS is not required. Tests and simulations performed when I/O-2 was connected to a 5 cm trace terminated with a high impedance also triggered the detector in I/O-2, due to the capacitance between the trace and VSS on the board.

4.2. System Level Tests. The detectors were also evaluated in system-level tests. The first test followed the methodology outlined in the IEC-61000-4-2 standard (Standard, 2007) for ESD testing of devices and equipment. A typical IEC-61000-4-2 setup is shown in Fig. 12. The test PCB with the microcontroller was placed on an insulated surface on a metallic table. An ESD gun was discharged to the return plane of the PCB, to the horizontal coupling plane and to the vertical coupling plane. Injections were made with the gun at multiple orientations to the horizontal and vertical coupling planes. Injections to the PCB were made normal to the return plane. These injections are expected to couple energy inductively and capacitively to the IC. Injections were separated sufficiently in time to allow the coupling planes to discharge through bleed resistors between tests.

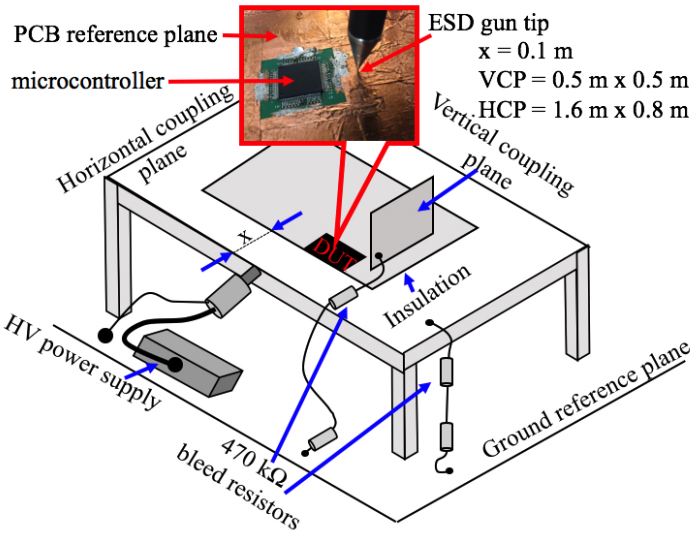

Figure 12. IEC-61000-4-2 system level test setup. The close-up of the DUT shows the microcontroller soldered on the test PCB with an exposed reference plane. Contact mode ESD tests were performed to the horizontal and vertical coupling planes and adjacent to the microcontroller.

When injecting to the return plane of the IC, the IC began detecting events for an ESD gun setting of 9 kV when the gun was discharged 1 cm from the microcontroller. The event was detected on two pins, the reset pin and a communication pin. No events were detected when injecting to the vertical coupling plane for an ESD gun setting up to 20 kV. This result was not surprising as there should be poor magnetic field coupling between the vertical plane and the microcontroller. When discharging the ESD gun to the horizontal coupling plane, events were observed but required a much higher level ($\geq$ 14 kV) to trigger the detectors than when discharging to the PCB. The common pins triggered from both the tests, however, were the same: the reset pin and the communication pin. The reset pin is connected to a capacitor. This capacitor can provide a low impedance path to the return plane for any energy coupled magnetically to the pin, allowing significant current through the ESD protection diode. The communication pin was connected to a 2 cm cable that was

unconnected (open) at the other end allowing significant electric field coupling to the pin. When the test was repeated with the cable removed, no detection was observed for the same stress level.

A similar study was conducted to measure the ESD events seen by a wearable electronic device (Patnaik *et al.*, 2017a). The microcontroller I/Os were connected to cables which were worn by a human test subject. The ESD events seen on the I/O were recorded for a variety of test scenarios, where the discharge electrode was located at different positions on the body when the test subject was charged to a high voltage, as well as the discharges seen during normal daily activity. Additional tests were performed when plugging a charged cable into an IC port to simulate a cable discharge event. The detector reliably detected human-metal model and cable discharge type ESD events.

5. ALTERNATIVE DESIGN

The circuit presented here was designed to minimize area. An alternative design is possible which uses modestly more area but reduces the sensitivity of the detector threshold to process variation. The alternative design is shown in Fig. 13. In this configuration, the current from the sense PMOS (M1) is mirrored through M17/M18 so that M1 drives against PMOS - M23 to switch the state of the latch. In the original design, the sense PMOS (M1) was driving against an NMOS, so the switching threshold was dependent on the characteristics of both FETs and their potentially mismatched process corner cases. Figure 14 shows the reduced variation in the threshold of the alternative design. The threshold varied by up to 1.2 A in the new design, and varied by up to 2 A in the original design. The impact of process corners was reduced by 40%.

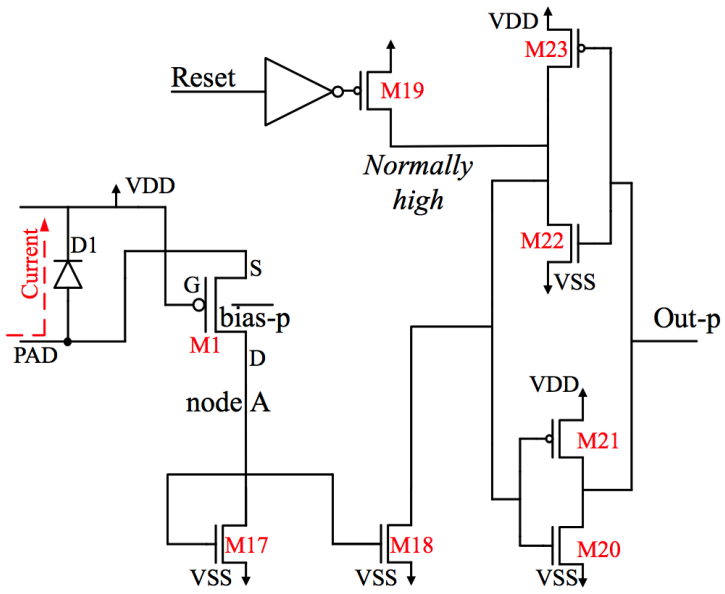

Figure 13. Proposed positive detector circuit for better matching across process corners.

6. DISCUSSIONS AND CONCLUSIONS

An on-chip detector for fast transient stress events was developed and shown to reliably detect transient events as short as 1 ns. These detectors allow the IC to actively determine when an I/O pin is affected by an electrical overstress event, as well as the polarity of the event.

System level tests and simulations have demonstrated that multiple pins may be triggered by a single event, due to inductive coupling between the pins. Even a small capacitance, like that of a short PCB trace, can allow a sufficiently low-impedance return path for the inductively-coupled current to exceed the detection threshold on a non-stressed pin. The detectors were also tested and performed well in an application environment where ESD events to a wearable device were studied.

Information about the presence of transient stress events can be used to improve the quality and reduce the time and difficulty of immunity testing of electronic systems. By directly measuring when transient stress events occur, these detectors could reduce the

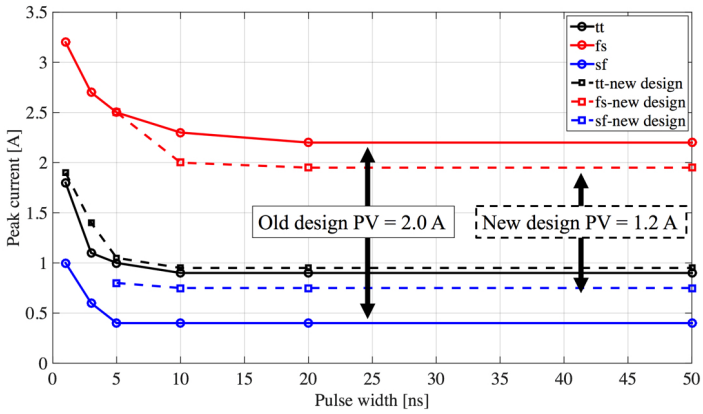

Figure 14. Comparison of implemented and proposed alternative circuit showing simulated ESD current switching threshold as a function of transient event pulse width and process corners.

uncertainty of soft-error testing, where it is often difficult to detect all errors. Transient stress detectors could allow for improved debugging of immunity errors by allowing the tester to focus their attention only on pins which are impacted by a transient event and by providing direct feedback as to whether a system-level design change eliminated the transient stress at those pins. This ability is particularly useful in compact electronic devices like cell phones where the addition of an external probe could significantly modify the coupling path of the transient current. Multiple detectors with varying thresholds could be placed in parallel on a I/O pad to estimate the level of an event, though more sophisticated level sensors have been proposed to work with the event detector shown here (Patnaik *et al.*, 2017b).

The ability to detect transient stress events in the field could also allow the product designer to take defensive actions when events occur, for example by restoring the system to a known safe state or by tracking when and how many events have taken place and notifying the user of the need for product replacement. In some systems, for example an electronic power meter, such a detector could be used to warn of tamper attempts by a system intruder.

The detector developed here was kept simple to ensure minimum size, leakage current, and cost. The design should be sufficiently cost-effective to include even in inexpensive commercial ICs.

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III. TRANSIENT PEAK VOLTAGE LEVEL SENSOR

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ABSTRACT

Testing and debugging electrostatic discharge (ESD) issues in modern electronic systems can be time consuming and difficult. Measuring the current generated by an ESD event is challenging because of the number of possible locations at which a current must be measured and because the connection of probes and cables may alter the ESD current path. This paper describes the design of an integrated sensor which can be added to the I/O pads of an integrated circuit (IC), and which can measure the peak level of electrical fast transient (EFT) stress events seen at the pad. Experiments and simulations with a 90 nm product test chip show the sensor can determine the peak magnitude of the transient event within 1 A for events larger than 0.7 A and duration longer than 1 ns. The level sensors were tested using transmission line pulse (TLP) injections as well as in the field in a wearable device test. Design improvements are proposed for reducing sensitivity to process variations for small events, for allowing the readout of individual level sensors in each I/O in the presence of stress on multiple I/Os, and for reducing static power consumption. The accuracy, size, and low power-consumption of the sensor makes it well suited for application in low-cost ICs.

Keywords: Electrostatic discharge (ESD); Electrical fast transient (EFT); System level testing; On-chip measurements; Detectors.

1. INTRODUCTION

Testing and debugging electronic systems for problems with electrostatic discharge (ESD) and other transient events can be notoriously difficult. Two identical tests may give different results, with one showing a problem and the other showing the product passes, in part because many errors depend on the state of a processor when the test is performed. Determining what component or component pin is responsible for a problem can be equally challenging. While knowledge of the voltages and currents at the pins of critical components could dramatically reduce testing and debugging time, attaching probes to determine these voltage and currents can be time consuming and, more importantly, may alter the transient discharge path and thus render the test useless.

Testing and debugging could be made easier with sensors that are integrated on a die and which measure the peak transient voltage or current at individual pins of integrated circuits (ICs) within the system. Several similar sensors have previously been proposed. In (Ker *et al.*, 2008) (Thomson *et al.*, 2017) circuits are described which can detect the presence of a transient stress event from the resulting on-die power supply noise. The state of a latch is changed if there is an under-voltage or a rapid change in the power supply beyond a set threshold. Similar circuits are proposed in (Chow and Hor, 2008) (Sehgal *et al.*, 2006) to measure power supply noise which might also be used to detect a transient event. While power supply noise can indicate the presence or level of an event, noise may result from several sources, the level of noise may depend on the printed circuit board (PCB) and package design, and the pin subject to the event cannot be determined. Circuits developed in (Gerdemann *et al.*, 2007) (Jack and Rosenbaum, 2011) overcome these limitations by measuring the peak transient voltage at individual pins, but were designed only for use in the lab. A more general approach was proposed in (Kuhn *et al.*, 2014) using a diode and

fuse combination in parallel with the ESD protection diode. The fuse is blown when the event exceeds a set threshold. Although this method can effectively detect an overstress event at each I/O pad, it is not reusable. In (Patnaik *et al.*, 2018) a circuit was designed to measure the occurrence, location and polarity of a transient event at an I/O pad that exceeds a specified threshold, and provide this information to an on-die processor, but without information about the level of an event. If this circuit were modified to trigger multiple latches at different thresholds, it could be used to measure the peak magnitude of the event. However, the achievable resolution would be limited to the number of latches, and the required layout area for this implementation may be relatively large.

In this work, integrated circuits are proposed for measuring the peak transient stress voltage and current experienced at I/O pins, based on previous work (Patnaik *et al.*, 2017b). The peak transient current can be determined from the peak voltage if the I-V characteristics of the ESD protection device in the I/O pad are known. Simulations demonstrate the accuracy of the circuit across temperature and process variations. An implementation of the circuit in a 90 nm microcontroller test IC was used to validate simulation results. The impact of system-level effects like mutual inductance between pins is discussed. Improvements to the circuit for reducing the sensitivity to process variations for small events, for improving the ability to distinguish between the level of events on multiple pins, and for reducing static power consumption are also explored.

2. LEVEL SENSORS

Area efficient on-die sensors were designed which can record the peak stress voltages across the I/O ESD protection diodes in each I/O pad (Patnaik *et al.*, 2017b). These voltages represent the levels of injected current. Depending on the polarity of the injected current, the stress event is measured either with a positive level sensor (during positive current injection) or a negative level sensor (during negative current injection). The schematic for the negative level sensor is shown in Fig. 1. During a stress event with negative current

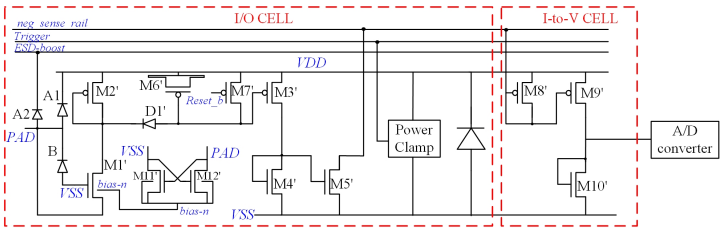

Figure 1. A typical IC ESD protection scheme showing conceptual schematics of an I/O cell with negative level sensor, the corresponding I-to-V cell, and the A/D converter. The ESD protection diodes and power clamp are also shown.

injection, the ESD protection diode B is turned on and conducts the injected current from VSS to PAD, the I/O pad. A sense NMOS M1 is connected across this ESD protection diode B. The gate of M1 is connected to VSS while the source is connected to PAD. If the voltage across the protection diode (in forward conduction) rises above an NMOS threshold voltage, M1 turns on and drives a current related to the diode voltage through PMOS M2. PMOS capacitor M6, which was initially discharged, is charged up via diode D1 to a voltage level

$$V_C = \max(V_{DS,M2} - V_{D1}) \tag{1}$$

where V_C is the voltage across capacitor M6, $V_{DS,M2}$ is the drain-to-source voltage of M2, and V_{D1} is the voltage across diode D1. This circuit is a peak detector, which stores the peak voltage of the transient event for readout after the event has passed. The voltage across the capacitor can be held for many microseconds and is only reduced by leakage current. The voltage on capacitor M6 drives a current onto the sense rail (“neg sense rail") through M3 and the current mirror stages M4 and M5. This “neg sense rail" is routed throughout the I/O ring connecting the level sensors from each I/O cell as will be shown later. The current on the sense rail is converted to a voltage at a central I-to-V cell, where it can be further converted from an analog into a digital value using an on-chip A/D converter and stored in on-chip memory. The A/D conversion may, for instance, be initiated by an Interrupt Service

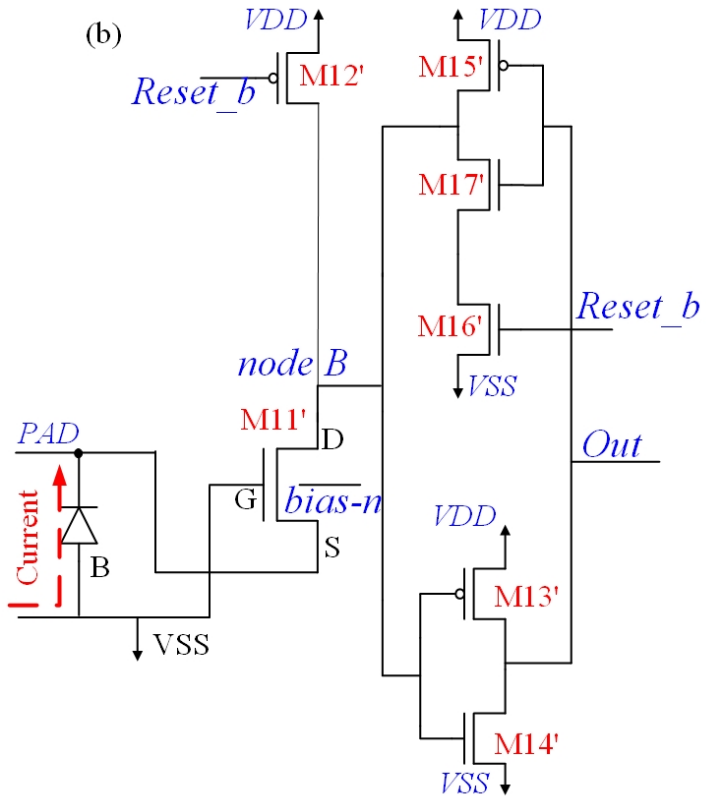

Figure 2. Negative event detector schematic with ESD diode.

Routine (ISR) which may be triggered using transient event detector circuits as discussed in (Patnaik *et al.*, 2018) (Patnaik *et al.*, 2017b). The schematic for a negative event detector is shown in Fig. 2. The negative event detector works on a similar principle as the level sensor, but instead of a diode and storage capacitor, a latch circuit is used, formed by devices M13 to M17. If diode B conducts current, it turns NMOS M11 on. This pulls the input of the latch low and flips the output of the latch from its default state. The output of the latch is routed to addressable registers within the chip core. If any latch output flips, the microcontroller triggers the ISR. Once the ISR has read the level sensors and stored the results in core registers, it resets the state of the latches and level sensors in each I/O by turning on M7 (Fig. 1) and M12, M16 (Fig. 2). M1 and M11 are implemented in an

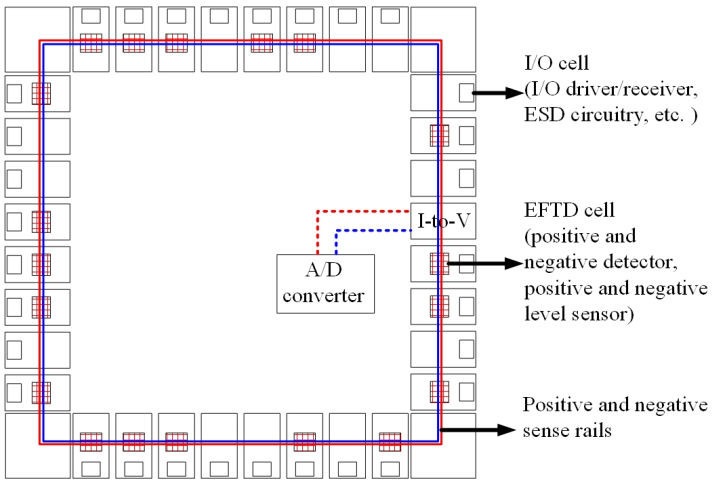

Figure 3. Placement of ESD detectors, level sensors, I-to-V converter, and the sense rails. The “pos sense rail” and “neg sense rail” are routed around the I/O ring and connected to a central I-to-V converter. The on-chip A/D converter converts the voltage to a digital value and stores it in on-chip memory.

isolated P-well where the well voltage is controlled by a well biasing circuit discussed in (Patnaik *et al.*, 2018) (Patnaik *et al.*, 2017b). This well biasing circuit drives the P-well potential to the lower of VSS or the I/O pad voltage.

The positive event detector and level sensor are designed similar to the negative detector and sensor and are not shown in this paper. The output of the positive detectors from each I/O cell are also routed to addressable registers within the core, and the current mirrors in the positive level sensors in each I/O cell are connected to a sense rail (“pos sense rail"). The negative and positive detectors and level sensors are implemented in the I/O pad ring as shown in Fig. 3.

3. SIMULATIONS

The transient level sensors were simulated in a 90 nm technology using SPICE. The block diagram for the simulation test bench is shown in Fig. 4. The test bench takes into account the power delivery network (PDN) model of the test PCB, the electrical fast transient

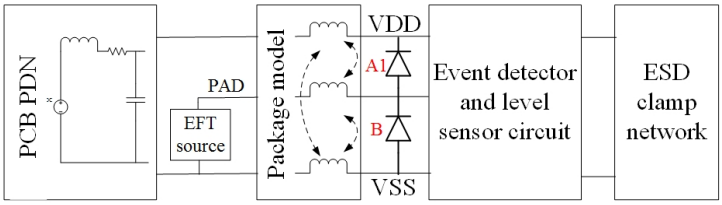

Figure 4. Block diagram of simulation model.

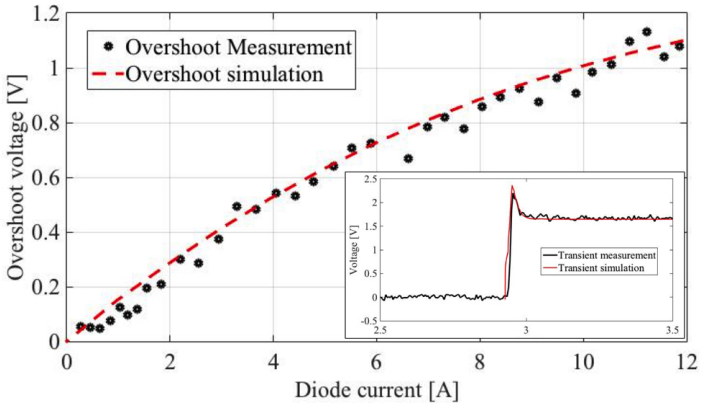

Figure 5. Comparison of measured and simulated transient overshoot voltage across the B diode during a 4 A TLP injection. The measured and simulated transient waveforms are shown in the inset. The applied TLP rise time is $\sim 200ps$.

(EFT) source model, the microcontroller package model, the ESD protection diodes, and the ESD rail protection circuits (clamp network). A 100-I/O pin package model was used. Initial simulations were performed with the level sensor circuits in just one I/O pad.

The PCB PDN impedance was measured using a network analyzer at one of the IC power pad locations, and an equivalent lumped model was derived. The equivalent lumped model was in good agreement with the measured impedance profile up to 3 GHz, the upper frequency range of typical EFT pulses. The EFT source waveform was measured using an oscilloscope. The waveform was then appropriately scaled and used directly in simulations as a source model. The package model included the self and mutual inductances, parasitic capacitances, and resistances associated with the package lead frame and bond wires. The ESD protection diodes were characterized using wafer-level TLP characterization methods

(Maloney and Khurana, 1985). The resulting SPICE ESD diode models include transient effects (self-heating and overshoot) (Stockinger and Miller, 2006). The simulated and measured overshoot voltage for the B diode as a function of the diode current is shown in Fig. 5. A simulated and measured 4 A transient event is also compared in the same figure. The ESD clamp network includes a boost bus, distributed power clamps, trigger circuits, and an on-die I/O power delivery network as described in (Stockinger *et al.*, 2013) (Ruth *et al.*, 2011) (Stockinger *et al.*, 2003). The rail clamps are designed for proportional triggering rather than strictly being "on" or "off", so that a collapsing power supply voltage can be prevented during a transient event (Stockinger *et al.*, 2013). The power clamp model accounts for a snapback mode of the clamp MOSFET during strong ESD events.

Simulations were performed with a TLP-type EFT source between the I/O pad and circuit board VSS, as indicated in Fig. 4. The circuit response for a 20 ns, 5 A negative stress event is illustrated in Fig. 6. The figure shows (a) the injected current through the B diode, (b) the voltage across the storage capacitor M6, the difference between VDD and VC, and (c) the local power supply fluctuations (difference between VDD and VSS) during the transient event. The circuit was initialized with a reset pulse at t=10 ns. The reset pulse resets the state of the latch and removes any residual charge across the capacitor. As a consequence of the rising edge of the reset pulse, some charge is injected into the capacitor and results in a small negative pre-charge voltage across the capacitor as shown in Fig. 6. Similar simulations were performed with a human metal model (HMM) type source between the I/O pad and circuit board VSS. Simulation results are also shown in Fig. 6. The circuit accurately captures and stores the peak voltage across the ESD protection diode even for the fast peak associated with an HMM event. The stored level is not impacted by variations in the power supply voltage during the event and can be maintained for milliseconds or longer without appreciable change.

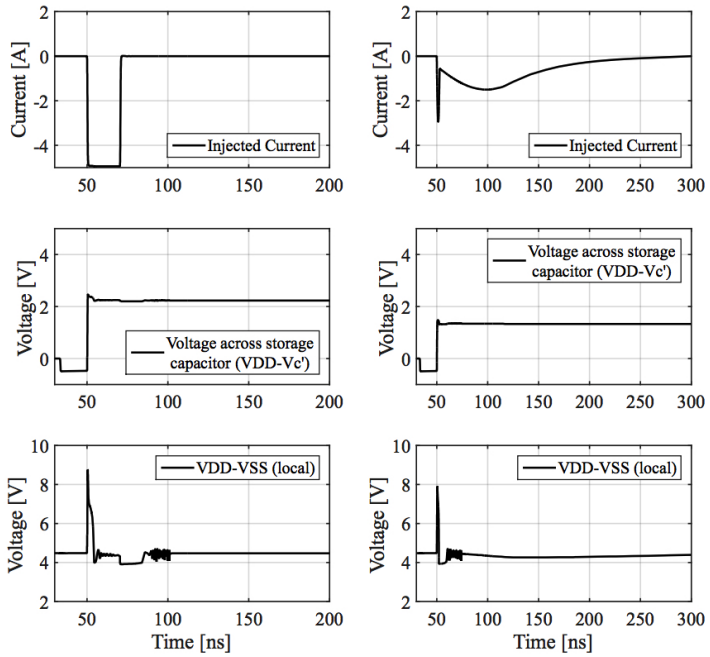

Figure 6. Simulated transient response during a negative 5 A TLP event (left side) and a negative 2 kV HMM event (right side).

Additional simulations were performed to determine the minimum current and minimum pulse width necessary for a reliable level sensor readout. Simulations with short EFT pulses showed the sensor was able to reliably measure the peak level of current pulses as low as 0.7 A with pulse widths of 1 ns and higher (Patnaik *et al.*, 2017b). For peak currents lower than 0.7 A, the pulse width for reliable detection was several tens on nano-seconds.

Simulations were also performed for evaluating the sensor's sensitivity to process variations. Corner cases were considered for PMOS, NMOS, diodes and resistors. Process corners for the ESD diode were not available. The simulated voltage levels at the A/D converter for stress events caused by 40 ns TLP pulses (negative injection) with different peaks and different process corners are shown in Fig. 7. The simulation shows the peak current can be measured with approximately ±0.5 A accuracy across process corners. Better accuracy could be achieved by performing a calibration measurement of the level sensor before first use.

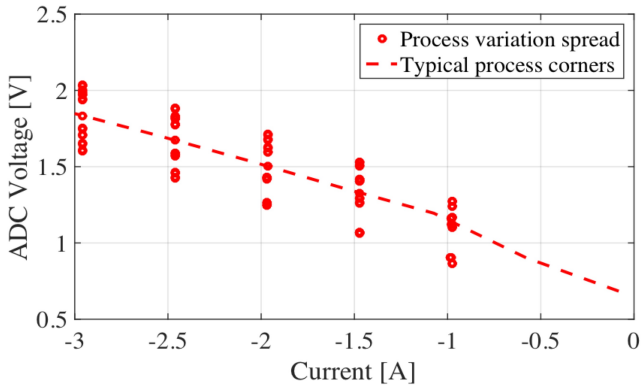

Figure 7. Voltage at A/D converter as a function of the peak ESD diode current for different process corners.

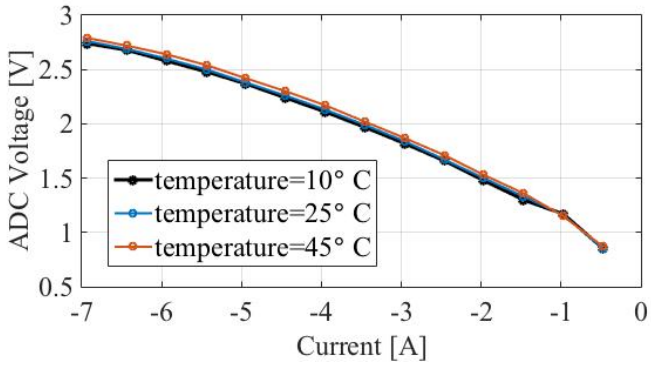

Figure 8. Voltage at A/D converter as a function of the peak ESD diode current for different operating temperatures.

Fig. 8 shows the simulated transfer curves for the negative level sensor for different temperatures. Curves were generated at 10°C, 25°C, and 45°C. The variation in output with temperature is less than 5% of the expected value. Process variations have a much greater impact on the sensor accuracy. It should be noted, however, that these results do not take into account the impact of temperature or process corners of the ESD diode, which was not available.

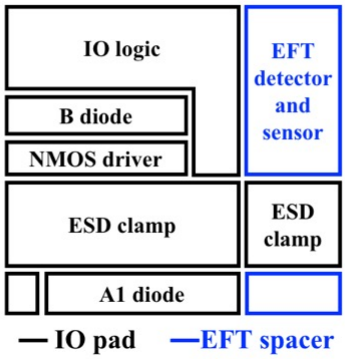

Figure 9. I/O floor plan with abutted EFT spacer cell.

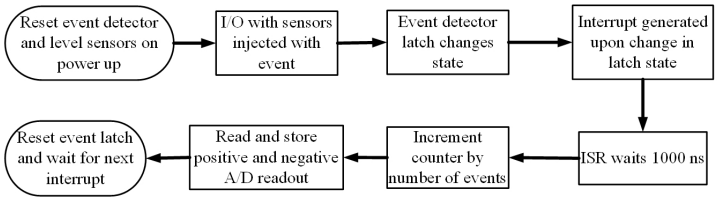

Figure 10. Functional flow diagram to read the level sensor values.

4. IMPLEMENTATION AND TESTING

The level sensors were implemented in a microcontroller test chip using 90 nm technology. The positive and negative level sensors and detectors were implemented in a spacer cell and attached to 72 of the 100 microcontroller I/O pads. A conceptual layout of the spacer cell and I/O pad is shown in Fig. 9. The level sensors and detectors add about 27% to the area of the I/O cell. While the circuit was generally designed for a small area footprint, layout optimization of the spacer cell was not a high priority for the test chip. With additional effort, the area of the spacer cell could be reduced.

The level sensors were tested using the procedure shown in Fig. 10. At power up, the event detectors and level sensors are reset. An EFT source is used to inject a transient current at an I/O pin on the test board. If the event detectors detect a transient event, an interrupt is generated. The ISR waits 1000 ns before reading the level sensor. The delay

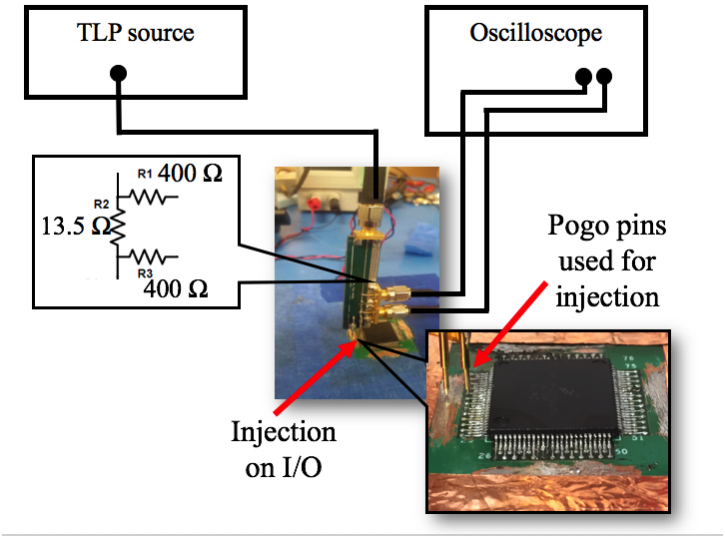

Figure 11. Test setup for characterizing level sensors using TLP injection.

ensures that any power supply fluctuation caused by the event has stabilized. After 1000 ns, an event counter is incremented, the A/D converter is read, and a register is read indicating which event detectors were triggered. After reading the A/D converter and the detector register, the level sensors and latches are reset to be ready for the next stress event.

During a stress event with positive current injection, the ground potential right at the injected pin can temporarily rise above the potential elsewhere on the die. Similarly, during a negative stress event, the local ground potential can drop. This is due to a voltage drop along the ESD path through a resistive supply grid. If the reset circuitry were designed poorly, this change in local ground potential could cause reset signal integrity issues and unintended resetting of the level sensors during a stress event. This was taken into account when deciding whether to use the direct or inverted reset signal at various points in the circuits.

4.1. Characterization of Individual Level Sensors. The level sensors were first characterized with a direct single pin injection method before performing full system-level tests. The injection probe is shown in Fig. 11. Spring loaded pogo pins were used to

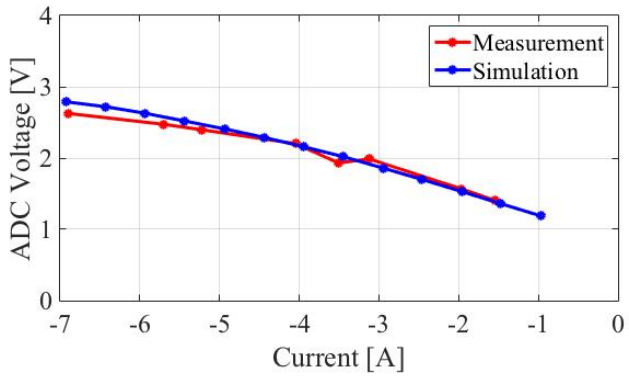

Figure 12. Measured and simulated voltage at the A/D converter for the negative level sensor as a function of the injected current.

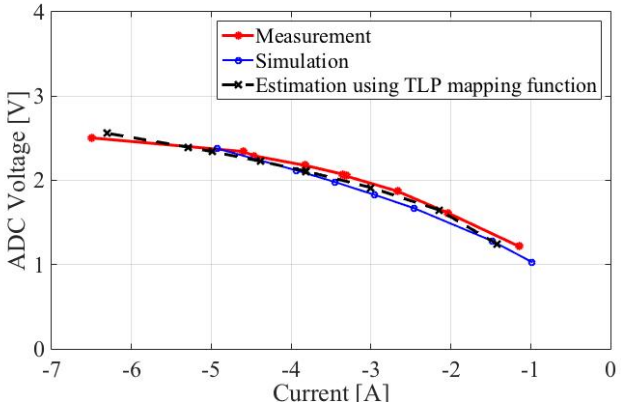

Figure 13. Comparison of measured and simulated A/D voltage as a function of injected current for negative HMM events.

make electric contact to an I/O pin and to exposed VSS metal on the board. TLP stress was applied to the I/O pin and the injected current was calculated using measurements of the voltage across a known resistor (13.5-ohm) embedded into the probe. The probe's resistive Pi-network was designed to minimize signal reflections due to line impedance mismatches. An external computer was used to read the output of the A/D converter from on-chip memory. Fig. 12 shows a comparison of the measured and simulated A/D voltages

as a function of the peak injected current for a negative stress event. In this case, using the simulated values with typical process conditions as a calibration curve would predict measurement results within 1 A.

The level sensors were also tested with HMM type injections using the setup shown in Fig. 13. The HMM type waveform was generated using a high-voltage source and a wave shaper device instead of the TLP source. The injected current waveform is similar to the HMM waveform of Fig. 6. The voltage returned from the A/D converter was used along with the calibration curves in Fig. 12 to estimate the peak stress level at the I/O pin. The estimated current was compared to the measured current as well as to the simulated values. A comparison of the estimated, measured and simulated curves are shown in Fig. 13. The red curve labeled 'Measurement' was generated using the true current measured with the pogo pin probe. The black curve labeled 'Estimation using TLP mapping function' was generated by estimating the current from the A/D voltage reading using TLP calibration curves (see Fig. 12). The peak current could be determined within about 0.2 A of the measured value using the simulated curve and within 0.4 A using the TLP calibration curve.

The accuracy of the level sensor reading also depends on the ability of the capacitor to reliably store a charge until it is read by the A/D converter. An experiment was performed where the capacitor voltage was read continuously for one second starting one microsecond after a negative injection. The capacitor was shown to discharge at a linear rate of about 2 mV/ms at room temperature. Given other variations between measurements and simulations, the negative level sensor should be able to be read milliseconds after an event with minimal impact on accuracy.

4.1.1. Impact of Mutual Inductance. Mutual inductive coupling between bondwires can couple transient events between nearby pins (Patnaik *et al.*, 2018). A positive injection on one I/O pin may induce a current in the opposite direction on adjacent I/O pins. The induced current can have a high magnitude if there is a low impedance return path on the pin, for example a direct short or a capacitive connection from the I/O pin to VSS on the

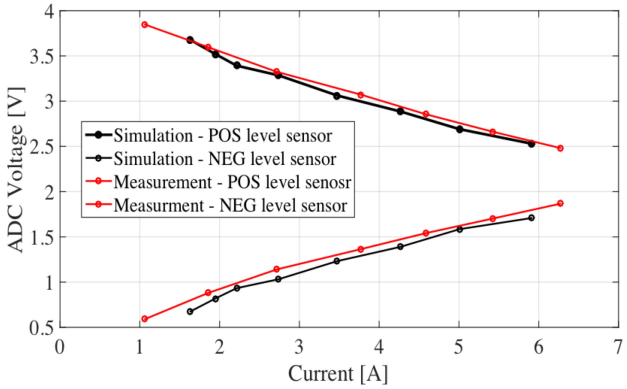

Figure 14. Comparison of measured and simulated transfer curves as a function of peak injected current. A positive injection was performed on I/O pin 1 and both positive and negative level sensor readings were observed due to mutual inductive coupling between the bond-wires and package pins.

PCB. The capacitance between a board trace and a VDD or VSS plane, for example, can be large enough to provide such a low impedance path. Fig. 14 shows the measured and simulated positive and negative sensor readouts with a positive injection on one I/O pin. The parasitic readout on the negative level sensor was captured in simulations within 1 A of the measured values.

The parasitic reading on the negative level sensor may be due to the coupling to a single neighboring I/O pin or to multiple adjacent I/O's, as all level sensors contribute current to the shared sense rail. The problems associated with the shared sense rail is discussed in greater detail in a later section.

4.1.2. Impact of Rise Time. The level sensors were tested to demonstrate the impact of event rise times on the measured reading. Tested rise times ranged from 400 ps to 20 ns for a 40 ns wide TLP pulse. The rise times were varied by adding filters between the TLP and the injection probe. As shown in Fig. 15, the measured negative level sensor reading is higher for a 400 ps rise-time pulse than for a filtered pulse with a rise time of 2 ns or more. Careful analysis through simulation showed that, during a fast rising pulse, the drain-to-source voltage $V_{DS,M1}$ of M1 in Fig. 1 can go high enough to

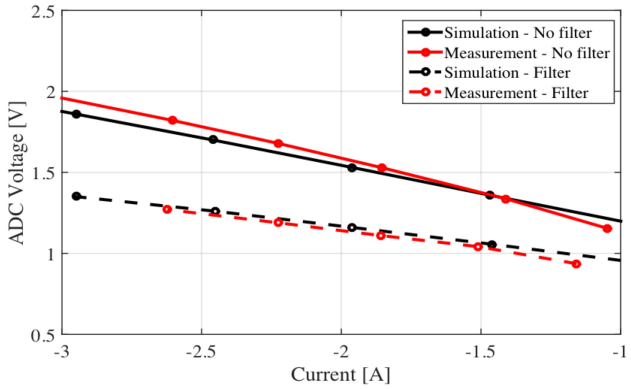

Figure 15. The impact of rise time on the negative level sensor reading. The unfiltered rise time was around 400 ps. The filtered rise times varied from 2 ns to 20 ns but produced the same reading.

turn on the parasitic lateral bipolar junction transistor (BJT) of the MOSFET ("snapback" of M1). The large current driven by M1 while in snapback mode is reflected in a larger voltage at the A/D converter. The higher sensor reading may be further affected by a slow response of the body-biasing circuit (Patnaik *et al.*, 2018). If the body potential of M1 were allowed to rise above its source potential, the threshold voltage of M1 would drop. This would allow more MOSFET channel current to flow. It would also make M1 more susceptible to snapback because its parasitic BJT would already be partially turned on due to the raised body potential. Simulations with an approximate snapback model of M1 were able to capture these effects.

4.2. System Level Testing. The level sensors were also evaluated in a system level environment where the test microcontroller was used in a simple experiment to determine the number and level of ESD events experienced by a wearable electronic device (Patnaik *et al.*, 2017a). The use of the on-die ESD detectors and sensors allowed the measurements to be performed without the use of additional equipment. The microcontroller was housed in a shielded enclosure and chosen I/O pins were connected to cables penetrating the enclosure. The cables were attached to electrodes at different locations on a human test subject. The

subject was charged to a high voltage, for example from a high-voltage source, by removing a sweater, or other actions, and then the subject was discharged through the electrodes during near-contact to a large metal plane. When a transient discharge event occurs, energy is coupled onto the cables and triggers the detectors and level sensors. The rise-time and peak current levels may be much larger than during a typical human-metal-model event because wearable electronics are more likely to experience a "brush-by" event. The detectors and level sensors accurately detected and sensed the peak discharge currents coupled onto the cables. The accuracy of the measurements was verified with an inductive current probe ("current clamp") placed on the cables. The system was also able to measure discharges occurring during everyday lab activity. Other tests included sensing peak transient currents of a cable discharge event when plugging a charged cable into a connector accessing an I/O pin of the microcontroller. These system level tests demonstrate the ability of the sensors to work well in a realistic system deployed in the field.

5. DESIGN IMPROVEMENT

While the level sensor proposed here works well, there is room for improvement. Under ideal conditions, the current mirror stages in the circuit in Fig. 1 are well matched and voltage at the A/D converter input would have minimum variation due to process variations in the circuit. The diode D1, however, introduces an "imperfection" to this method because it causes a voltage offset in the current mirror stage M2/M3. Another potential problem with the original design is that multiple level sensors can generate sense currents on a sense rail at the same time. If more than one sensor drives a current to the shared sense bus, the A/D reports the voltage created by the sum of the individual sensor currents. This does not allow one to distinguish individual sensor current levels. A third potential issue with the scheme in Fig. 1 is that no effort was made to limit leakage current when the sensor is in the "OFF" state. These issues have been addressed in a modified design shown in Fig. 16.

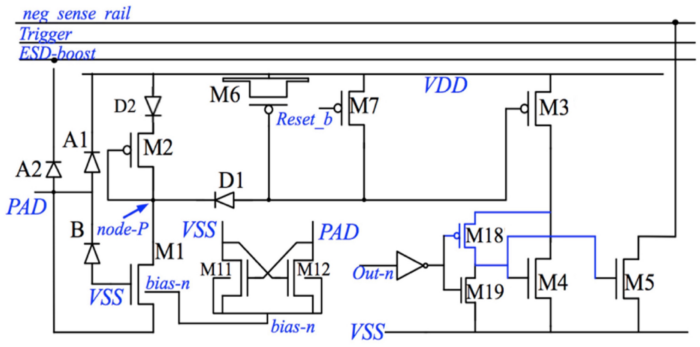

Figure 16. Alternate sensor design with improved DC current control and reduced process variation.

The most significant design modification between the circuit in Fig. 1 and Fig. 16 is the addition of the diode D2 at the source of PMOS M2. In the original circuit, the gate-to-source voltage of M3 is given by the peak gate-to-source voltage across M2 minus the voltage drop across diode D1:

$$V_{GS,M3} = V_{GS,M2} - V_{D1} \tag{2}$$

where, $V_{GS,M3}$ is the gate-to-source voltage at M3, and $V_{GS,M2}$ is the gate-to-source voltage at M2. The voltage across PMOS M2 should be greater than a diode voltage drop in order to drive current on the sense bus. The addition of diode D2 adds a diode voltage drop to correct this relationship, as

$$V_{GS,M3} = V_{GS,M2} - V_{D1} + V_{D2} \tag{3}$$

where, V_{D2} is the voltage drop across D2.

For ideal diodes, $V_{D1} = V_{D2}$ so that $V_{GS,M3} = V_{GS,M2}$. In this case, the drain current through M2 and M3 would be matched assuming ideal current mirrors throughout the circuit as mentioned earlier, and this matching would minimize process variations. In

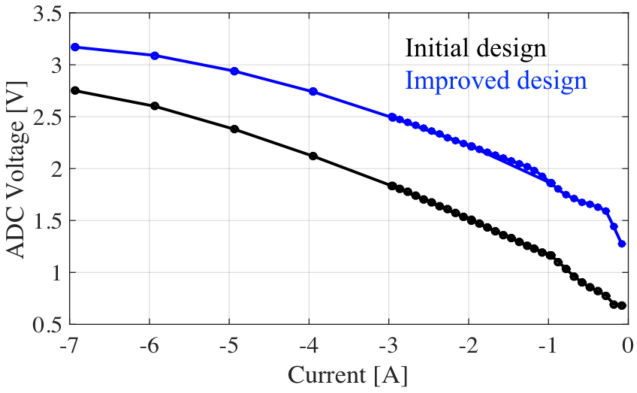

Figure 17. Comparison of output voltage as a function of voltage across ESD protection diode for the initial design shown in Fig. 1 and the improved design in Fig. 16.

reality, however, the currents through D1 and D2 differ and the voltage drops across these diodes are not precisely equal. The current through D1 at the peak of the stress event is approximately zero, while the current through D2 is equal to the drain current through M1. To minimize this unwanted mismatch, the sizes of D1 and D2 were optimized in simulations to maximize the matching of the drain currents through M2 and M3 across the operating range of the sensor. To have a fair comparison between the original and the new circuit, the slope of the transfer curve (A/D input voltage vs injected current) for the new circuit was optimized to be approximately the same as the original circuit as shown in Fig. 17. Both circuits are sensitive to pulse width at low current levels, since the capacitor M6 may not fully discharge. The impact of process variation at room temperature is demonstrated in Fig. 18. Simulations were performed for the corner cases of the PMOS, NMOS, diodes and resistors. Sixteen possible combinations of corner cases were tested. Complete ESD diode models were not available, so simulations were performed with the typical ESD diode case. Compared to the original circuit (Fig. 7), the variation in the predicted input current for a given output reading is reduced by 50% at injection levels around -1 A for the new circuit. The circuits performed roughly the same at higher injection levels.

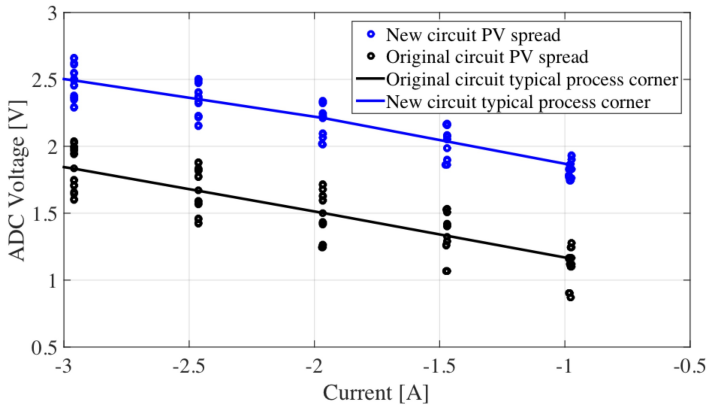

Figure 18. . Comparison of original and new circuit showing simulated voltage at A/D converter as a function of peak ESD diode current for all process corners.

Problems with determining the injected current level on an individual I/O pin may occur when multiple sensors are triggered at the same time, since each sensor will drive a certain current onto the shared sense bus. The impact of multiple sensors driving the sense bus is illustrated in Fig. 19. Depending on the number of active sensors, an A/D reading of 3 V, for example, could be associated with a 10 A event on a single I/O pin, a 6 A event on two I/O, a 4.5 A event on three I/O, or some combination of different levels on multiple I/Os. Adding a control signal "Out-n" and control circuitry (M18 and an inverter) as shown in Fig. 16, allows the microcontroller to select which level sensor can drive current onto the shared sense bus, and therefore allows sensor levels to be read out selectively. Such a control signal could be provided separately to each I/O pin or using a scan-chain to reduce area requirements, so that levels could be read one at a time in a sequential manner, similar to a JTAG boundary scan.

The control circuitry provided by the signal "Out-n", M18, and the associated inverter can also be used to reduce the unintended current consumed by the level sensor. The original circuit in Fig. 1 draws current after an event is sensed and may draw non-negligible leakage current through M5 since the gate-to-source voltage of M4 may be close to a threshold voltage even if M3 is "OFF". The leakage may be even worse if the voltage

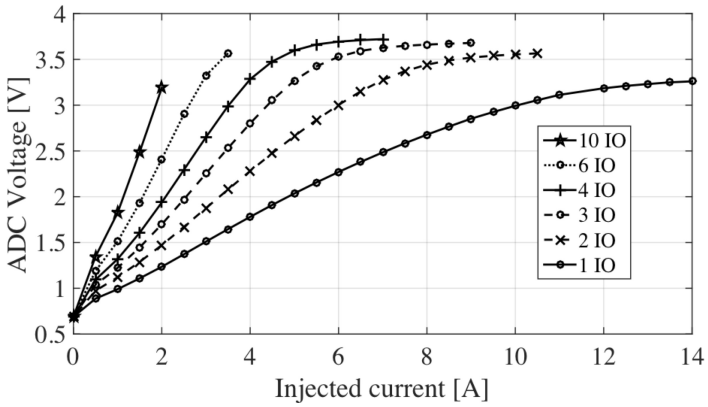

Figure 19. A/D converter voltage as a function of the injected current when the injected current is seen by multiple level sensors.

across M6 were allowed to drift above a PMOS threshold voltage. By providing control circuitry, the level sensor can be set to only drive current onto the sense rail when the microcontroller wants to read the level sensor.

6. DISCUSSION AND CONCLUSIONS

On-die sensors were developed which can reliably determine the peak of transient events with a ±0.5 A accuracy across process and temperature variations for events greater than 0.7 A and a pulse width of at least 1 ns. Measurements on a product test chip showed that currents were detected on multiple pins, not only the pin which received the stress. Simulations with the full package model showed this result is due to mutual inductance between nearby pins and confirmed that the reading was correct. These simulations also demonstrated that accurate models of the power bus and traces on the PCB were needed to obtain accurate results. Snapback in the sensor was observed for fast rise time events. The snapback could be eliminated by adding a small protection resistor between M1 and M2, but this result emphasizes the importance of using MOSFET models which capture their snapback characteristics. The sensors were tested in system level applications and performed

well. An alternative design was proposed which improves the performance across process corners at low injection levels, reduces leakage current, and adds the capability to read level sensors one at a time.

The proposed sensors allow the test engineer to measure the peak level of transient events at the I/O pins without the addition of external equipment, by embedding the measurement capability in the IC itself. This capability can substantially improve product testing effectiveness, test time, and the ability to debug transient immunity problems. This circuit also gives the engineer the opportunity to collect information about transient stress events in the field. The microcontroller could use knowledge of the presence and level of a transient event to trigger a software response designed to minimize the impact of soft failures. Data collected about transient stress events could be used to show the rate and level of events or to better understand the cause of failures experienced in the field.

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IV. CHARACTERIZING ESD STRESS CURRENTS IN HUMAN WEARABLE DEVICES

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ABSTRACT

Currents induced on an I/O of a human wearable device IC are predicted using a test IC as a wearable device capable of transient event detection and level sensing. ESD on this pseudo wearable device using the test IC is characterized for different test scenarios and compared to the prediction.

Keywords: Electrostatic Discharge (ESD), Electrically Fast Transient (EFT), Sensors, Wearable device, Testing.

1. INTRODUCTION

Wearable electronics are becoming ubiquitous. Smart phones, watches and glasses located on the human body experience severe stress events due to ESD. These ESD events can be quite complicated and the range of events that the wearable device must be immune to or how to adequately test them is poorly understood. IEC-61000-4-2 (Standard, 2007), for example, specifies that the device under test (DUT) is subjected to ESD when it is

placed on an insulated surface above a ground plane. This setup does not accurately represent conditions seen by human wearable technology as the wearable device (DUT) is now mounted on the charged human body.

Previous studies have investigated the maximum possible potential and currents that body worn equipment may experience under certain test situations, though experimental characterization of ESD to wearable electronics is still lacking. The authors in (Yoshida, 2015) measured the voltage waveforms induced on a human worn device. The study concluded that the electrical stress induced by the ESD event on a wearable device depends on the circuit structure and its impedance. An extensive study of the characteristics and generation of long ESD pulses to wearable electronics was studied in (Yoshida, 2016). Both the device and its wearer were charged together, or the device was kept within a certain proximity of the discharge event. This study helped show the test conditions which might cause a long discharge current. A long discharge is more likely to cause thermal damage to an IC than a short discharge of the same magnitude. Another study (Ishida *et al.*, 2015) investigated the worst case discharge current that would occur when a human worn device approaches a grounded conductor. The authors measured the currents through a hand-held metal probe or a semi-spherical metal device attached to the human at different locations. The hand-held metal probe or the semi-spherical device were considered as replicants of the charged wearable device. The peak current through the worn semi-spherical device depended on its location on the body and was higher than the current experienced by the hand-held probe. The event duration also depended on the type of discharge performed. Although these studies give an idea of the intensity and shape of the ESD current that might be experienced by wearable electronics, there are no measurements of the actual transient disturbance experienced by the electronics inside the wearable device.

This article studies the current levels an IC in a wearable electronic device must withstand. This is done by monitoring the discharge current through an I/O pin of an IC in a wearable device which is mounted on a human.

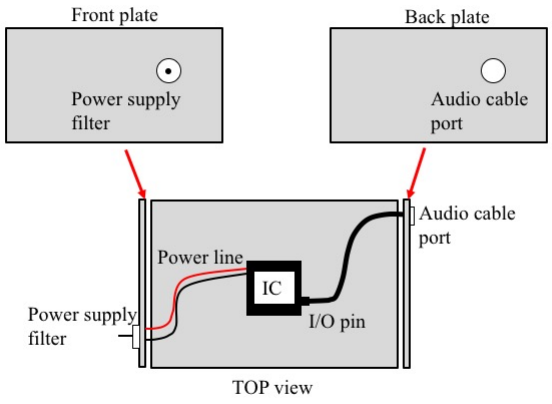

Figure 1. Test IC housed in a metal shielding box - pseudo wearable device.

2. WEARABLE DEVICE UNDER TEST

A metal enclosure containing a single IC was used as a replicate of a wearable electronic device. This particular IC has added circuity with the capability to detect the occurrence and peak levels of transient events it is exposed to, so long as the event is above a certain threshold (~ 1 A). Separate characterization of the test IC has shown successful detection for both positive and negative events as well as repeatable detection of the level of the event. The design and characterization of the test IC is described by the authors in separate articles (Patnaik *et al.*, 2017b) (Patnaik *et al.*, 2018) (Patnaik *et al.*, 2017a). The IC will provide the number of transient overstress or understress events experienced by the IC and level of each event upon query from the user.

The test IC is housed in a well shielded box and is battery powered. The enclosure prevents any direct coupling to the pins of the IC. The power line from the battery pack is filtered before entering the shielded box. The only other port defined from within the box to the outside environment is through an audio jack to which external headphones can be

connected. Inside the box the audio jack is connected to a single I/O pin of the test IC as shown in Fig. 1, and constitutes the device test port. This box can be considered equivalent to a wearable device, which may be worn by a human during ESD level testing.

The IEC standard for ESD testing subjects devices to a different test case than is typically experienced by a human worn device. The ESD events experienced by a human worn device are closer to a "brush-by" case where the discharge currents are significantly higher than those seen in the human-metal discharge case, since the device itself can provide a lower-impedance discharge path than can be provided by a hand-held conductor.

3. TEST SCENARIOS

The currents induced in the I/O of the wearable DUT are characterized under different test scenarios. The test scenarios are grouped based on the different discharge situations that a wearable device may be subjected to. The different groups are: A. Brush-by contact discharge. B. Cable plugin to user interface of device. C. Daily activity in a laboratory environment.

A Brush-by contact discharge represents the scenario where the wearable device is on the human while the human charges up and discharges through different locations of the body. It is necessary to have the cable close to the discharge point so that part of the discharge current is coupled through the cable to the I/O of the DUT. The cable in this scenario is associated with headphones which are often connected to a smartphone or portable audio player.

Cable plug into an user interface like an audio, USB, power or other interface cables represents a cable discharge event (CDE). Cables can easily accumulate charge by being dragged on the floor or over another surface and through other handling situations. This triboelectric charging results in charge accumulating on the inner signal wires. When this cable is subsequently plugged into a user interface there is a discharge path based on the lowest inductance path. This scenario is replicated by plugging in an intentionally charged

cable into a user interface connected to the I/O of the IC. This arrangement can estimate the currents the I/O of a wearable device can experience for a CDE. This is a complete non-intrusive method to estimate the currents in a fully functional system where no additional hardware is added to monitor the stress levels.

The final scenario for evaluating the currents induced on a wearable device is to have a test subject perform daily activities while wearing the DUT. In this test case, the human body along with the DUT charges up while walking on the carpet flooring. The discharge occurs when the human comes in contact with metal planes or objects such as door knobs, metal doors, etc.

3.1. Brush-by-Contact Discharge.

3.1.1. Test Setup. The test setup showing the human wearing the DUT, the high voltage (HV) charging source, the discharge plane, and the shielded measurement setup is illustrated in Fig. 2. A headphone is connected to the audio jack on the DUT and is wrapped along the human arm. When the human charges up to a certain potential, the DUT potential rises along with the potential of the host human body. During the discharge to a grounded conductor, the audio cable provides a low impedance conduction path forcing the current through the I/O pin of the IC. This current is measured using a current clamp and an oscilloscope. The IC in the DUT observes the same current and records this value, which is later read out by the user.

To simulate the "brush-by" ESD case, the discharge was performed through a body-mounted semi-sphere metal probe held at different locations on the human body. Tested locations included: a) Hand held metal rod b) Wrist mounted c) Arm mounted d) Waist mounted as these are the most common locations of discharge to a grounded conductor by a "brush-by" action. The test cases study events that might occur on a daily basis as a person performs typical activities like walking or standing up from a chair. For each test case, the headphones are routed close to the discharge location so as to carry most of the current. Fig.

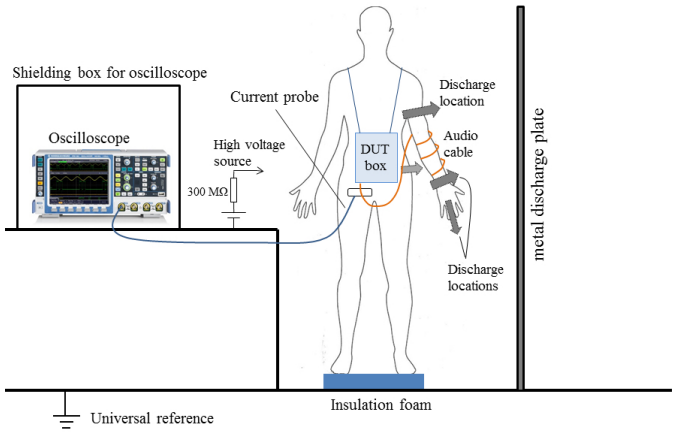

Figure 2. Test setup for characterizing ESD to wearable electronics under different discharge cases.

3 shows the mounting of the discharge sphere and the hand-held metal rod for the test cases studied in this article. The routing of the audio cable is shown for the hand-held discharge case.

3.1.2. Test Procedure and Results. For testing, the human in Fig. 2 first charges himself by touching the high voltage electrode momentarily and lets go of the electrode while simultaneously discharging into the vertical ground plane through the metal semi-sphere or the hand-held metal probe. The peak current during this discharge is recorded through the audio cable using a FCC-F-65 current clamp. This induced current is measured using an oscilloscope and is then corrected with the transfer impedance of the probe to obtain the current on the wire connected to the I/O of the IC. The transient waveforms for the current on the audio cable for a 3 kV charge is demonstrated in Fig. 4 for different discharge locations on the human body. Each of the current waveforms was produced with the same charge setting of the high voltage source. At the same setting, the maximum

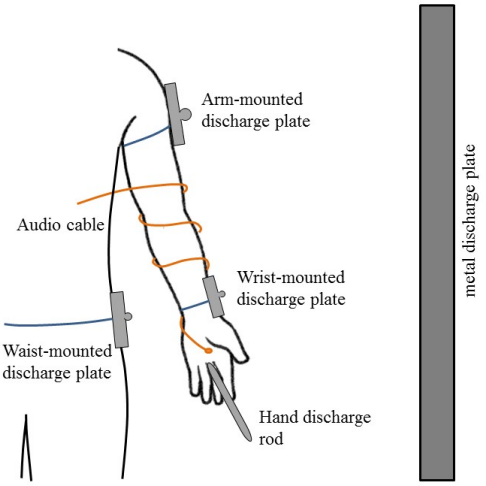

Figure 3. Discharge locations showing the metal sphere and hand-held metal rod.

discharge current through the arm is larger than the maximum discharge current through the hand-held metal probe. The current induced on the audio cable is lower than the discharge current through the body connected metal electrode and grounded conductor.

The repeatability of the shape and amplitude of the discharge currents were verified by observing these parameters on the oscilloscope over many discharge events. Once the repeatability was established, the magnitude of the events was read from the IC in the DUT using an external computer. Upon query, the DUT successfully detected and recorded the transient event. The IC is capable of reporting the magnitude as well as the polarity of the transient event. The DUT correctly detects the transient disturbance on the pin to which the wire of the audio cable was connected. When there is a positive and negative swing in the current (Fig. 4) beyond the threshold, the DUT reported back both positive and negative event detection on the correct I/O. The voltage value received from the DUT is plotted against the measured current through the single wire of the audio cable. These results are shown in Fig. 5.

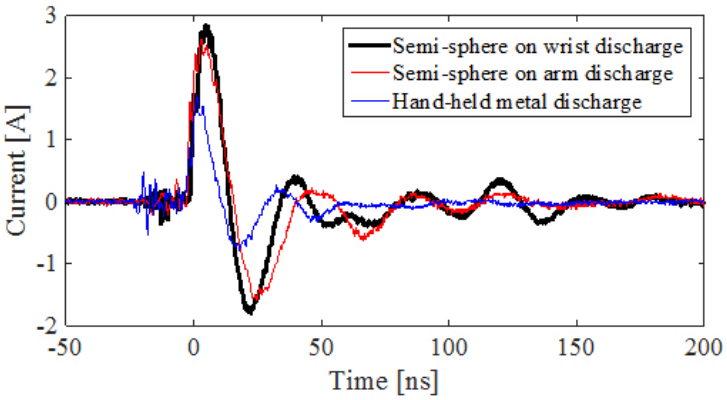

Figure 4. Transient current waveforms induced on the audio cable under different discharge scenarios.

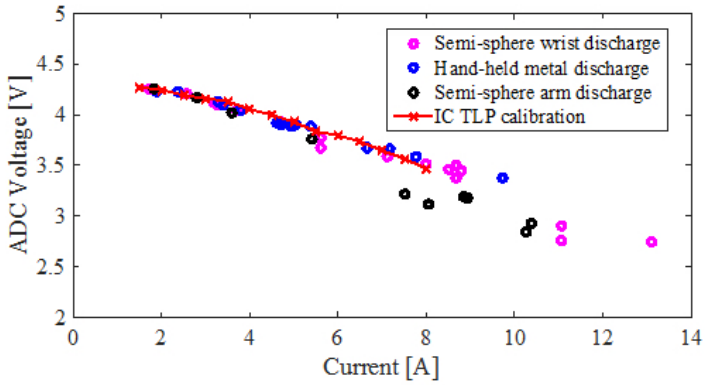

Figure 5. Comparison of current on audio cable as measured by oscilloscope and by test IC.

The red curve in Fig. 5 shows a calibration transfer curve that gives the relationship between the injected current and the voltage read from the internal transient level sensor. This curve was obtained by injecting a 30 ns TLP pulse into the I/O pin while monitoring the voltage readout from the IC (Patnaik *et al.*, 2017a). The voltage and current readouts for different test cases are plotted on Fig. 5 as well.

The ability of the test IC to accurately predict the peak current of the transient event is demonstrated in the figure. The voltage readout from the IC is used along with the IC TLP calibration curve to back calculate the current the I/O of the IC experienced.

This estimation of the current using the TLP characterization curve correlates well with the measured currents using the current clamp as shown in the figure. The maximum error between the measured (current clamp method) and estimated (using voltage readout and TLP calibration curve) transient level current was less than 0.5 A. In a scenario where the user has a wearable device mounted and experiences an ESD event, the test IC will record the voltage proportional to the current flowing in the I/O. A test performed with the human charged at 3 kV who discharges through his arm (here through the semi-sphere mounted on his arm), the IC reported a voltage of 4.2 V. Now using the calibration curve of the IC, it was predicted that the ESD event caused 2.5 A of current through the I/O. This correlates well with the current observed earlier using the current clamp on the audio cable (Fig. 4). For all the test cases, the trend between the current and voltage readouts follow the calibration curve well up to 9 A of peak current.

For a 5 kV charge, the voltage readout from the DUT for a hand-held discharge will be higher than the voltage readout for an arm mount or a wrist mount discharge. This is due to the fact that the discharge current is lowest for the hand-held discharge case. A lower discharge current induces lower currents on the audio cable which results in a higher voltage readout from the IC. The current clamp measurements showed that the currents induced in the audio cable followed the expected trend. The voltage readout from the IC used along with the calibration curve supported this measurement.

3.2. Cable Plug into User Interface of Device.

3.2.1. Test Setup. Wearable devices frequently come into contact with the user especially through user interfaces. This includes headphone jacks, USB interfaces, data cards, etc. A charged cable being plugged into a device is a classical representation of a CDE. An alternate situation could be the DUT is charged up and is plugged into a cable. In this article, a CDE where the cable is charged and plugged into the DUT has been demonstrated. The test setup is shown in Fig. 6. The test is performed with an audio cable which has a twisted pair configuration.

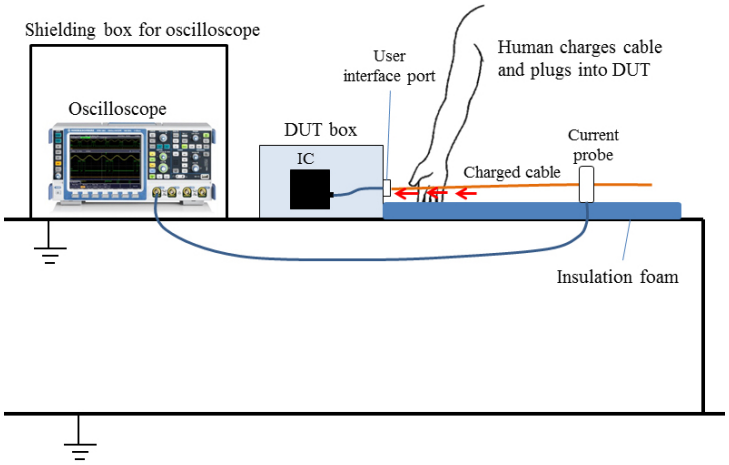

Figure 6. Test setup for cable plugin test.

3.2.2. Test Procedure and Results. The test procedure is similar to earlier test cases. The human stands over an insulating surface and charges the cable with himself by holding a HV charging source simultaneously. For discharging, the HV source is let go and the cable is plugged into the DUT immediately. This was performed at different HV source settings for different layout arrangement of the audio cable on the insulation foam. Once the cable is plugged in, the data of the recorded events from the DUT is retrieved. The DUT successfully detected the I/O location as well as returned a voltage value which is then used with the TLP calibration curve to estimate the current. This is demonstrated in Fig. 7. Initial tests were performed with a current clamp on the audio cable which was compared with the estimated current peak value using the voltage value returned from the DUT. When the DUT returned 4.1 V, the estimated current from the calibration curve is 3.2 A while the current measured using the current clamp is 3.6 A. The current clamp is removed after validation for a few discharge events. This test was repeated with different head phone cables and showed similar results. This scenario can be extended to different type of cable-connector interfaces. When using USB cables for plugin tests, the shield quality along with termination of the cable determined the currents induced in the

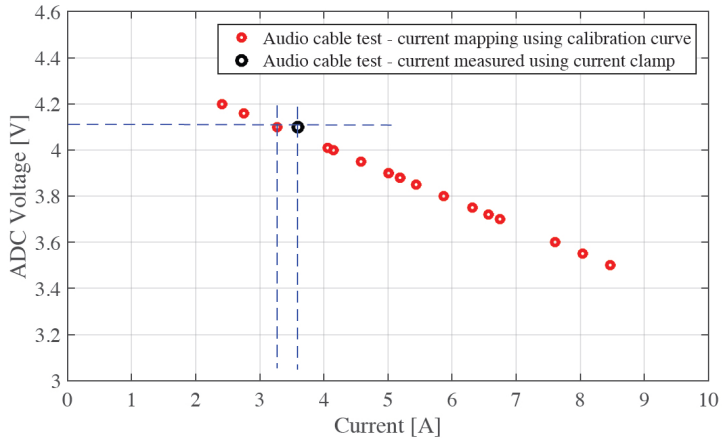

Figure 7. Estimation of current using the ADC voltage and TLP calibration curve for cable plug in tests.

inner wire and the I/O. This is being investigated in a different study. This test setup can therefore non-intrusively measure the peak currents which an I/O of a wearable device may experience during CDE.

3.3. Daily Activity in a Laboratory Environment. This test deals with the daily activities a human may perform while wearing a wearable electronic device. The audio cable was connected to the I/O throughout the tests. In this test case the charging of the human and the DUT was not controlled. In the previous test cases a HV source was used to charge the human or the human along with the cable. Here the charging of the human/DUT is solely based on activities such as walking on a carpet floor, sitting down and standing up from a chair, and getting in and out of a car. Because the DUT is battery powered and compact, the human being could move around performing his daily activities, during which he randomly discharges through the wearable device.

The data from the DUT is measured at regular intervals. Fig. 8 shows the results after mapping the voltage readout from the DUT with the TLP calibration curve. The correct I/O is identified by the DUT. For some readouts there is only a positive or negative detector flagged, which indicates that the discharge current was either a unidirectional current or the

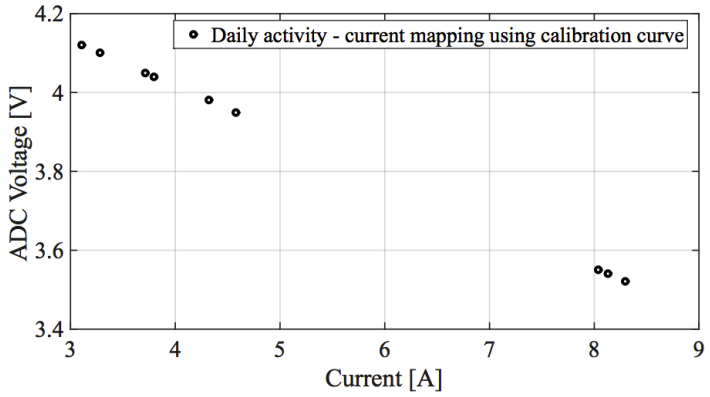

Figure 8. Estimation of current using the ADC voltage and TLP calibration curve for daily activity tests.

peak was less than the negative or positive detector thresholds. This is valuable information which is now possible to retrieve from a wearable device without addition of an oscilloscope or a current clamp, which would thwart daily activities and alter the system.

In this case it is important to route the audio cable close to the discharge location. This was done so as ensure there was enough current coupled into the I/O.

4. DISCUSSION AND CONCLUSIONS

Using the test IC, it is now possible to get an estimate of the induced current through the I/O pin of an IC of a wearable device without altering the system. Based on the test scenarios discussed, a relation between the charge voltage and current on the I/O of an IC can be estimated. This information is important so that design improvements can be made to the overall ESD protection and software stability on wearable devices. Using the current pseudo wearable DUT, studies for the statistical distribution of the number and level of ESD events experienced by the wearable device during normal human activity can be investigated. Discharge electrodes at different locations on the human body can be

connected to different I/O's on the test IC and monitored for the number of events triggered. Such studies can be expanded to include relative humidity, different flooring conditions, different apparel material types, and more.

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V. A TRANSIENT EVENT SENSOR FOR EFFICIENT SYSTEM LEVEL ESD TESTING

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ABSTRACT

Testing and debugging of immunity issues is challenging in part because it is not known which components inside a system are impacted by an immunity test or at what level. Attaching cables and probes to determine stress voltages and currents within a system is time-consuming and can alter the test results. Sensors are proposed for measuring the peak stress voltage experienced within a system during a transient immunity test. The peak current can also be found when the sensor is placed across a transient voltage suppressor with a known I-V curve. The peak level is transmitted wirelessly to a receiver outside the system using frequency-modulated magnetic or electric fields, thus allowing multiple measurements to be made without opening the enclosure or otherwise modifying the system. Two sensing circuits are proposed, one which stores the peak voltage on an external capacitor and another which uses an analog-to-digital (A/D) converter to store the level in a register. The capabilities of the circuits were validated with a combination of SPICE and electromagnetic simulations when the sensor was placed inside a typical cell phone enclosure. Simulations demonstrate the sensors can accurately detect the peak transient voltage and transmit the level to an external receiver.

Keywords: Electrostatic Discharge (ESD), Electrically Fast Transient (EFT), Sensors, Transient Voltage Suppressor (TVS), Testing.

1. INTRODUCTION

Electrostatic discharge (ESD) problems are notoriously difficult to debug, in part because it is difficult to determine the path of the ESD current or the level of voltages or currents seen by individual components within a system. Adding probes or making other modifications to the system is not only time consuming but can change the ESD current path and thus render the measurement useless. The ability to measure voltages and currents within a system without adding significant hardware could substantially improve the ability of an engineer to test and correct for issues with ESD and other transient electromagnetic events.

A number of previous studies have proposed possible solutions to this problem. In (Kuhn *et al.*, 2014), the level of an event is detected with a fuse and diode combination implemented on-die in parallel with the ESD protection device. The occurrence of a stress event beyond a set limit causes the fuse to melt. While effective, measurement of the fuse is cumbersome and the fuse can only be used once. In (Chow and Hor, 2008; Ker *et al.*, 2008; Thomson *et al.*, 2017) the power supply noise created by a transient event is used to detect the event. The noise is coupled to a latch input. If the power supply voltage changes more rapidly than a set threshold, a latch is triggered and an event recorded. Circuits have also been proposed which use an on-die diode and capacitor combination to store the peak level of an event at an I/O pin (Jack and Rosenbaum, 2011). The capacitor requires external laboratory equipment to read its voltage and must be read shortly after an event to prevent excessive charge leakage. An alternative sensing methodology was proposed in (Patnaik *et al.*, 2018) (Patnaik *et al.*, 2017b) where sensors are implemented in the I/O of a microcontroller. These sensors can detect when an I/O pin experiences a transient stress event and can determine the peak level of the event. The sensors allow the microcontroller

to determine on which pins an event occurred and the polarity of the event. The level of the event is stored on a capacitor and can be read by the microcontroller using an on-chip analog-to-digital (A/D) converter. Experiments with these sensors show they work well in system level tests (Patnaik *et al.*, 2017a), but the system must include a microcontroller which has these sensors implemented in its I/O in order to use them.

New sensors are proposed in the following article to detect the peak level of a transient stress event during an immunity test. The sensor can be added to system ESD protection structures, like a transient voltage suppressor (TVS), before testing with minimal changes to the hardware and to the ESD current path. The peak level of the event is stored in an external capacitor or by converting the level to a digital value using a simple on-chip A/D converter. The sensors wirelessly transmit the peak level of the event to an external probe through a frequency-modulated electric or magnetic field. Wireless transmission enables the test engineer to detect and read information from the sensors without the need to disassemble the product between tests or to add cables which penetrate the enclosure and which may change the test result.

2. TRANSIENT EVENT SENSORS

System level ESD protection is often achieved using a combination of transient protection devices acting together, such as an on-board TVS device and on-chip ESD protection as indicated in Fig. 1. Both, the TVS and internal I/O protection devices share the transient stress current, with the bulk of the current passing through the TVS.

The sensors developed here can be added to any trace or pin, though would often be added in parallel with an on-board TVS as shown in Fig. 1. While the sensors are designed to measure the peak stress voltage during a transient test, the peak current associated with the event could be determined from the I-V curve of the TVS. In most cases, the sensors would be mounted only during testing and would not be included in the commercial product.

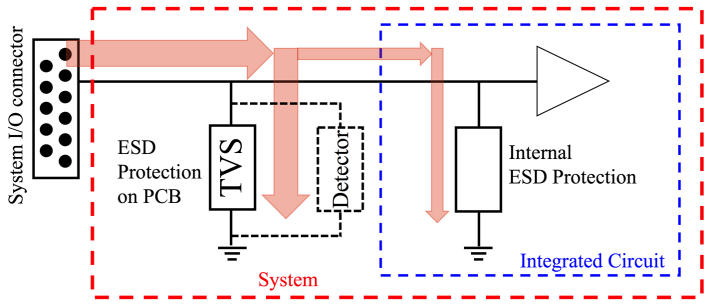

Figure 1. Block diagram of a typical ESD protection scheme showing internal and external ESD protection devices.

Two variations of the peak transient sensors were investigated. Block diagrams of the implementations are shown in Fig. 2. The sensors are connected to a pin or trace of interest within the system under test, possibly across a TVS diode, and are also connected to a power source. Each sensor measures the peak transient voltage, stores a measure of the peak voltage either on a capacitor or on a register after performing an A/D conversion, and then uses the stored result to drive a current controlled oscillator (CCO). The CCO can be connected to a loop, which drives an oscillating magnetic field, or to a floating metal conductor, which drives an oscillating electric field. The frequency of oscillation depends on the peak level of the transient event. The user can determine the peak level of the event by measuring the frequency of the oscillating magnetic or electric field. It is important to communicate the peak level through the frequency rather than the magnitude of the signal, since the magnitude can vary considerably depending on the placement of the transmitting and receiving probes. Each circuit is discussed in detail in the following sections. Designs are only presented for measuring negative transient stress events, but similar designs could easily be made for measuring positive transient stress events.

2.1. Implementation I - Storage on an External Capacitor. This version of the transient sensor stores a measure of the peak negative transient voltage as a voltage across an external capacitor. The external capacitor can retain this voltage long after the transient

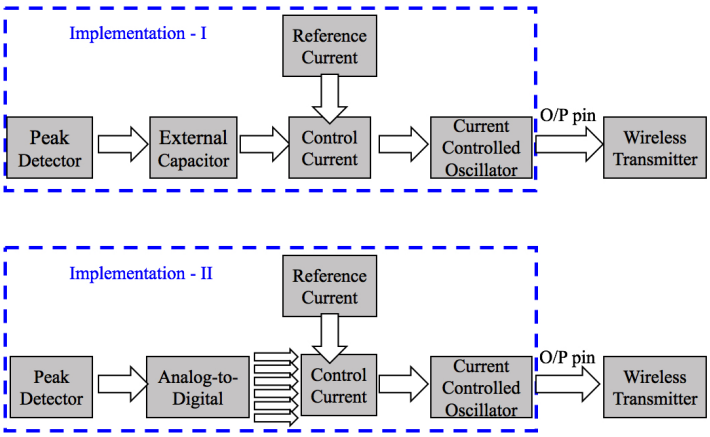

Figure 2. Block diagram of transient event sensors. Implementation I: level stored on external capacitor. Implementation II: level stored in register.

event has passed. It is important to retain the charge for at least milliseconds in order to transmit a clear indication of the peak level. A measure of the peak level is first stored on an internal capacitor, which can be charged quickly but cannot store charge for a long duration due to its small size. The voltage on the internal capacitor is used to (more slowly) charge an external capacitor which can retain its charge for significantly longer than the internal capacitor. The voltage across the external capacitor generates a current which controls the oscillation frequency of the CCO.

The overall circuit consists of a circuit to detect the peak and charge the external capacitor, a current reference (used to create a reference oscillation at the CCO), a circuit to combine the current from the external capacitor and from the reference current source, a CCO, and an external loop or conductor to create the oscillating magnetic or electric fields, as suggested in in Fig. 2. Each circuit is discussed in the following sections.

2.1.1. Peak Detector with External Capacitor. The negative peak detector stage, shown in Fig. 3, is modeled after the peak detector in (Patnaik *et al.*, 2017b). Current only flows through the input diode D0 when the pad voltage goes below VSS, so the sensor has minimal impact on the measured circuit except during a negative stress event. Resistors

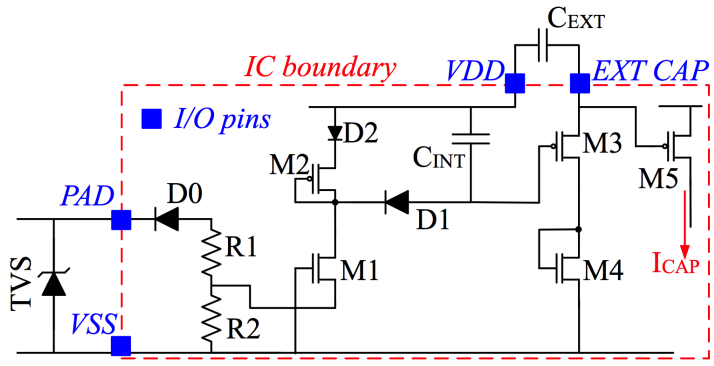

Figure 3. Peak detector stage for Implementation I, using an external storage capacitor. Four I/O pins are shown in the schematic: PAD, VDD, VSS, EXT CAP. The TVS device is connected between PAD and VSS. The external capacitor is connected between VDD and EXT CAP.

R1 and R2 are used to scale the input voltage to a level which can be handled by NMOS M1 without causing oxide damage or snapback. M1 is implemented in an isolated P-well, with the body and source connected, so the source-to-body voltage is zero throughout the transient event. D0 is implemented at the pad to ensure the parasitic bipolar junction transistor (BJT) associated with the diode has minimal impact on the current through R1 and R2. A negative stress event will cause a positive gate-to-source voltage at M1, and thus a current through M2 when the gate-to-source voltage is greater than an NMOS threshold. The corresponding voltage drop across diode D2 compensates the voltage drop across diode D1 and allows a measure of the peak voltage across M2 to be stored on capacitor C_{INT}. C_{INT} drives a source follower which charges C_{EXT} to within a PMOS threshold voltage of the voltage on C_{INT}. Since C_{INT} is small it may be charged very quickly. While C_{INT} may only hold its charge for microseconds, that time is sufficient to fully charge the much larger C_{EXT}. Simulations show that when C_{INT} is on the order of femtofarads, C_{EXT} can be on the order of hundreds of picofarads. C_{EXT} subsequently drives PMOS M5, which drives a current I_{CAP}. I_{CAP} is directly related to the peak voltage at the input pad.

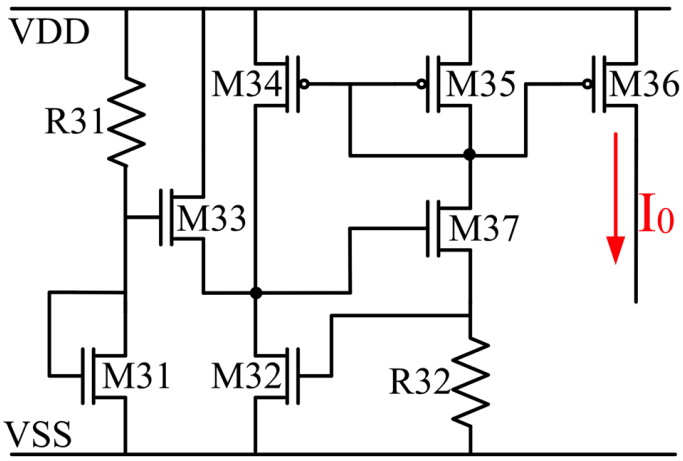

Figure 4. Threshold referenced current source. I_0 shows minimal variation with variation in VDD.

2.1.2. Reference Current. The CCO is set to oscillate at a default frequency, f_0, when no transient event has occurred. The generated signal demonstrates to the user that the sensor is working, allows the user to find a good receiver location, and can be used to determine the peak voltage from the change in frequency before and after an event. The reference frequency is generated by a reference current fed to the CCO. For the implementation in this paper, the reference current was created by a threshold referenced source (Allen and Holberg, 2002), as shown in Fig. 4.

A threshold voltage referenced source produces a reliable output current with minimal sensitivity to variations in power supply voltage. The circuit was designed to operate at 3.3 V. The reference current, I_0, created at the drain of M35, is mirrored to PMOS M36, and passed to the current summation block where it can be fed to the CCO. While better stability with temperature or process variation might have been possible with another reference, for example a bandgap reference source (Allen and Holberg, 2002; Feng *et al.*, 2013), a threshold reference source was used because of the availability of good FET models and the lack of good BJT models for the chosen implementation technology.

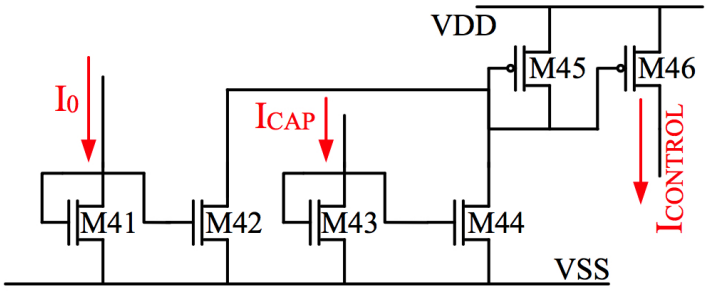

Figure 5. Current summation block. Without an event, $I_{CONTROL} = I_0$. After an event, $I_{CONTROL} = I_0 + I_{CAP}$.

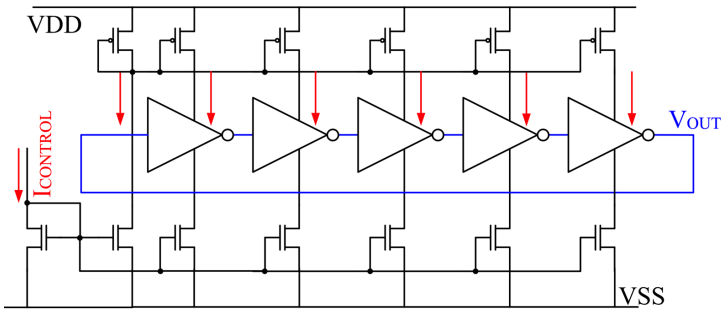

Figure 6. Current controlled oscillator implemented using current starved inverters.

2.1.3. Control Current Generation. The CCO control current is generated from a sum of the reference current, I_0, and the current generated by the peak detector, I_{CAP}, using the circuit shown in Fig. 5. When there is no transient event, $I_{CAP} = 0$ and $I_{CONTROL}$ depends only on the reference current, I_0. When a transient event occurs, $I_{CONTROL}$ increases directly with I_{CAP}. This arrangement allows the CCO to oscillate at a well-known default frequency during normal operation, and for the oscillation frequency to increase in proportion to the peak detected voltage after a transient stress event.

2.1.4. Current Controlled Oscillator. The CCO was designed using five current starved inverters as shown in Fig. 6 Baker (2010). The oscillation frequency of the CCO is determined by the control current generated by the current summation block. The CCO was designed to operate from 240 MHz to 600 MHz, with 240 MHz corresponding to no

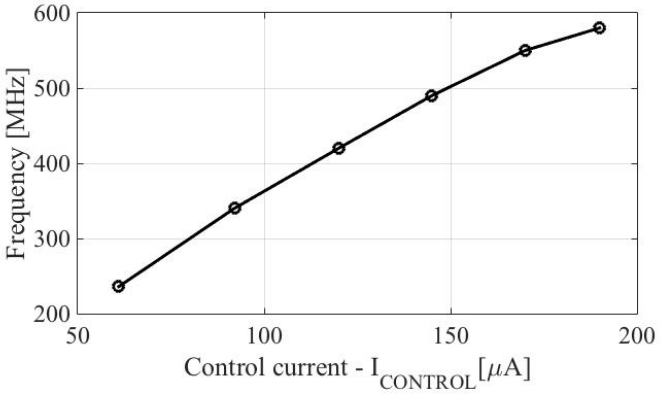

Figure 7. Simulated oscillation frequency of the CCO as a function of the control current.

event and 600 MHz corresponding to the largest transient event of interest. The oscillator was designed here to operate at relatively low frequencies and over a relatively large range of frequencies in order to show proof of concept, though a much higher base operating frequency or much smaller operating frequency range could be used. Fig. 7 shows the oscillation frequency of the CCO as a function of the control current. The relationship between the control current and the oscillation frequency is largely linear to above 150 μA, where linearity begins to be lost as the current mirror stages in the CCO go out of saturation.

2.1.5. Wireless Transmission of Oscillating Signal. For the proposed sensor to be used without performing any significant modifications to an existing system or enclosure, the peak detected transient voltage must be transmitted wirelessly through the enclosure without adding cables or other hardware. The value of the peak detected voltage can be communicated through oscillating electric or magnetic fields by connecting the CCO output to an external loop or metal structure as illustrated in Fig. 8.

In Fig. 8a, the CCO output pin is connected to a wire shorted to a neighboring VSS pin. The oscillating current generates oscillating magnetic fields. Depending on the application and the required magnetic field, the loop could be large, for example by using an external wire to make the loop, or could be small, for example by shorting the CCO output

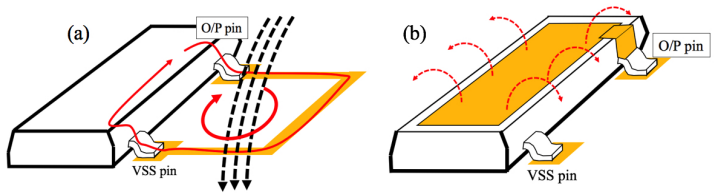

Figure 8. The sensor can communicate with an external sensor by (a) shorting the CCO output pin to the reference pin to form a large inductive loop and creating oscillating magnetic fields, or (b) shorting the CCO output pin to a large floating metal plane and creating oscillating electric fields.

and VSS package pins and using the package lead frame to create the loop. Typically, a large driver implemented in the I/O pad is needed between the CCO and output pin to create the large currents required to create detectable magnetic fields. Fig. 8b shows one possibility for creating an oscillating electric field, in this case by connecting the CCO output to a metal plate placed directly on the package of the transient sensor. The value of the peak detected voltage can be determined for both implementations by sensing the change in the oscillation frequency of the fields using a probe placed just outside the system enclosure.

2.2. Implementation II - Peak Detector with Digital Storage. This implementation of the sensor stores a digital representation of the peak transient voltage using Set-Reset (SR) latches. A measure of the peak voltage is stored across an internal capacitor similar to the previous implementation, but the capacitor is used to drive a set of comparators which quantize the stored voltage and trigger the SR latches. A latch is set if the capacitor voltage (or more specifically the current driven by the voltage) exceeds a given threshold. A/D conversion is done after the transient event has passed, to ensure the power supply has had time to settle. The number of triggered latches determines the amount of current which drives the CCO, and thus determines the output oscillation frequency. The CCO is used to drive an external loop or floating conductor to drive oscillating magnetic or electric fields, as before. Details of each block are discussed in the following sections.

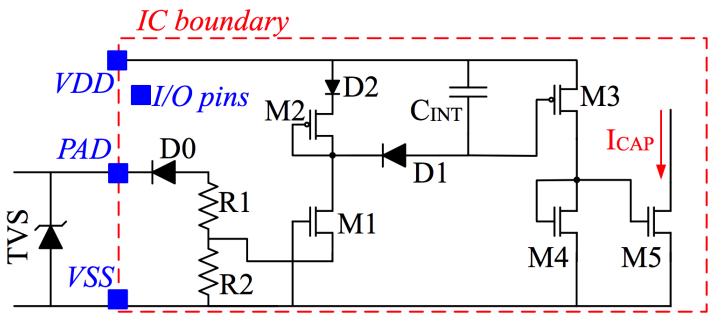

Figure 9. Peak detector stage for Implementation II.

2.2.1. Peak Detector. The peak detector stage for this implementation is shown in Fig. 9. This circuit is similar to the peak detector in Implementation I (Fig. 3), but does not charge an external capacitor. In this version, the small internal capacitor is only required to hold a charge long enough to allow the power supply voltage to settle and the A/D converter to record a digital representation of the capacitor voltage. As before, a measure of the peak transient stress voltage is stored as a voltage across C_{INT}. This voltage is used to drive a current, I_{CAP}, which is passed to the A/D stage where the comparison and storage is performed.

2.2.2. Analog-to-Digital Conversion. The A/D converter is shown in Fig. 10. I_{CAP} is passed to a number of current comparators and compared with a reference current, I_0, generated by a current source like the one in Fig. 4. In the first stage, I_{CAP} is compared with I_0, in the next stage with $2I_0$, in the next with $3I_0$, and so on. For the implementation studied here, five comparators were used corresponding to five quantization levels. More comparators could be used if higher resolution was desired. The output of each comparator drives an SR latch. No SR latch can be triggered, however, until a fixed amount of time has passed since a transient stress event was detected. This delay is implemented along with the lowest level comparator (which compares I_{CAP} with I_0).

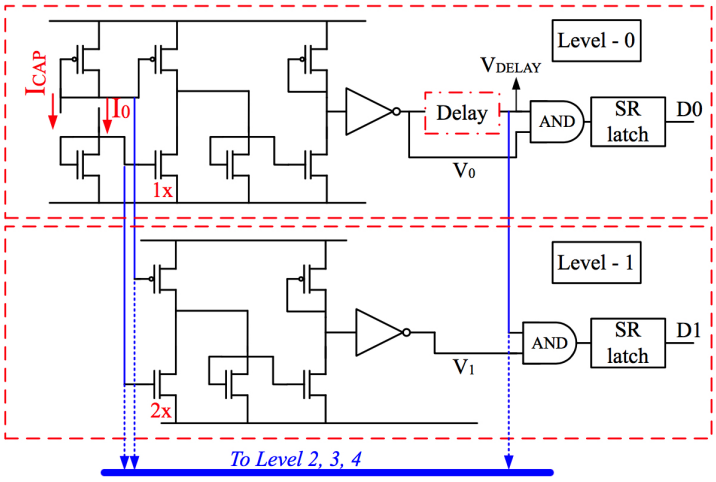

Figure 10. Block diagram of A/D stage. The stored voltage is quantized by current comparators which trigger SR latches after a set delay.

A schematic of the delay block is shown in Fig. 11. V_0 is the output of the lowest level comparator. Under normal conditions, when no transient event has been detected, V_0 is low, node-B is high, capacitor C3 is discharged, and the output, V_{DELAY}, is low. If an event occurs which exceeds the lowest quantization level (i.e. $I_{CAP} > I_0$), V_0 goes high causing M98 to turn “off" and M97 to turn “on" and the capacitor C3 to discharge through M97 and M92. The discharge rate is controlled by the reference current I_0 (provided by the reference current source). The discharge time can be set by adjusting the sizes of M91, M92, and C3. For the implementation shown here, the delay was set to approximately 600 ns as shown in the simulation in Fig. 12. An approximate delay is sufficient, as most transient events of interest should be much less than 600 ns in length, and previous experience suggests the capacitor C_{INT} (holding a measure of the peak transient voltage) will not discharge significantly for several microseconds (Patnaik *et al.*, 2017b). To avoid redundancy, the delay block is only added to the comparator with the lowest threshold level. The output V_{DELAY} is AND’ed with the output of each comparator so that the latches can be triggered only after the delay is complete. This arrangement not only ensures sufficient time has passed for the power supply to have settled, thus ensuring that the comparator outputs are

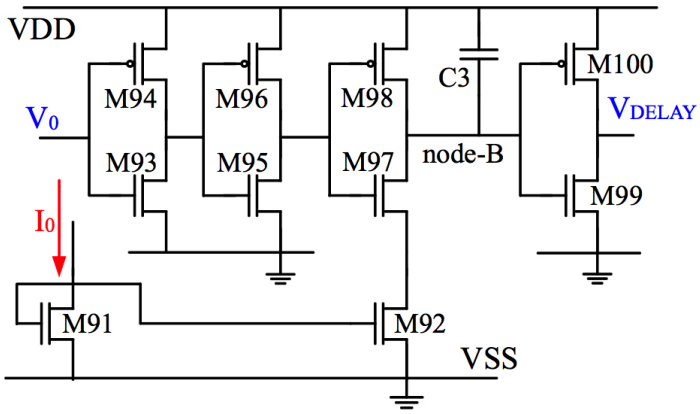

Figure 11. Delay block introducing an approximately 600 ns delay between the detection of a transient stress event and the triggering of an SR latch.

accurate, but also prevents glitches or noise from falsely triggering the latches. The SR latches will retain the digitized values so long as power is maintained and the latches are not reset. While not shown here, in a practical implementation it would be reasonable to use a second delay element to reset the latches after a long delay (e.g. a few seconds). This delay would allow sufficient time for an external probe to adequately measure the frequency of the generated oscillating magnetic or electric fields, but would also automatically reset the latches to make them ready for another test without additional input from the user.

Each latch in Fig. 10 generates an output, D0-D4, which goes high when the latches are triggered. These latch outputs determine the current generated by the digital-to-analog (D/A) converter stage as shown in Fig. 13. The reference current, I_0, is mirrored to legs of a current adder. The legs are turned “on" or “off" by the latch outputs. The output control current, $I_{CONTROL}$, is thus given by:

$$I_{CONTROL} \approx I_0 + \sum D_i.I_0 \tag{1}$$

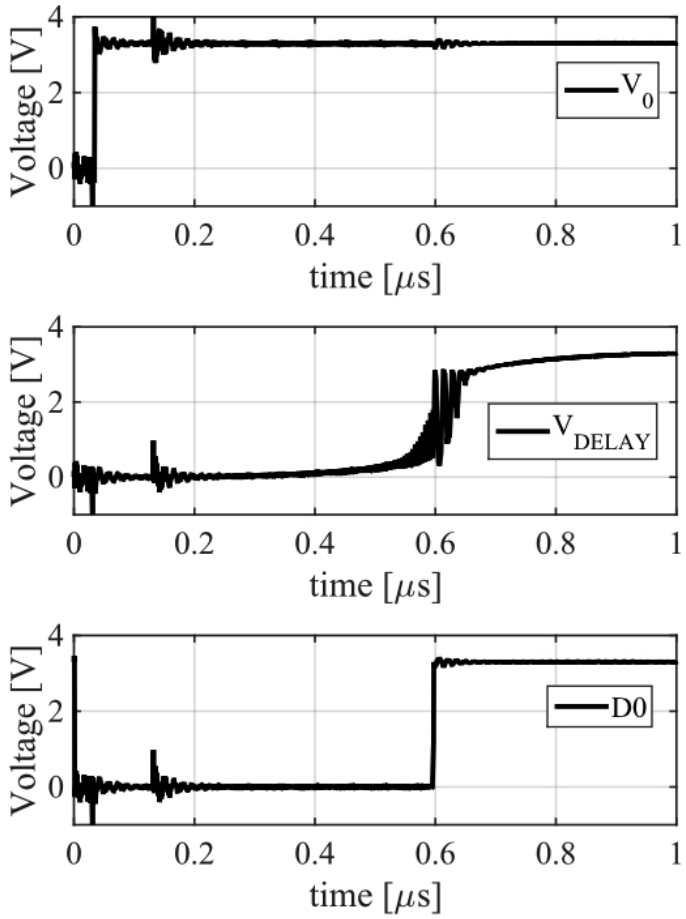

Figure 12. Simulated output of the delay stage shown in Fig. 11. (Top) output of the comparator block, V_0; (Middle) output of the delay stage, V_{DELAY}; and (Bottom) output of the switched latch, D0.

where, I_0 is the current from the reference circuit and D_i is the digital output from each latch stage. When no latch has been triggered, $I_{CONTROL} = I_0$. The control current increases by roughly I_0 for each triggered latch, as shown in Fig. 14.

2.2.3. Current Controlled Oscillator and Output Stage. The control current, $I_{CONTROL}$, from the D/A is fed to a CCO which drives an external loop or large floating conductor, similar to Implementation I as shown in Fig. 6 and Fig. 8. The oscillation frequency of the generated magnetic and electric fields are thus directly related to $I_{CONTROL}$, which is directly related to the peak transient stress voltage.

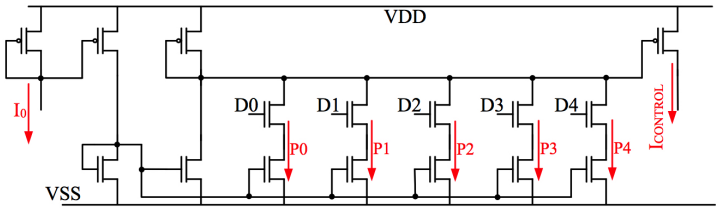

Figure 13. The digital-to-analog converter. Latch outputs D0-D4 control the current mirror stages and the output current, $I_{CONTROL}$.

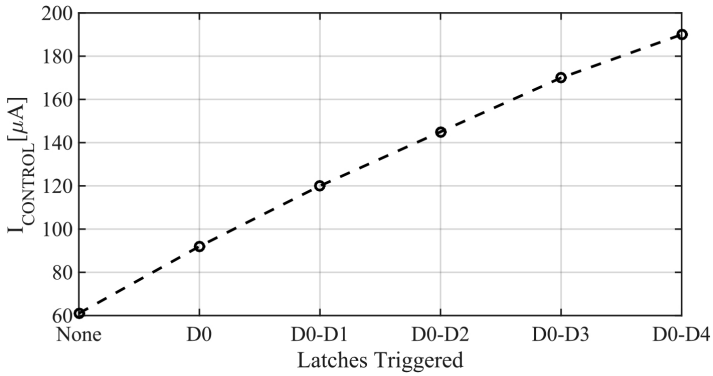

Figure 14. Simulated control current as a function of the number of triggered latches.

3. SIMULATION AND IMPLEMENTATION

The transient level sensors were designed in a 180 nm technology. The sensors were first tested in SPICE, and later using an electromagnetic modeling tool to demonstrate the signal could be received at a probe external to the test system enclosure. A block diagram for the SPICE-level test bench is shown in Fig. 15.

The power delivery network (PDN) of the printed circuit board (PCB) was represented with the PDN model. This model uses a simple circuit approximation of the PDN impedance based on PCB PDN impedance measurements, similar to the model in (Patnaik *et al.*, 2017a,b, 2018). This model matches the measured PDN impedance within a few decibels up to 3 GHz, the upper frequency range of interest for most transient events. The

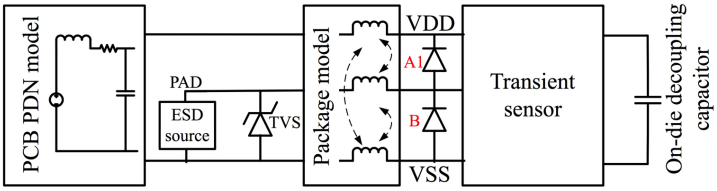

Figure 15. Block diagram of the test bench used to characterize the transient sensors.

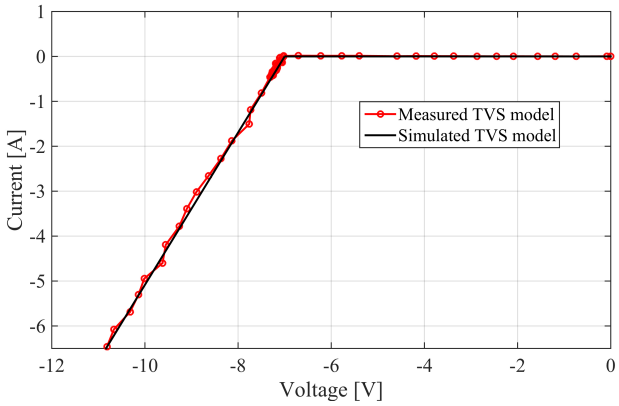

Figure 16. Simulated and measured I-V curve for the TVS diode.

PCB PDN includes several hundreds of nanofarads of on-board decoupling capacitance. The die and package model includes the self- and mutual-package inductance, on-die ESD protection diodes, I/O models, and approximately 1 nF of on-die decoupling capacitance.

A model of the on-board TVS diode was developed based on measurements of a commercial TVS diode with a turn on voltage of -7 V. The simulation model for the TVS device was matched to the measured quasi-static I-V diode characterization curve as shown in Fig. 16. The simulated and measured curves match within a few hundred millivolts.

Both sensor implementations were tested using the same test bench. The sensors were characterized using a transmission line pulse (TLP) source (Maloney and Khurana, 1985). Simulations were performed by stressing the I/O pad with negative stress events, where the I/O pad was pulled below VSS. The applied TLP stress varied from -1 A to -6.5 A and had a pulse width of 100 ns. Each sensor was tested independently.

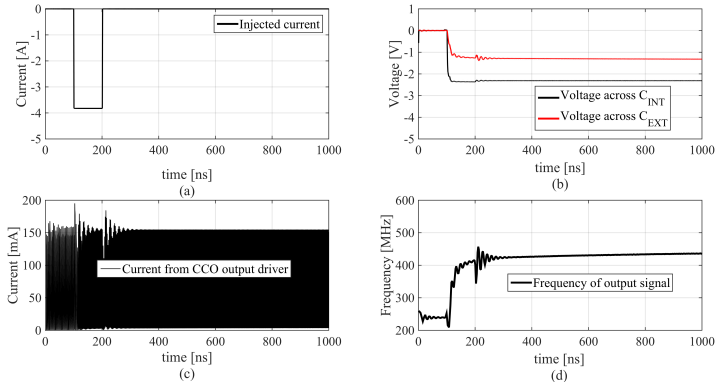

Figure 17. Transient response for Implementation I using an external capacitor: (a) Injected current between I/O pad and VSS; (b) Voltage across internal and external capacitor; (c) Switching current waveform at the output of the CCO; (d) Frequency of the CCO output.

The transient response for Implementation I, with an external capacitor, is shown in Fig. 17 when the TVS was subjected to a -3.9 A TLP event. The output of the CCO was shorted to the sensor's reference pin to form an inductive loop. Fig. 17a shows the injected current. The voltage across both C_{INT} and C_{EXT} fall at the moment of the event, though the voltage across C_{EXT} falls more slowly and is a PMOS threshold voltage higher than C_{INT}, as expected. The CCO oscillation frequency changes after the event, in relation to the voltage across C_{EXT}. The ringing around 100 ns and 200 ns in these plots was caused by the rising and falling edges of the TLP pulse and the associated disturbance to the power delivery network. For this test, the CCO generates a 435 MHz signal which is available to be read out long after the event has passed. The ability to read the signal with a probe placed outside of the test system enclosure is demonstrated later in this section.

Implementation II, using a digital latch, was similarly tested with a TLP event at the TVS diode. The transient circuit response for a -2.1 A injected current pulse is shown in Fig. 18. Because the event was relatively small, only the first two latches, D0 and D1, were triggered while the other latches remained in their reset state. The D0 and D1 latches did not switch state until 600 ns after the beginning of the transient event as determined by the delay element. The frequency of the CCO output signal was 430 MHz.

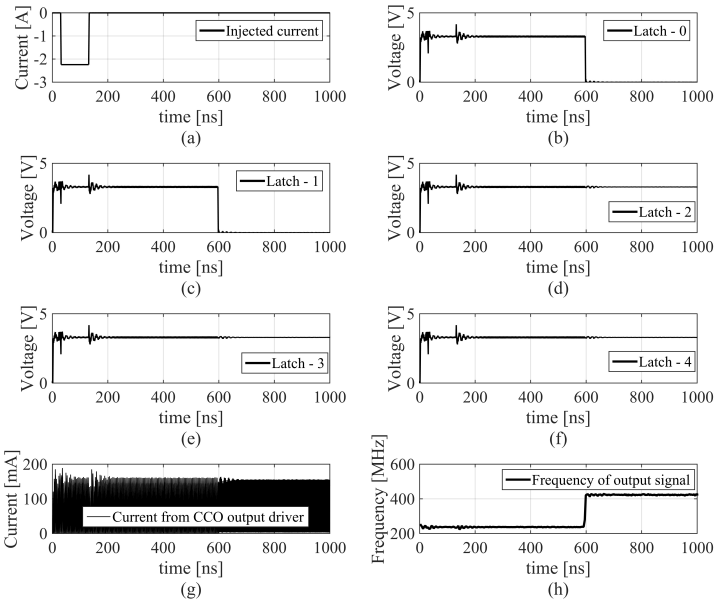

Figure 18. Transient response for Implementation II using an A/D converter: (a) Injected current between I/O pad and VSS; (b)-(f) Outputs of latches D0-D4; (g) Switching current measured at the output of the CCO; (h) Frequency of the CCO output.

Fig. 19 shows the CCO output signal frequency for different magnitudes of the stress event applied to both design implementations. As expected, the external capacitor configuration is able to provide a finer resolution representation of the peak current than the digital storage technique, as the digital implementation must quantize the input voltages into specific bins. Both designs were able to accurately transmit the peak current value for injections having a magnitude below 6 A. Larger currents could be detected through small modifications to the sensors, particularly at the input stage. The two implementations were not designed to have similar current-frequency curves, so the fact that a specific current generates a different frequency output for the two sensors is not unexpected.

Electromagnetic simulations were used to demonstrate the ability of an external sensor to receive the signal from the CCO and determine the peak transient voltage. A 3-D electromagnetic model was built of a typical cell phone as shown in Fig. 20. The model includes the geometry and material properties for the liquid crystal display, the PCB, metal

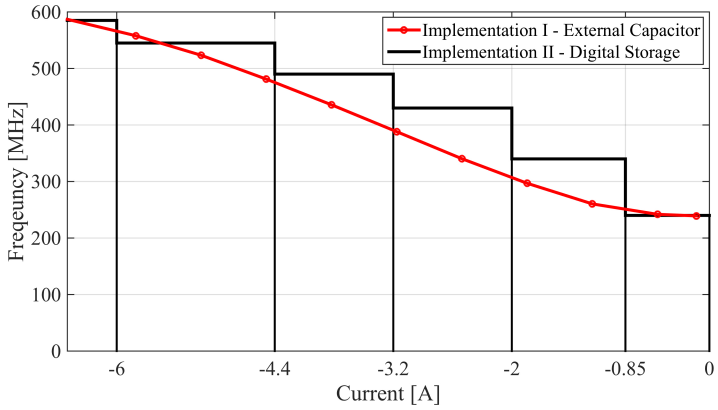

Figure 19. Injected current versus output frequency for both implementations of the peak transient sensors.

chassis, and the plastic housing. The sensor was placed on the PCB and configured to drive a 2 mm x 1 mm loop from the CCO output pin. The receiving loop was 4 mm x 4 mm in size and placed 5 mm above the body of the cell phone. A full wave simulation was used to determine the S-parameters between the transmitting loop at the sensor and the receiving loop.

The signal at the receiving probe was estimated in SPICE from the calculated S-parameters for the loop. The output driver of the CCO was designed to supply roughly 100 mA of drive current. The overall current was simulated when the CCO was driving an inductance equivalent to the loop inductance of the 2 mm x 1 mm loop. This current was then used with the full wave S-parameter block to estimate the voltage measured across the 50-ohm load of an oscilloscope or spectrum analyzer hooked to the external loop probe. The CCO output was similar to the output shown in Fig. 18.

The received signal spectra before and after the transient event are shown in Fig. 21. Each spectrum was calculated over a 2 μs window just before and just after the event. Before the event, the receiver detects a signal at 240 MHz and its harmonics. After the event, the baseline oscillation frequency shifts to 430 MHz. The received signal strength is approximately -87 dBm. This signal strength is easily readable on a spectrum analyzer or

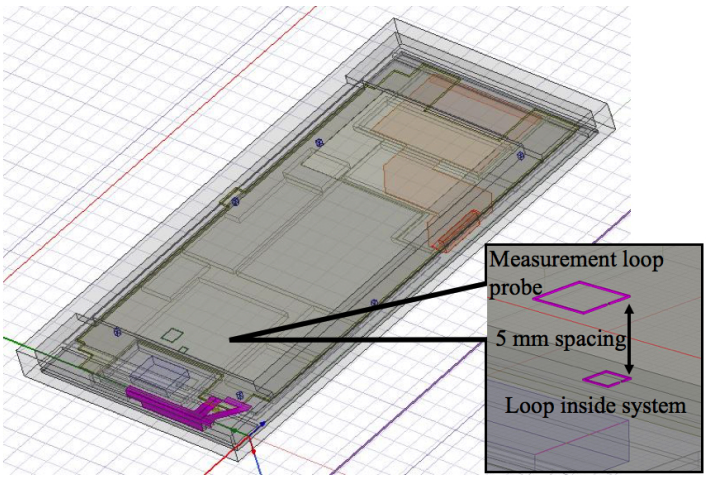

Figure 20. Full wave model of a cell phone replica used to model the coupling from a sensor on the main PCB to a field probe place 5 mm outside the cell phone.

through a suitably long measurement on an oscilloscope. A weak received signal could be further boosted by a low noise amplifier at the receiver. The choice of a magnetic field or an electric field transmission depends on the system set up. For example, a floating wire connected to the CCO output and run close to an opening in the enclosure might generate a stronger signal outside the enclosure than a small loop at the sensor.

For the implementation shown here, the CCO was designed to have a relatively wide bandwidth, 240 MHz to 600 MHz, and no attempt was made to “clean" the signal to remove higher order harmonics. The presence of the harmonics can be seen both as an advantage and disadvantage. For example, in Fig. 21, the CCO generates a signal at both 240 MHz and 480 MHz and the user must be certain to look at the lowest transmitted frequency to get a clean reading of the signal level. While this might be considered a disadvantage, if there were significant system noise which obscured the ability to read the signal around the base frequency (here 240-600 MHz), the presence of the harmonics could allow the user to alternatively read the transmitted signal at a higher frequency from the signal. If transmission at multiple frequencies was not desired, narrowing the bandwidth and low-pass filtering the CCO output could easily remove the higher order harmonics.

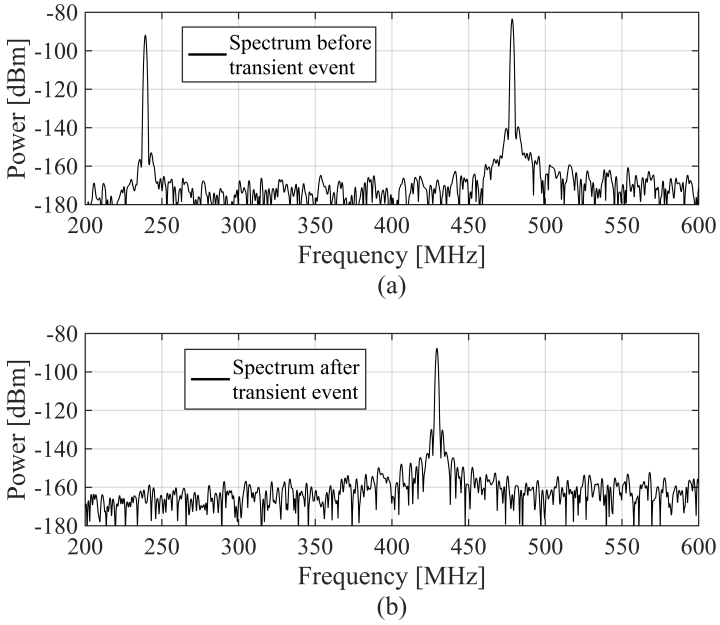

Figure 21. Spectra of the simulated signal measured by the oscilloscope calculated by passing the CCO output through the simulated S-Parameter coupling network: (a) Before the transient event; (b) After the transient event.

Example layouts of the two implementations are shown in Fig. 22. The circuits are implemented in 180 nm technology. Implementation I, using an external capacitor, requires 26000 μm^2 of die area. Implementation II, using an A/D converter, requires 42000 μm^2 of die area. Both implementations require pins for VDD, VSS, the TVS input, the CCO output, and reset, to reset the storage capacitors and the SR latches. Implementation I also requires a pin for the external capacitor. These modest requirements should allow the sensor to be manufactured at relatively low cost. The reset pin could be eliminated using an internal delay circuit, as mentioned earlier.

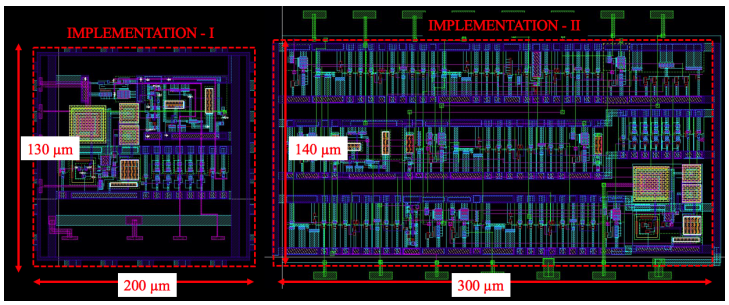

Figure 22. Layout and dimensions of the two sensors designed in 180 nm technology: (Left) Implementation I using an external capacitor; (Right) Implementation II using an A/D converter.

4. DISCUSSION AND CONCLUSION

Peak transient event sensors were developed which can be added to an existing electronic system to improve testing and debugging of transient immunity issues. The sensors were designed to be small and to communicate the peak transient voltage wirelessly so that they could be added with minimal disruption to the system. No probe cables or other alterations to the enclosure are necessarily required. The input impedance to the sensor is relatively small, so is expected to have minimal impact on signal integrity when added to a trace. Both sensor implementations were shown to perform their functions well. The implementation using an external capacitor requires an additional pin and, of course, an external capacitor, but is not limited to showing the peak voltage at only discrete values and requires a smaller die area than the implementation using an A/D converter. The area and number of pins required by both designs is sufficiently small that the manufactured cost of these sensors is expected to be low. Simulations in SPICE and using 3-D electromagnetic modeling tools demonstrate the sensors can detect the peak of typical transient stress events, will generate a frequency-modulated signal which can be adequately read by a receiving probe outside the system, and can be used to accurately predict the peak transient voltage. Demonstrations were only performed for sensors which detect negative events, though the design of similar sensors which detect positive events should be straightforward. While the

sensors were built to measure the peak transient voltage, if they are added across a TVS device with a known I-V curve, they could also be used to estimate the peak transient current through the TVS.

The CCO's for the circuit implementations shown here were designed to operate between 240 MHz and 600 MHz. This frequency range is adequate for a proof of concept demonstration of sensor operation, but might be changed in the final implementation. A higher oscillation frequency could allow better coupling between the sensor and the external receiving probe. A narrower frequency range could also better take advantage of filtering at the transmitter and at the receiver. For very narrow bandwidth transmissions, a resonant probe (Li *et al.*, 2014; Shinde *et al.*, 2016) could be used to further enhance the ability to receive the signal. With the addition of extra pins, the CCO baseline frequency could be made user selectable, allowing the user to avoid frequencies where there is significant in-system noise or to place multiple sensors within the system, each working over a different frequency range. The baseline frequency could be changed using a mux which adds or removes inverters from the CCO ring oscillator, though other options are also available.

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SECTION

2. SUMMARY AND CONCLUSIONS

Soft-failures were observed in a robot-docking station system when the robot performed a docking action. The robot charges up to a certain voltage and then discharge upon making first contact with the docking station. SPICE models were created to characterize soft-failures in a robot-charging station system. Tribo-charging studies under different climatic conditions were performed on the robot system. The SPICE based models were created based on S-parameter measurements. The source voltage was determined from the tribo-charging studies. The measurements involved addition of probes in the system to monitor voltages and currents during the transient event. An alternate method to perform these tests is to use on-chip sensors which can monitor the peak disturbance on a signal line during a transient event. Different circuits are designed which are capable of determining if an event occurred, its polarity, location and level. Part of these sensors were designed into a commercial test microcontroller. Tests were performed on the manufactured device to validate the successful implementation of these sensors. The application of these sensors was demonstrated on a pseudo-wearable device. The sensors designed allowed the user to determine if there were ESD events detected on the wearable device. The tests were performed without the addition of any additional probes. The sensors could reliably determine the peak level as well as the number of occurrences the device would experience in a normal laboratory environment. A separate sensor was also developed which can detect and transmit the peak disturbance on the signal line using a frequency modulated signal. This sensor can be added later to the system under test during testing purposes. The sensor can be operated with as low as five pins making it suitable for compact devices. The sensors developed can significantly assist in system level ESD debugging of electronic devices.

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