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Comparison of Via Equivalent Circuit Model Accuracy Using Quasi-Static and Full-Wave Approaches

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Abstract
The EMC and signal integrity impact of printed circuit board (PCB) trace discontinuities, such as vias, where the signal is transitioned from one layer to another in the PCB stackup, have become significant recently with the use of very high speed signals in today's systems. If these discontinuities are ignored, significant distortion of the high speed signal can occur, and in many cases, cause data errors. A fast and accurate technique to include the effect of via discontinuities in the typical design process is needed to ensure this distortion is considered if significant. Therefore, a simple equivalent circuit for the via discontinuity is needed so that this equivalent circuit can be easily used in the normal signal integrity analysis tools.

This paper demonstrates the effect on the equivalent circuit values as the distance between the signal via and the return-current via is increased. Also, the frequency range where a quasi-static based equivalent circuit is accurate or where a full-wave model is required is shown for the various distances between vias.

Introduction
The EMC and signal integrity impact of printed circuit board (PCB) trace discontinuities, such as vias where the signal is transitioned from one layer to another in the PCB stackup, have become significant recently with the use of very high speed signals in today's systems. If these discontinuities are ignored, and depending on the data rate and rise time of the signals, significant distortion of the high speed signal may occur, and in many cases, cause data errors. A fast and accurate technique to include the effect of via discontinuities in the typical design process is needed to ensure this distortion is considered (if significant at the appropriate data rate and rise time). Therefore, a simple equivalent circuit for the via discontinuity is needed so that this equivalent circuit can be easily used in the normal signal integrity analysis tools. [1-5]

There are two basic classes of tools to find the effects of the via (or other discontinuity). Either quasi-static or full wave tools may be applied to help solve this problem. When to use which class of tool is an important consideration.

There are a number of popular full wave modeling technqiues and software tools. However, these techniques and tools usually require an expert user to correctly create the model, and significant computation time to provide an accurate solution that covers a wide frequency range. Full wave techniques and tools have the advantage of high accuracy, but the disadvantage of not being able to easily fit into the normal real-world design process.

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Quasi-static techniques usually provide very fast results for problems where the physical dimensions are electrically small. In order to get fast results, the quasi-static modeling technique assumes there is no wave propagation delay. This criterion is usually met for PCB vias, but as the frequency content of the signals increase, the assumption that the structure is electrically small may not hold. Even if the structure is electrically small, the path the signal current (and especially the return current) takes may not be electrically short. When a user must transition between quasi-static and full wave techniques, depends on the frequency content of the signal, and the amount of error allowed in the final results.

Return Current Via Location

A further consideration that is very important is the distance between the signal via and the return current via. This distance will affect the equivalent circuit model's inductance significantly. Figure 1 shows an example of a multilayer PCB with six ground-reference planes. The signal approaches and leaves the signal via from internal layers. The simplest equivalent circuit model for this structure is a PI circuit, with two capacitors to "ground" and an inductor between the capacitors and in series with the signal path.

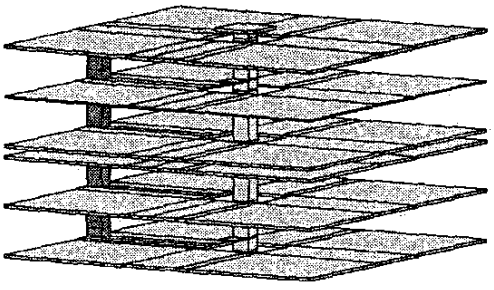

Figure 1 Multilayer PCB Example with Via Changing Reference Planes

When a quasi-static tool is used, and the return current via is moved further away from the signal via, the equivalent circuit inductance calculation requires all the return current to flow through the return current via. Figure 2 shows an example using a quasi-static version of the Partial Element Equivalent Circuit (PEEC) technique for the inductance for a simple PI equivalent circuit as the return-current via is moved further away from the signal via.

If the return current via is placed at a great distance from the signal via, the quasi-static inductance continues to increase. This is misleading, since the return current will not actually travel a great distance to the return via. Instead, the return current will find the path of least inductance (smallest loop area), resulting in a combination of displacement current between the adjacent planes and the return via.

Quasi-static and Full Wave Comparison

Using this equivalent circuit model for the various distances between vias, the quasi-static transfer function (S21) was obtained and compared to the full wave transfer function obtained using a full-wave PEEC and full-wave Finite-Difference Time-Domain (FDTD) techniques. This analysis allows engineers to decide when the full-wave analysis is required, depending on the required accuracy and frequency content of their signals.

Whenever modeling is performed, it is important to validate the results. In this work, the validation was performed using a variety of different simulation tools and techniques. Quasi-static simulations were performed with IBMciao (PEEC), SPECCTRAQuest (MoM), and ADS (MoM) to find an equivalent circuit, and then Hspice was used to find the loss transfer function (S21). Full wave simulations were performed with EZ-FDTD (FDTD) and IBMciao (PEEC) and the transfer function found directly from the simulations. The results for an example with the return

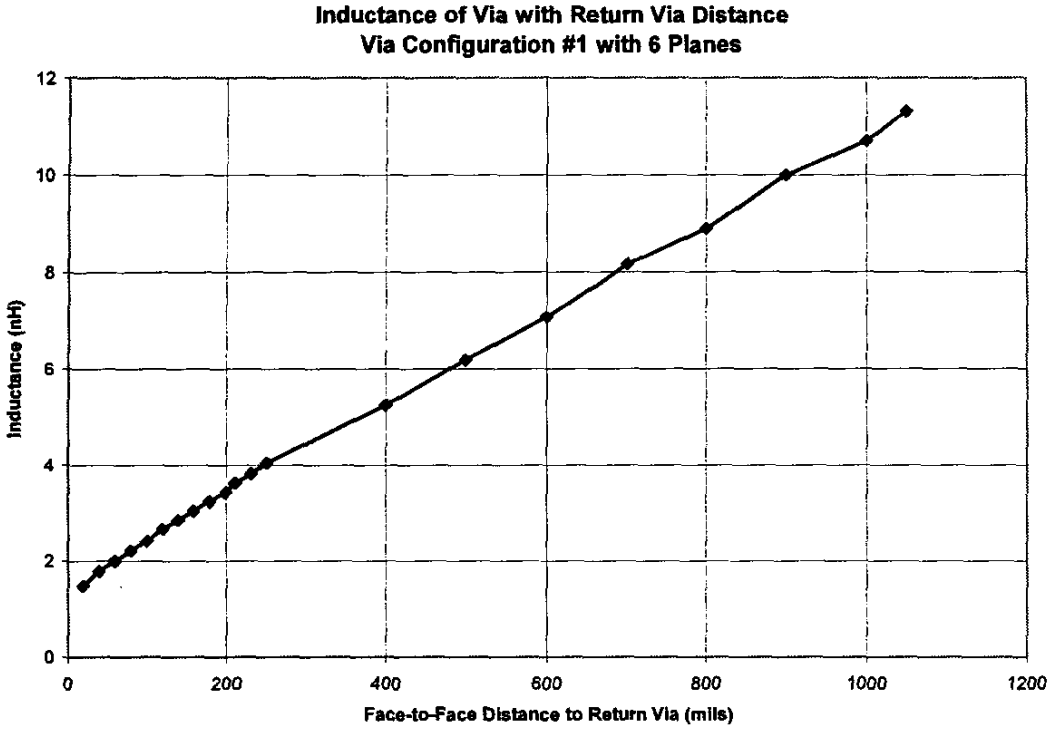

Figure 2 Example Inductance vs. Return-Current Via Distance from Signal Via

current via at 98 mils from the signal via are shown in Figure 3.

Figure 3 shows good agreement between all tools/techniques at lower frequencies, and a definite difference between the full wave simulation results and the quasi-static simulation results at higher frequencies. As frequency increases, the differences between results increase as well. Depending on the data rate and rise time for the signal (and therefore the frequency spectrum of the signal), and the amount of allowable error, the quasi-static results are not useable above some frequency.

Return Via Distance

Figure 2 shows how the (quasi-static) equivalent circuit inductance varies as the distance between the return current via and the signal via increase. However, the return current will follow the path of least impedance and minimize the loop size (and therefore minimize the inductance). As the return via is placed further away from the signal via, more of the return current will flow through the dielectric as displacement current. At some distance, depending on the separation between the planes, the return via will have no effect on the transfer function of the via. Figure 4 shows the transfer function for a variety of distances between the signal via and the return via. Note that when this distance becomes about 200 – 300 mils, the effect is the same as completely removing the return via. This means it is very important to keep the return via very close to the signal via, or these high frequency currents will be spreading out to use the displacement current path.

Using Eye Patterns to Determine Allowable Model Error

It is difficult to decide if the quasi-static model is accurate enough for a given data rate by simply using the S21 transfer

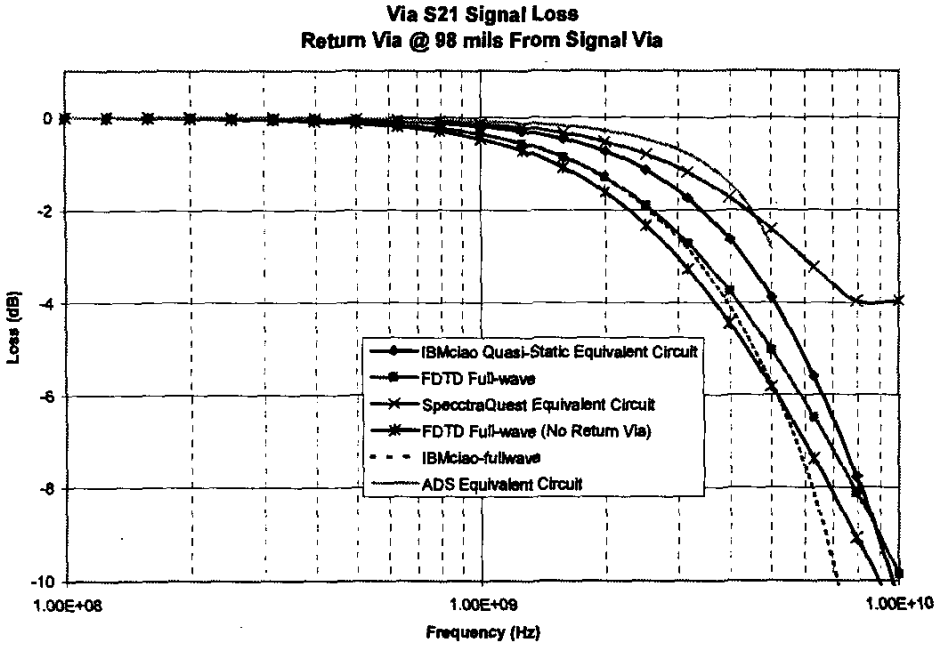

Figure 3 Comparison of Loss Through Via with Various Quasi-Static and Fullwave Tools

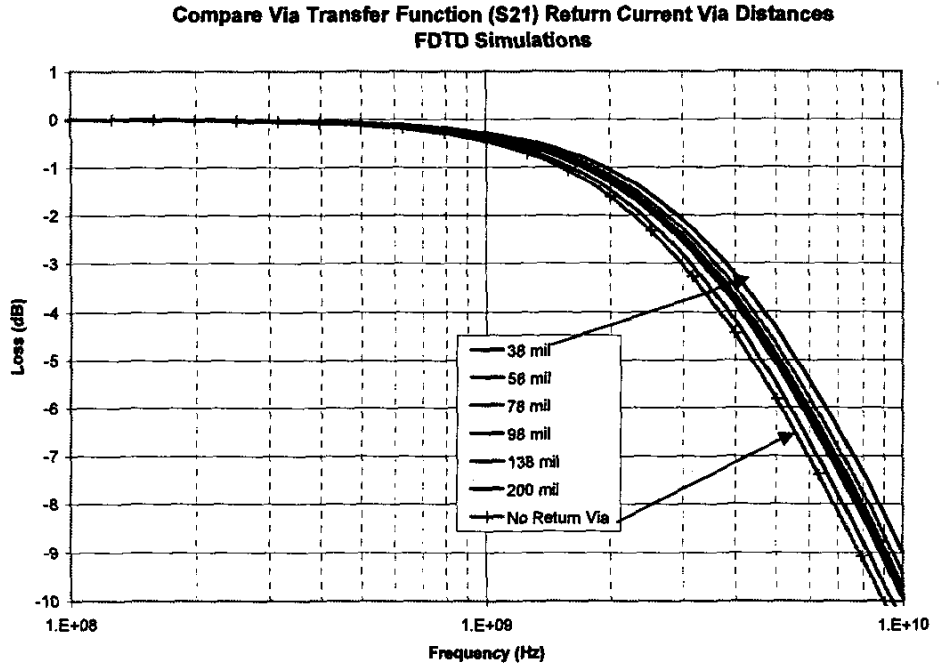

Figure 4 Comparison of Loss Through Via From Fullwave FDTD for Different Return Current Via Distances from Signal Via

function curves. One way to evaluate the accuracy for different data rates is to use the size of the eye pattern opening. Figure 5 shows an example of the eye pattern for the quasi-static and full wave simulations. The data rate and rise time is varied, as well as the distance between the signal via and the return via, and the results are summarized in Table 1. The eye opening decreases as the data rate increases, and the difference between the simulation techniques is apparent. The decision to use the quasi-static modeling techniques will depend on the amount of loss (at the data rate and rise time) for the remainder of the trace, etc.

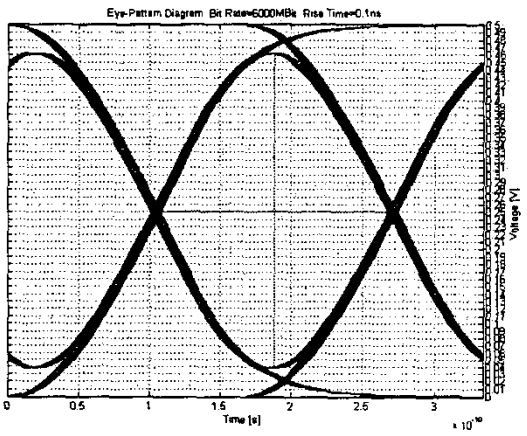

Figure 5b Eye Pattern Example for Example with Return Current Via at 98 mils from Signal Via (10 Gb/s 50 ps rise/fall time)

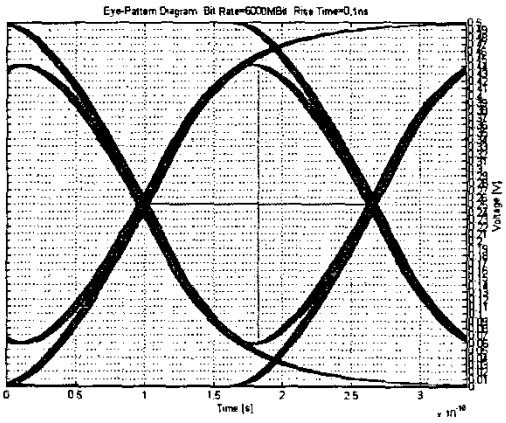

Figure 5a Eye Pattern Example for Example with Return Current Via at 98 mils from Signal Via (6 Gb/s 100 ps rise/fall time)

Summary

This work has compared the results using both full wave and quasi-static modeling tools to show the effect of a via transition between reference plane layers. The effect of the return via distance from the signal via is also shown. A variety of simulation tools and techniques were used to show the differences between full wave and quasi-static results, as well as to validate the individual tools.

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Table 1 Comparison of Results from Quasi-Static and Full-wave Simulations on Eye Pattern Vertical Opening For Different Data Rates and Distances to Return Current Via

Data Rate	Rise time	Distance to Return Current Via	FDTD (Full-wave) (normalized to 1.0)	Quasi-Static (normalized to 1.0)
2 Gb/s	100 ps	38 mils	0.995	0.999
2 Gb/s	100 ps	98 mils	0.994	0.999
2 Gb/s	100 ps	None	0.987	
4 Gb/s	100 ps	38 mils	0.94	0.999
4 Gb/s	100 ps	98 mils	0.92	0.976
4 Gb/s	100 ps	None	0.892	
6 Gb/s	100 ps	38 mils	0.8	0.95
6 Gb/s	100 ps	98 mils	0.757	0.845
6 Gb/s	100 ps	None	0.708	
10 Gb/s	50 ps	38 mils	0.663	0.857
10 Gb/s	50 ps	98 mils	0.615	0.688
10 Gb/s	50 ps	None	0.562	