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Jun Fan

Missouri University of Science and Technology, [jfan@mst.edu](mailto:jfan@mst.edu)

Hao Shi

James L. Knighten

James L. Drewniak

Missouri University of Science and Technology, [drewniak@mst.edu](mailto:drewniak@mst.edu)

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## DC Power Bus Modeling in High-Speed Digital Designs Including Conductor and Dielectric Losses

Jun Fan, Hao Shi\*, James L. Knighten\*\*, and James L. Drewniak  
Electromagnetic Compatibility Laboratory  
Department of Electrical and Computer Engineering  
University of Missouri-Rolla  
[jfan@umr.edu](mailto:jfan@umr.edu)  
\*HP-EEsof Division  
Hewlett-Packard Company  
\*\* NCR Corporation

### Abstract

Power bus design is a critical aspect in high-speed digital circuit designs. A circuit extraction approach based on a mixed-potential integral equation formulation is presented herein to model arbitrary multilayer power bus structures including vertical discontinuities associated with surface mount (SMT) decoupling capacitor interconnects. Both conductor and dielectric losses are incorporated, and included into the first principles formulation. The agreement of modeling and measurements demonstrates its effectiveness and utilization in power bus designs.

### I. Introduction

High-speed digital circuit designs commonly use a power bus structure with two or more planes entirely devoted into power and ground. This geometry provides a high-frequency inter-plane capacitance that is effective in decoupling high-frequency noise, when bulk and surface mount technology (SMT) capacitors may be ineffective, at frequencies where the board distributed resonances dominate [1]. The design of the power bus structure, including the placement of decoupling capacitors, is an important design aspect [2], especially with higher clock frequencies, faster edge rates, and more dense circuit layouts. Simultaneous switching noise

(delta-I noise) generated by integrated circuit (IC) chips propagates on power and ground planes, resulting in interference among various circuits, and can couple to the chassis cavity as well to radiate through apertures, slots, and other radiation mechanisms. There are suggested approaches for reducing the effects of this high-frequency noise in practical designs, such as using power island structures, placement of decoupling capacitors, using high-dielectric-constant materials in the power layer, high-loss materials, *etc.* However, proven guidelines are not well established. Power bus modeling provides a more cost-effective, quick-and-easy way of performing various *what-if* scenarios that can be easily used to verify designs, as well as develop general guidelines for similar applications, compared with hardware trial-and-error. A good power-bus modeling tool should be able to handle commonly used geometries, be easily incorporated into high-speed digital designs, be accurate and fast, and have a good user interface.

A full-wave power bus modeling approach, denoted *CEMPIE*, to designate a Circuit Extraction approach based on a Mixed-Potential Integral Equation (MPIE) formulation is presented herein. Circuit models have several advantages over electromagnetic models. Their quantities are currents and voltages, which are more intuitive and easily used with other signal integrity tools than field quantities. Further,

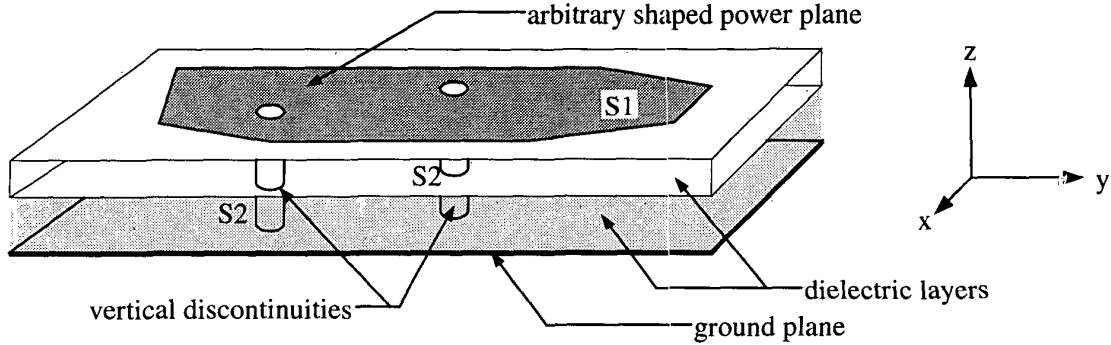


Figure 1: A typical power bus structure, with arbitrary metallization on the power layer(s).

the extracted circuit model is reusable for various frequency- and time-domain modeling. Conductor and dielectric losses can be both included in the first principles formulation. This approach is not only suitable for power bus modeling, but also easily extended to applications of planar structures with multiple planes.

## II. MPIE Formulation

The mixed-potential integral equation (MPIE) formulation used in the CEMPIE modeling is quite similar to that of a classic scattering problem. An incident electric field  $\vec{E}^{inc}$  is assumed. Then, surface currents  $\vec{J}(\vec{r})$  and charges  $\sigma(\vec{r})$  are induced on the conducting planes of concern (power planes), and on the surfaces of vertical discontinuities such as vias, in responding to the incident field. Ground planes and dielectric layers are assumed to be infinite in the modeling, and are incorporated into the Green's functions. The vector sum of the incident and induced electric fields needs to satisfy the boundary conditions on the remaining conducting surfaces, thus an electric field integral equation is derived as

$$\hat{n} \times [j\omega \int_{S1+S2} \vec{G}^A(\vec{r}, \vec{r}') \cdot \vec{J}(\vec{r}') ds' + \nabla \phi] = Z_s \hat{n} \times \vec{J}(\vec{r}), \quad (1)$$

where  $\phi$  is the induced scalar electric potential;  $S1$  refers to horizontal planes of concern; and  $S2$  refers to vertical surfaces of vias and/or ports, as shown in Figure 1;  $Z_s$  is surface impedance of conductor structures; and,  $\vec{G}^A$  is a dyadic Green's function for the vector magnetic potential. The incident electric field is assumed to be zero in (1), since the discretized problem is not solved; rather, an equivalent circuit is extracted. Therefore, the excitation (source) can be easily defined and incorporated in the circuit simulator. Conductor losses are included and characterized by the right-hand-side term in (1). At DC and low frequencies where skin depth is greater than conductor thickness, the surface resistance  $R_s$  is constant, and

$$R_s = \frac{1}{\sigma \cdot h}, \quad (2)$$

where  $\sigma$  is the conductivity of conductor structures, and  $h$  is the thickness of power planes or via walls. However, when frequency reaches the point where skin depth is smaller than conductor thickness, the surface impedance increases with square root of frequency as [3]

$$Z_{s,skin} = (1 + j) \sqrt{\frac{\pi f \mu_0}{\sigma}} \quad (3)$$

Representing the surface impedance as

$$Z_S = R_S + Z_{S,skin} \quad (4)$$

enables the characterization of both low- and high-frequency conductor-loss behaviors.

Triangular patches and rectangular patches are used to discretize the horizontal planes and the surfaces of vertical discontinuities, respectively. Vector basis functions are employed, and anchored by the interior edges of all triangular surface patches [4], while the basis functions associated with vertical rectangular cells are chosen to have the form of one-dimensional linear functions and associated only with horizontal edges of rectangles [5]. The surface currents are assumed to flow axially on the vertical surfaces, since the height of vias and ports is relatively small, normally of less than 100 mils. Using the standard Method of Moments procedure of expansion and testing, (1) becomes

$$([\mathbf{R}] + j\omega[\mathbf{L}])[\mathbf{i}] - [\mathbf{\Lambda}][\boldsymbol{\varphi}] = 0, \quad (5)$$

where  $[\mathbf{i}]$  is the branch current vector;  $[\boldsymbol{\varphi}]$  is the node (cell) scalar-potential vector;  $[\mathbf{\Lambda}]$  is the connectivity matrix relating mesh cells (circuit nodes) and edges (circuit branches);  $[\mathbf{L}]$  is the branch-wise inductance matrix; and,  $[\mathbf{R}]$  is the branch-wise resistance matrix that results from the right-hand-side of (1). Further, assuming the induced surface charge density is constant in every cell, an equation can be derived from the continuity equation, which is

$$[\mathbf{I}] + j\omega[\mathbf{K}]^{-1}[\boldsymbol{\varphi}] = -[\mathbf{I}^e], \quad (6)$$

where  $I_n$  and  $I_n^e$  are the induced current and the injected current associated with Cell  $n$ , respectively; and,  $[\mathbf{K}]^{-1}$  is the node-wise inverse capacitance matrix.

Dielectric losses can be accounted for by ascribing a complex permittivity to the material, *i.e.*,

$$\varepsilon = \varepsilon' - j\varepsilon'', \quad (7)$$

where  $\varepsilon'' = \varepsilon' \tan \delta$ , and  $\tan \delta$  is the loss tangent of the material. Values of the loss tangent are experimentally measured or given by the material manufacturer. The complex dielectric constant is used in the derivation and calculation of Green's functions. It can be shown that only the  $[\mathbf{K}]^{-1}$  matrix is affected by the imaginary part of the dielectric permittivity, and

$$j\omega[\mathbf{K}]^{-1} = \omega[\mathbf{G}_d] + j\omega[\mathbf{C}], \quad (8)$$

where the  $[\mathbf{G}_d]$  and  $[\mathbf{C}]$  matrices are both real,  $[\mathbf{G}_d]$  is a conductance matrix that results from the dielectric losses, and  $[\mathbf{C}]$  is a pure capacitance matrix.

Based on (5) and (6), a discretized form of the mixed-potential integral equation, represented by equivalent circuit elements, results

$$\begin{bmatrix} \mathbf{R} + j\omega\mathbf{L} & -\mathbf{\Lambda}^T \\ \mathbf{\Lambda} & \omega\mathbf{G}_d + j\omega\mathbf{C} \end{bmatrix} \begin{bmatrix} \mathbf{i} \\ \boldsymbol{\varphi} \end{bmatrix} = \begin{bmatrix} \mathbf{0} \\ -\mathbf{I}^e \end{bmatrix}. \quad (9)$$

This equation has a standard form of Modified Nodal Analysis that is utilized in many circuit simulators.

### III. Circuit Extraction

Equation (9) gives the nodal admittance matrix  $[\mathbf{Y}]$  of the system as

$$[\mathbf{Y}] = [\mathbf{\Lambda}^T(\mathbf{R} + j\omega\mathbf{L})^{-1}\mathbf{\Lambda}] + \omega[\mathbf{G}_d] + j\omega[\mathbf{C}]. \quad (10)$$

A circuit model can be easily extracted from this admittance matrix. To reduce the computational time, a quasi-static

approximation of the Green's functions is employed so that the filling of the moment matrix needs to be performed only once. This approximation imposes an additional mesh limitation to keep the extracted circuit valid over a given frequency range. This limitation is determined by the highest frequency of interest, layer stackup, and dielectric materials [6].

The extracted circuit model from (10) can have an extensive netlist. There is a series LR branch in parallel to a parallel CG branch between an arbitrary pair of two nodes, as well as a shunt parallel CG branch between each of the nodes and the ground node, as shown in Figure 2. For a small number of nodes with their surface currents flowing to the ground associated with the via interconnects, there is also a shunt series LR branch connecting them to the ground node. The extracted circuit is exported into SPICE where various frequency- and time-domain simulations are performed. Well-developed SPICE models for various sources, loads, transmission lines, *etc.* can be easily incorporated into the extracted circuit model.

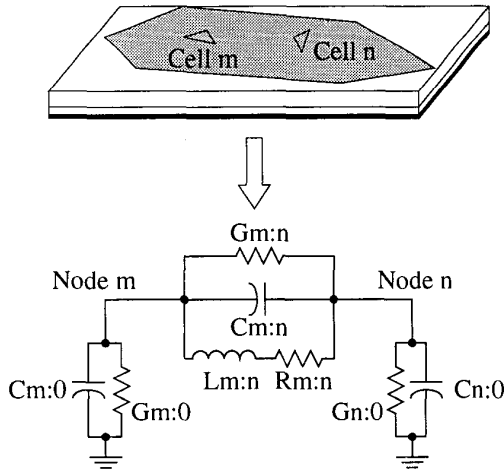


Figure 2: A circuit model between two nodes  $m$  and  $n$ , extracted from the CEMPIE formulation.

#### IV. Calculation of Green's Functions

There are two steps in the calculation of the Green's functions in a stratified medium. First, the spectral-domain expressions are derived based on the concepts of the generalized reflection and transmission coefficients [7], where dielectric layers and ground planes are assumed of infinite extent so the problem is only one-dimensional ( $z$ -direction). These spectral-domain expressions are then approximated by an expansion of complex images as [8],[9]

$$\tilde{G} = \frac{1}{2\gamma} \sum_{p=1}^M \alpha_p e^{a_p \gamma}, \quad (11)$$

where  $\gamma = jk_z$ ,  $M$  is the total number of complex images,  $\alpha_1, \dots, \alpha_M$  are complex magnitudes, and  $a_1, \dots, a_M$  are complex images. The Sommerfeld identity is used to obtain the inverse Fourier transform from spectral domain to spatial domain as [7]

$$f^{-1}\left(\frac{e^{-jk_z|z|}}{2jk_z}\right) = \frac{e^{-jk_r r}}{4\pi r}. \quad (12)$$

Then, the desired spatial-domain expressions of Green's functions are determined from (11) and (12) as

$$G = \sum_{p=1}^M \alpha_p \frac{e^{-jk_p \sqrt{x^2 + y^2 + a_p^2}}}{4\pi \sqrt{x^2 + y^2 + a_p^2}}.$$

Several numerical methods have been developed to approximate a spectral-domain Green's function into a series of complex images, such as the original Prony's method [8], and the least-square Prony's method. Prony's methods are known for their high sensitivity to noise. The generalized pencil of function (GPOF) method was then introduced to improve the performance. It was observed,

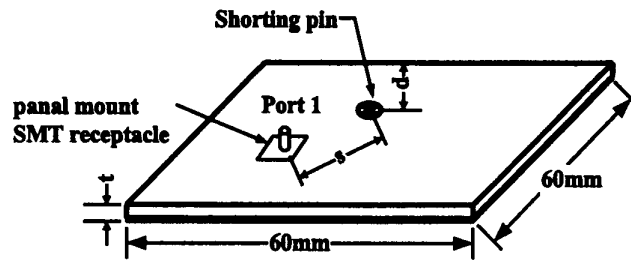


Figure 3: A power bus test geometry.

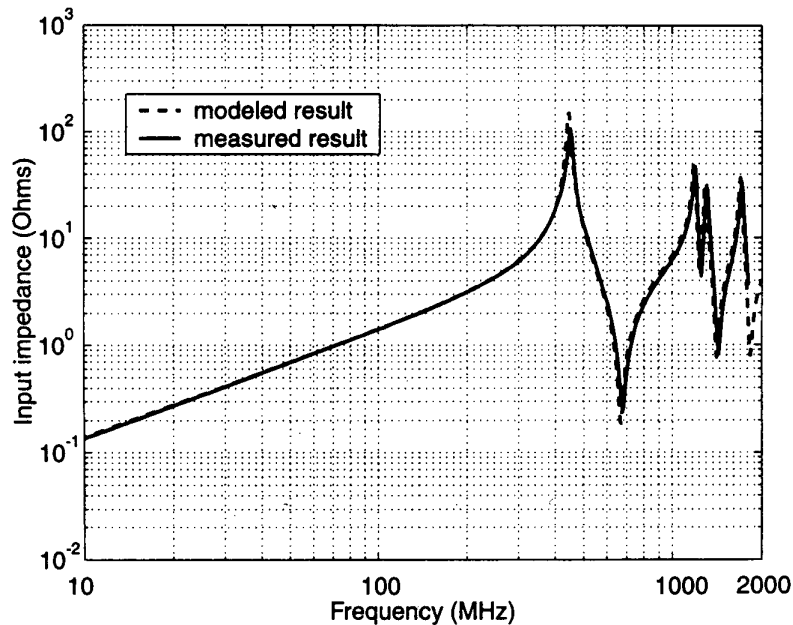


Figure 4: Comparison of modeled and measured results for the power bus structure shown in Figure 3.

however, that the GPOF method was not robust for slowly converging rapidly changing functions. A further improvement to the GPOF method, denoted the two-level approach [9], is used in the CEMPIE modeling described in this work.

## V. Power Bus Modeling

The CEMPIE modeling approach was demonstrated by comparison with experiment. Figure 3 illustrates a test-board geometry, which was a two-layer printed circuit board (PCB) with two solid planes representing power and ground planes,

respectively. The PCB was fabricated using FR-4 dielectric material with a dielectric constant of 4.7, and loss tangent of  $\tan\delta=0.02$ . The layer thickness was 43 mils. There were two vertical discontinuities. One was a shorting post connecting two planes together, and the other was an SMA test probe. The input impedance at the test port was measured using an HP4291A impedance analyzer. The reference plane was located at the input port of the test geometry. The modeled results are compared with the measurements in Figure 4. Good agreement is demonstrated up to 1.8 GHz, which is the maximum frequency of the impedance analyzer. Other  $|S_{21}|$

measurements showed that CEMPIE modeled results agreed well with measurements up to 5 GHz, provided that the additional mesh limitation discussed previously was satisfied.

## VI. Conclusion

The CEMPIE modeling approach provides a useful and powerful tool in designing power bus structures, and predicting power bus noise distribution. Measurements demonstrate the effectiveness of the modeling. It can also be used to model many SI problems, IC packaging problems and other applications with multi-layer geometry.

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