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Abstract—**A novel approach of equivalent circuit model extraction is developed for modeling of integrated package and PCB power distribution networks (PDN). The integrated PDNs are formulated from a full-wave finite-difference algorithm, and the resulting matrix equations are converted to equivalent circuits. The equivalent circuits, as well as the decoupling capacitors and the attached circuit components, can be analyzed with a SPICE-like solver in both the time and frequency domains. The modeling of dielectric loss is also addressed. The method is used to model three PDN problems including a simple power bus, a BGA package mounting on a PCB, and a 3-D power bus structure. The results are compared to either measurement data or other numerical results. The limitations of the method are also discussed.**

Keywords—*equivalent circuit; power dilivery network; FDTD; SPICE*

I. INTRODUCTION

A good PDN design is an essential issue to ensure the performance of high-speed systems. Since full-wave tools are not computationally efficient, and cannot handle easily active devices or nonlinear components, SPICE compatible circuit models of the system-level PDN are desired. Methods of extracting a circuit model, e.g., cavity model [1], PEEC method [2], parallel-plate transmission line model [3], etc., are widely used for PDN analysis. However, the applicability of these methods to complex structures, e.g., interconnections between a package and a PCB, is limited by either the large number of extracted circuit components or the simulation inaccuracy due to the lumped approximation of complex structures for high-speed design. In this paper, an equivalent circuit model extraction approach is given [4]. The finite-difference algorithm is employed to formulate the PDNs, and the resulting matrix equations are reformulated to derive an equivalent circuit network, which is SPICE compatible. In Section II, the formulation of an equivalent circuit extraction based on the finite-difference algorithm is derived in detail. A 2-D example is presented. In Section III, the formulation is applied to three problems, e.g., a simple two-layer power bus, a BGA package mounted on a PCB, and a 3-D power bus structure, to investigate the effectiveness and limitations of the proposed method. In Section IV, the limitations of the method are discussed. Finally, conclusions are drawn in Section V.

II. METHODOLOGY OF THE EQUIVALENT CIRCUIT EXTRACTION

The finite-difference formulation can be applied to frequency-domain modeling, as well as time-domain modeling (FDTD). The frequency-domain Maxwell's equations in the integral form are,

$$\oint_l \bar{\mathbf{H}} \cdot d\bar{l} = \int_s \left[(j\omega\varepsilon + \sigma)\bar{\mathbf{E}} + \bar{\mathbf{J}} \right] \cdot d\bar{\mathbf{S}} \, ,$$
$$\oint_l \bar{\mathbf{E}} \cdot d\bar{l} = -\int_s j\omega\mu\bar{\mathbf{H}} \cdot d\bar{\mathbf{S}} \tag{1}$$

and can be discretized using central differences and staggered spatial grids as,

$$\begin{cases} \mathbf{Q}_{(n\times m)}\mathbf{l}_{h,(m\times m)}\mathbf{H}_{(m\times 1)} = j\omega\mathbf{M}_{\varepsilon,(n\times n)}\mathbf{S}_{e,(n\times n)}\mathbf{E}_{(n\times 1)} \\ \mathbf{Q}^{\mathrm{T}}_{(m\times n)}\mathbf{l}_{e,(n\times n)}\mathbf{E}_{(n\times 1)} = -j\omega\mathbf{M}_{\mu,(m\times m)}\mathbf{S}_{h,(m\times m)}\mathbf{H}_{(m\times 1)} \end{cases} \tag{2}$$

For simplicity, assume that the computational domain is a source-free region with only lossless media, and the mesh is uniform, i.e., all the cells have the same size (Δx by Δy by Δz). All the discretized E-field components as well as the H-field components are collected into one-dimensional vectors. The discretized H-fields and E-fields loop integral operators are represented with matrices $\mathbf{Q}$ and $\mathbf{Q}^{\mathrm{T}}$, respectively. $\mathbf{Q}$ is a highly sparse matrix filled with +1 and -1. For each row of the matrix, the non-zero elements give the geometry connection of the cell edges, and the positive and negative signs indicate that the direction of the related field component is the same as or opposite to the direction of the loop integral. The duality of Maxwell's equations ensures that $\mathbf{Q}$ and $\mathbf{Q}^{\mathrm{T}}$ have a transpose relation. $\mathbf{l}_{e,(n\times n)}$ and $\mathbf{l}_{h,(m\times m)}$ are n^{th} -order and m^{th} -order diagonal matrices that give the lengths of the integral path for all the E-field and H-field components, i.e., the physical length of the edges of the cells, as

$$\mathbf{l}_{e,(n\times n)} = \mathrm{diag}(\Delta x, \Delta y, \Delta z, \Delta x, \Delta y, \Delta z, \ldots, \Delta x, \Delta y, \Delta z) \tag{3}$$

$$\mathbf{l}_{h,(m\times m)} = \mathrm{diag}(\Delta x, \Delta y, \Delta z, \Delta x, \Delta y, \Delta z, \ldots, \Delta x, \Delta y, \Delta z). \tag{4}$$

The surface integral operators for the E-field components and H-field components are discretized as diagonal matrices

$\mathbf{S}_{e,(n\times n)}$ and $\mathbf{S}_{h,(m\times m)}$, respectively. $\mathbf{S}_{e,(n\times n)}$ and $\mathbf{S}_{h,(m\times m)}$ give the areas of the integral surfaces, which have the form

$$\mathbf{S}_{e,(n\times n)} = \mathrm{diag}(\Delta y\Delta z, \Delta x\Delta z, \Delta x\Delta y, \Delta y\Delta z, \ldots, \Delta y\Delta z, \Delta x\Delta z, \Delta x\Delta y) \quad (5)$$

$$\mathbf{S}_{h,(m\times m)} = \mathrm{diag}(\Delta y\Delta z, \Delta x\Delta z, \Delta x\Delta y, \Delta y\Delta z, \ldots, \Delta y\Delta z, \Delta x\Delta z, \Delta x\Delta y). \quad (6)$$

$\mathbf{M}_{\varepsilon}$ and $\mathbf{M}_{\mu}$ are the diagonal matrices defining the material properties, which have the form

$$\mathbf{M}_{\varepsilon,(n\times n)} = \mathrm{diag}(\varepsilon_{1,x}, \varepsilon_{1,y}, \varepsilon_{1,z}, \varepsilon_{2,x}, \varepsilon_{2,y}, \varepsilon_{2,z}, \ldots, \varepsilon_{n,x}, \varepsilon_{n,y}, \varepsilon_{n,z}) \quad (7)$$

$$\mathbf{M}_{\mu,(m\times m)} = \mathrm{diag}(\mu_{1,x}, \mu_{1,y}, \mu_{1,z}, \mu_{2,x}, \mu_{2,y}, \mu_{2,z}, \ldots, \mu_{m,x}, \mu_{m,y}, \mu_{m,z}). \quad (8)$$

The vector $\mathbf{H}_{(m\times 1)}$ from the second equation in (2) can be solved as

$$-\frac{1}{j\omega}\mathbf{M}_{\mu,(m\times m)}^{-1}\mathbf{S}_{h,(m\times m)}^{-1}\mathbf{D}_{(m\times n)}^{T}\mathbf{l}_{e,(n\times n)}\mathbf{E}_{(n\times 1)} = \mathbf{H}_{(m\times 1)}. \quad (9)$$

By substituting (9) to the first equation in (2), the vector $\mathbf{H}_{(m\times 1)}$ is eliminated. The resulting equation is

$$\left[j\omega\mathbf{l}_{e,(n\times n)}^{-1}\mathbf{M}_{\varepsilon,(n\times n)}\mathbf{S}_{e,(n\times n)} + \mathbf{Q}_{(n\times m)}\left(j\omega\mathbf{l}_{h,(m\times m)}^{-1}\mathbf{M}_{\mu,(m\times m)}\mathbf{S}_{h,(m\times m)}\right)^{-1}\mathbf{Q}_{(m\times n)}^{T}\right]\mathbf{l}_{e,(n\times n)}\mathbf{E}_{(n\times 1)} = 0 \quad (10)$$

Since the matrix $\mathbf{l}_{e,(n\times n)}^{-1}\mathbf{M}_{\varepsilon,(n\times n)}\mathbf{S}_{e,(n\times n)}$ has units of capacitance, and $\mathbf{l}_{h,(m\times m)}^{-1}\mathbf{M}_{\mu,(m\times m)}\mathbf{S}_{h,(m\times m)}$ has the unit of inductance, they are renamed as

$$\mathbf{C} = \mathbf{l}_{e,(n\times n)}^{-1}\mathbf{M}_{\varepsilon,(n\times n)}\mathbf{S}_{e,(n\times n)} = \mathrm{diag}(C_{1,x} \quad C_{1,y} \quad C_{1,z} \quad C_{2,x} \quad \ldots\ldots \quad), \text{ and}$$

$$\mathbf{L} = \mathbf{l}_{h,(m\times m)}^{-1}\mathbf{M}_{\mu,(m\times m)}\mathbf{S}_{h,(m\times m)} = \mathrm{diag}(L_{1,x} \quad L_{1,y} \quad L_{1,z} \quad L_{2,x} \quad \ldots\ldots).$$

Then, (10) can be rewritten as

$$\left[j\omega\mathbf{C} + \mathbf{Q}(j\omega\mathbf{L})^{-1}\mathbf{Q}^{T}\right]\mathbf{V} = 0. \quad (11)$$

A passive equivalent L-C circuit network can be generated according to (11). The proposed method has the potential to model not only simple 2-D power bus structures, but also 3D complex structures, e.g., interconnections between a BGA and a PCB, etc. The extracted circuit model is a full-wave model equivalent.

The dielectric loss can play a significant role on degrading the signals. For a lossy dielectric media, the dielectric constant is a complex number, and the imaginary part defines the loss. The dielectric loss can be modeled as frequency dependant resistors. Since the real part of the dielectric constant is associated with a shunt capacitor to ground, the imaginary part can be associated with a resistor, and the resistance is inversely proportional to frequency. The capacitor and the resistor are in parallel. The loss of a dielectric is often given as the loss tangent as

$$\varepsilon = \varepsilon' - j\varepsilon'' = \varepsilon' - j\varepsilon'\tan\delta. \quad (12)$$

With (12), (11) can be rewritten as

$$\left[j\omega\mathbf{C} + \mathbf{R}^{-1} + \mathbf{D}(j\omega\mathbf{L})^{-1}\mathbf{D}^{T}\right]\mathbf{V} = 0, \quad (13)$$

where R is defined as

$$\mathbf{R} = \frac{1}{\omega}\mathrm{diag}\left(\frac{\Delta y\Delta z}{\varepsilon_{1,x}\tan\delta\Delta x} \quad \frac{\Delta y}{\varepsilon_{1,y}\tan\delta\Delta x\Delta z} \quad \frac{\Delta z}{\varepsilon_{1,z}\tan\delta\Delta x\Delta y} \quad \frac{\Delta x}{\varepsilon_{2,x}\tan\delta\Delta y\Delta z} \quad \ldots \ldots\right) \quad (14)$$

In this fashion, the dielectric loss can be represented with frequency-dependent resistors in parallel with the shunt capacitors at every node.

A 2-D FDTD model is used as an example to illustrate the process of generating the equivalent circuit from the derived equations. The model is shown in Figure 1. The circuit connections for E-field components, E_n and E_m, are investigated. For convenience, only the relevant E-field and H-field components are labeled. Assume that the mesh is uniform and that all the cells are square with the length of the edge equal to Δl. The boundary conditions are set as perfect electric conductors (PEC), i.e., all the tangential E-Field components on the boundary are zero.
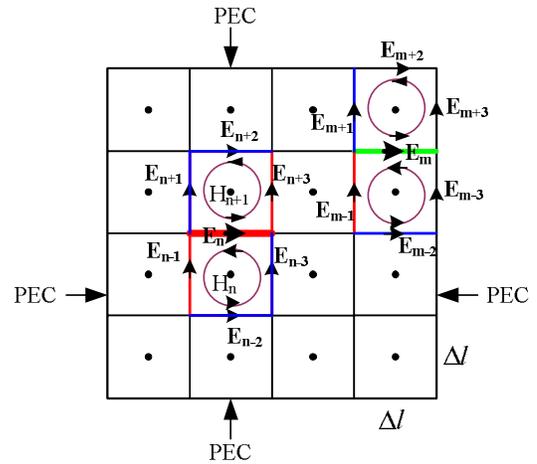

Figure 1. Top view of a simplified 2-D example used for illustration of the equivalent circuit generation for node E_n and E_m.

The update equations for E_n are

$$\begin{cases} j\omega\varepsilon E_n = \frac{1}{\Delta l}\begin{bmatrix} -1 & 1 \end{bmatrix}\begin{bmatrix} H_n \\ H_{n+1} \end{bmatrix} \\[2em] j\omega\mu\begin{bmatrix} H_n \\ H_{n+1} \end{bmatrix} = -\frac{1}{\Delta l}\begin{bmatrix} 1 & 1 & -1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & -1 & 1 \end{bmatrix}\begin{bmatrix} E_{n-3} \\ E_{n-2} \\ E_{n-1} \\ E_n \\ E_{n+1} \\ E_{n+2} \\ E_{n+3} \end{bmatrix} \end{cases}. \quad (15)$$

The KCL equation for voltage at node n can be obtained by substituting one equation into another to eliminate the H-filed vector as

$$j\omega C V_n + (j\omega L)^{-1}\begin{bmatrix} -1 & -1 & \mathbf{1} & 2 & -1 & -1 & \mathbf{1} \end{bmatrix}\begin{bmatrix} V_{n-3} \\ V_{n-2} \\ V_{n-1} \\ V_n \\ V_{n+1} \\ V_{n+2} \\ V_{n+3} \end{bmatrix} = 0 \quad , \quad (16)$$

where $V_{n+j} = E_{n+j}\Delta l$, $j = -3, -2,..., 2, 3$, $C = \varepsilon\Delta l$, and $L = \mu\Delta l$. Equation (16) can be further rewritten as

$$j\omega C V_n + \frac{1}{j\omega}\left(\begin{array}{l} \dfrac{V_n - V_{n-3}}{L} + \dfrac{V_n - V_{n-2}}{L} + \dfrac{V_n - V_{n-1}}{-L} + \\[2mm] \dfrac{V_n - V_{n+1}}{L} + \dfrac{V_n - V_{n+2}}{L} + \dfrac{V_n - V_{n+3}}{-L} \end{array}\right) = 0 \cdot \quad (17)$$

The circuit can be generated according to (17), as shown in Figure 2 (a).

(a) Node V_n (b) Boundary node V_m

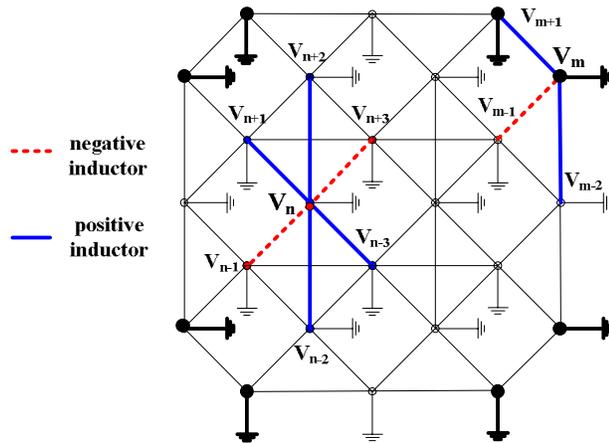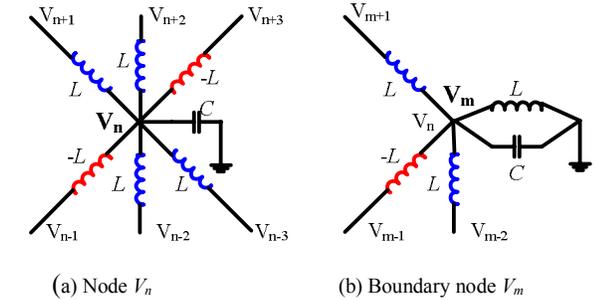(c) The schematic representation of the entire equivalent circuit

Figure 2. 2-D equivalent circuit for, (a) node V_n, (b) boundary node V_m, and (c) the schematic representation of the entire equivalent circuit.

For nodes adjacent to the PEC boundary, e.g., E_m in this case, the KCL equation can be derived as

$$j\omega C V_m + \frac{1}{j\omega}\left(\frac{V_m - V_{m-2}}{L} + \frac{V_m - V_{m-1}}{-L} + \frac{V_m - V_{m+1}}{L} + \frac{V_m}{L}\right) = 0 \cdot \quad (18)$$

The equivalent circuit is shown in Figure 2 (b). Note that the tangential E-field components, e.g., E_{m-3}, E_{m+2} and E_{m+3} are zero due to the PEC boundary conditions. In this circuit, there is one inductor connected to the ground due to the PEC boundary conditions, which corresponds to the term V_m/L in (18). The entire equivalent circuit of this problem is shown in Figure 2 (c). For simplicity, the elements on the circuit branches are omitted. The highlighted parts of the network represent the circuit connections of the node V_n and the boundary node V_m. Eight bold dots at the four boundary corners

represent boundary nodes that have a capacitor in parallel with an inductor to the ground according to the formulations.

The equivalent circuit for a 3D FDTD model, as shown in Figure 3, can be extracted in the same fashion. The KCL equation is derived as

$$j\omega C_y V_{y2} + \frac{1}{j\omega}\left\{\begin{array}{l} \dfrac{V_{y2} - V_{x1}}{-L_z} + \dfrac{V_{y2} - V_{x2}}{L_z} + \dfrac{V_{y2} - V_{x3}}{L_z} + \dfrac{V_{y2} - V_{x4}}{-L_z} \\[2mm] + \dfrac{V_{y2} - V_{z1}}{-L_x} + \dfrac{V_{y2} - V_{z2}}{L_x} + \dfrac{V_{y2} - V_{z3}}{L_x} + \dfrac{V_{y2} - V_{z4}}{-L_x} \\[2mm] + \dfrac{V_{y2} - V_{y1}}{L_x} + \dfrac{V_{y2} - V_{y3}}{L_x} + \dfrac{V_{y2} - V_{y4}}{L_z} + \dfrac{V_{y2} - V_{y5}}{L_z} \end{array}\right\} = 0 \quad .(19)$$

The detailed equation derivation is omitted here. Note that all the inductors in the equivalent circuit are uncoupled according to the formulations. However, a portion of inductors have negative values, as marked with $-L$ in the figure.
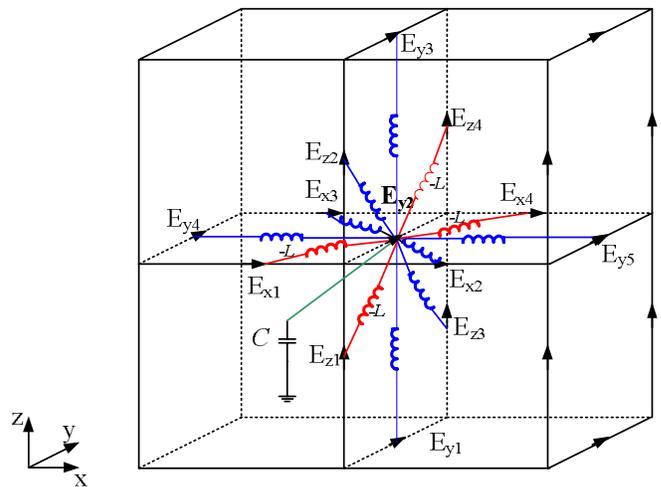

Figure 3. 3-D equivalent circuit for voltage node V_{y2}.

III. NUMERICAL SIMULATIONS AND EXPERIMENTAL VALIDATIONS

The proposed method was applied to three structures to assess its effectiveness and limitations.

A. Application to simple power bus structures

The proposed method is well-suited for power bus modeling. Figure 4 shows a typical two-layer power bus structure. TABLE I gives the model geometries, parameters of the dielectric material, and the port locations. The two parallel sheets were modeled as PECs. Perfect magnetic conductor boundary conditions were applied to the four vertical boundary surfaces. For simplicity, the whole structure was discretized as identical cubic cells, and only one layer of cells was used to model the dielectric. The dimension of the discretized cells is 2 mm by 2 mm by 2 mm. Based on the proposed method, the extracted equivalent circuit contains 546 nodes and 2137 elements of R, L, and C. To eliminate inductor loops, a small-value dummy resistor is added to each inductor branch.
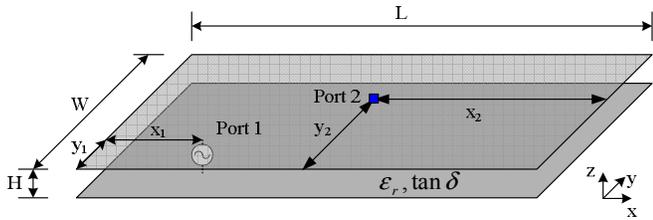
Figure 4. Schematic of a two-layer power bus structure modeled with the proposed FDTD-SPICE method.

TABLE I.   PARAMETERS OF THE POWER BUS

Conductor plane (cm)			Port location (cm)				Dielectric properties	
			Port 1		Port 2			
L	W	H	x_1	y_1	x_2	y_2	ε_r	$\tan\delta$
5.2	4.2	0.2	2.1	1.1	3.1	2.1	4.2	0.02

The result of the transfer impedance between Port 1 and Port 2 is compared to the result from the cavity model using 20 by 20 modes, as shown in Figure 5. The solver time using HSPICE for 200 frequency points is less than five seconds, which is also comparable to the cavity model. Good agreement is achieved up to 5 GHz. At high frequencies, there is a small frequency shift at the resonances, which is probably related to the numerical dispersion caused by the spatial discretization of the FDTD model. A step response at Port 1 was performed using the equivalent circuits extracted with the cavity model and the FDTD-SPICE method.
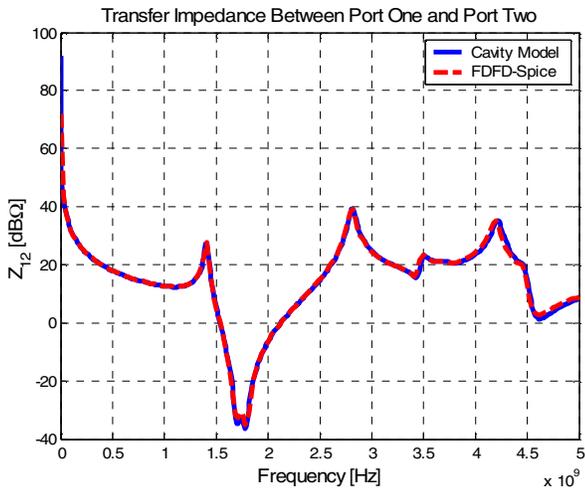

Figure 5. Comparison of the transfer impedance between Port 1 and Port 2 simulated with the cavity model method and the FDTD-SPICE algorithm.

B. Application to package/PCB PDN interactions

The proposed method was further extended to simulate the interactions between the power delivery networks of a BGA package mounted on a PCB. The geometry detail of the measurement setup is shown in Figure 7. The two-layer PCB is 10 cm × 8 cm with a BT substrate of 0.7 mm thickness. The BGA package consists of four copper layers with a BT substrate, and the dimensions of 27 mm × 27 mm.
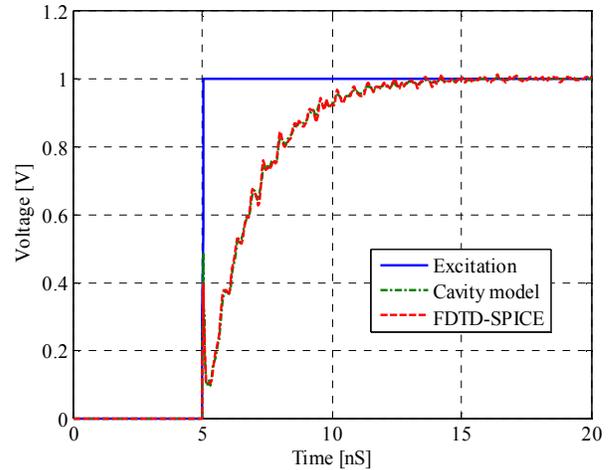

Figure 6. Comparison of the step response at Port 1 up to 20 ns simulated with the cavity model method and the FDTD-SPICE algorithm.

The top layer is for signal routing and power/ground rings, and bottom layer is for soldering balls. The second layer and the third layer are ground and power planes, respectively, with a 0.15mm BT substrate. The PDN of the BGA package is electrically connected with that of the PCB by 16 pairs of solder balls. To evaluate the impedance characteristics of the power distribution system, S_{21} was measured and simulated at the locations of Port 1 and Port 2, as shown in Figure 7. The measurement was performed with a vector network analyzer (HP8510C) from 50 MHz to 5 GHz along with a Cascade Microtech probe station.
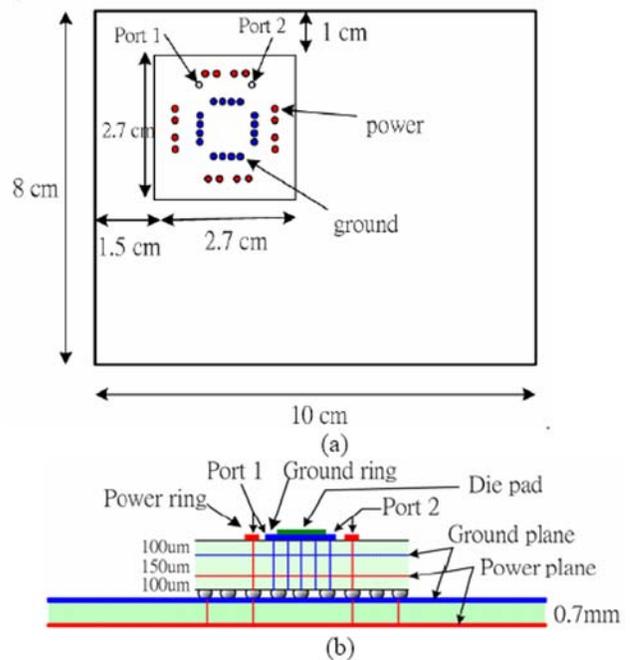

Figure 7. Geometry of the BGA package mounted on the PCB, (a) top view and (b) side view.

The comparison of the measurement and simulation results is shown in Figure 8. For the present model, the package and PCB PDNs were modeled as 2-D power buses, and the equivalent circuits of the package and PCB PDNs were extracted with the proposed FDTD-SPICE method. The interconnecting solder balls and vias were approximated with lumped inductors for simplicity. Up to 2GHz, there is a general good agreement between the measurement and simulation results.
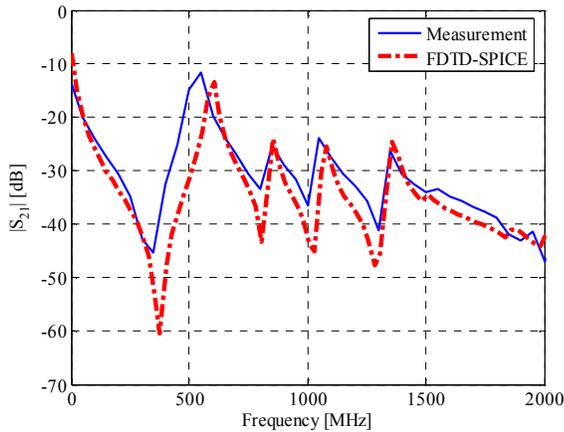

Figure 8. Comparison of the simulation result and the measurement result.

C. Application to 3D power bus structures

A simple 3-D power bus structure, as shown in Figure 9, was used to evaluate the capability and limitations of the FDTD-SPICE on the modeling of 3D structures. The structure consists of three metallic sheets. There is a 2 cm by 2 cm hole on the second metallic sheet, so there is signal coupling between the top and bottom cavities. Two ports were defined as shown in the figure. The input impedance at Port 1, and the transfer impedance between Port 1 and Port 2 were simulated and compared with 3-D full-wave simulation results.

Figure 10 shows the comparison of the input impedance simulated with the FDTD-SPICE method and a commercial FEM solver. From 50 MHz to 5GHz, the result from the FDTD-SPICE method matches with the FEM results very well. However, below 50 MHz, the FDTD-SPICE results demonstrate a second-order inductive behavior instead of a capacitive behavior, as shown in the figure at the lower-right corner of Figure 10. The reason for this discrepancy is that with PEC boundary conditions, the equivalent circuit has inductors connected to the ground. At DC, they form a short circuit. The details will be discussed in the next section. Figure 11 compares the transfer impedance between Port 1 and Port 2 simulated with the FDTD-SPICE method and the FEM solver. A general good match can be seen below 3.5 GHz. Beyond 3.5 GHz, there is a significant frequency shift between two curves. The reasons may be that the mesh around the hole edges at the second metallic sheet is not sufficient to account for the rapid field variations at high frequency. Moreover, the mesh dimension in the *z*-direction is 2 mm, which is also not sufficient especially around the hole-region. Again, the low frequency behavior is incorrect as cited above.
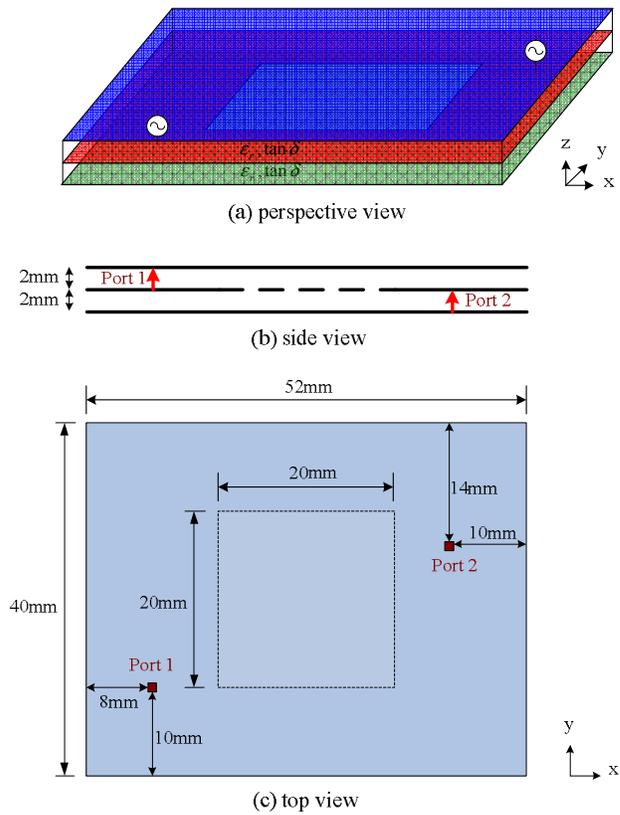

Figure 9. Schematic of a 3-D test structure, (a) perspective view, (b) side view, and (c) top view.
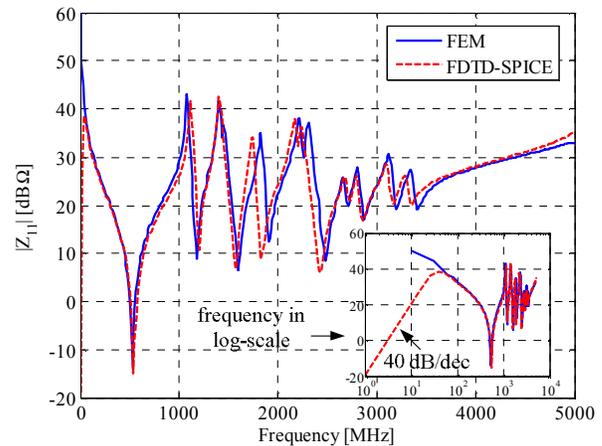

Figure 10. Comparison of the input impedance at Port 1 simulated with the FDTD-SPICE method and commerecial FEM solver.
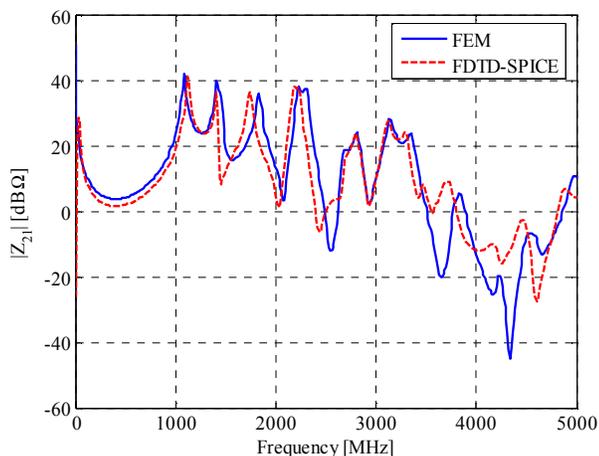
Figure 11. Comparison of the transfer impedance between Port 1 and Port 2 simulated with the FDTD-SPICE method and commerecial FEM solver.

IV. DISCUSSION

Theoretically the proposed method is suitable for any problems that a full-wave FDTD solver can handle. But practically this is not true because of referencing issues when converting full-wave problems into equivalent circuit problems, the limitations of a SPICE solver, etc.

A referencing problem occurs during the conversion of the 3-D electromagnetic models into equivalent circuit models with PEC boundary conditions for the proposed FDTD-SPICE method. 3-D electromagnetic models take the infinity as the zero potential or ground reference. Since the tangential E-field components are zero with PEC boundary conditions, practically the FDTD-SPICE treats the PEC as the zero potential, which is not correct. The consequence is that if an inductor connects two adjacent E-field nodes, but one E-field node vanishes because of PEC boundary conditions, then the inductor connects the other E-field node to the ground. This referencing problem leads to incorrect simulation results at low frequencies as shown in the previous section. The formulation with PEC boundary conditions and the resulting equivalent circuit for a 2-D example are shown in Section II. The referencing problem for a 3-D structure can be illustrated with Figure 3. Suppose the top and bottom planes are PECs, then E_{y1} and E_{y3} are zero. Two inductors that connect E_{y2} to E_{y1} and E_{y3} now connect E_{y2} to the ground in parallel. If the two

inductors have the same values but opposite signs, they effectively cancel each other, which is the case for 2-D power buses. So for the 2-D example shown in Section II, although there are two PECs at top and bottom, there are not inductors connected to the ground in parallel.

The number of elements easily handled by a SPICE solver also limits the usage of the FDTD-SPICE method. A full-wave electromagnetic field solver can easily handle millions of electric and magnetic field components, but it is very difficult for a SPICE solver to manipulate a circuit with more than 100,000 elements due to the large size of the resulting matrix. However, with the help of non-uniform meshing techniques, this problem can be minimized to some extent. Moreover, the proposed method can also benefit significantly from model order reduction techniques.

The negative inductor, which is inevitable due to the formulation, may cause instability problems in the time-domain simulations as well.

V. CONCLUSION

The proposed FDTD-SPICE method can be used to extract the equivalent circuits of complex 3-D structures with a full-wave finite-difference formulation. This method allows users to analyze complex power delivery networks with a SPICE solver at a full-wave equivalent accuracy. Three power delivery network structures were modeled to validate the formulation. Good agreement was achieved between the FDTD-SPICE method, full-wave simulation results, and measurements. The limitations of the method were also discussed. Further work is needed to tackle these limitations.

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