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Abstract

DC power-bus modeling in high-speed digital design using the FDTD method is reported herein. The dispersive media is approximated by a Debye model to account for the loss. A wide band frequency response (*100 MHz - 5 GHz*) is obtained through a single FDTD simulation. Favorable agreement is achieved between the modeled and measured results for a typical DC power-bus structure with multiple SMT decoupling capacitors mounted on the board. The FDTD tool is then applied to investigate the effects of local decoupling on a DC power-bus. The modeled results agree with the results from another modeling tool, the CEMPIE (a circuit extraction approach based on a mixed-potential integral equation formulation) method.

I. Introduction

A DC power-bus structure in a multi-layer printed circuit board (PCB), which employs multiple planes as DC power and ground, is a common scenario in high-speed digital circuits. Surface-mount technology (SMT) decoupling capacitors are often placed in proximity to high speed switching devices to mitigate simultaneous switching noise, and reduce the RF noise propagation on the power plane [1], [2]. A reliable power-bus model is a powerful tool that can be integrated into the design procedure to provide design insight, and can be used for developing design guidelines. Several methods have been applied to power bus modeling. The simplest one is the lumped element model, which considers the power bus as a parallel-plane capacitor, and works well at frequencies below board resonance frequencies [1]. For higher frequencies, an appropriate method utilizes the wire-antenna and radial transmission-line modeling to take into account the distributed behavior of the power bus [3]. Traditional full-wave numerical solvers include the finite element method (FEM) [4], and finite-difference-time-domain (FDTD) [5]. Another class of modeling approaches are extracted equivalent-circuit models, in particular, partial element equivalent circuit (PEEC) method [6], and a circuit extraction based on a mixed-potential integral equation (CEMPIE) method [7]. The FDTD and the CEMPIE methods are used in this study.

In Section II, a sample board is modeled using the FDTD method. It is a two-layer structure with a power plane and a ground plane, and sixteen SMT decoupling capacitors are placed uniformly on the board. In the next section, the FDTD method is applied to investigate the effect of local decoupling on DC power-bus design. The modeled results are compared with the results obtained from the CEMPIE method.

II. FDTD modeling of a sample board with dispersive media

A sample two-layer board was built to mimic a simple two-layer DC power-bus structure as shown in Fig. 1. The board was a *150 mm × 200 mm* double-sided PCB, and the dielectric was *1.65-mm (65- mil.)* FR4 material. Sixteen decoupling capacitors were uniformly distributed over the board. One end of each decoupling capacitor was soldered directly to the top plane, while the other end was connected to the bottom plane by a short piece of *AWG 24* wire. Two test ports were built on the board using semi-rigid coaxial cables. The outer shield of these cables was soldered to the ground plane with a 360-degree connection, and the center conductors were extended through the thickness of the board and soldered to the power plane. A two-port measurement was conducted using an *HP 8753D* network analyzer. Prior to the measurement, a full-path two-port calibration was performed to remove the effects of the semi-rigid coaxial cables and set the reference plane of the measurement at the ground plane of the test board.

To model this particular board, the traditional frequency-domain methods (MoM, FEM, PEEC, CEMPIE, etc.) are suitable candidates, as well as the FDTD technique. However, for more complex designs of PCB's, e.g., boards with a significant number of SMT capacitors, or boards with segmented power or ground planes, the unknowns for traditional

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frequency-domain methods may increase significantly. The FDTD method has the advantage of allowing for more complicated layouts to be modeled without increasing the computational domain or burden. In addition, extending the method to three or more layer structures is straightforward. Another advantage is that broad-band spectrum is often preferred for power-bus design studies, and this can be done with one FDTD simulation.

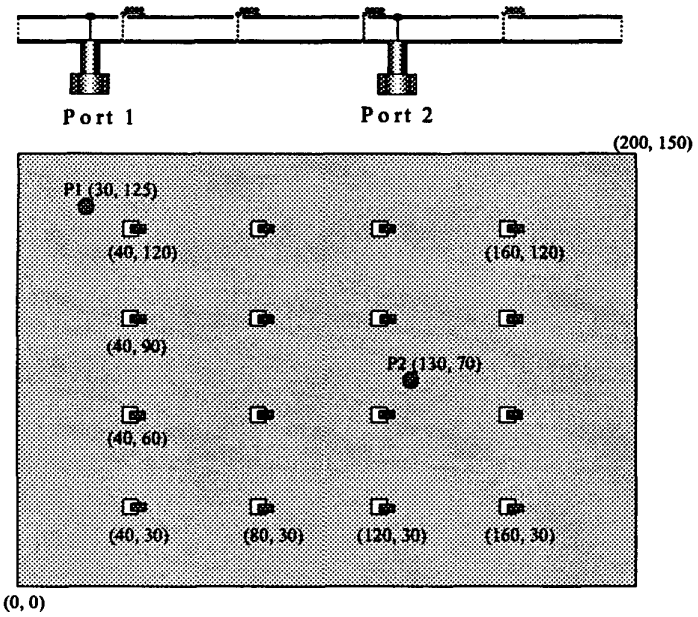

Fig. 1. Schematics of the test board – side view and top view. All dimensions are in mm.

The sample board was modeled with the FDTD method using a uniform mesh size of *1 mm × 1 mm × 0.055 mm (x, y, z)*. A sinusoidally modulated Gaussian *50 Ω* voltage source was used in the simulation. The power plane and the ground plane were modeled as perfect electric conductors (PECs) of zero thickness. Eight perfectly matched layers (PML) were placed at each boundary plane of the computational domain, and seven white-space layers were placed between the PML and the test board. Each SMT decoupling capacitor was modeled by an ideal capacitor in series with an effective series resistor. The nominal capacitance used was *9 nF* and the resistance was *130 mΩ*. These values were determined by an impedance measurement on one SMT component using an *HP 4291A* impedance/material analyzer. By including the leading wires of the capacitor in the modeling, the parasitic inductance of the SMT capacitor interconnect was taken into account. The algorithm for incorporating a capacitor or a resistor sub-cell in the FDTD modeling can be found in [9].

The dielectric loss has a dominant effect on the Q value of the PCB at higher frequencies, and it was necessary to include it in the numerical modeling. A simple FDTD approach describes the frequency dependence of the media by a constant real value of effective conductivity, which can only model the dielectric loss within a rather narrow frequency range. Multiple simulations are required to generate the results of a wide bandwidth, which is time-consuming. An approach using recursive convolution of constitutive parameters in the time domain and corresponding field components for linear isotropic frequency-dependent complex permittivity was applied [8]. The behavior of the FR-4 material (in the frequency range of *100 MHz* to *5 GHz*) was approximated using the Debye model [10]:

$$\varepsilon_r = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1 + j\omega\tau_r} - \frac{j\sigma_e}{\omega\varepsilon_0},$$

where ε_∞ is the "optic" dielectric constant, ε_s is the "static" dielectric constant, τ_r is the relaxation time, and σ_e is conductivity of the dielectric. The Debye parameters were determined by setting the loss tangent as *0.022* at *500 MHz* and *0.025* at *5 GHz*, which yields good agreement of loss tangent between the result from the Debye model and that from measurements for the frequency range of interest.

The FDTD method described above was then applied to model the test board shown in Fig. 1. The modeled and measured results ($|S_{11}|$ and $|S_{21}|$) are shown in Fig. 2. Good agreement was achieved in a wide bandwidth from *100 MHz to 5 GHz* by a single FDTD simulation.

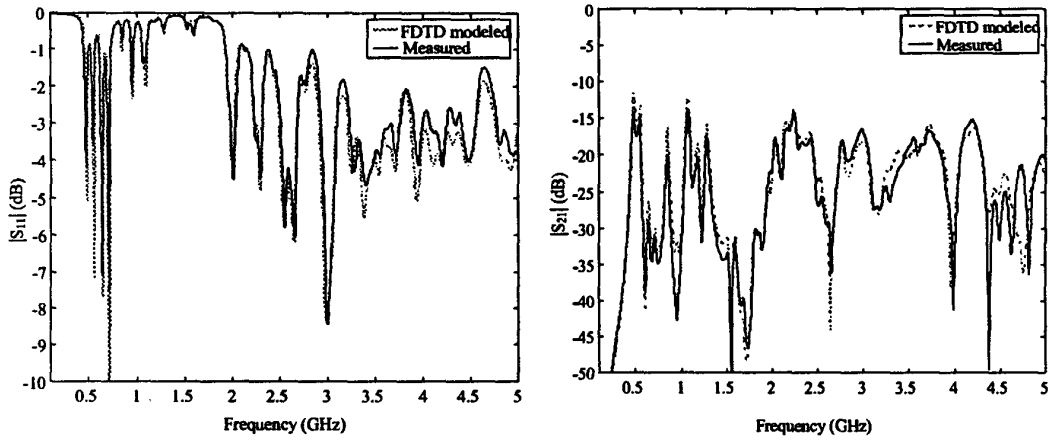

Fig. 2. Measured and FDTD modeled $|S_{11}|$ and $|S_{21}|$ of the test board.

III. Application of the numerical modeling

At high frequencies, the parasitic self inductance of the decoupling capacitor dominates the electrical performance, and the capacitor itself can not provide a low impedance path for bypassing of the noise current on the power-bus. However, a decoupling capacitor placed close to an IC can be tightly coupled to the power pins of the IC as a result of mutual inductance between the vias of the IC and the decoupling capacitor. This mutual inductance works as a current divider over a wide frequency range, and it reduces the power-bus noise magnitude. This effect of locally placed decoupling capacitors was investigated using both FDTD and the CEMPIE method. A more detailed study on quantifying the decoupling capacitor location can be found in [11].

A *152.4 mm × 228.6 mm (6" × 9")* two-layer PCB with *1.118-mm (44-mil.)* FR4 dielectric shown in Fig. 3 was the power-bus structure studied herein. There were 39 global decoupling capacitors with an individual value of *0.01μF* uniformly distributed on the board. The spacing between any two adjacent capacitors was *25.4 mm (1")*. Either zero or four local decoupling capacitors were added adjacent to Port 1. The spacing between these local decoupling capacitors and Port 1 was *2.54 mm (0.1")*. The $|Z_{21}|$ between Port 1 and Port 2 was modeled. A higher Z_{21} magnitude means that more noise can be transferred from the source to Port 2. Fig. 4 shows both the FDTD and CEMPIE modeled results. The comparison shows that the local decoupling does exhibit lower magnitudes by *5-10 dB* than the case without local decoupling over the entire frequency range. The agreements between the CEMPIE results (only calculated up to *2 GHz*) and the FDTD results are generally good.

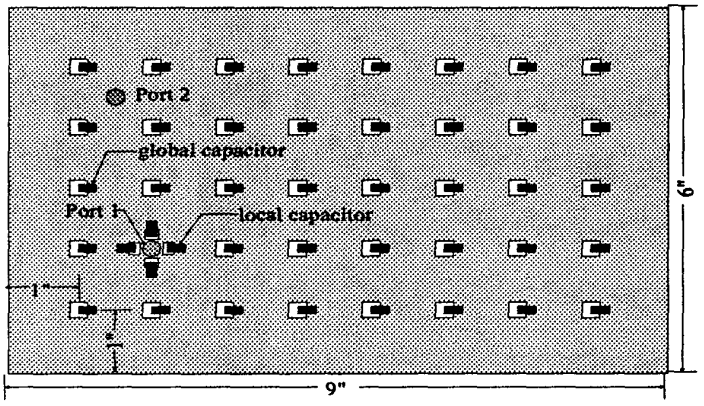

Fig. 3. Modeling structure for local decoupling study.

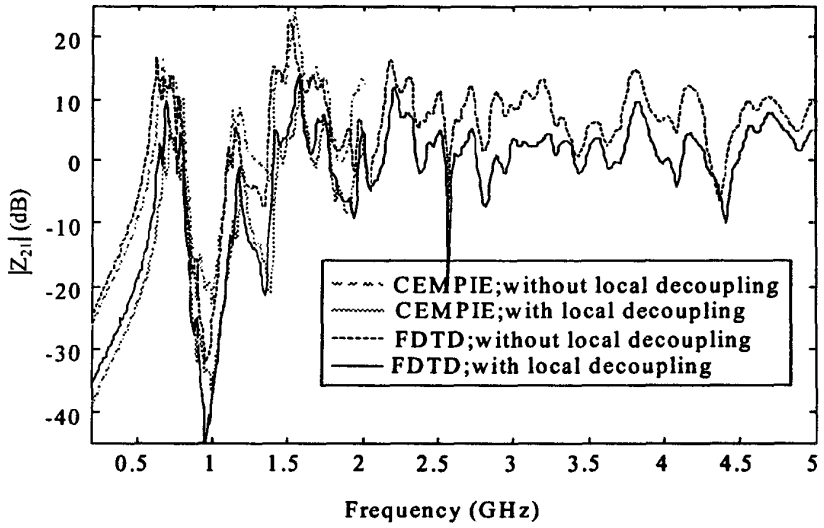

Fig. 4. Modeled results for the structure shown in Fig. 3 with and without local decoupling capacitors.

IV. Conclusions

The FDTD method taking into account the dispersive nature of FR-4 is capable of modeling the wide-band response of a typical DC power bus structure. The dielectric is approximated by a Debye material. Favorable agreement is achieved between the modeled and measured results, demonstrating the effectiveness and application of the FDTD method in DC power-bus design. The FDTD tool applied to investigate the effects of local decoupling in DC power-bus yields good agreement with an independent method, CEMPIE modeled results. The FDTD method is a powerful full-wave power-bus modeling tool. It can be used as an alternative cost-effective approach for hardware trial-and-error measurements. Various *what-if* scenarios can be easily and rapidly performed using this modeling approach.

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