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RADIATION MECHANISMS FOR SEMICONDUCTOR DEVICES AND PACKAGES

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Abstract: VLSI semiconductor devices are often the source of radiated electromagnetic emissions from electronic devices. Noise coupled from these devices to resonant structures on the printed circuit board, resonant cables or resonant enclosures can result in EMI problems that are difficult or expensive to solve at the board or system level. This paper reviews three mechanisms by which noise can be coupled from semiconductor devices and packages resulting in radiated electromagnetic emissions.

Key words: IC, VLSI, Integrated Circuit, Radiated EMI

I. Introduction

As VLSI devices gave grown in size and power consumption, they have come to play an increasingly important role in the electromagnetic compatibility of the products in which they are found. Well designed VLSI devices can operate at GHz clock speeds and dissipate watts of power without being significant sources of radiated electromagnetic emissions. On the other hand, poorly designed devices are often the source of electromagnetic interference that is difficult to suppress without expensive shielding and/or filtering.

In general, VLSI devices and packages are not large enough to radiate significantly by themselves. So although they are the ultimate source of the radiated emissions, they need to be able to drive a larger structure in order for significant radiation to occur. This paper reviews three possible mechanisms by which high-frequency energy from a VLSI device can couple to printed circuit board structures to generate significant radiated emissions. Each of these radiation mechanisms has been observed in the EMC Laboratory at the University of Missouri-Rolla. All three mechanisms can produce radiated electromagnetic interference problems that are difficult or expensive to solve at the system level, but might easily be solved by better chip and package designs.

2. Radiation Mechanisms

2.1 Coupling to heatsinks

Perhaps one of the more obvious radiation mechanisms in VLSI designs that require a large heatsink is the tendency of the device to generate a voltage between the heatsink and the printed circuit board. Large heatsinks can become relatively efficient antennas at frequencies as low as a few hundred megahertz. When boards with heatsinks are located in shielded enclosures, the heatsinks can facilitate the coupling of energy that drives enclosure resonances [1].

The average voltage on the surface of the semiconductor device is different than the voltage on the surface of the PCB due to the signal voltages themselves or the voltage dropped across the connections between the device and the board as illustrated in Figure 1. One possible solution to this problem is to attempt to bond the heatsink to the PCB. Another possible solution is to attempt to shift the resonances of the PCB/heatsink structure so that they don't correspond to enclosure resonant frequencies [2]. Both of these solutions can be difficult to implement in a reliable and cost-effective manner.

A much better solution is to design the chip and package to prevent significant coupling to the heatsink. This can be done by reducing the inductance of the connections between the chip and the PCB or by designing the package to facilitate an effective bond between the heatsink and the PCB.

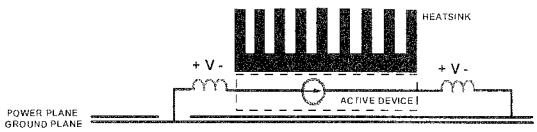

Fig. 1. Component voltage coupling to heatsink.

2.2 Coupling to traces

High-speed VLSI devices generally transmit and/or receive high-speed digital signals by means of traces on the PCB. Generally, PCB designers recognize the importance of routing these high-speed traces in a manner that minimizes radiated emissions. However, poorly designed VLSI devices may exhibit significant levels of high-frequency noise on all of the input and output pins. High-frequency noise voltages developed between any two pins on a device can drive noise currents onto traces that are nominally low-speed.

Figure 2 shows a magnetic near-field scan for an RDRAM memory device. The device is clocked at 200 MHz and the magnetic field is measured at 200 MHz. The magnetic fields are strongest just above the lead frame where the currents are the strongest. As the figure illustrates, the strongest currents are flowing in the VCC and GND pins. The currents in these nominally low-frequency pins are significantly stronger than the currents in the clock and data pins. Modifying the chip and/or package design (e.g. to reduce shoot-through current or provide decoupling capacitance) might significantly reduce the level of these noise currents without adversely affecting signal integrity.

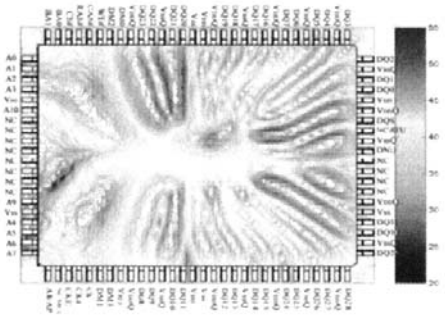

Fig. 2. H-Field surface scan of RDR memory module at 200 MHz.

Figure 3 shows a magnetic near-field scan for the same RDRAM memory device as Figure 2. This time however, the frequency measured was 400 MHz, twice the clock frequency. Note that the pattern of currents flowing through the device is significantly different. Generally, the noise induced on the various pins of a VLSI device is frequency dependent.

In Figures 2 and 3, the RDRAM was measured while data was being read from memory. Figure 4 shows the magnetic near-field scan for the same RDRAM while writing to memory. This scan was also done at 200 MHz. The distribution of the current in the package is completely different and the average amplitude of the current is approximately 10 – 20 dB lower in this case.

The authors have observed several cases where harmonics of clocks that were generated and used internal to a device have appeared on all of the pins connected to that device. This can be a difficult problem to address at the board level, since it becomes necessary to route all traces connected to that device as if they were high-speed traces. On the other hand, noise problems such as this can be minimized relatively inexpensively through the use of effective on-chip decoupling techniques [3]. Models currently being developed to estimate noise voltages on pins and to help develop better integrated circuit designs include ICEM [4,5] and LECCS [6].

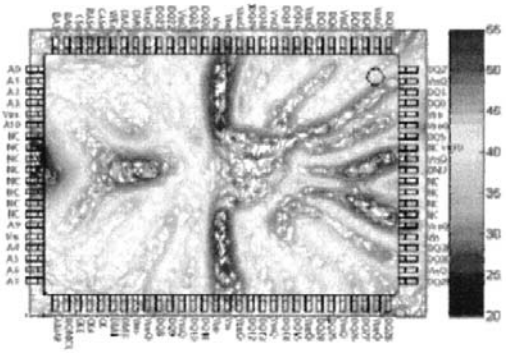

Fig. 3. H-Field surface scan of RDR memory module at 400 MHz.

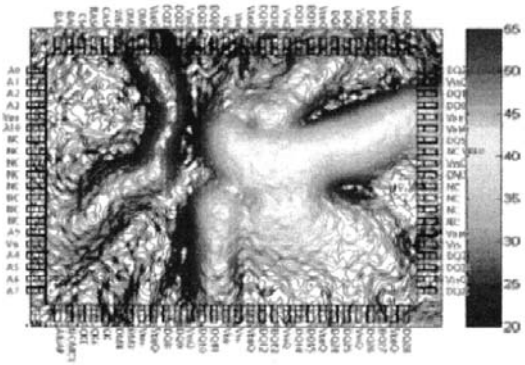

Fig. 4. H-Field surface scan of RDR memory module at 200 MHz (write mode).

2.2 Coupling to the printed circuit board

Another way that VLSI devices can radiate is by driving the reference plane. A voltage difference between two reference (e.g. ground) pins will induce a current to flow in the reference plane below the device. This current loop generates an effective voltage between two sides of the

reference plane that can drive common-mode currents onto cables and other metal objects that are also attached to the plane as illustrated in Figure 5. A few millivolts of effective voltage induced across a plane are capable of driving enough common-mode current on attached cables to exceed radiated emissions requirements [4].

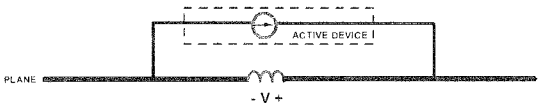

Fig. 5. Effective voltage induced across reference plane by a current loop.

Figure 6 shows the magnetic field scan just above the surface of a clock driver device. This device exhibits a relatively strong common-mode current that flows from the upper left corner of the package to the middle of the lower side. This current is drawn from the VSS/VDD plane pair on the board. Even though the plane-pair is solid beneath the clock driver package, the magnetic flux generated by this current loop is capable of driving common-mode currents onto cables and/or enclosures attached to the plane pair.

Fig. 6. H-Field surface scan just above the surface of a clock driver.

Although there are many VSS/VCC pins on both sides of this device, most of the current flows between two pins on opposite sides of the package. Without knowing the details of the semiconductor design, it is not clear why this device behaves this way. However, this behavior creates significant EMI challenges for any product that uses this device. It is likely that inexpensive improvements in the VLSI layout would result in significant cost savings for any product that employed this clock driver.

3. Modeling challenges

Perhaps one of the greatest challenges for engineers who want to model VLSI sources is that the model parameters tend to depend on aspects of the VLSI design that are not publicly available. For example, the model for a particular output pin driver may depend on the driver's location or even the state of the other pins near it.

Figure 7 shows a magnetic field scan just above the surface of a Field Programmable Gate Array (FPGA). This device was programmed to emulate an 8-bit microprocessor. The processor was clocked at 24 MHz and the measurement was made at 72 MHz. The FPGA was mounted on a board that did not have solid power and ground planes, so the current distribution in the package was affected significantly by the routing of the power and ground traces on the board. The strongest currents are observed above the clock and data leads.

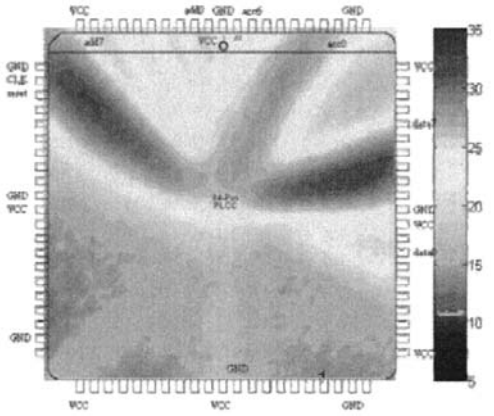

Fig. 7. H-Field surface scan of FPGA running an 8-bit microprocessor.

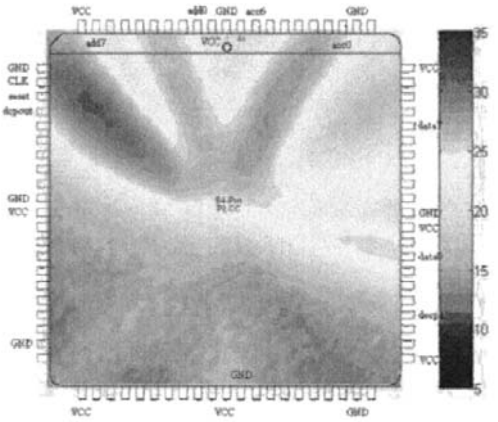

Fig. 8. H-Field surface scan of FPGA running an 8-bit microprocessor and containing additional idle circuitry.

Figure 8 shows a magnetic field scan of the same FPGA device programmed with the same 8-bit microprocessor plus additional inactive circuitry. Even though the FPGA was performing the exact same function in the exact same manner, the

current distribution in the package was different. In particular, the average amplitude of the currents was about 5 – 10 dB lower on the data pins on the right-hand side of the FPGA with the additional circuitry.

4. Summary

Although most VLSI devices are too small to be the direct source of radiated EMI problems, noise coupled from these devices is a significant concern. Three mechanisms for coupling noise from electrically small semiconductor packages are coupling to heatsinks, coupling to traces and coupling to the printed circuit board. Good semiconductor and packages designs can minimize each of these coupling mechanisms.

The information required to model VLSI devices as EMI sources is not generally available in product data sheets. IC models such as ICEM and LECCS are a step in the right direction. However, significantly more development is required before these models can be used to reliably predict the amount of noise coupled from competing IC designs.

Component designs that minimize coupling reduce the need for relatively expensive shielding and filtering on the printed circuit board. Hopefully, as the development of new standards for IC modeling progresses, IC designers will have better guidance and increased motivation for designing quieter devices.

References

[1] M. Li, J. Nuebel, J. Drewniak, T. Hubing, R. DuBroff, and T. Van Doren, "EMI from cavity modes of shielding enclosures – FDTD modeling and measurements," *IEEE Trans. on EMC*, vol. 42, no. 1, Feb. 2000, pp. 29-38.

[2] Y. Huang, J. Butler, M. de Sorgo, R. DuBroff, T. Hubing, J. Drewniak and T. Van Doren, "EMI considerations in selecting heat-sink-thermal-gasket materials," *IEEE Trans. on EMC*, vol. 43, no. 3, Aug. 2001, pp. 254-260.

[3] S. Zhao, K. Roy and C. Koh, "Decoupling capacitance allocation and its application to power-supply noise-aware floorplanning," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 1, Jan. 2002, pp. 81-92.

[4] IEC EMC Task Force. IEC62014-3 Integrated circuit electromagnetic model. Draft technical report.

[5] C. Lochot and J. L. Levant, "ICEM: A new standard for EMC of IC definition and examples," Proceedings of the 2003 IEEE International Symposium on EMC, Aug 18-22, 2003, pp. 892-897.

[6] H. Osaka, T. Kinoshita, D. Tanaka, O. Wada, Y. Toyota and R. Koga, "Power Current Modeling of IC/LSI with Load Dependency for EMI Simulation," 2003 IEEE Symposium on EMC, Boston, Aug.18-22, 2003, pp.16-21.

[7] D. Hockanson, J. Drewniak, T. Hubing, T. Van Doren, F. Sha, C. Lam, and L. Rubin, "Quantifying EMI resulting from finite-impedance reference planes," *IEEE Trans. on EMC*, vol. 39, no. 4, Nov. 1997, pp. 286-297.