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Interleaved coupled-inductor boost converter with multiplier cell and passive lossless clamp

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INTERLEAVED COUPLED-INDUCTOR BOOST CONVERTER WITH MULTIPLIER CELL AND PASSIVE LOSSLESS CLAMP

by

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ABSTRACT

As photovoltaic panels become a more dominant technology used to produce electrical power, more efficient and efficacious solutions are needed to convert this electrical power to a useable form. Solar microconverters, which are used to convert a single panel's power, effectively overcome issues such as shading and panel-specific maximum power point tracking associated with traditional solar converters which use several panels in series. This thesis discusses a high gain DC-DC converter for incorporating single low-voltage solar panels to a distribution level voltage present in a DC microgrid. To do this, a converter was developed using coupled inductors and a capacitor-diode multiplying cell which is capable of high-gain power transmissions and continuous input current. This approach improves the efficiency of the system compared to cascaded converters typically used in this application. Challenges with this converter are discussed, a passive lossless clamp is introduced, and simulation results are presented. This converter has additional applications where high gain DC-DC conversion is required, including fuel cells and energy storage systems such as batteries and ultracapacitors.

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1. BACKGROUND

1.1 MICROGRIDS

As the world continues to increase the amount of power it consumes, researchers have attempted to determine the best way to deliver power to consumers. In the past, when generation equipment was expensive and difficult to maintain, it made sense to have centralized generation with long transmission lines [1]. As our technology improves, however, it makes more sense to eliminate some of the inefficiencies in long distance transmission, as well as allow greater consumer access to renewable energy sources, through DG (Distributed Generation) and DER (Distributed Energy Resources). Unfortunately, the conventional electrical grid was designed to allow power transmission in only one direction, top to bottom. This limit to the integration of distributed generators is especially relevant when considering intermittent renewable sources (one of the more important consideration when looking to the future of power generation) and areas of the grid which are considered weaker.

The concept of a Microgrid began through attempts to combat these limitations by providing a single Point of Common Coupling (PCC) with the grid, ensuring the whole Microgrid network is treated as a single load or generation unit [2]. In addition, researchers have implemented the idea of the smart grid, or a grid which uses technology to react to changing system conditions for the purpose of optimizing and protecting its components. Coupling these concepts, it is easier to understand one of the definitions of a Microgrid. "A Microgrid is a localized group of distributed energy resources that can be operated coordinately as an energy generator, as an energy storage and as a load. It normally operates connected to a traditional centralized grid (macrogrid or general grid) to provide maximum electrical efficiency with a minimum incidence to loads profile in the local power grid"[1].

1.2 DC DISTRIBUTION

In the early 19th Century, a battle occurred between Thomas Edison's DC distribution system and George Westinghouse's AC distribution system. As we know

today, AC power emerged as our primary method of delivering electrical power. An idea today is that in some situations DC distribution has several key advantages which overshadow those of AC distribution. AC initially won favor due to its ease in changing the system voltage between transmission and distribution levels, requiring only an iron core and some copper wire. Additionally, when AC power is produced by a conventional generator the power produced is naturally AC. DC power, by contrast, required complicated grid design and many loads placed in series to achieve the same results. In a conventional grid, DC distribution would require all naturally produced AC power to be rectified to some defined DC voltage [3].

These considerations change when discussing Microgrids. With Microgrids, the expectation is that power will be produced through a variety of technologies, such as microturbines and renewable energy, most of which require some type of power electronics to generate an AC waveform and complicated Microgrid-level control to instill a consistent frequency. With DC distribution there is no need to worry about a consistent grid frequency and no inefficiencies introduced by the inverting state of the power converter. In a Microgrid, there is also a need for some type of energy storage mechanism, such as batteries, which conveniently lends itself better to a DC system. Additionally, traditional Microgrids are operated in residential areas where computers, electronics, and lighting are typical loads, all off which can be powered by a DC system. These systems could operate more efficiently if there was no need to first rectify an AC signal [3].

As with an AC system, there are trade-offs to the different voltage levels the system can use. The main DC systems in use today are operated by the telecommunication systems. The standard dc communication system utilizes a -48V system, while some alternate systems rely on 140V architecture [4]. Power delivery systems used before general acceptance of AC transmission utilized ±110V and ±220V systems, while some current DC Microgrids utilize 300, 320-345, and 620 V. As with current AC systems, tradeoffs must be made with the chosen distribution voltage. In general, the higher the voltage used, the lower the losses and the higher the efficiency, but the greater the difficulty in mitigating safety and component compatibility issues [4].

1.3 DC GRID WITH HIGH SOLAR PENETRATION

Perhaps the most important consideration for DC distribution is the rising use of renewable resources, including wind, and most important for this thesis, solar power. Solar panels directly convert solar radiation into DC power. In a typical solar installation a solar inverter is used to convert the received DC power from several panels in series to AC power. The problem with this strategy is that the current a panel allows to pass through itself is directly related to the solar radiation it is receiving, so in certain situations where part of the array are shaded more than others you can quickly lose large amounts of generating capability. For this reason, research is being done into so-called micro-converters, where each individual panel has a converter capable of converting all of its power. In current installations, this micro-converter has multiple internal stages, generally a DC-DC converter, converting the incoming panel voltage to a mid-stage voltage conducive to AC conversion, and a DC-AC converter which inverts the mid-stage DC voltage to AC.

In a DC grid, this last micro-converter stage is not required, eliminating power losses present in that stage, and lowering the overall cost of the converter. This thesis will attempt to provide a solution for a micro-converter to be used in conjunction with a DC Microgrid, one which converts the base panel voltage, such as 20V, to a reasonable DC grid distribution voltage, such as 400V. This converter would require an overall transfer ratio of 20, which is either outside the range of feasible implementation or outside the capabilities of many conventional topologies. Ideally, solar panels are used at the Maximum Power Point (MPP), which requires a relatively constant solar panel output current, which means our ideal high gain DC-DC converter should have constant input current [5]. Several topologies exist which attempt to solve this same problem with a different solution [6-16]. This thesis presents one method of approaching the problem.

2. REVIEW OF EXISTING TOPOLOGIES

2.1 BOOST CONVERTER

While the generic boost converter cannot be usefully used as a high gain DC-DC converter, it is important to understand its characteristics before continuing on to other topologies presented in this thesis. The boost converter is a voltage-increasing switched-mode power converter, which utilizes two switches, one passive (i.e. diode) and one active (i.e. MOSFET), as well as an energy storing inductor to achieve a voltage boosting effect. Figure 2.1 below shows the boost converter, as well as its two modes of operation.

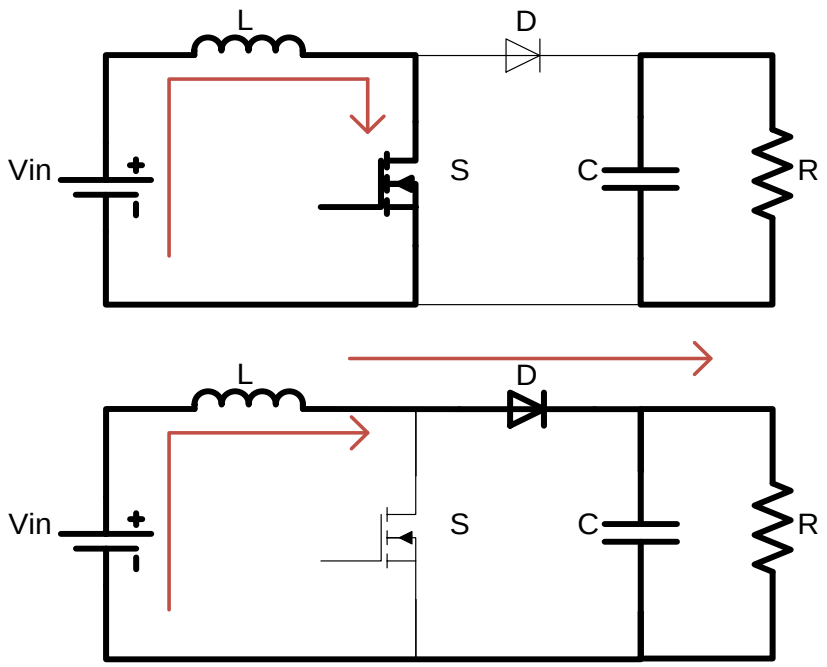

Figure 2.1. Boost converter operating modes

2.2.1. Operating Modes. The boost converter, as one of the most elementary power converters, has two, easily understood operating modes.

Mode I occurs when the active switch, S, is in the ON state, and the passive switch, D, is in the OFF state. In this operating mode, the voltage across the inductor is

positive, and the inductor current as well as energy stored in the inductor is increasing. The output power is being provided by capacitor C, and its total charge is decreasing.

Mode II occurs when the active switch, S, is in the OFF state, and the passive switch, D, is forced to the ON state by the energy present in the inductor. In this state, the voltage across the inductor is negative, the inductor current is decreasing, and energy is being moved to the output capacitor, C, increasing its overall charge.

Combining the equations representing the voltage present across the inductor in the ON and OFF states of the converter with the respective time spent in each state yields the following overall input to output transfer ratio. The duty ratio, D, represents the percentage of time spent in the on state.

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{2.1}$$

2.2.2 Advantages and Disadvantages. When comparing existing topologies with the topology presented in this thesis, it is important to understand the various advantages and disadvantages of each type of converter. Some advantages of the boost converter include its inherent simplicity as a very basic converter, which also means it is fairly simple to design an effective converter. The boost converter also has constant input current, which is one of the requirements for a converter used in conjunction with solar panels. The converter has no leakage inductance, or other transient producing effects, which means that there is no need for a clamping circuit.

Easily one of the most harrowing disadvantages for the boost converter for the application of a high gain DC-DC converter is that it does not have a high gain. In use as a power converter, the boost converter has a hard time achieving a gain greater than three or four. This is mainly due to the two-thirds or three-fourths duty cycle required for these gains, which amplify the effects of parasitic losses and decrease the time available for charging and discharging energy storing components. Additionally, boost converters are a non-isolated topology, rendering it unusable in some situations, and have a pulsed output current, requiring a larger output capacitor to reduce voltage oscillations [17].

2.2 TAPPED-INDUCTOR BOOST CONVERTER

The tapped-inductor boost converter is the natural extension to the normal boost converter. In converters such as a flyback converter, a coupled inductor is used to transfer the energy from the input to the output, allowing the designer to change the turns ratio to affect the voltage transfer ratio. The tapped-inductor boost converter uses a similar approach, allowing one to change the turns ratio as well as the duty ratio, to affect the voltage transfer function. This converter operates and appears very similar to the typical boost converter, utilizing both a single active and passive switch [18]. Figure 2.2 shows the tapped inductor boost as well as its two modes of operation.

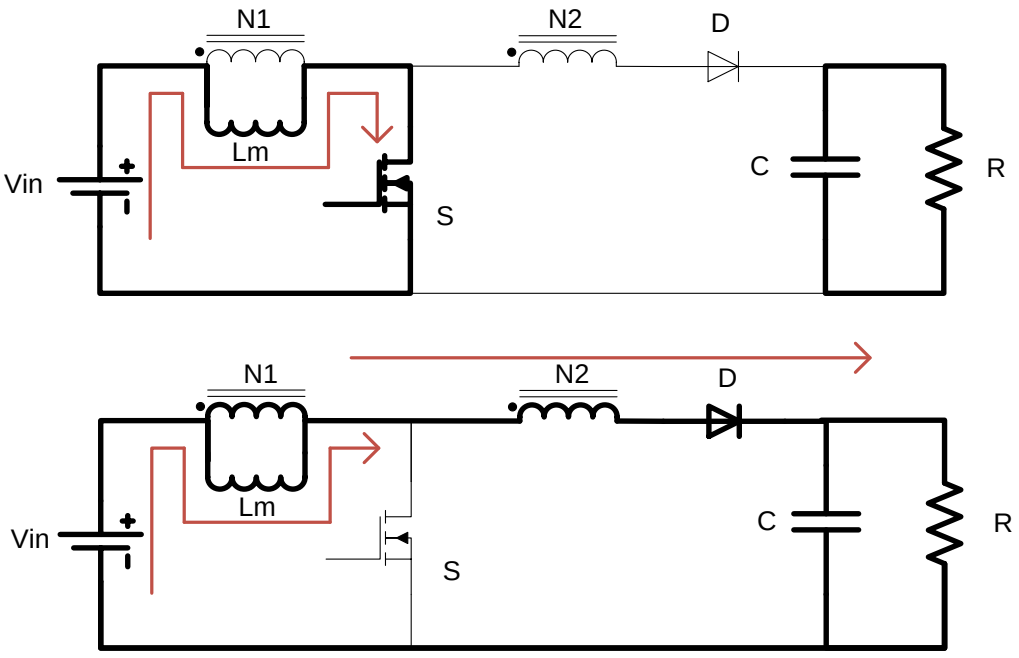

Figure 2.2. Tapped inductor boost converter operating modes

2.3.1 Modes of Operation. As with the boost converter the tapped-inductor boost converter benefits from having only two modes of operation, one where the active switch S is in the ON state and one where it is in the OFF state.

Mode I takes place with switch S in the ON state, diode D in the OFF state, and current flowing through the winding N1 of the tapped inductor. In this state, the current

through the inductor winding N1 and the energy stored in the tapped inductor's magnetizing inductance Lm is increasing due to the input voltage across N1. The output power is provided by capacitor C and its total charge is decreasing.

Mode II takes place when switch SW1 is in the OFF state and diode D is forced to the ON state by the tapped inductor. In this state the current flows through both windings N1 and N2 of the tapped inductor. This current, along with the energy stored in the magnetizing inductance Lm, decreases due to the difference between the input and output voltage across the coupled windings. The output power is being provided by the coupled inductor and the total charge of capacitor C increases. At the beginning of this mode when S is turned off, the leakage inductance present in winding N1 causes a voltage spike across switch S. Additionally, when this mode is entered the input current drops dramatically with respect to the turns ratio between windings N1 and N2.

When attempting to find the transfer ratio of this converter it is necessary to find the voltages across magnetizing inductance Lm. This requires the utilization of equations relating the inductance of each winding to the turns of each winding. Doing this yields the following transfer function, where N = N2/N1. [18]

$$\frac{V_o}{V_i} = \frac{1}{1-D} + \frac{D}{1-D} N \tag{2.2}$$

2.3.2 Advantages and Disadvantages. This converter, being very similar to a typical boost converter, derives all of its different advantages and disadvantages from the addition of the tapped inductor. Since the converter is very similar to the typical boost converter the tapped-inductor boost converter is advantageously simple, especially compared to other higher transfer ratio converters. The converter also has a transfer ratio with more upwards mobility compared to the boost converter due to the transfer function's additional term dependent upon the turns ratio N.

While the converter has a more flexible transfer function dependent upon a tunable value, N, it would still be unfeasible to implement this converter with a gain of twenty, to do so would require a turns ratio of somewhere around twenty, the desired gain. Further, the addition of the secondary winding causes this converter to have two

problems typical to tapped inductors. The first is the change in input current caused by moving power through one or two of the tapped inductor's windings. This occurs because the magnetic energy stored in a tapped inductor must remain constant. For this to happen when current flows through a different number of turns of the inductor the current through the inductor windings must decrease or increase to keep the inductor's energy constant. This leads to a non-constant input current, a large problem when the converter is to be used with solar panels. The second problem is the leakage inductance present in the first winding, N1. When switch S is turned off, the leakage inductance will resist the sudden change in current previously discussed, resulting in a large voltage spike to occur across switch S. This problem requires the use of some type of clamp circuit with this converter, further increasing the complexity and cost of the system. As with the boost converter, this converter has pulsed output current, requiring a larger output capacitor to be used [18].

2.3 INTERLEAVED COUPLED INDUCTOR BOOST CONVERTER

One of the largest disadvantages to the tapped inductor boost converter when considering its use with solar panels is its non-continuous input current. For the converter to be successfully used for this application, a prohibitively large input capacitor would need to be used. A method in use which causes a converter utilizing coupled inductors to have continuous input current involves using two interleaved stages, each of which increases its own current in response to a decrease in the other stage's current. This is achieved through an additional backwards polarity coupled winding which interleaves the two stages. The interleaved coupled inductor boost converter, as well as two of its four operating modes, is shown below in figure 2.3 [19].

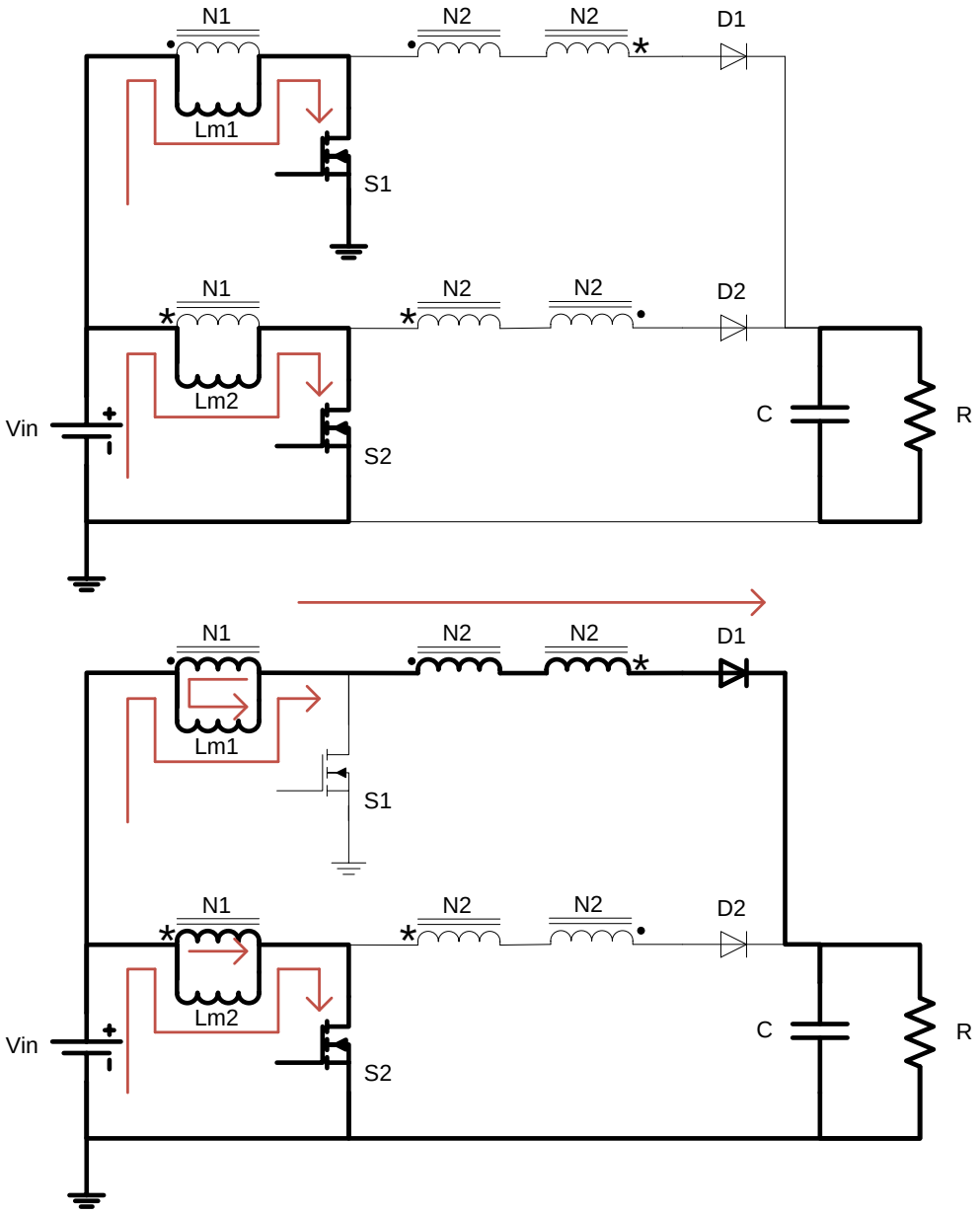

Figure 2.3. Interleaved coupled inductor boost converter

2.3.1 Modes of Operation. The interleaved coupled inductor boost converter is a converter with four main modes of operation. Modes I and III have the same profile, and modes II and IV only change the stage whose switch is off. For this reason, only modes I and II will be detailed here.

Mode I occurs when both switches S1 and S2 are in the ON state, and the diodes D1 and D2 are in the OFF. During this mode the current and the energy stored in both

Lm1 and Lm2 is increasing and the output power is being provided by capacitor C. Of note is that no current is flowing through the N2 windings of either stage, meaning that all of the current flowing through each switch is flowing through the magnetizing inductance and not the coupled N1 and N2 windings.

Mode II occurs when switch S1 turns OFF and S2 stays ON. When this happens, the magnetic energy stored in Lm1 forces diode D1 to the ON state and power is delivered to the output, charging capacitor C and providing power to R. The current and the energy stored in Lm1 decreases while the energy and current in Lm2 continue to increase. When mode II is entered the leakage inductance in N1 of the first stage causes a voltage spike across S1, necessitating some sort of clamp protecting the switches. As mentioned, when S1 turns OFF the current through the first stage of the converter decreases, and through the orientation of the N2 windings of each stage, the current through the second stage increases to keep the overall input current of the converter continuous.

This converter only works with desirable characteristics if each stage is 180 degrees out of phase, and the overall duty ratio is greater than 0.5. This is because the constant input current to the converter relies upon a stage with an ON switch responding to the undesirable effects of turning a switch OFF. Additionally, the converter's gain relies upon current flowing freely through N1 of the stage with the ON switch, multiplying the input voltage through the secondary windings of the coupled inductor. When equations describing the behavior of the magnetizing inductance are taken into consideration, it can be found that the overall transfer function of the converter is as follows.

$$\frac{V_o}{V_i} = \frac{N+1}{1-D} \tag{2.3}$$

As will be important later, the transfer ratio introduced by each part of the converter can also be determined. The ratio X, produced by the N1 winding of each stage, then the ratio produced collaboratively by the N2 windings of each stage Y, follow. These two gains can be considered in series and added together to give our overall transfer ratio [19].

$$X = \frac{1}{1-D} \tag{2.4}$$

$$Y = \frac{N}{1-D} \tag{2.5}$$

2.3.2 Advantages and Disadvantages. This converter has several advantages, the most important of which is its constant input current, as this is a design requirement for a solar power converter. The coil configuration not only causes this natural input current balancing, they also cause the increased transfer ratio. For a converter with a decent transfer ratio, the switch stress is still respectably small, corresponding to the switch stress seen in a normal boost converter. Additionally, the leakage inductance present in the N2 windings causes the diodes to be naturally soft current switching, reducing switching losses of the converter.

There are some disadvantages to this converter. While the coil configuration increases the gain of the converter without increasing the base voltage stress of the switches the leakage inductance present in the N1 winding also causes voltage spikes to appear across the switches at the beginning of their off cycle, requiring some type of clamp to be used. The other main difficulty with implementing this converter as a high gain DC-DC converter is its still insufficient transfer function. To achieve a gain of 20 with this converter it would be necessary to use greater than a 1:4 N1:N2 as a lower ratio would necessitate an unfeasible duty ratio. This means the converter does not lend itself for use as a high-gain solar DC-DC converter.

While this converter does have some disadvantages, they are not so bad as to be unmanageable. After utilizing a clamp across the switches, this converter has several desirable characteristics which allow it to be used as the base for a converter with higher gain. The only thing required would be to modify the converter with some gain-increasing components [19].

2.4 INTERLEAVED BOOST CONVERTER WITH INTRINSIC VOLTAGE-DOUBLER CHARACTERISTIC

While the previously discussed converters display an advantageous voltage gain from the use of coupled inductors, the following converter uses an additional diode and capacitor to achieve voltage doubling from a typical interleaved boost converter [20]. The interleaved boost converter with intrinsic voltage-doubler characteristic, as well as some of its operating modes, is shown below in figure 2.4.

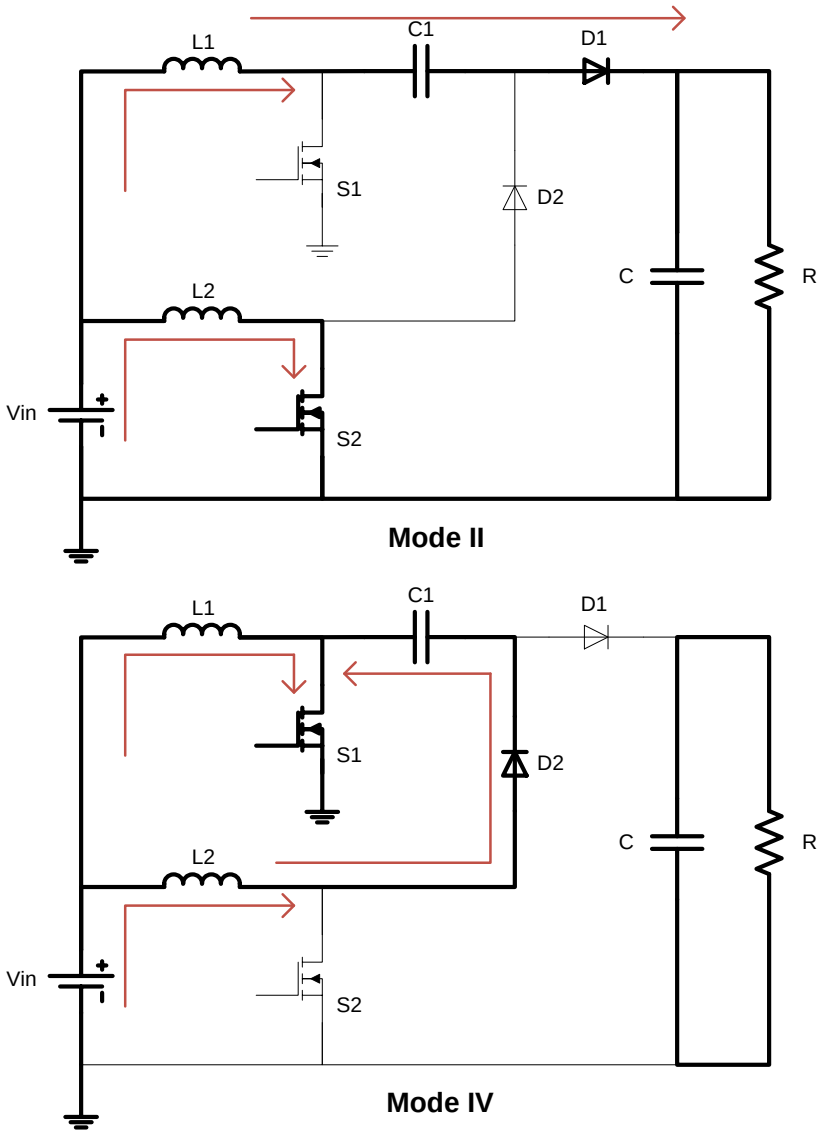

Figure 2.4. Interleaved boost converter with intrinsic voltage-doubler characteristic operating modes

2.4.1 Modes of Operation. The interleaved boost converter with intrinsic voltage-doubler characteristic has four main modes of operation. Modes I and III have the same profile and modes II and IV change which switch is off, changing the charging and discharging pattern of capacitor C1. For this reason, modes II and IV are shown in figure 2.4 and modes I, II, and IV will be described.

Mode I, the same operation as mode III, occurs when both of the active switches S1 and S2 are in the ON state. Both system diodes are OFF and the current and energy in inductors L1 and L2 are increasing. The output power to resistor R is provided by capacitor C.

Mode II occurs when switch S1 turns to the OFF state and switch S2 stays ON. When this happens, inductor L1 forces diode D1 to the ON state, moving current through C1 and D1 and reducing the current and energy stored in L1. The charge present on capacitor C1 from mode IV boosts the voltage the output capacitor C is charged to, and inductor L2 continues to increase its current and stored energy. Diode D2 remains in the OFF state, and current from D1 charges capacitor C and provides the output current to R.

Mode IV occurs when switch S2 turns to the OFF state and switch S1 stays ON. When switch S2 is turned off, diode D2 is forced ON, and the charge on capacitor C1 increases through the discharging of energy from L2. Diode D1 remains in the OFF state, and the output power to resistor R is provided by capacitor C. Of note is the increased current switch S1 experiences during this mode, as the current which charges capacitor C1 also passes through this switch.

When this converter's switches are operated 180 degrees out of phase, and with a duty cycle greater than 0.5, the output voltage of the converter is essentially two-times that of a typical boost converter. When switch S2 turns off inductor L2 discharges, acting like a normal boost converter when current flows through diode D2 to charge "output" capacitor C1. When switch S1 turns off, inductor L1 discharges through diode D1, charging C similar to a typical boost converter. In this converter, however, capacitor C1 acts similar to a constant voltage source in series with the current delivered to the output, creating the voltage doubling effect. Using this observation, the voltage transfer ratio can be calculated to be as follows.

$$\frac{V_o}{V_i} = \frac{2}{1-D} \tag{2.6}$$

2.4.2 Advantages and Disadvantages. This converter has many useful advantages. Similar to a typical boost converter the use of the multiplying cell does not cause the input current of the converter to become discontinuous, a necessity if it is to be used with a solar panel. The added gain to the converter is achieved with minimal parts, a diode and capacitor, not appreciably increasing system complexity. Additionally there is no leakage inductance to worry about with this converter, making the use of a clamping circuit unnecessary.

There are a couple disadvantages to this converter, one of which is the current through switch S1 having a higher peak than switch S2. While being a minimal problem, the solution would involve the use of a greater current carrying switch, slightly increasing system cost. The main disadvantage to this converter, as with the others in sections 2.1 to 2.3, is its low transfer function, preventing this converter alone from being used in a high gain DC-DC converter [20].

3. INTERLEAVED COUPLED INDUCTOR BOOST CONVERTER WITH MULTIPLIER CELL

3.1 INTRODUCTION TO THE CONVERTER

The existing topologies presenting in Sections 2.1 to 2.4 all shared problems preventing them from being utilized in a high gain DC-DC converter. This section presents the topology which is the topic of this thesis, the interleaved coupled inductor boost converter with multiplier cell. One familiar with the topologies presented in the previous sections 2.3 and 2.4 may notice some similarities, namely that the topology presented here is an interleaved coupled inductor boost converter with the multiplying circuit from the interleaved boost converter with intrinsic voltage-doubler characteristic. While this multiplier is achieved with the lone addition of a capacitor and diode the configuration of the multiplying cell in this topology has an effect greater than just doubling. This desirable effect, the modes of operation for the converter, converter transfer functions, and idealized simulation results will be presented in the following sections. The proposed interleaved coupled inductor boost converter with multiplier cell is shown in figure 3.1.

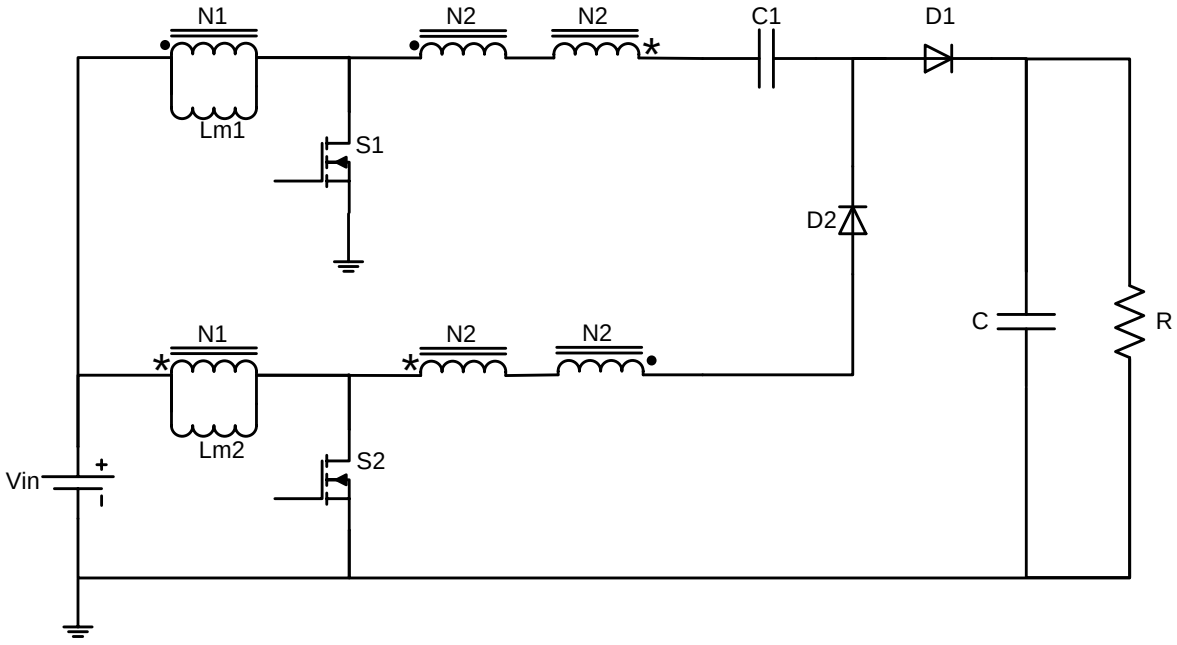

Figure 3.1. Interleaved coupled inductor boost converter with multiplier cell

3.2 CONVERTER OPERATION

3.2.1 Modes of Operation. The operating modes of this converter are quite similar to those presented in section 2.4 for the interleaved boost converter with intrinsic voltage-doubler characteristic. This time, however, the addition of the coupled inductor changes how the power moves through the circuit. As with section 2.4, there are four modes of operation, and modes I and III have the same characteristic.

Mode I and mode III occur when both switches are in the ON state. During these modes, the current and energy flowing through magnetizing inductances Lm1 and Lm2 are increasing. The system diodes D1 and D2 are in the OFF state, and the output power to R is being provided by capacitor C.

Mode II occurs as switch S1 turns to the OFF state and S2 stays ON. In this mode the energy present in magnetizing inductance Lm1 forces current through the N2 windings of the upper stage, continuing through C1 and D1 to the output. The reverse current flow through C1 discharges the capacitor, reducing its charge and transferring the stored energy to the output. The current and energy stored in inductance Lm1 decreases, while the current and energy stored in Lm2 continues to increase. Diode D2 remains in the OFF state and the current flowing through D1 both charges C and proves power to the output resistance R.

Mode IV occurs as switch S2 turns to the OFF state and S1 stays ON. In this mode the energy present in magnetizing inductance Lm2 forces current through the N2 windings of the second stage, continuing through D2 and C1 and increasing the current carried by switch S1. The positive current flow through C1 charges the capacitor, increasing its charge, and capturing energy which was stored in inductance Lm2. The current and energy stored in inductance Lm2 decreases, while the current and energy stored in Lm1 continues to increase. Diode D1 to the output remains in the OFF state, and the output power to resistor R is provided by capacitor C. Figures 3.2(a) and 3.2(b) show these four operating modes.

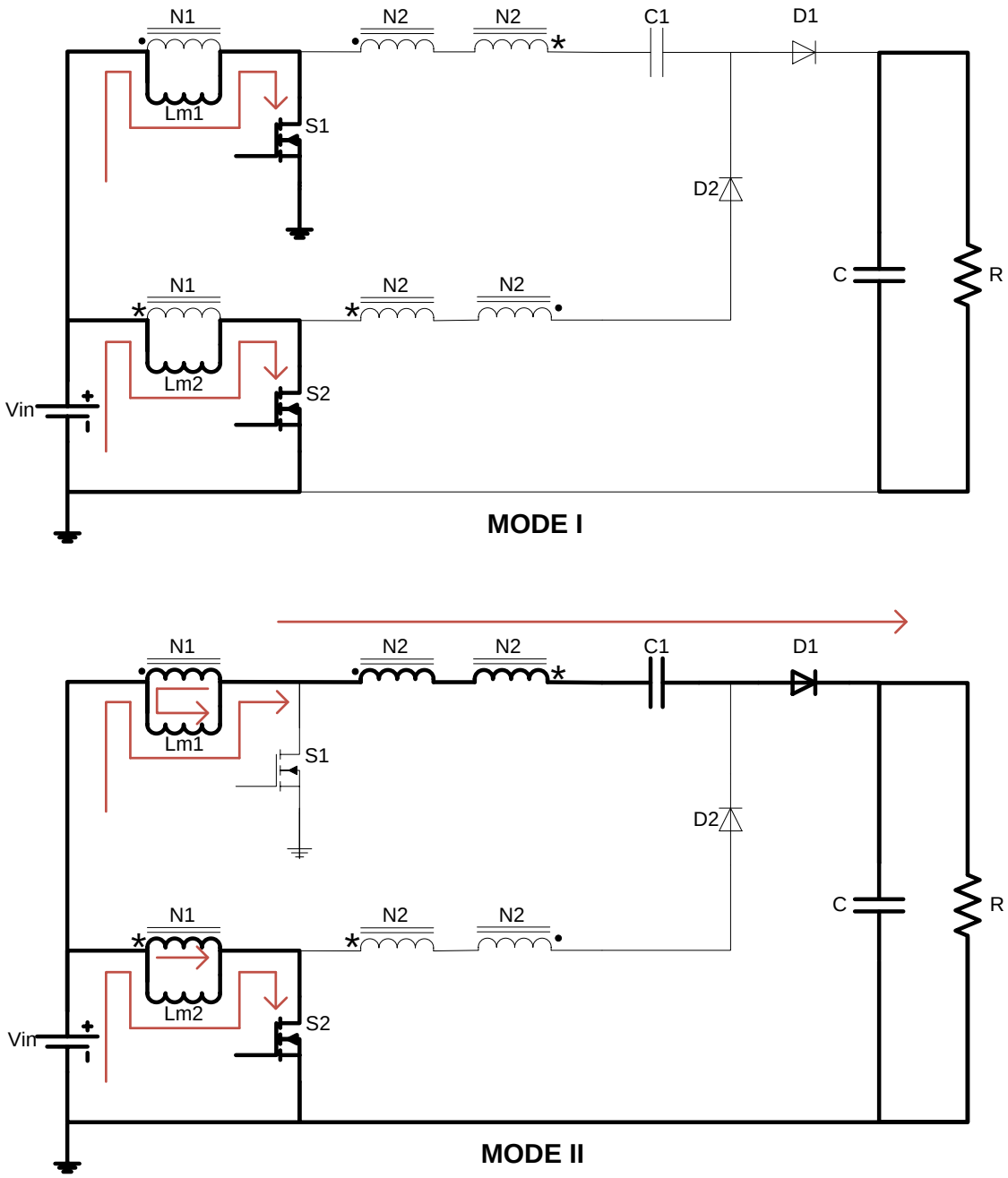

Figure 3.2(a). Proposed converter operating modes I and II

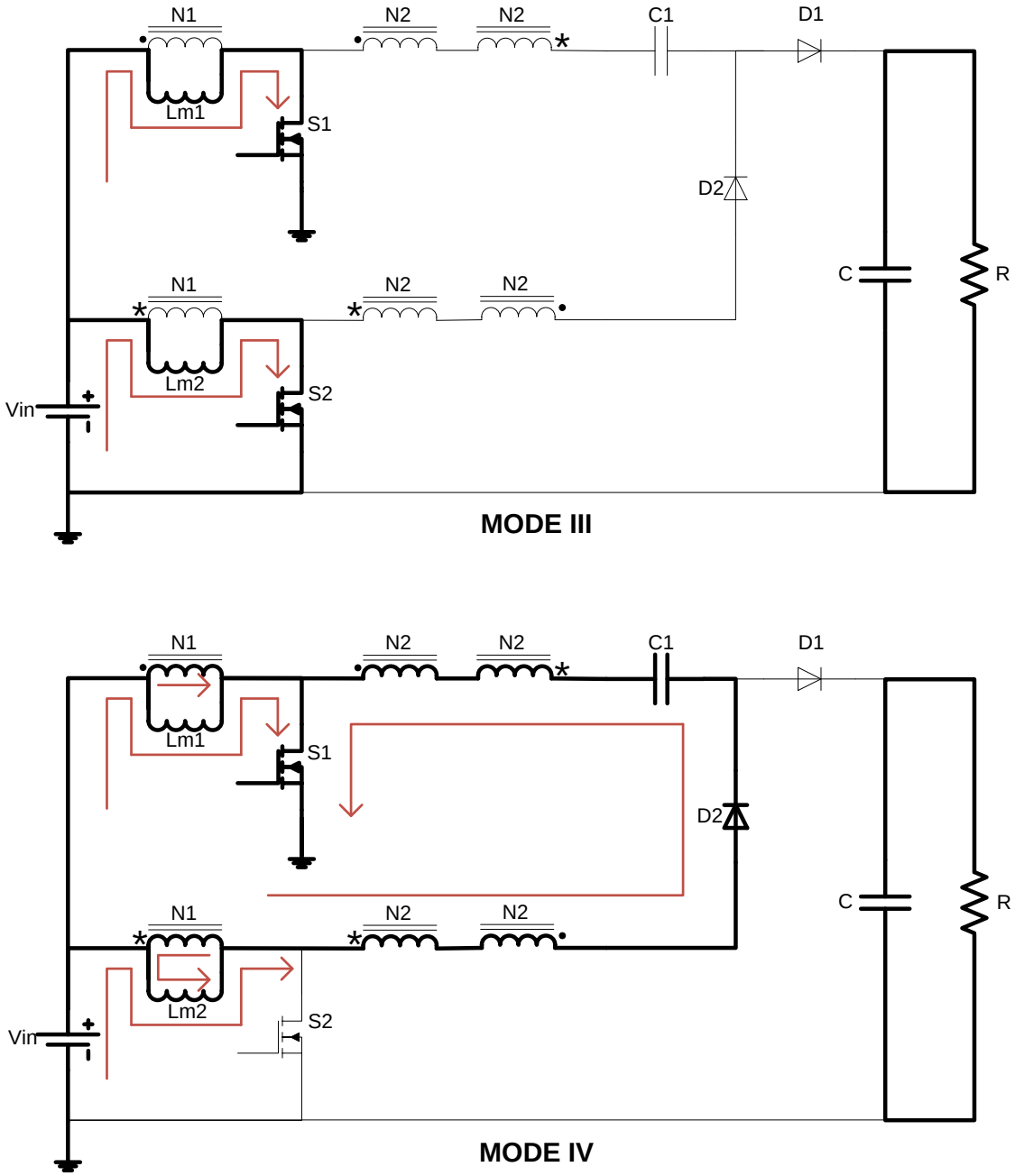

Figure 3.2(b). Proposed converter operating modes III and IV (cont.)

3.2.2 Converter Transfer Functions. These four modes happen with the switches 180 degrees out of phase and with each switch having an equivalent duty cycle, D, greater than 0.5. This means that modes I and III will have the same duration and modes II and IV will have the same duration. To determine the transfer function for this converter it is necessary to take into account the time spent in each of these modes and to use Kirchhoff's voltage law (KVL) around the circuit loops.

Another method to determine transfer functions is to recognize that as long as the duty ratio is maintained above 0.5, the gains of each component in the system, or group of components, remains the same. This was discussed in 2.3.1 for the interleaved coupled inductor boost converter, and the gains X and Y, equations 2.4 and 2.5, were found. When these components are considered in a circuit loop, using KVL, the unknown voltage across a component can be found.

The first loop is that found in mode IV, used to calculate the voltage present across capacitor C1. Noticing the long current flow through magnetizing inductance Lm2, the N2 windings of the lower stage, and the N2 windings of the upper stage, the overall capacitor voltage can be found.

$$\frac{V_{C1}}{V_i} = X + 2Y = \frac{1}{1-D} + 2 \times \frac{N}{1-D} \tag{3.1}$$

$$\frac{V_{C1}}{V_i} = Z = \frac{2N+1}{1-D} \tag{3.2}$$

Now that capacitor C1's voltage has been determined it is possible to calculate the output voltage transfer function. Similar to finding C1's voltage, the output voltage can be found by adding all of the gains in series during mode II. During this mode notice that current flows through magnetizing inductance Lm1, the N2 windings of the upper stage, and capacitor C1. The output voltage transfer function follows.

$$\frac{V_o}{V_i} = X + Y + Z = \frac{1}{1-D} + \frac{N}{1-D} + \frac{2N+1}{1-D} \tag{3.3}$$

$$\frac{V_o}{V_i} = \frac{3N+2}{1-D} \tag{3.4}$$

Another important consideration for power converters is the switch voltage stress. Even though this converter displays a highly advantageous transfer function, the active switch stress still remains the same as that in a typical boost converter. Diode D1 sees its maximum voltage stress in mode IV. In this mode the voltage across the diode is equivalent to sum of the output voltage and N2 winding gain Y, minus the capacitor C1 gain Z. This yields a switch stress equivalent to the voltage across capacitor C1, Z. The diode D2 experiences its maximum voltage stress in mode II when power is being delivered to the output. In this mode the diode stress is equivalent to the output voltage with the addition of the Y gain provided by the N2 windings of the lower stage. The switch stress equations and derivations are shown below.

$$\frac{V_{S1\&S2}}{V_i} = \frac{1}{1-D} \tag{3.5}$$

$$\frac{V_{D1}}{V_i} = \frac{V_o}{V_i} + Y - Z = \frac{3N+2}{1-D} + \frac{N}{1-D} - \frac{2N+1}{1-D} = \frac{2N+1}{1-D} \tag{3.6}$$

$$\frac{V_{D2}}{V_i} = \frac{V_0}{V_i} + Y = \frac{3N+2}{1-D} + \frac{N}{1-D} = \frac{4N+2}{1-D} \tag{3.7}$$

Figure 3.3 below shows the voltage stress of S1 and S2 under a 20V input voltage, 400V output voltage, duty cycle of 0.6, and turns ratio of 2. Figure 3.4 below shows the voltage stress of D1 and D2 under the same conditions.

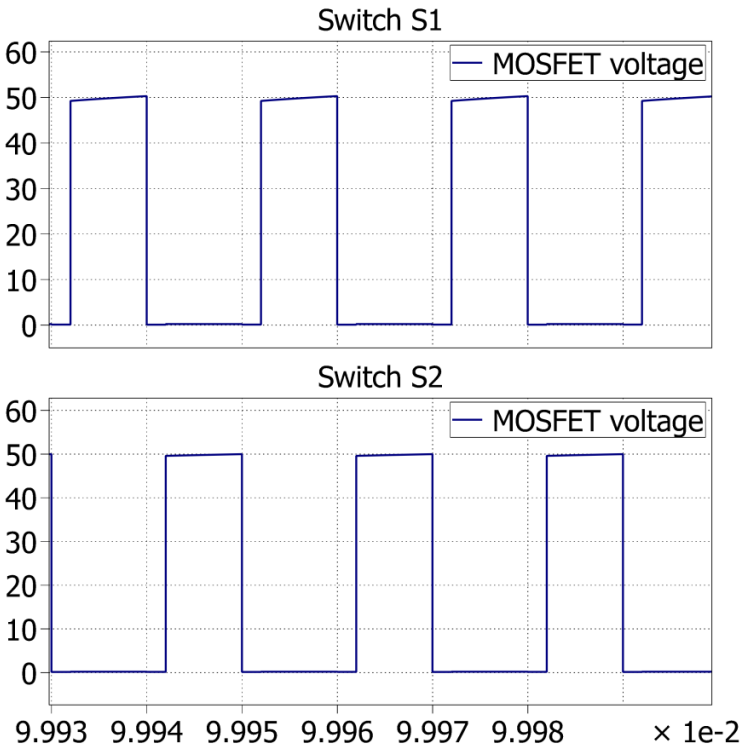

Figure 3.3. Active switch voltage stress

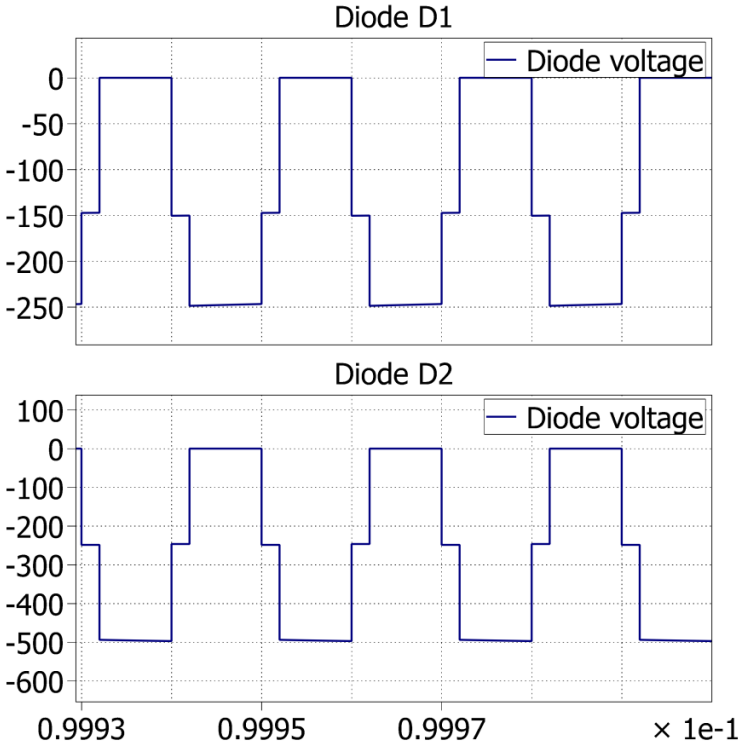

Figure 3.4. Passive switch voltage stress

3.3 ADVANTAGES OF TOPOLOGY

3.3.1 Voltage Transfer Ratio. There are several advantages to this converter, the most beneficial being its transfer function. This highly desirable transfer function, with a turns ratio N of 2, yields a gain of 20 when at a duty ratio of 0.6. This low of a duty ratio is highly helpful because at this duty ratio the voltage stress of the active switches is only 2.5 times the input voltage. At an input voltage of 20V the switch stress is only 50V, meaning that low voltage, high current, low on-resistance MOSFETs can be used. The first graph, figure 3.5, plots the voltage gain of this converter vs. the duty cycle D, and shows how the turns ratio affects the possible gain. The next graphs, figure 3.6 and 3.7, show the active switch voltage stress at different duty cycles.

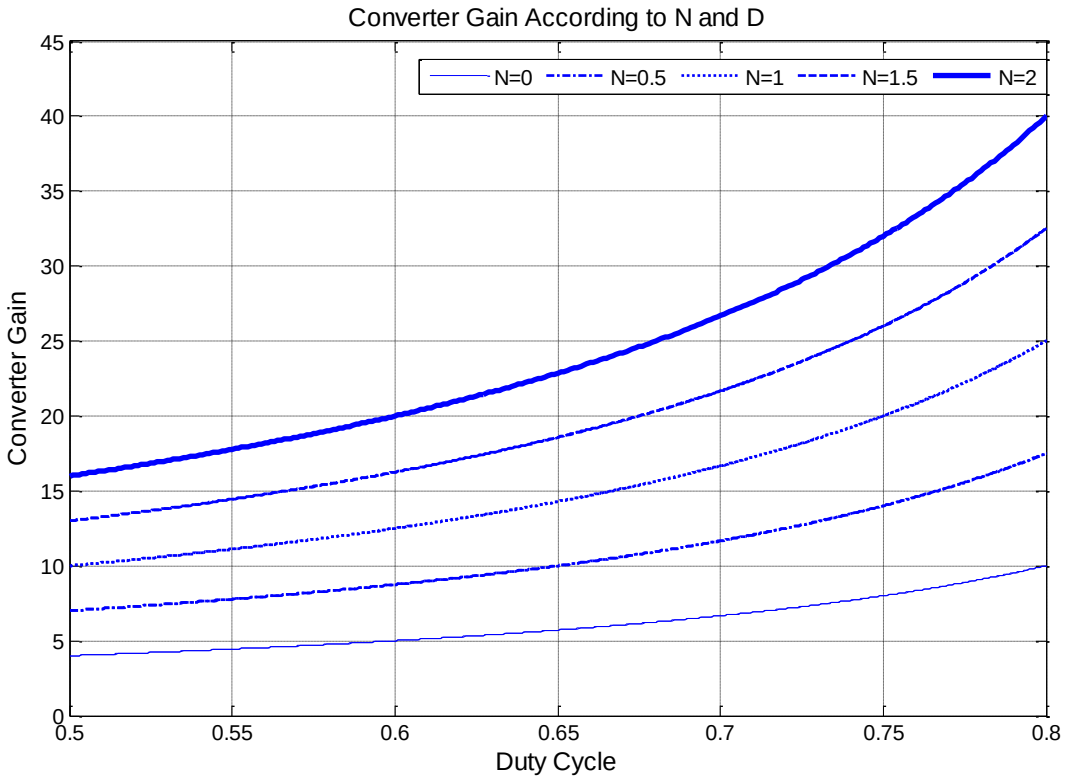

Figure 3.5. Converter gain vs. duty cycle and turns ratio

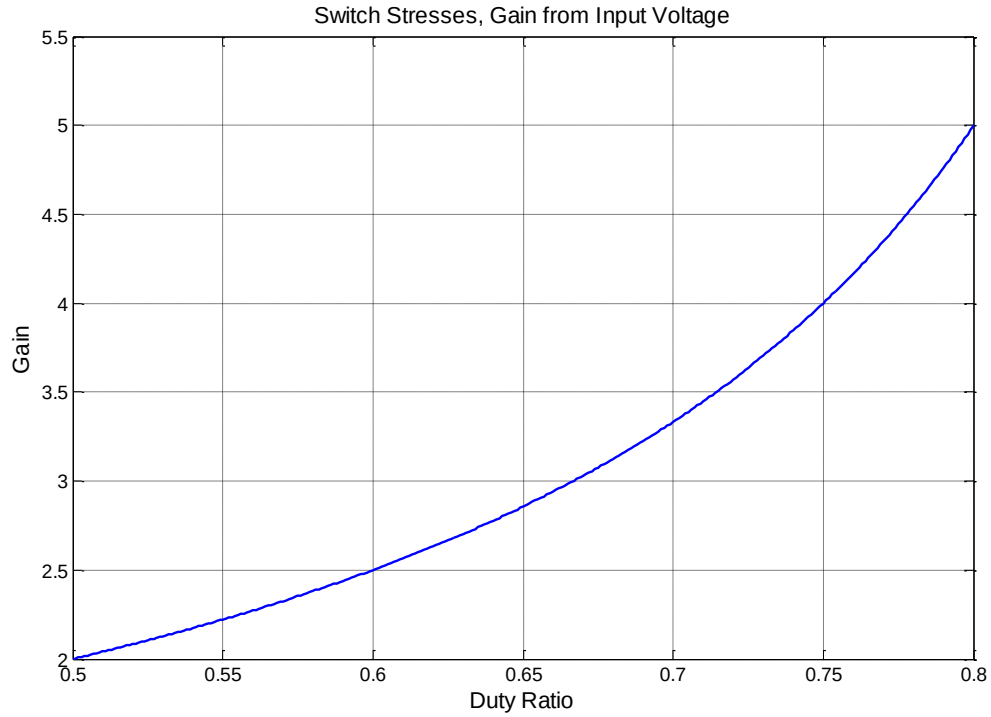

Figure 3.6. Active switch voltage stress vs duty cycle, multiple of input voltage

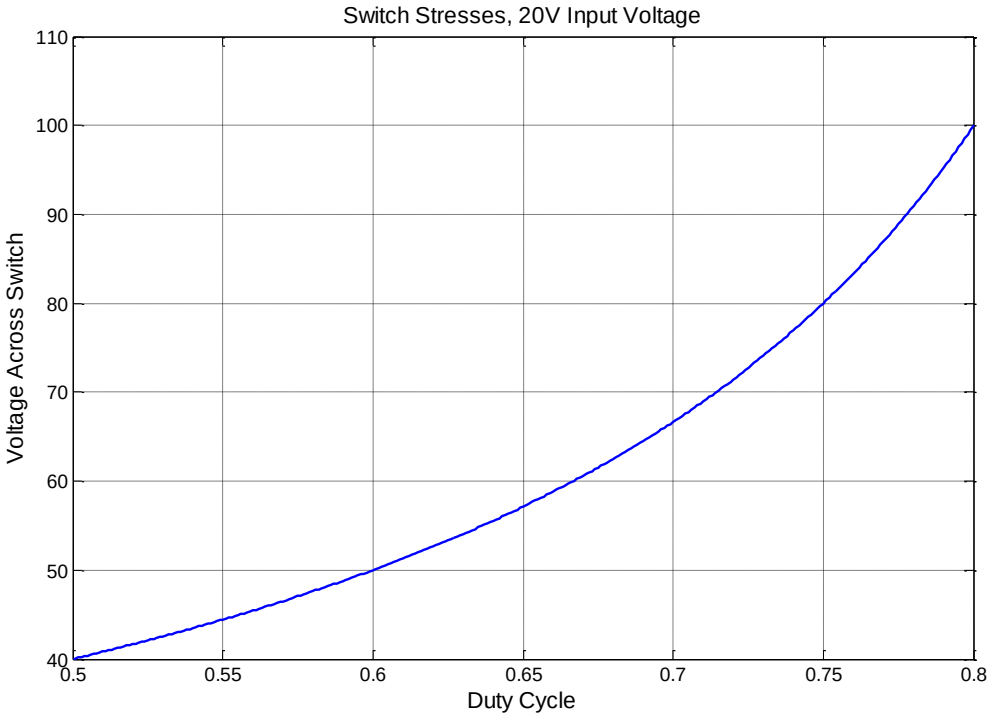

Figure 3.7. Active switch voltage stress vs. duty cycle, input voltage 20V

An interesting point to examine about the gain of this converter is the effect the multiplying cell. In section 2.4 the interleaved boost converter with intrinsic voltage doubler could only attain a doubling effect for the simple reason that only one component, inductor L2, and one stage of the converter interacted with the multiplying capacitor in the charging phase. In this converter, however, when adding the multiplying cell to the interleaved coupled inductor boost converter, the capacitor interacts with both stages in the capacitor-charging mode IV. This both increases the overall voltage gain of the converter and makes more effective use of the system components. It is the configuration and constant use of the coupled inductor coils in each stage which makes this converter desirable and the multiplying cell so effective at bringing the topology to its exceptional transfer function.

3.3.2 Input Current. Discussed in the introduction to this thesis were two requirements for a DC-DC solar microconverter. The first, a high transfer ratio, has already been demonstrated by this converter. The second requirement, continuous input current, is also an advantage of this converter. Similar to the interleaved coupled inductor boost converter the orientation of the coils in the N2 windings counteracts the change in current each leg experiences when switches are turned off and on, leaving the overall input current to not experience any large jumps.

The addition of the output voltage multiplier cell, however, changes the equivalent current sharing between the two stages in the system. In an interleaved coupled inductor boost converter, the energy stored and current through each of the magnetizing inductances is equivalent. In this converter, the multiplier cell and constant duty cycle causes the current through each switch to be non-symmetrical. This does not cause the switches to carry a different average current, it just changes the waveform each switch experiences.

The magnetizing inductance in the second stage carries more current than the first stage. In the simulation, Lm1 carries an average of 7.48A and Lm2 carries an average of 12.35A. The switch in the first stage, S1, carries a higher peak current than the second switch, S2. S1 experiences its highest peak current when switch S1 turns to the OFF state. This occurs in mode IV because switch S1 must carry both the current flowing through the magnetizing inductance and the current which is charging capacitor C1. In contrast,

the second stage never carries additional current from the first stage. Switch S1 only carries current originating from the first winding of the coupled inductor, leading it to not have as significant of a peak current.

This leads to an additional effect on the N2 windings of the converter. Since the N2 windings of the upper stage carries current both forwards and backwards in modes II and IV, it experiences a higher RMS current that the lower stage N2 windings, which only carry current in mode IV. This means that the converter could be designed with the N2 windings serving the lower stage being of smaller diameter wire than the upper stage, potentially augmenting converter cost and size.

While the addition of the voltage multiplier cell augments the current flowing through each of the switches, it does not change the ideal triangular waveform which is seen in an interleaved coupled inductor boost converter. Any non-symmetrical behaviors in the switches and magnetizing inductances cancel out overall, preventing the input current from becoming discontinuous. This advantage allows the proposed topology to be used for a DC-DC solar microconverter. Figures detailing the previously described system observations are found below from a simulation operated under previously stated conditions, input voltage of 20V, output voltage of 400V, output resistance of 400Ω, output power of 400W, duty cycle of 0.6, turns ratio of 2, magnetizing inductance of 100μH, and output capacitance of 10μF. Figure 3.8 show the input current to the converter, figure 3.9 shows the active switch current, figure 3.10 shows the magnetizing inductor current, figure 3.11 shows the magnetizing inductor currents imposed upon the active switch currents, and figure 3.12 shows the N2 winding currents.

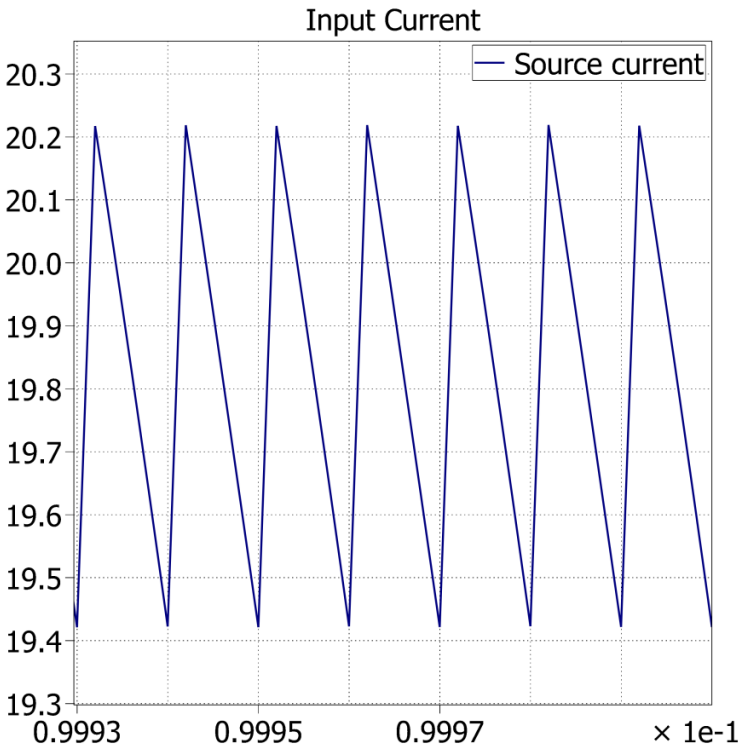

Figure 3.8 Input current waveform

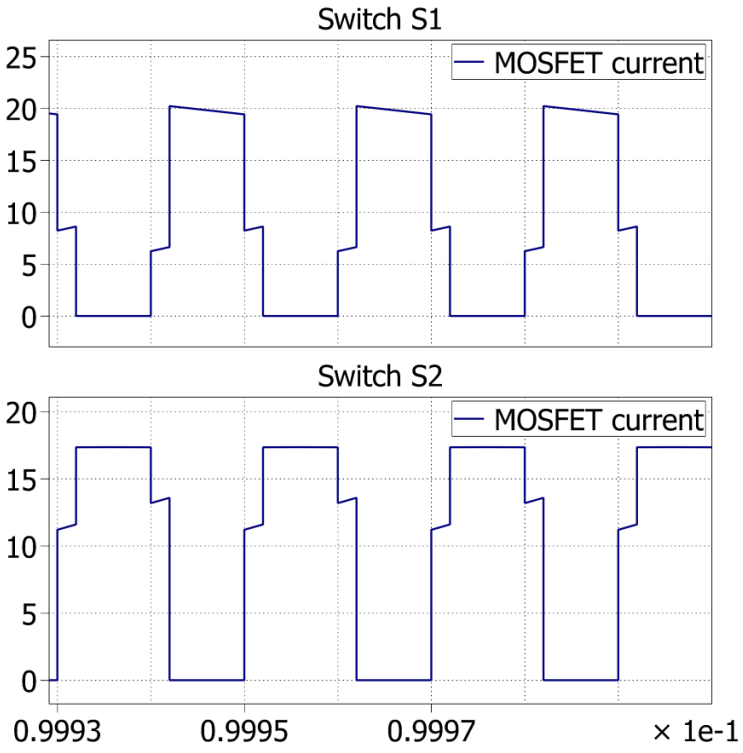

Figure 3.9. Active switch current waveform

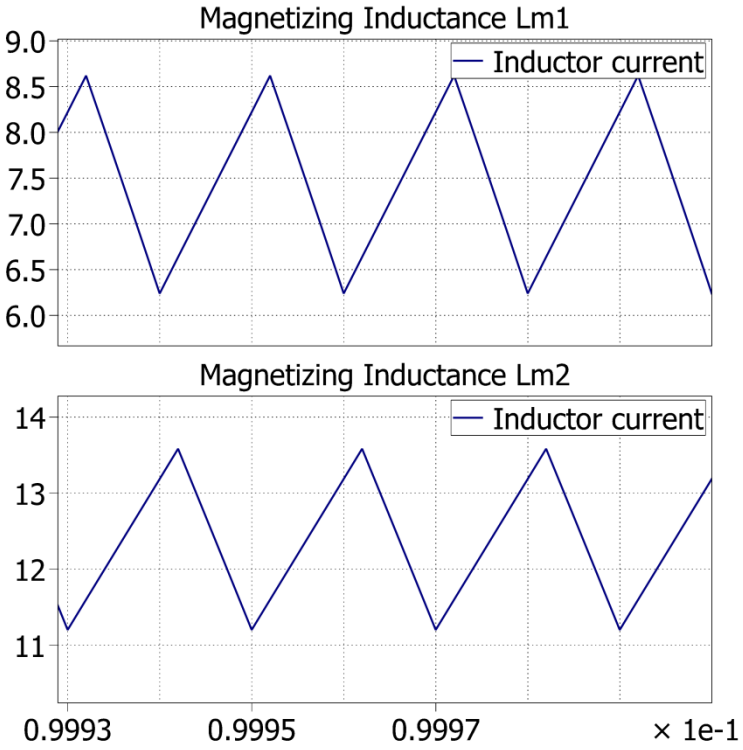

Figure 3.10. Magnetizing inductance current waveform

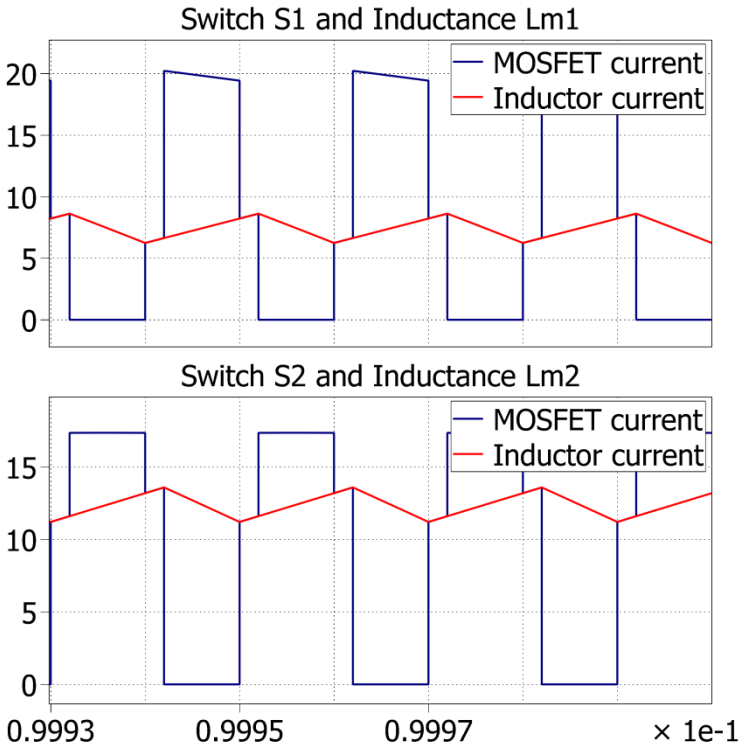

Figure 3.11. Active switch and magnetizing inductance current waveform

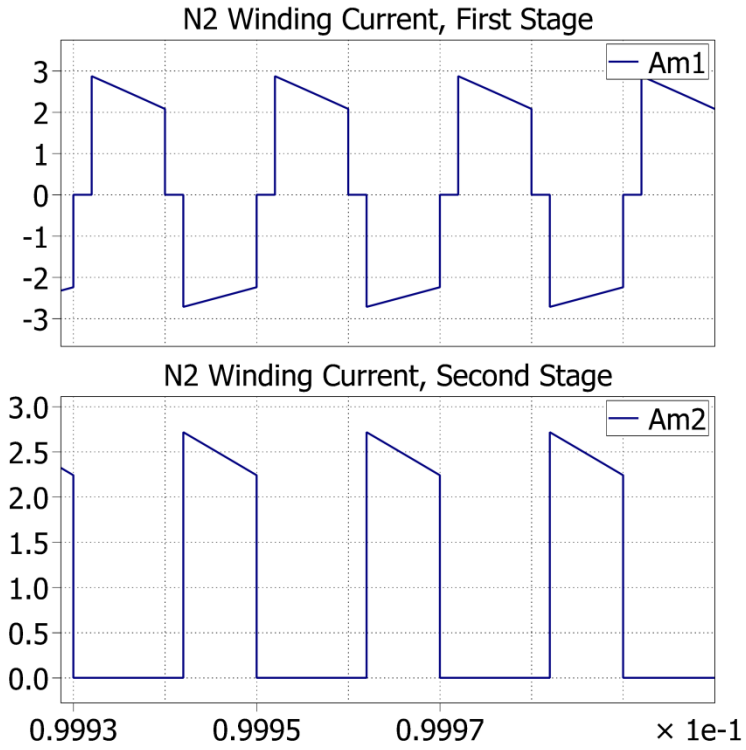

Figure 3.12. N2 winding current waveform

3.3.3 Component Stresses. Another advantage of this converter is, despite and because of its large gain, the voltage and current stresses on the different system components are all very reasonable. In other converters with a less desirable voltage transfer function the converter would likely need to be run at a higher than ideal duty ratio to produce the required output voltage. Since many of these converters have a switch stress equivalent to that of a normal boost converter's gain of X (see equation 2.4), the gain of the converter should primarily come through other methods, such as increasing the turns ratio, to keep the duty cycle and switch stresses as low as possible. The previous figures 3.6 and 3.7 illustrated this consideration well.

Section 3.2.2 also discussed the stresses on the system diodes. The simulation results show a voltage stress across diode D2 of 500V with a 400V output. While this is a large voltage across the diode it is important to consider the current through a component as well. In general, it is acceptable for components in a system to have either a large voltage stress or a large current stress, but not both. This is because the larger current a

component is required to carry the lower the on-state resistance of the component needs to be. In order for a component to be capable of handling larger voltages it is common for the on-state resistance and other negative component characteristics to increase. The easiest way to avoid these negative attributes is to design the system so components do not experience both extremes of high voltage and high current.

For each of the switching components in the system, none experience large voltage and current stresses. Switches S1 and S2 experience large current stresses, and diodes D1 and D2 experience large voltage stresses. For a visual explanation of this, simulation results for S1, S2, D1, and D2's voltage and current stresses are shown below for the parameters given in 3.3.2. Figure 3.13 shows the voltages across switches S1 and S2, figure 3.14 shows the voltages across diodes D1 and D2.

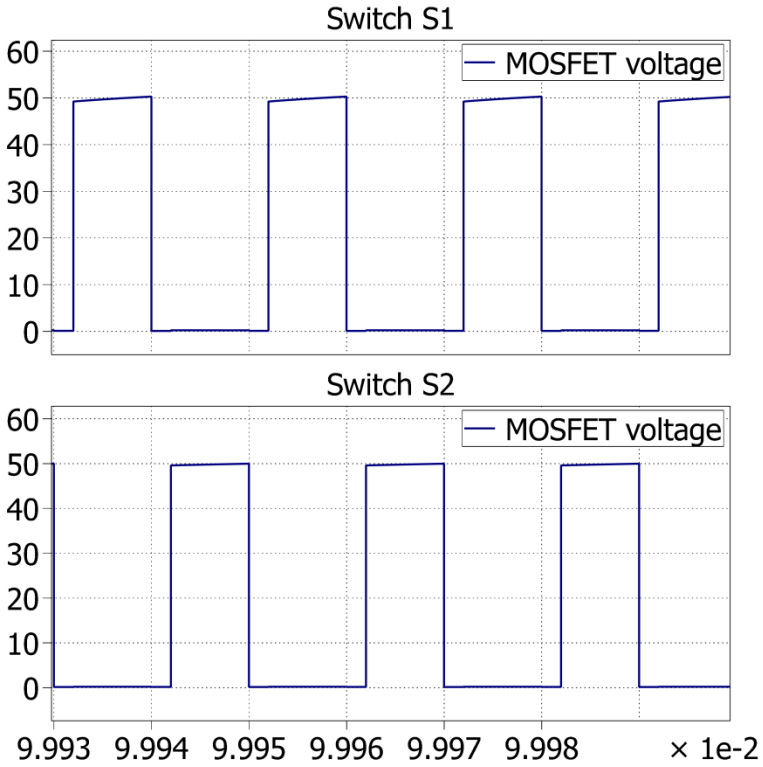

Figure 3.13. Active switch voltage stress

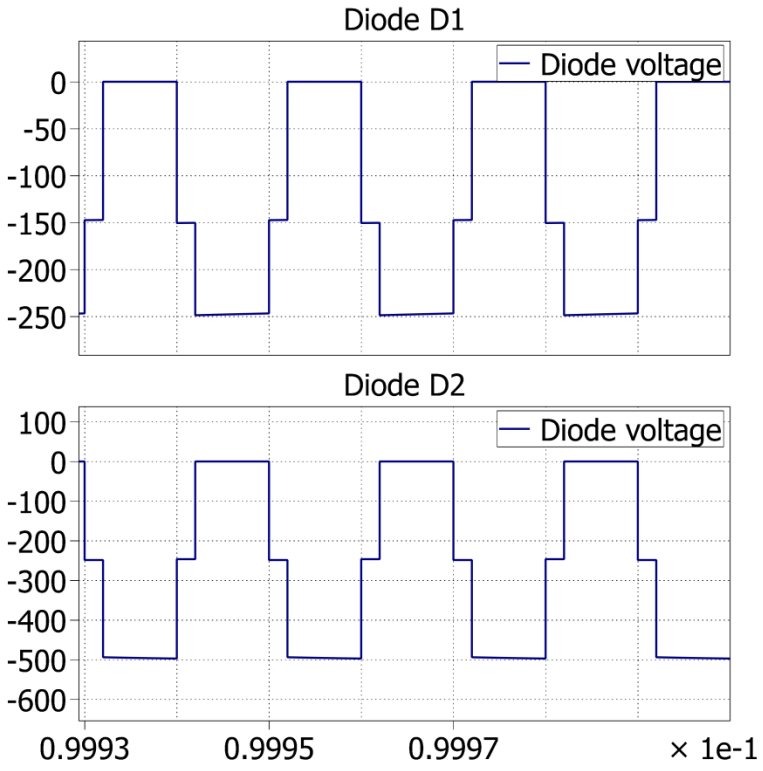

Figure 3.14. Passive switch voltage stress

An important design consideration is how the stresses of the switches changes according to the turns ratio and duty cycle. Figure 3.6 and 3.7 showed how the voltage across the active switches and diodes changed according to the duty ratio. Figure 3.15 shows how the voltage across D1 changes according to a change in duty cycle and turns ratio, and figure 3.16 shows the same for D2. These graphs show the voltage stress in multiples of the input voltage, so a stress of 20 and an input voltage of 20V produce a switch stress of 400V.

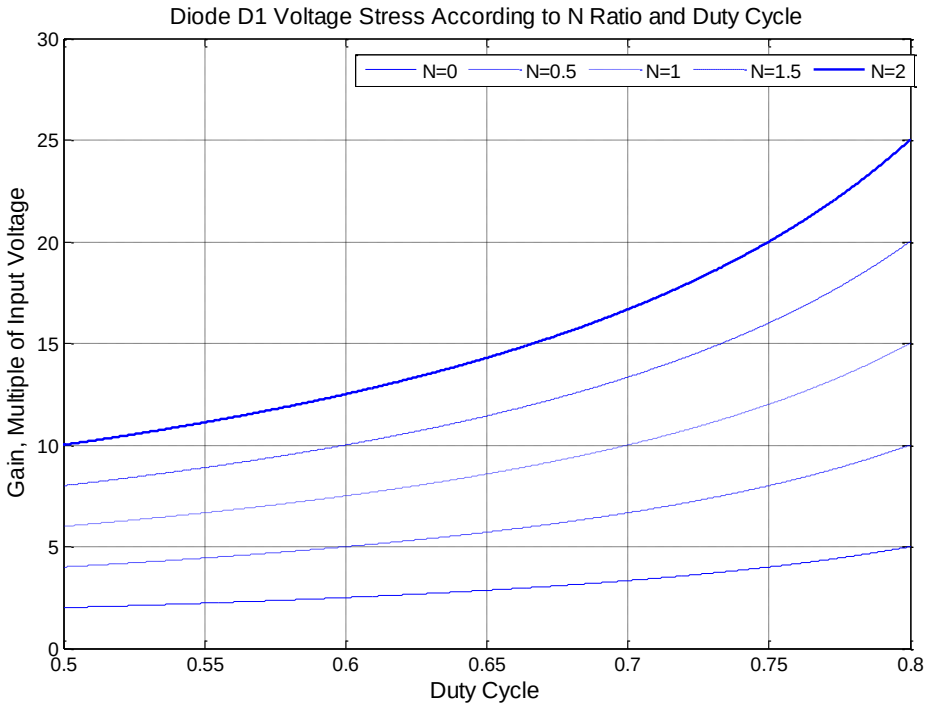

Figure 3.15 Diode D1 voltage stress in multiples of input voltage

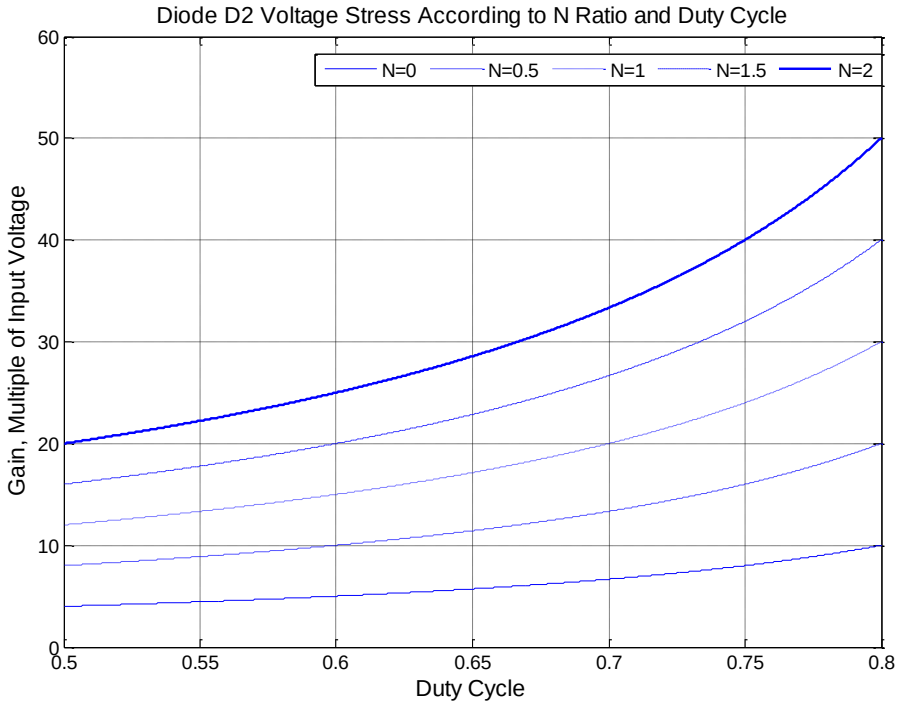

Figure 3.16 Diode D2 voltage stress in multiples of input voltage

While not a switch itself, it is also important to know what type of maximum voltages capacitor C1 could experience. As such, the graph relating the voltage present across C1, related to duty cycle and turns ratio, is shown in figure 3.17 below. Since the peak voltage of C1 has the same equation as D1, the two curves are the same.

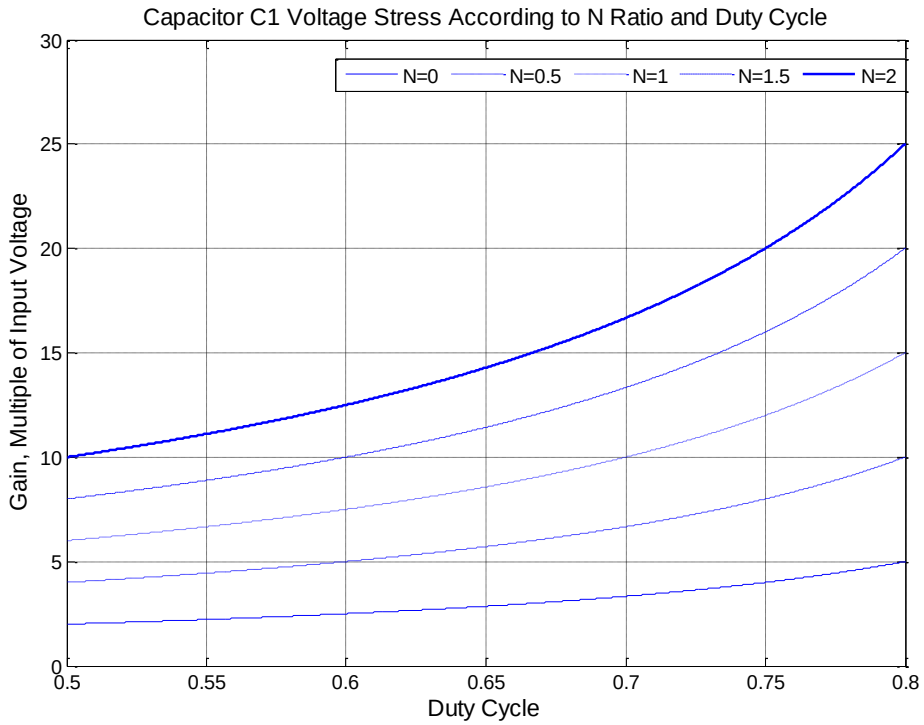

Figure 3.17 Capacitor C1 voltage stress in multiples of input voltage

3.4 IDEALIZED SIMULATION RESULTS

Several simulation results for the converter have already been shown in the previous sections, but there are still figures which need to be shown to determine if our converter is acting as it should. All of the previous and the following simulation figures use these simulation parameters: input voltage of 20V, output voltage of 400V, output resistance of 400Ω, output power of 400W, switching frequency of 50kHz, duty cycle of 0.6, turns ratio of 2, magnetizing inductance of 100µH, and output capacitance of 10µF. Not mentioned previously is the small resistances and forward voltage drops added to the

switches to create a stable simulation. Simulation MOSFETs used 0.01Ω ON-state resistances, and simulation diodes used 0.01Ω ON-state resistances and 0.01V Vf forward voltage drops.

The previous figures detailed specific component voltages and currents, but it is necessary to determine if the converter is operating in accordance with the design equations found. Figures 3.18 shows the output voltage and input current waveforms of the converter, and figure 3.19 shows capacitor C1's voltage and current waveform.

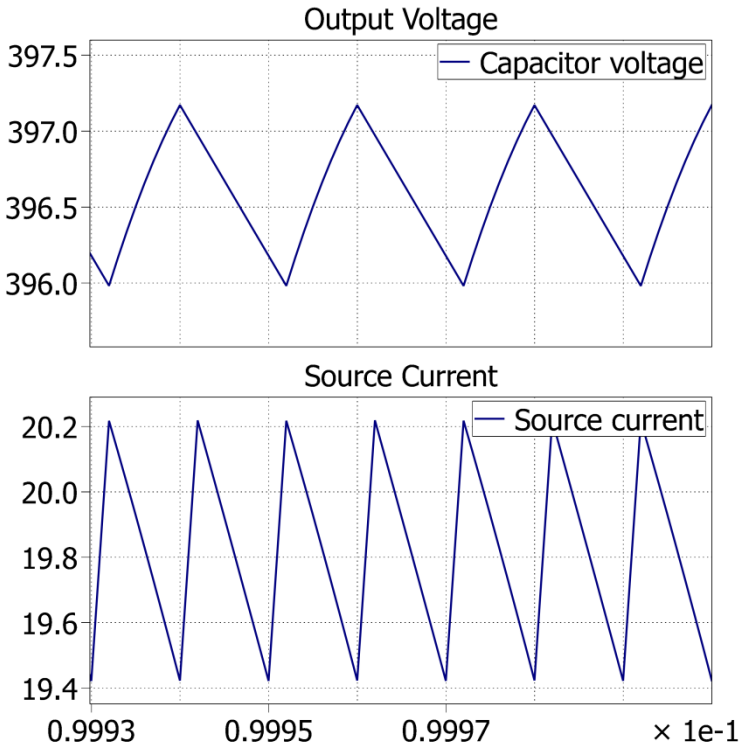

Figure 3.18. Output voltage and input current waveform

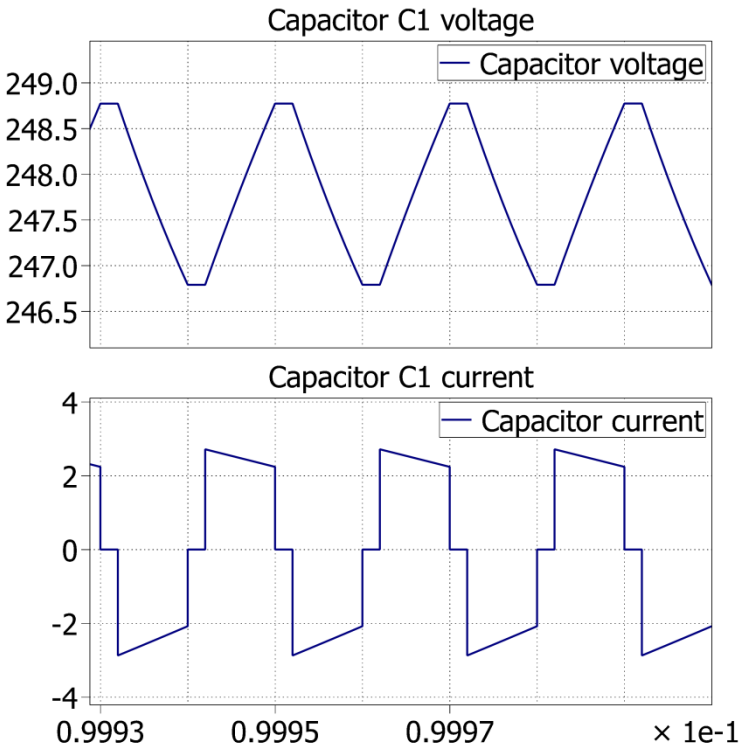

Figure 3.19. Capacitor C1 voltage and current waveform

The design equations, for a turns ratio of 2 and a duty cycle of 0.6V, predict an output voltage of 400V and a C1 voltage of 250V. These design equations successfully predicted the simulation results, meaning the results can be considered valid.

3.5 SYMMETRICAL CONVERTER OUTPUT

The previous parts of this section, 3.1-3.4, discussed an interleaved coupled inductor boost converter with multiplier cell whose output is non symmetrical. The next part of this section will detail this converter with a symmetrical output multiplier cell. This output cell results in the same transfer functions and characteristic equations as the proposed converter, with a few operational differences which will be described below [21, 22] . Figure 3.20 shows the proposed converter with two of its operating modes.

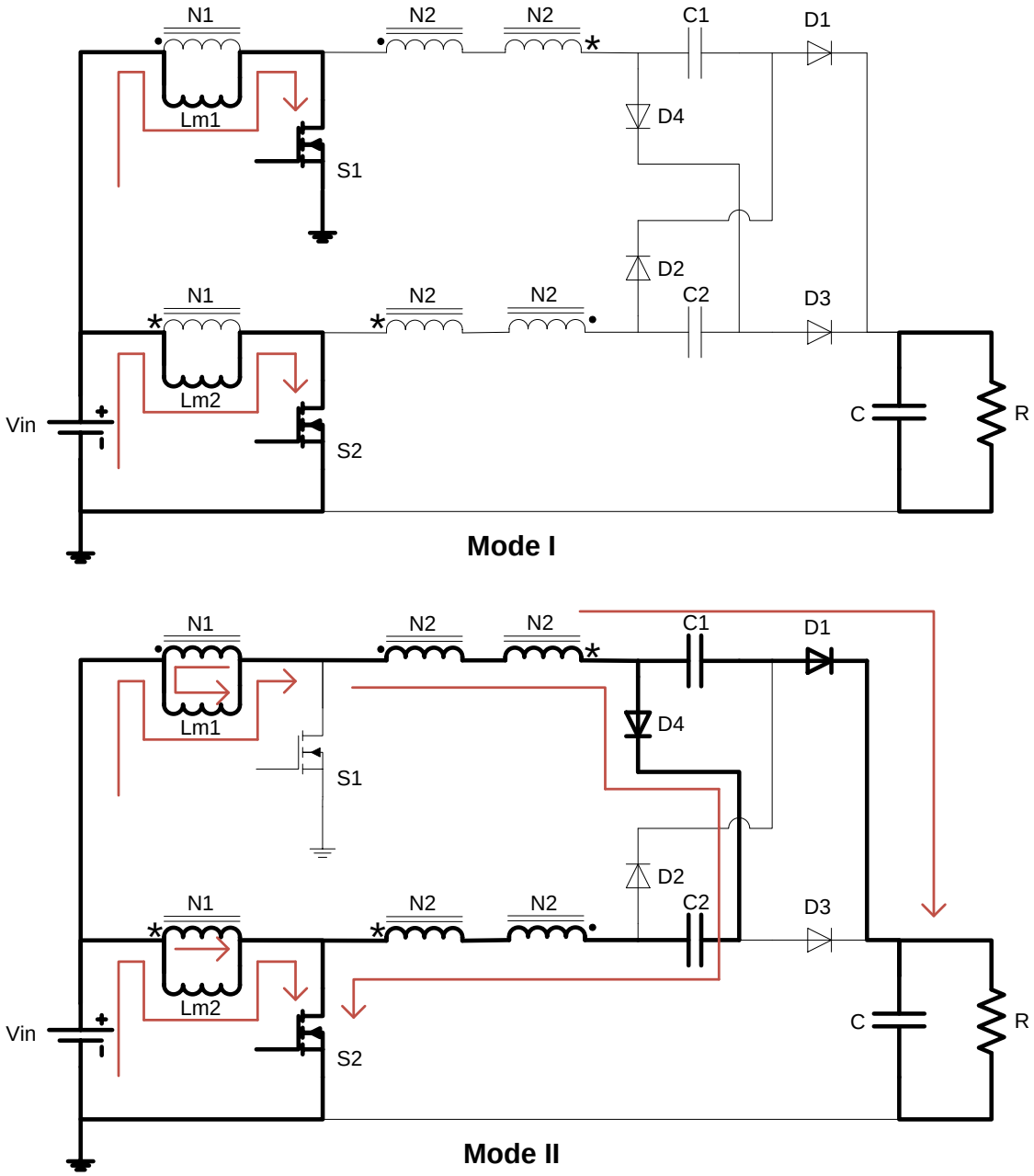

Figure 3.20. Symmetrical output converter operating modes

3.5.1 Modes of Operation. The symmetrical output of the converter changes two of the four modes of operation, modes II and IV. In the proposed converter, one of these modes, mode II, was responsible for transferring power to the output, while the other mode, mode IV, was responsible for creating the charge across the multiplying cell's capacitor. When the output voltage multiplying cell is symmetrical, however, the effects of these two modes happen at the same time. For this reason only two modes need to be discussed, as the other two modes have the same effect but with the opposite stage used.

Mode I of the converter is very similar to mode I of the proposed converter. It, as well as mode III, occurs when both S1 and S2 are in the ON state. In this mode the current and energy through the magnetizing inductances is increasing and all system diodes are in the OFF state. The output power is being provided by the output capacitor C.

Mode II, the same as mode IV with the reciprocal switches, diodes, and capacitor effected, occurs when switch S1 turns to the OFF state. When this happens, the energy present in magnetizing inductance Lm1 causes two diodes, D1 and D4, to enter the ON state. In this mode, unlike in the proposed converter, energy from Lm1 is moved to both charge a multiplying cell’s capacitor, C2, and a multiplying cell’s capacitor, C1, is discharged to charge the output capacitor. As this happens the energy and current flowing through Lm1 decreases and the output power and capacitor C1 charging current is being provided by D1.

3.5.2 Advantages and Disadvantages. Compared to the proposed topology, the interleaved coupled inductor boost converter with symmetrical output multiplier cell has some advantages and disadvantages. The first advantage is that keeping the output of the converter symmetric keeps the rest of the converter operating symmetrically. With the proposed topology switches S1 and S2 operate without symmetric currents. While this was previously described as not being a true disadvantage, keeping the currents of the switches symmetric removes one part of the design and optimization process.

Another positive aspect of this converter is the reduction in the current carried by the high-voltage output components. Section 3.3.3 discussed advantages associated with keeping high voltage components low in current and the additional reduction in current carried through the output diodes could prevent some additional system losses.

These additional components can also be considered a disadvantage. Adding these components would increase the cost and complexity of the system while not adding any additional functionality. Furthermore, these added components could produce more instead of fewer system losses. While the current is split through the output components the output diodes would switch more often, causing more switching losses in the system which would likely offset any gains achieved through current sharing.

While this converter shares challenges with the proposed topology which will be explained in detail in section 4 it is not able to implement the simple solution proposed in section 4. While this does not prevent the converter from using other solutions to the challenges, this limitation led the symmetrical output converter to be treated as a secondary, rather than a primary thesis topic.

3.5.3 Simulation Results. Since the interleaved coupled inductor boost converter with symmetrical output multiplying cell has many similarities to the proposed converter it can be observed that the equations governing the component stresses remains the same. This does not mean that the waveforms of these switches will stay the same as the proposed converter, and as will be shown below, they do not. The first thing to verify is that the output voltage and input current remain acceptable for use in a high gain DC-DC converter. Figure 3.21 shows the converter's output voltage and input current. All simulation results are for the same specifications used in 3.4.

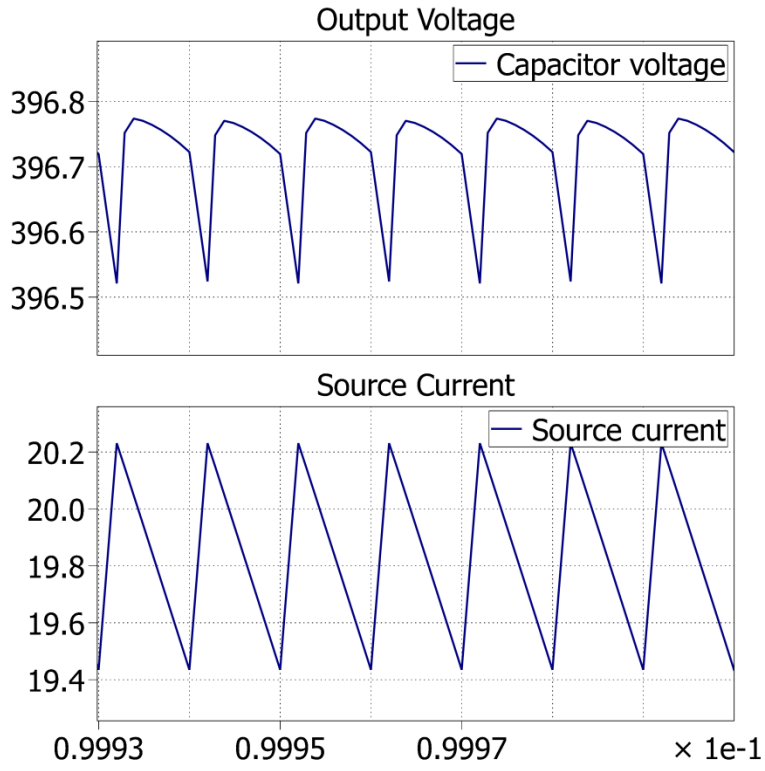

Figure 3.21. Symmetrical multiplier converter output voltage and input current

The output voltage does not have as ideal of a waveform as the non-symmetrical, proposed converter, but its ripple is still acceptably small. The input current to the symmetrical converter is still continuous with a small ripple, leading one to conclude this converter would be suitable for a DC-DC solar converter. The waveform showing the current through each switch is shown below in figure 3.22, the current through each magnetizing inductance is shown in figure 3.23, and the current through each magnetizing inductance superimposed upon the switch current is shown in figure 3.24.

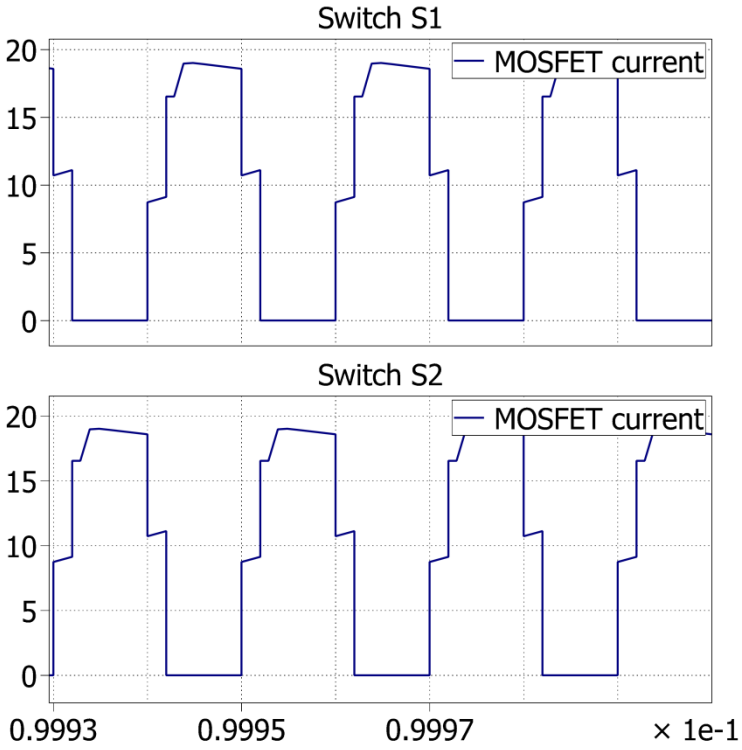

Figure 3.22. Symmetrical multiplier converter active switch current

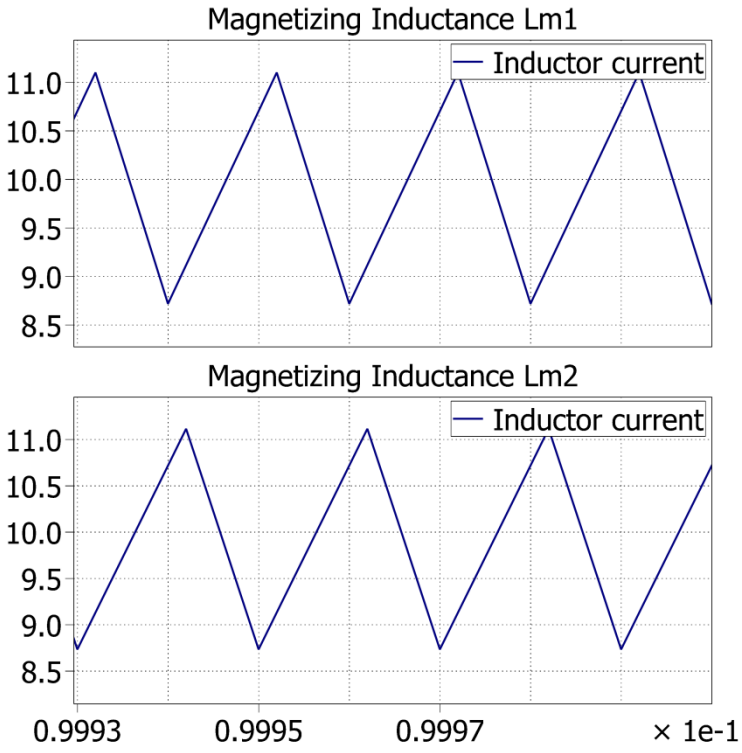

Figure 3.23. Symmetrical multiplier converter magnetizing inductance current

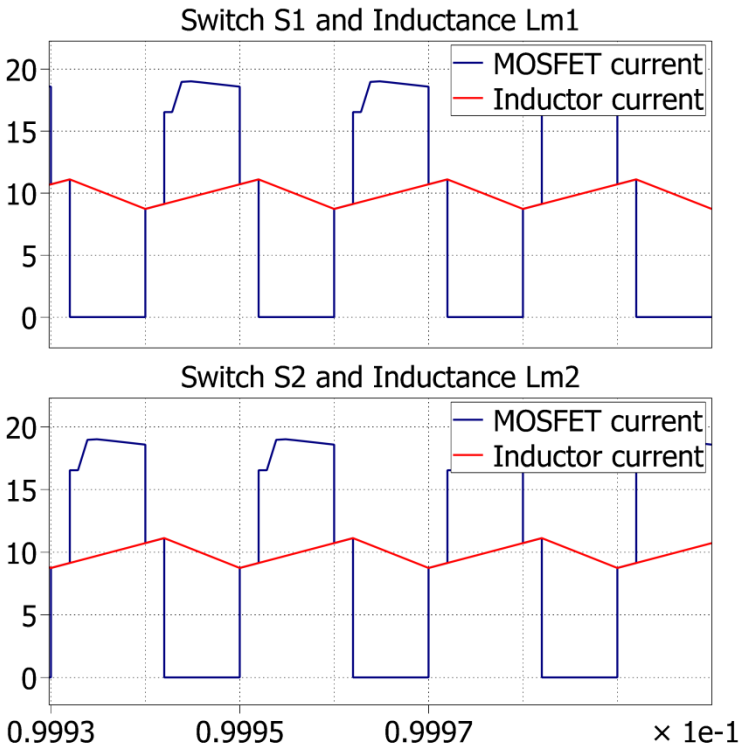

Figure 3.24. Symmetrical multiplier converter active switch and magnetizing inductance current

As expected the current through each switch and the current through each inductor is the same in each stage. Quite noticeable in each switch current is a notch in the current waveform before the peak current is reached. The peak current in each of the switches occurs when the opposing stage's switch turns to the OFF state and current charging the multiplying circuit flows through the ON state stage's switch. This notch occurs due to interactions of the output multiplying circuit with the output capacitor. When the switch first turns off a larger portion of the stage's current flows to the output capacitor instead of charging the opposite stage's multiplying circuit. This creates an initial dip in the current of the opposite stage's switch until the current of the output diodes equalizes. Figure 3.25 shows diode D1 and D4 current, and figure 3.26 shows diode D1 and D4 current, as well as the summation of these two currents.

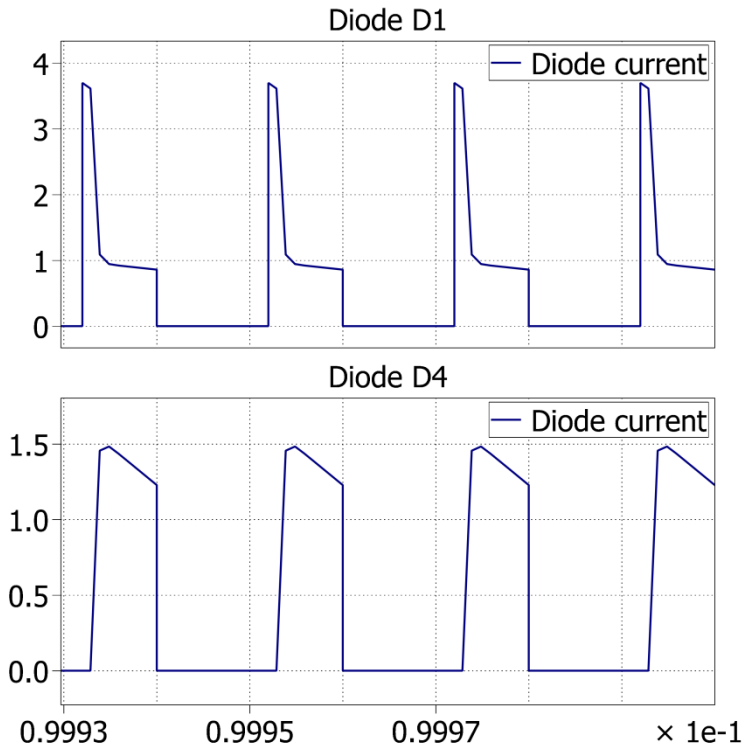

Figure 3.25. Symmetrical multiplier converter D1 and D4 current

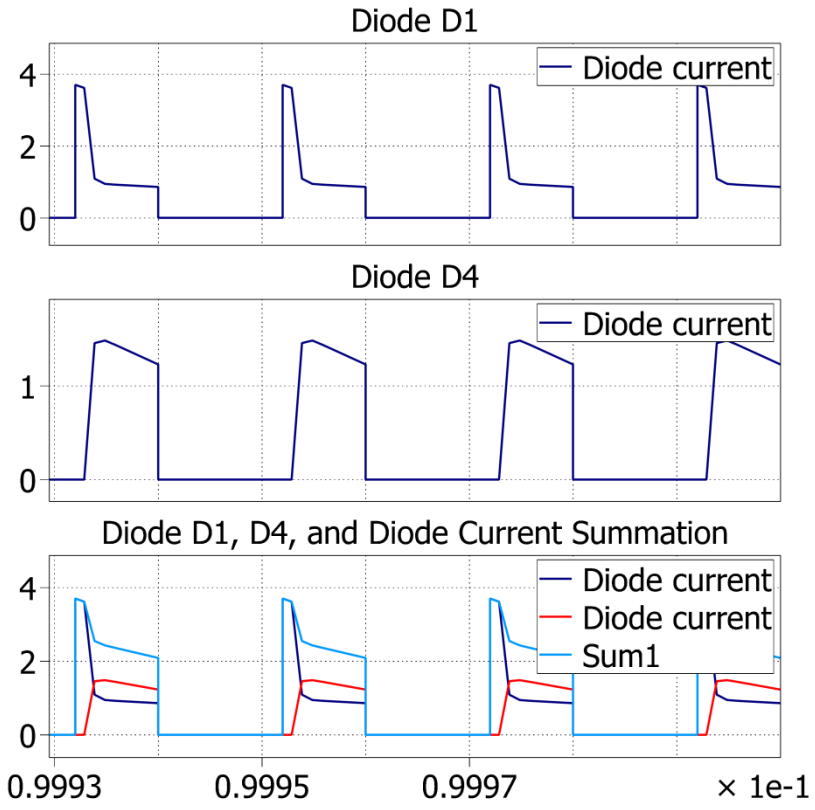

Figure 3.26. Symmetrical multiplier converter D1, D4, and summation current

This abnormal current flow almost creates a trapezoidal waveform when the currents are summed, but as seen it does not do a perfect job. This is likely due to the high rate of charging the output capacitor initially requires. After the initial charging current peak, diode D1 returns to a current of 1 amp. Given the system parameters this is the continuous current required by the output resistance R. This shows that the diode initially carries a large current to charge the output capacitor, and when the capacitor is fully charged, the diode reduces its carried current to match that required by the output resistance. Figure 3.27 shows the output capacitor's voltage and current waveforms, and figure 3.28 shows capacitor C1's voltage and current waveforms.

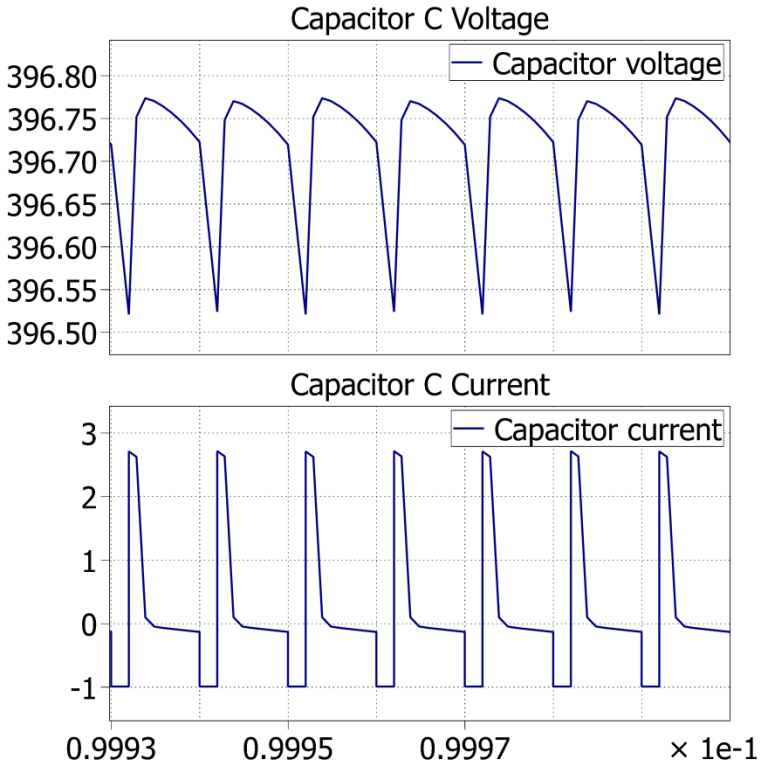

Figure 3.27. Symmetrical multiplier converter output capacitor voltage and current

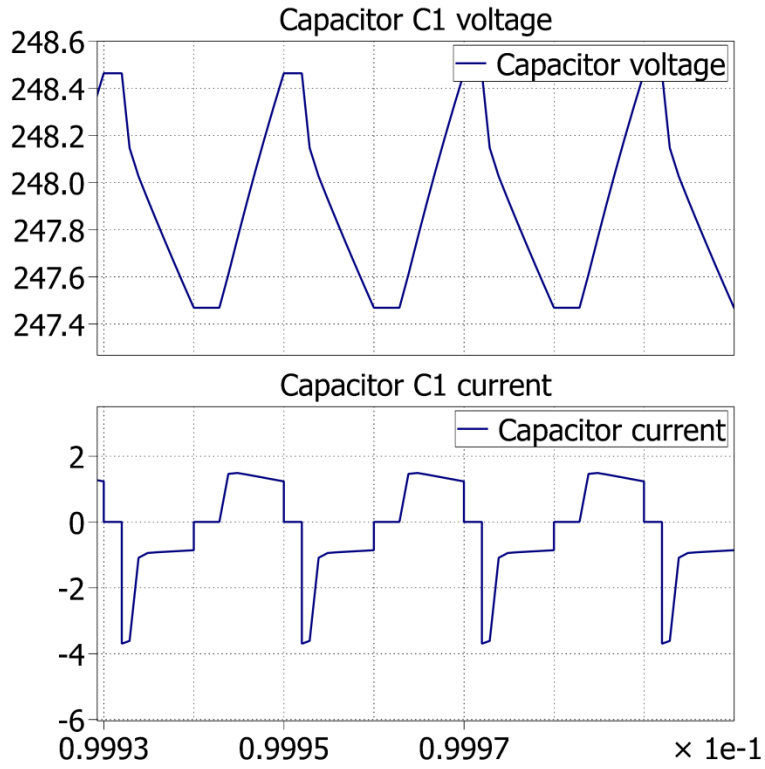

Figure 3.28. Symmetrical multiplier converter capacitor C1 voltage and current

Since the diode provides much of the output current, the output capacitor can be much smaller than the one shown here. In this case, a 400V output converter using a reasonable 50kHz achieves a remarkable output voltage ripple of less than 0.3V. This comes at the cost of higher output diode peak-current levels, and more system components. Overall, this converter has some advantages and disadvantages compared to the proposed non-symmetrical output converter, and could likely be used as a high-gain DC-DC solar power converter.

4. CHALLENGES OF THE TOPOLOGY: SWITCHLESS CLAMP

4.1 TOPOLOGY CHALLENGES

While this converter has several properties which make it desirable when used for a high gain DC-DC solar converter there are challenges this topology faces when the converter is not considered ideally. In the ideal simulation shown in section 3 no switch parameters were taken into consideration, including on-state resistance and output capacitance, and no leakage inductance was included. Figure 4.1 shows the proposed topology when considered non-ideally.

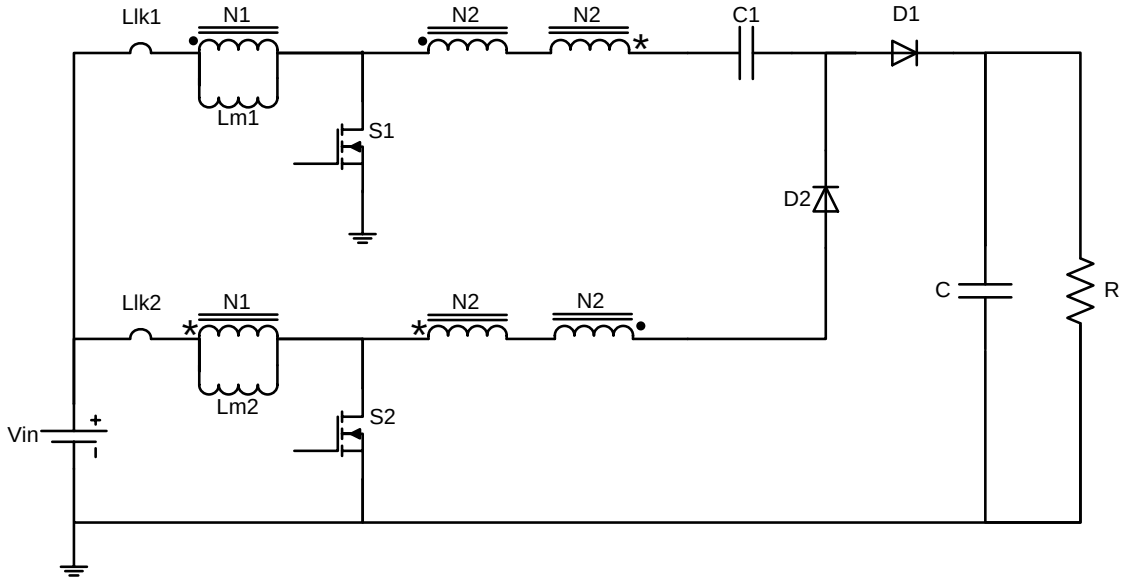

Figure 4.1. Non-ideal interleaved coupled inductor boost converter with multiplying cell

Including the switch parameters into the simulation does not cause a large change in system dynamics, the main difference is slightly reduced output voltage at the same duty cycle and reduced system efficiency.

A large difference in system dynamics occurs when adding even a small amount of leakage inductance. In this system the current flowing through each winding of the coupled inductors experiences a large change when a switch turns to the ON or OFF state. Leakage inductance present in each winding, or inductance which is not coupled

with the other inductor windings, resists these rapid changes in current. In the instant a system switch is turned to the OFF state a large voltage spike occurs across the switch, the intensity of which depends on the relationship between the energy stored in the leakage inductance and value of capacitance across each switch. This is the challenge associated with this converter, and generally the largest challenge of converters which utilize coupled inductors.

Thankfully though this leakage inductance does not have an entirely negative influence on the system. The same system function which causes voltage spikes across the active switches also causes the diodes in the system to be soft-current switched. In a non-soft-current switched system the diodes continue to conduct for a short period in the instant they are reverse-biased, causing additional conduction and switching losses. Diodes have specifications describing how many amps per second of change they are able to handle without reverse-conduction. As the active switch in each stage is turned on in this converter the leakage inductance in the N2 windings allows the current in each stage's diodes to ramp down slowly, preventing reverse-conduction and reducing system losses.

4.2 CLASSICAL METHODS OF CLAMPING

The problematic voltage spikes across the active switches in the system require the use of a clamping circuit. A clamp is used in the system to add a location where transient energy can be stored so that it does have any harmful effects on the rest of the components in the system. Existing methods of clamping a system will now be discussed to provide an argument for the use of the developed clamp presented in the following section.

4.2.1 RCD Clamp. The RCD clamp utilizes a resistor, a capacitor, and a diode to limit the voltage spikes across the system switches. Figure 4.2 shows the configuration of this clamp.

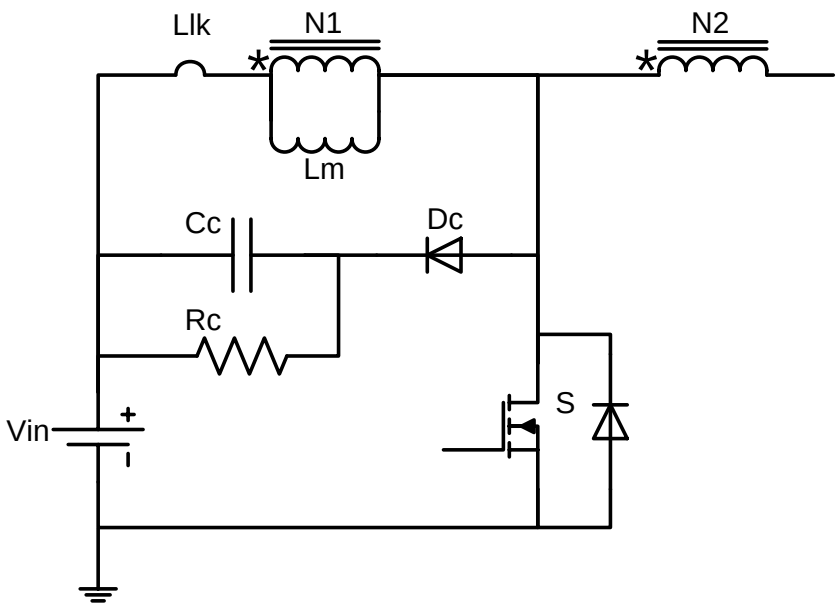

Figure 4.2. RCD clamp schematic

When the active switch turns to the OFF state the energy stored in the leakage inductance causes an increase in the voltage across switch S. Eventually the switch voltage increases enough to cause diode Dc to turn to the ON state. This is determined by the voltage present across capacitor Cc, which itself is a product of the ideal OFF-state switch voltage, input voltage, and speed at which resistor Rc depletes the capacitor's charge. This leads the switch's voltage to be clamped at some value higher than its ideal switch-stress equation would conclude. While problematic at times, careful component design can reduce this issue.

An advantage of this clamp is its simplicity, not requiring any additional system control and adding only simple components to the system. There are many disadvantages to this clamp, the most pointed of which is its usage of the leakage inductance energy. Clamps are most effective when they transfer the leakage energy to some other part of the system, rather than dissipate the energy. In a RCD clamp, all of the leakage inductance energy is wasted as heat, lowering overall system efficiency. Another RCD clamp disadvantage is the design of its components. While the system is rather simple, the resistor and capacitor should be sized to keep the voltage across each switch as low as possible, to keep the component size as small as possible, and to keep the system as

efficient as possible. While not an impossible task, it does require some foresight and planning when implementing the clamp [23, 24].

4.2.2 Active Clamp. The active clamp utilizes an active switch with a capacitor to limit switch stresses. Figure 4.3 shows the configuration of the active clamp.

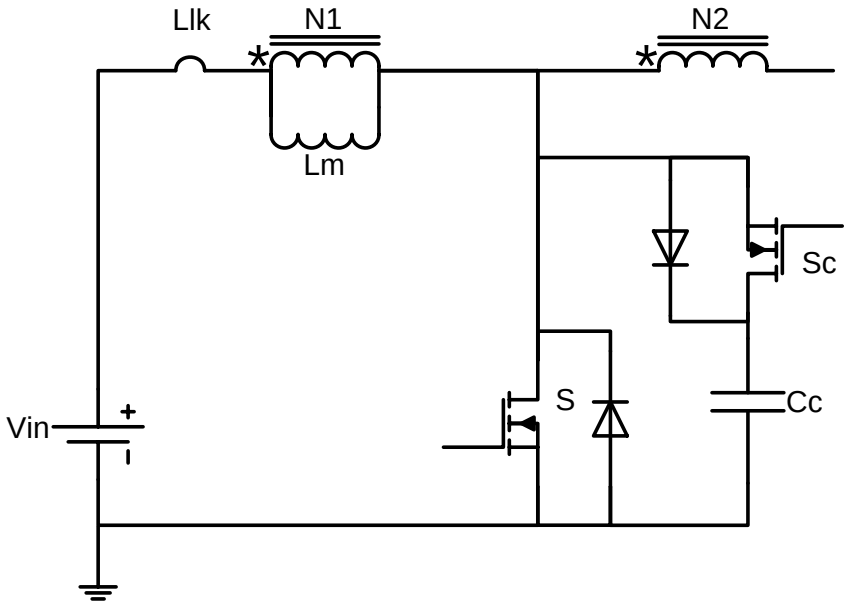

Figure 4.3. Active clamp schematic

When the active switch S turns to the OFF state the energy from the leakage inductance increases the voltage across switch S. When this switch voltage rises above the voltage of capacitor Cc, the diode across switch Sc turns to the ON state, allowing current to flow and charge Cc. Capacitor Cc's voltage effectively becomes that of the output of a boost converter, and as such, switch S is effectively clamped to some value slightly above to the switch stress equation voltage of X (see equation 2.4). Eventually, the clamp capacitor is discharged when switch Sc turns ON, and a portion of the energy stored is recycled to the system. When switch Sc is turned on, and what effect turning the switch to the ON state has on the system, depends upon the control scheme used for the active clamp [25-27].

Many variations of the active clamp exist, some achieve soft switching through ZVS (Zero Voltage Switching) or ZCS (Zero Current Switching) by changing when switch Sc turns ON and by sizing capacitor Cc to make a resonant circuit with the leakage inductance. This is the primary advantage of the active clamp, its flexibility to be used in a variety of situations and in a variety of switching schemes. Another advantage of the active clamp is that it makes use of the leakage energy, recycling it instead of dissipating it as heat.

There are disadvantages to this clamp, and one should make certain to note the active clamp's complexity. While the clamp adds only two components, a switch and a capacitor, the real system complexity would come from the control algorithm, which could easily be more involved than the converter's normal switch operation. This unnecessary complexity makes this clamp undesirable for the proposed topology, as the only needed solution is switch voltage spike reduction. For this reason it would be convenient if an effective clamp existed which did not require any control and recycled all of the captured energy.

4.2.3 Passive Lossless Clamp. Another alternative to the previously mentioned clamp is a passive lossless clamp, which utilizes only diodes and capacitors to effectively clamp the switch voltage spikes. Figure 4.4 shows the configuration of the passive lossless clamp.

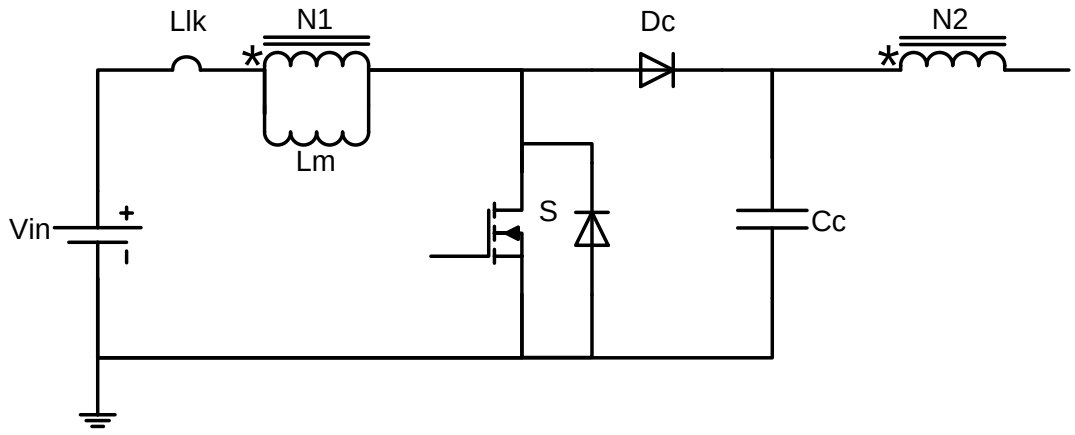

Figure 4.4. Passive lossless clamp schematic

When the active switch S turns to the OFF state the energy from the leakage inductance causes the voltage across switch S to increase. When the switch voltage rises above the voltage of capacitor Cc diode Dc turns to the ON state. This conducts current to charge Cc and the output and also clamps switch S's voltage to that of Cc. This charging only takes place until the leakage energy is dissipated, effectively charging Cc to some value slightly above the ideal switch stress equation (equation 2.4, or X). After the capacitor has absorbed the energy from the leakage inductance diode Dc turns to the off state. Because diode Dc is OFF and in the conduction path of power for the system the current seen at the output is from the magnetizing inductor coupled through the N2 windings. This discharges capacitor Cc, leaving it ready to be charged when the switch turns OFF again. When switch S turns to the ON state, the output current ramps down in accordance with the leakage inductance present in the coupled inductor.

This clamp has the noticeable advantage of its simplicity and lack of control. With only a diode and capacitor this clamp is the most basic viable clamping method. With no control there is no need for complex control algorithms and design equations. This converter also effectively transfers the leakage energy to the output instead of dissipating it, increasing overall system efficiency.

A disadvantage of this clamp is that the clamping diode resides in the main conduction path of the converter. For a converter without a multiplying output circuit this is not an issue as energy from the magnetizing inductance can flow to the output through the coupled N2 windings. For the proposed converter, however, current needs to flow not only towards the output, but also back towards the active system switches to charge the multiplying circuit's capacitor. The addition of this clamp for the proposed topology would prevent the converter from working as designed, severely reducing the output transfer ratio. This eliminates the passive lossless clamp seen here from being used in the proposed converter[19].

4.3 PROPOSED CLAMP

Section 4.2.3 discussed a passive lossless clamp which can be used to effectively mitigate voltage spikes across the active switches. As discussed in that section, the clamp cannot be used for the proposed topology due to the reverse current induced by the multiplying cell. It is easy to notice that in the proposed converter reverse current only flows in the upper stage and not the lower stage. This means the passive lossless clamp as shown in section 4.2.3 will work for the lower stage of the converter, but not the upper stage. It is then possible to protect the upper stage of the converter by connecting a diode from the upper stage's switch to the clamp capacitor in the lower stage. Figure 4.5 shows the schematic for the proposed passive lossless clamp.

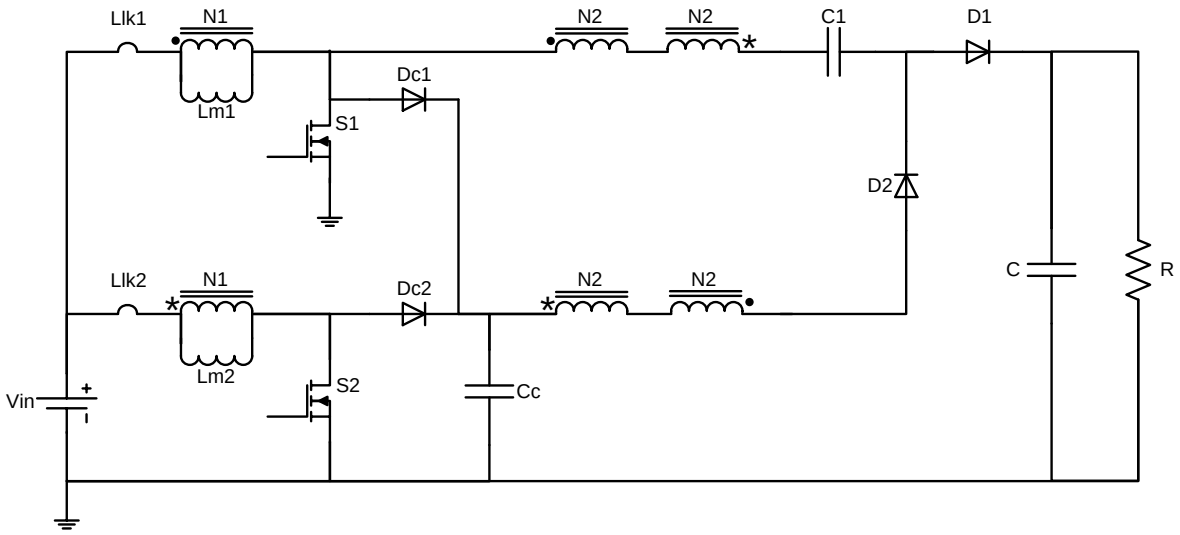

Figure 4.5. Proposed passive lossless clamp

4.3.1 Modes of Operation. The addition of the proposed passive lossless clamp has a large effect on the modes of operation of the converter. While the generalized operation remains the same the instantaneous power flow in each stage becomes more complex as the leakage inductances charge clamp capacitor Cc and the clamp capacitor discharges while charging capacitor C1. There are eight total modes in this converter, of which all will be briefly discussed. This increase in modes occurs due to the action of the clamp with the leakage inductance, having short transient modes where the leakage inductance is either charging or discharging. As these modes are rather complex, the operating modes are shown in figures 4.6 to 4.9 before they are described.

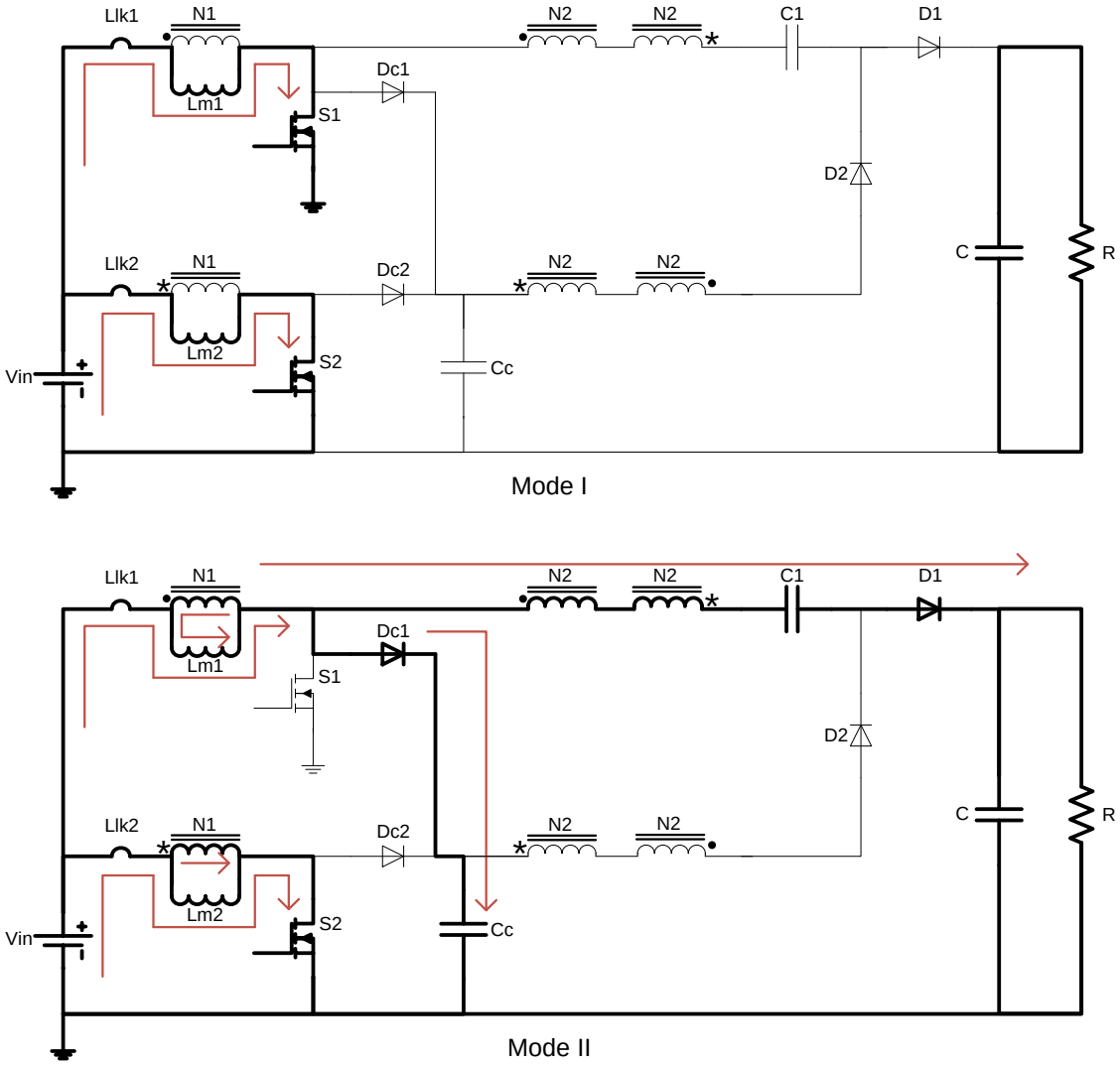

Figure 4.6. Clamped converter operating modes I and II

Mode I of the clamped converter is the same as modes I in the non-clamped converter. Both active switches are in the ON state, increasing the current and energy stored in each magnetizing inductance. The output power is provided by output capacitor C. Depending on system configuration, this mode may not occur at all, mode VIII may become mode II.

Mode II occurs as switch S1 turns to the OFF state. The voltage across the switch increases until diode Dc1 is forward biased, at which time diode Dc1 conducts the extra current from leakage inductance Llk1 to the clamp capacitor Cc. As the leakage inductor current is decreasing to match the current through the coupled windings diode D1

conducts the increasing current of the N2 windings across the upper stage. Power begins to be delivered to the output by diode D1, discharging capacitor C1.This mode ends when the leakage current in each stage equalizes.

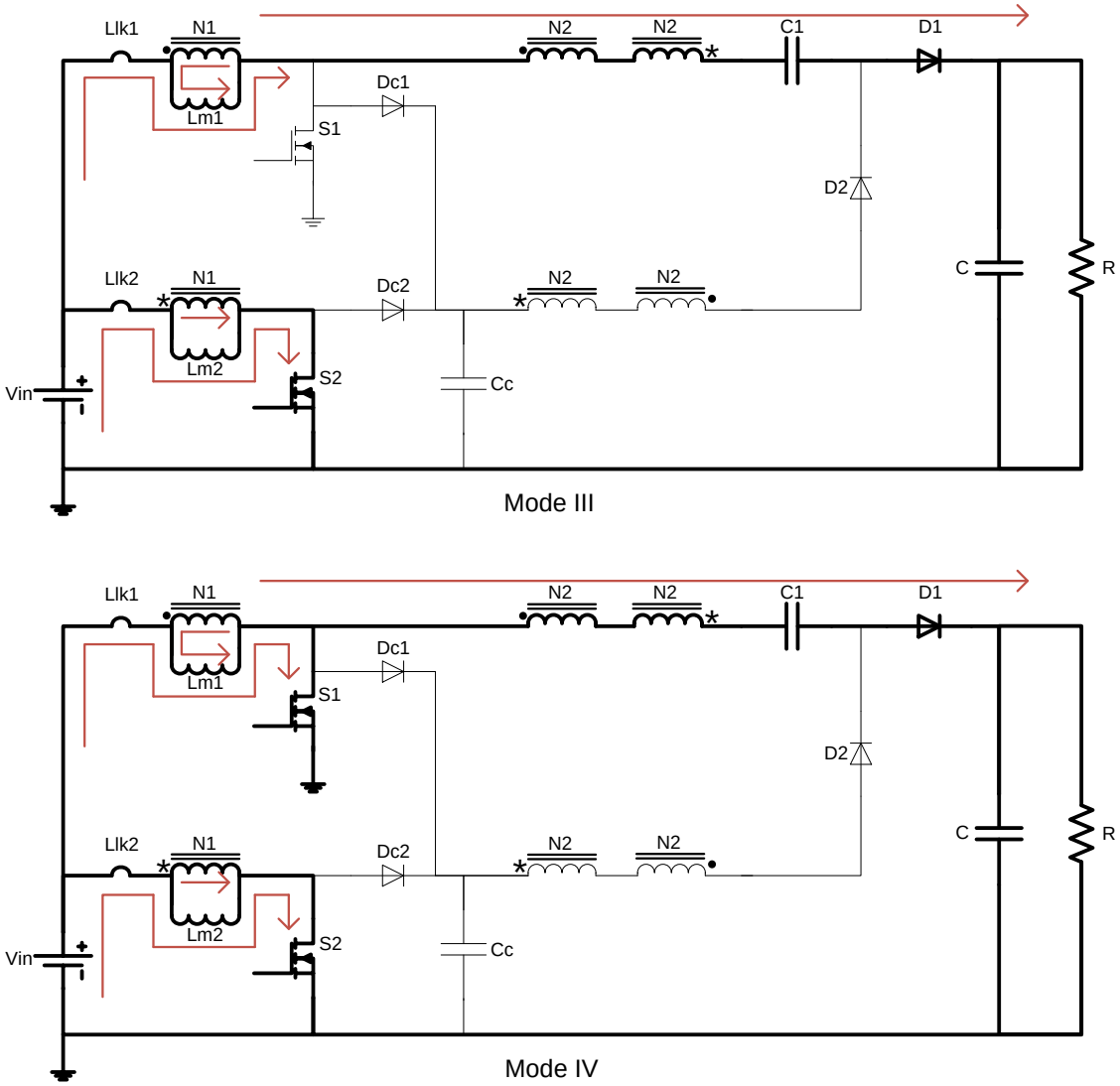

Figure 4.7. Clamped converter operating modes III and IV

Mode III is the same as mode II from the non-clamped converter. Switch S1 is in the OFF state and the upper stage of the converter is discharging capacitor C1, both delivering output power to R and charging capacitor C.

Mode IV occurs when switch S1 turns back to the ON state. In the non-clamped converter this would mean the N2 windings of the upper stage immediately stop conducting current. Due to the leakage inductance the upper stage's N2 windings conduct current which continues to decrease as the leakage inductor current properly equalizes. An effect of this decreasing current is diode D1 is soft-current switched instead of hard-current switched in the non-clamped converter.

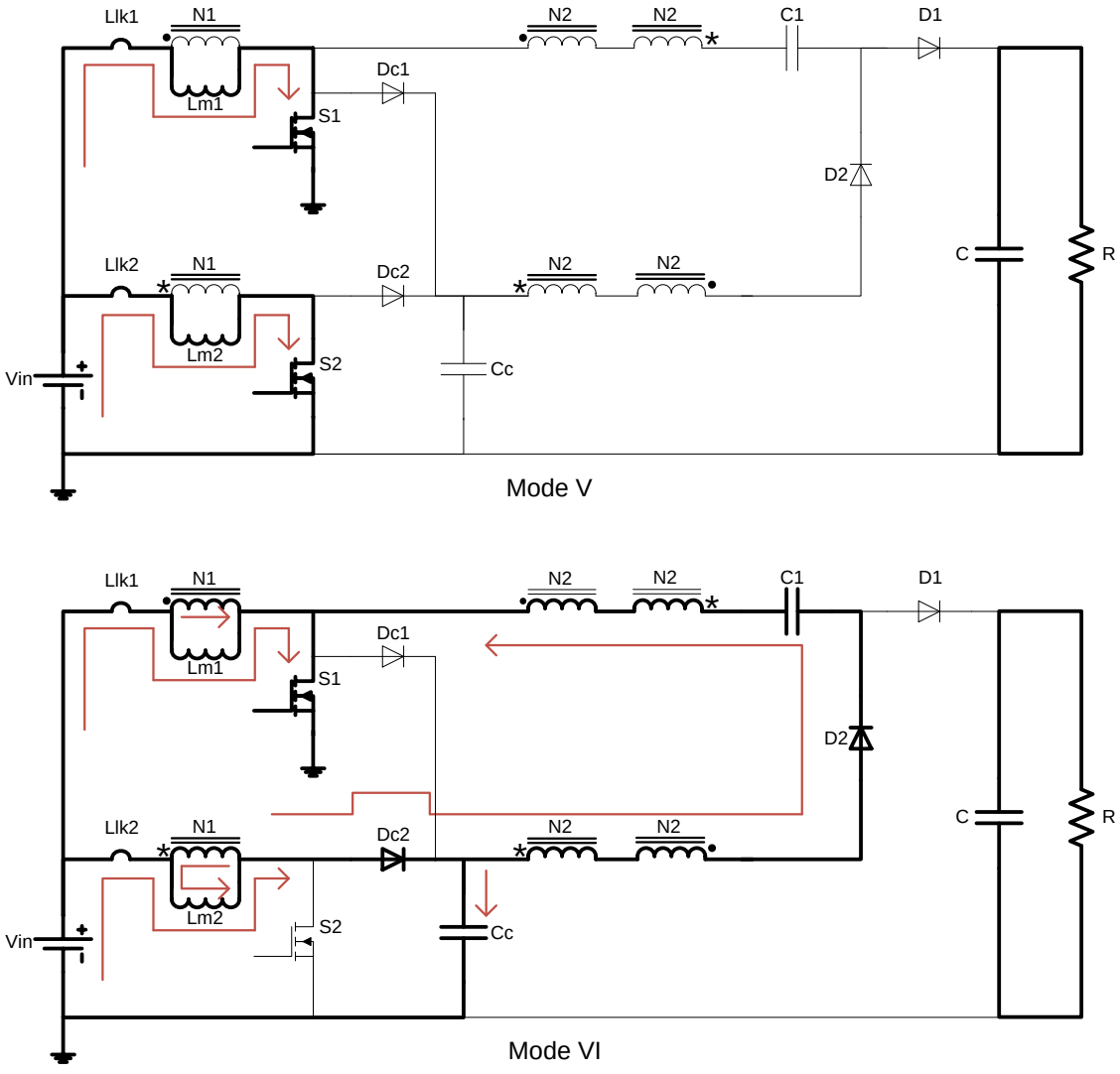

Figure 4.8. Clamped converter operating modes V and VI

Mode V of the clamped converter is the same as modes III in the non-clamped converter. Both active switches are in the ON state, increasing the current and energy stored in each magnetizing inductance. Output power is provided by output capacitor C.

Mode VI occurs when switch S2 turns to the OFF state. As this happens, the energy stored in leakage inductance Llk2 forces diode Dc2 to the ON state, charging clamp capacitor Cc. The current flowing through the N2 windings of both stages begins to increase, charging capacitor C1. Llk2 loses energy to capacitor Cc, reducing the leakage inductor's current.

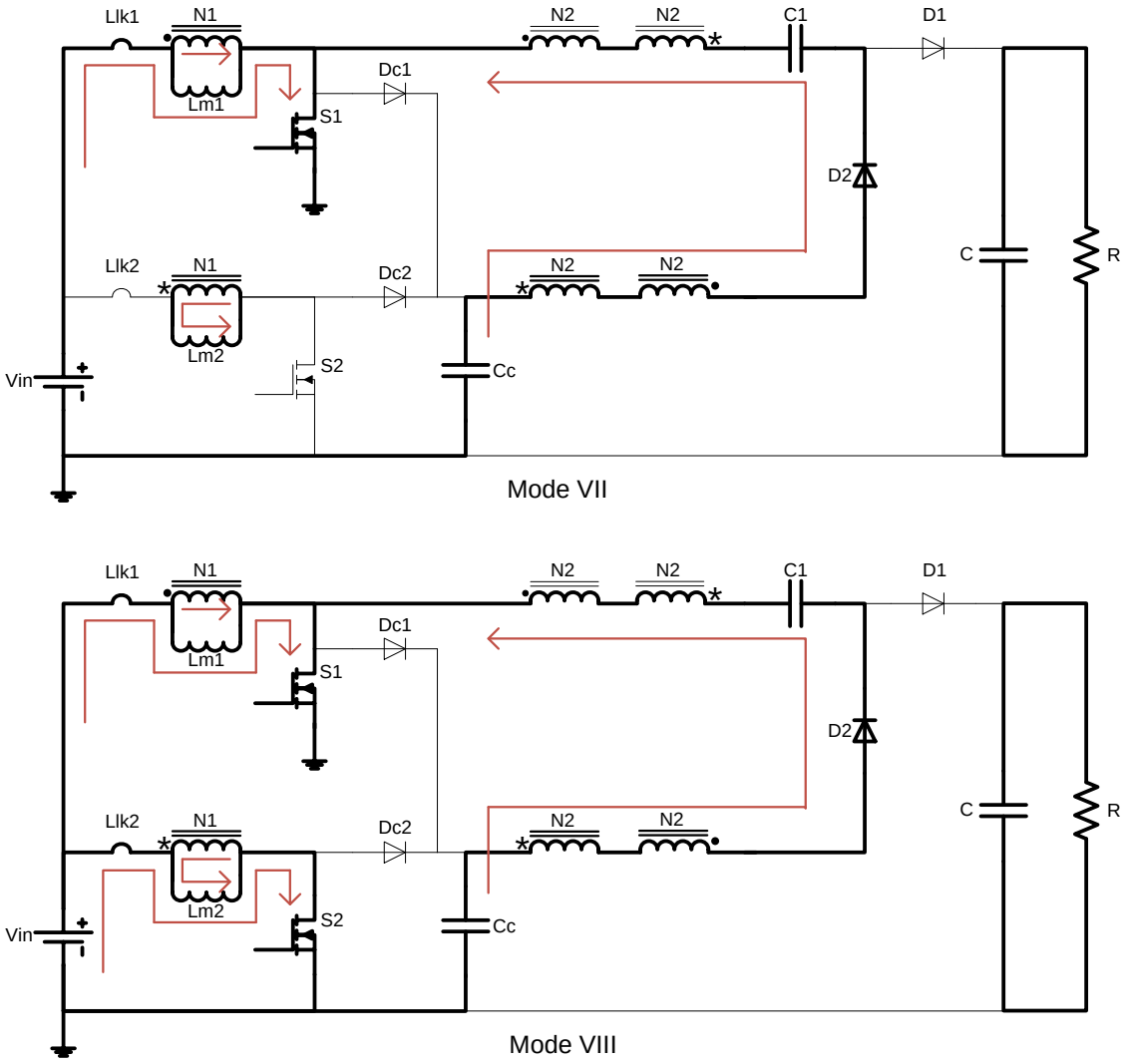

Figure 4.9. Clamped converter operating modes

Mode VII of the clamped converter is most similar to mode IV in the non-clamped converter and occurs when leakage inductor Llk2's current reduces to zero. As this happens diode Dc2 turns to the OFF state and capacitor Cc begins to discharge. Capacitor C1 continues to be charged by both stages of the converter.

Mode VIII occurs when switch S2 turns to the ON state. Similar to mode IV the current through the N2 windings does not reduce to zero immediately. The N2 windings continue to charge capacitor C1 and their currents decrease as the leakage inductance equalizes to the change in the system. This decreasing current has the added effect of soft switching diode D2.

Overall these modes of operation are very similar to those of the non-clamped converter. Instead of changes to current in the coupled windings happening instantaneously it occurs over a short transient period. This allows soft switching to occur in many of the system components, at the same time not affecting system viability.

4.3.2 Advantages and Disadvantages. The main advantage of this clamp is its simplicity. With a total converter addition of two diodes and a capacitor, this clamp works with less than two components per stage. Each additional system component adds a point of failure in the system, but it also contributes to total system cost. Another advantage of this clamp is its passive nature, requiring no control for the clamp to function, preventing complex system controls. This clamp's components are also operated under low voltage and current stresses, preventing excessive losses and increasing system efficiency. The disadvantage of this clamp is its lack of control. This clamp cannot be used in a variety of controlled soft switching methods.

4.4 CLAMPED CONVERTER SIMULATION RESULTS

Similar to section 3.4 it is important to verify the functionality of the system through simulations. The simulation parameters are as follows: input voltage of 20V, duty cycle of 0.6 (output voltage transfer equation value of 400V), turns ratio of 2, output resistance of 400Ω, output power of 400W, switching frequency of 50kHz, output capacitance of 10µF, clamp capacitance of 10µF, magnetizing inductance of 100µH, and leakage inductance of 2% (2µH). Simulation MOSFETs used 0.01Ω ON-state

resistances, and simulation diodes used 0.01Ω ON-state resistances and 0.01V Vf forward voltage drops. Idealized values of resistances and forward voltage drops were used as this simulation is meant to verify clamp viability. Figure 4.10 shows the output voltage and input current to the converter, figure 4.11 shows capacitor C1 voltage and current, figure 4.12 shows diode D1 and D2 voltage, and figure 4.13 shows diode D1 and D2 current.

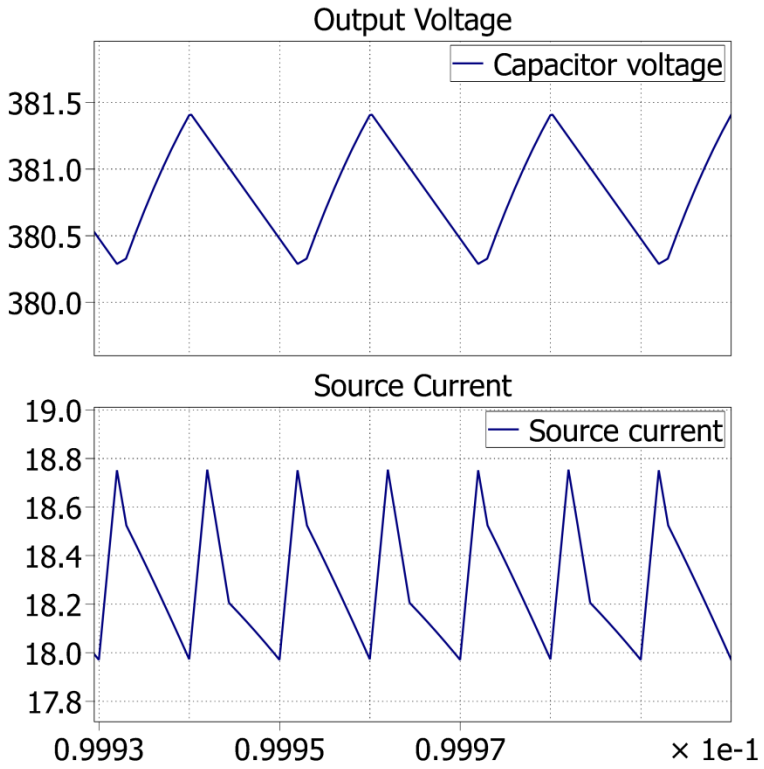

Figure 4.10. Clamped output voltage and input current

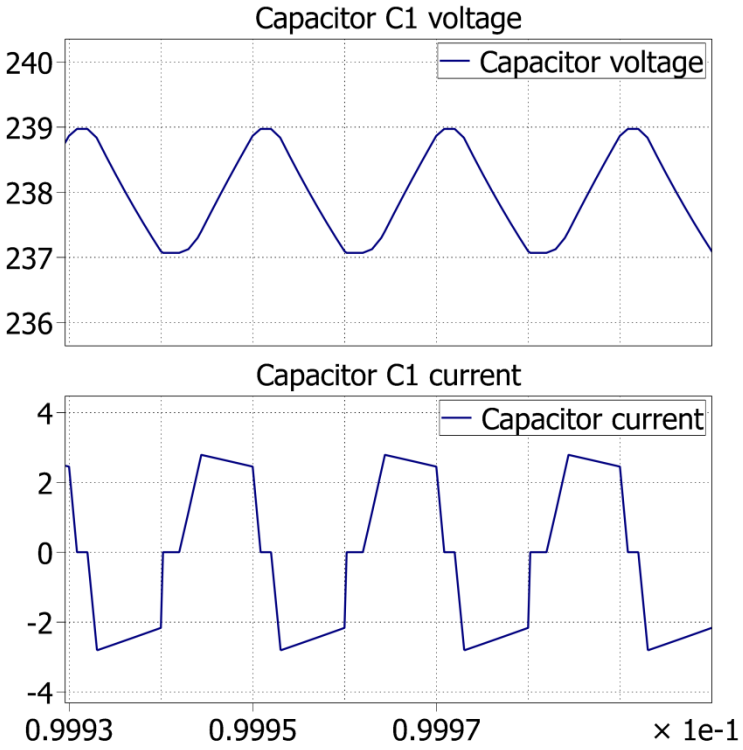

Figure 4.11. Clamped capacitor C1 voltage and current

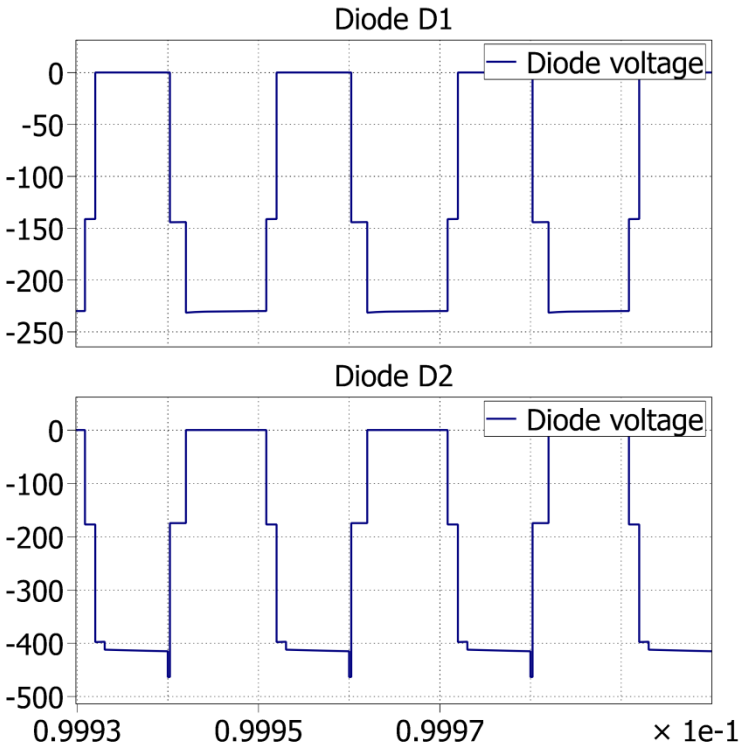

Figure 4.12. Clamped diode D1 and D2 voltages

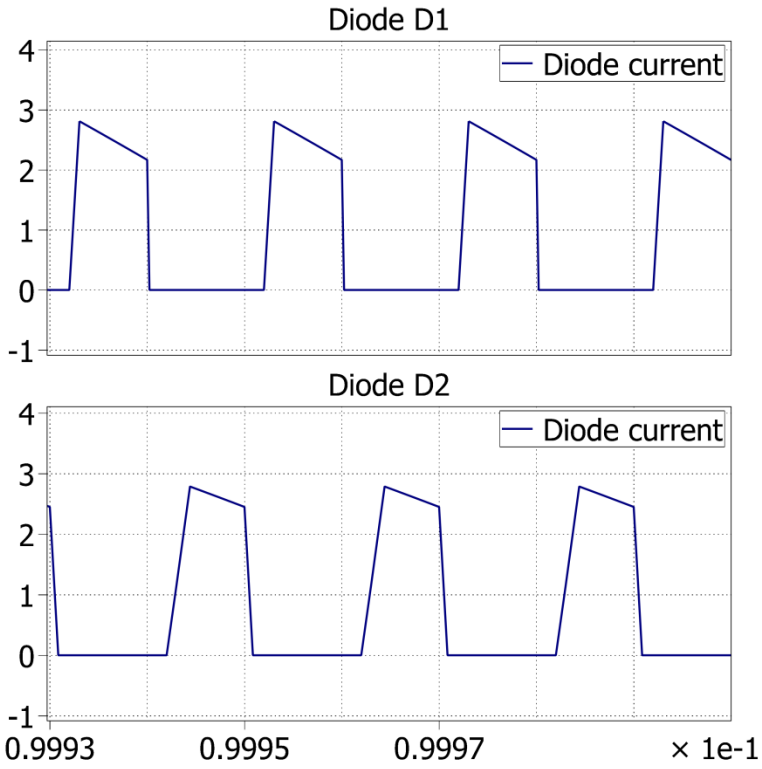

Figure 4.13. Clamped diode D1 and D2 currents

The output voltage looks rather odd compared to the ideal simulation results. The waveform still shows a low ripple, but is more triangular than the non-clamped converter. Of more distinction is the input current. The current remains continuous, acceptable for use in a solar converter, but is no longer triangular in waveform. This is due to the interaction of the clamp, magnetizing inductances, and leakage inductances in the system. Capacitor C1's voltage and current remain similar to the ideal converter, with the clamped converter showing quick, rather than instantaneous changes between zero and peak current. The waveforms of diode D1 and D2 are as expected. The only anomaly is the short voltage "spike" diode D2 experiences, caused by the transient period mode III.

Figure 4.14 shows switch S1 and S2 voltages, figure 4.15 shows switch S1 and S2 currents, figure 4.16 shows magnetizing inductance Lm1 and Lm2 currents, and figure 4.17 shows the magnetizing inductor currents imposed upon the switch currents.

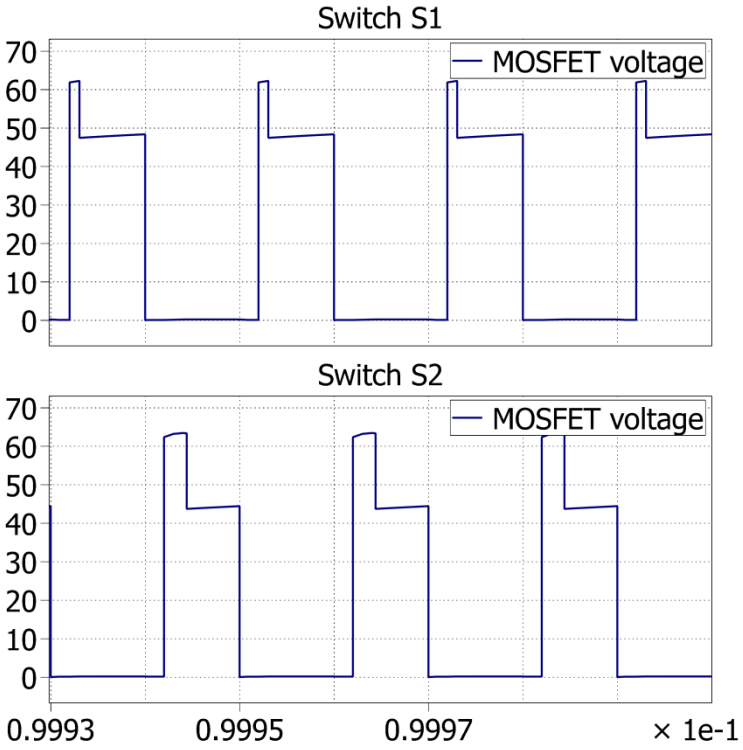

Figure 4.14. Clamped switch S1 and S2 voltages

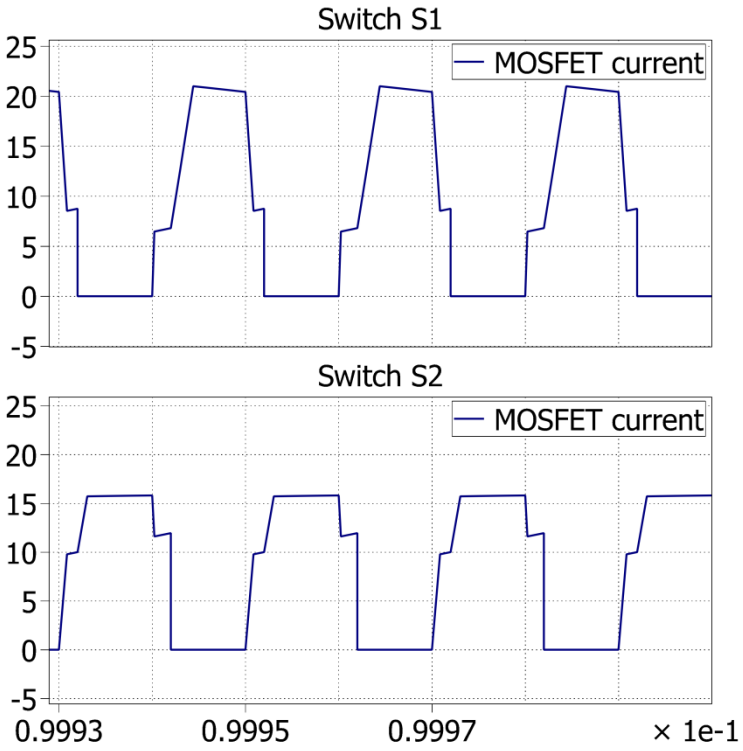

Figure 4.15. Clamped switch S1 and S2 currents

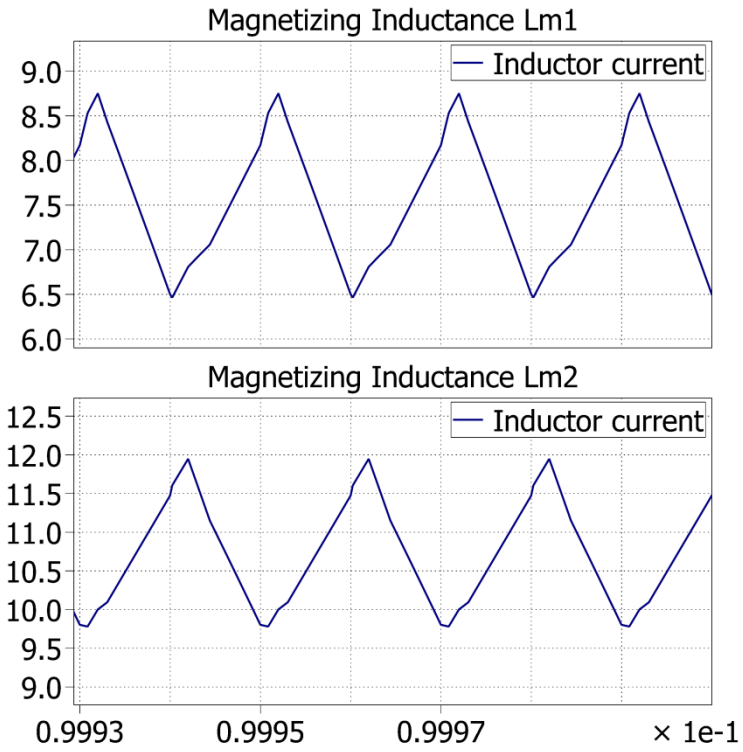

Figure 4.16. Magnetizing inductance Lm1 and Lm2 currents

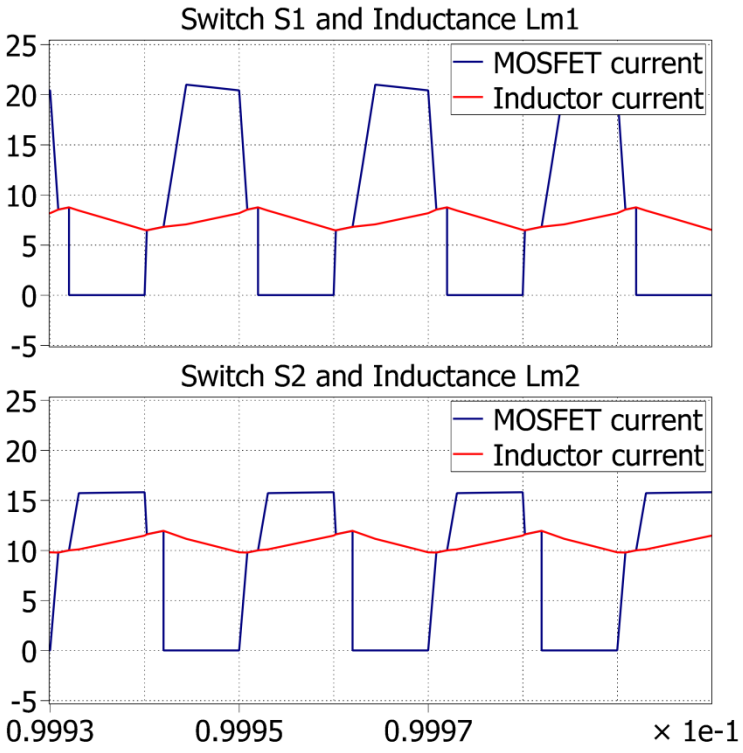

Figure 4.17. Switch S1 and S2, Inductor Lm1 and Lm2 currents

Figure 4.14 shows the voltage across switches S1 and S2. This is an important waveform as it shows the effectiveness of our clamping circuit. While the clamping circuit does not keep the voltage of the switches at the voltage inferred from the switch voltage equation, it does a sufficient job. The switch voltage equation gives a voltage of 50V for our simulation while our switchless clamp keeps the voltage under 80V. While this value may seem high, a large number of 100V MOSFETs are available for use which has optimal characteristics. This maximum switch voltage can also be altered slightly by changing the clamping capacitor and other system values. The switch and magnetizing inductor currents have similar waveforms to the ideal simulations. The lower stage switch and inductor have a higher average current, while the upper stage switch has a higher peak current.

The following figures show waveforms of the clamp. Figure 4.18 shows capacitor Cc voltage and current, figure 4.19 shows diode Dc1 and Dc2 voltages, figure 4.20 shows diode Dc1 and Dc2 currents, and figure 4.21 shows the leakage inductor currents.

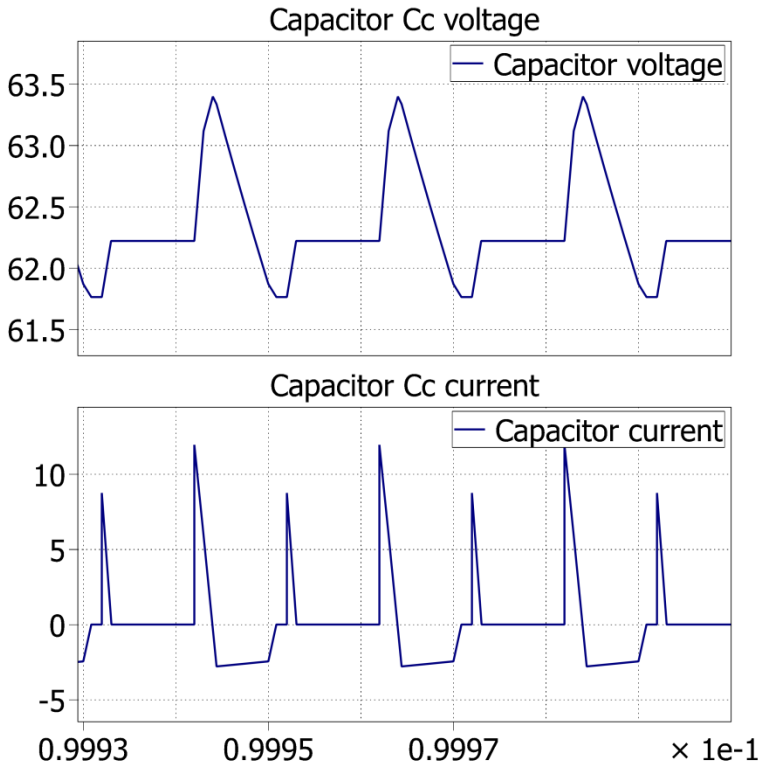

Figure 4.18. Capacitor Cc voltage and current

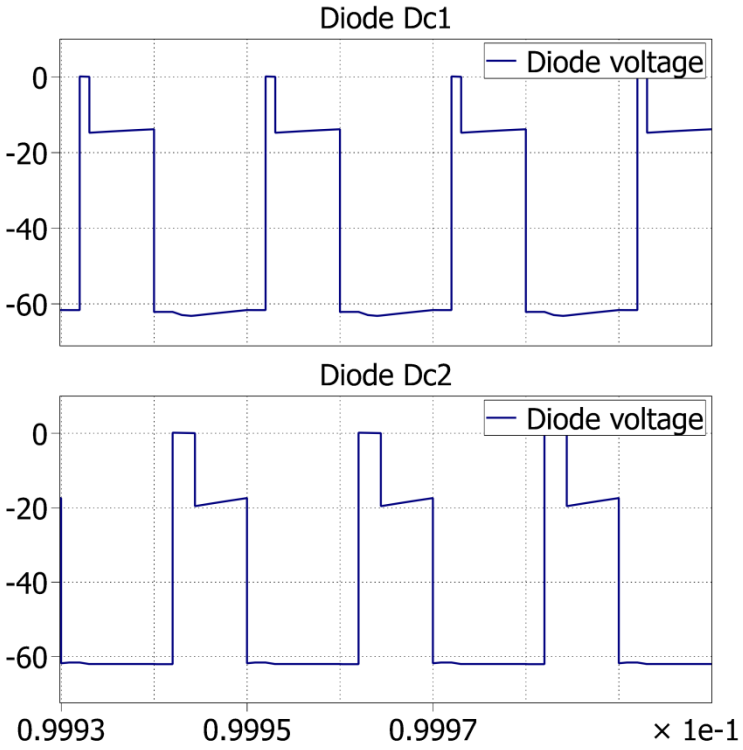

Figure 4.19. Diode Dc1 and Dc2 voltages

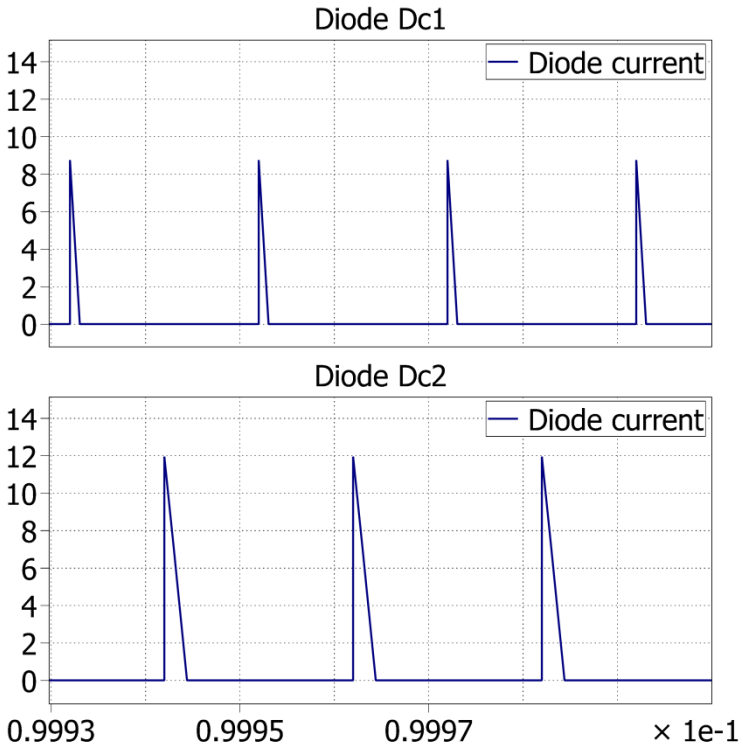

Figure 4.20. Diode Dc1 and Dc2 currents

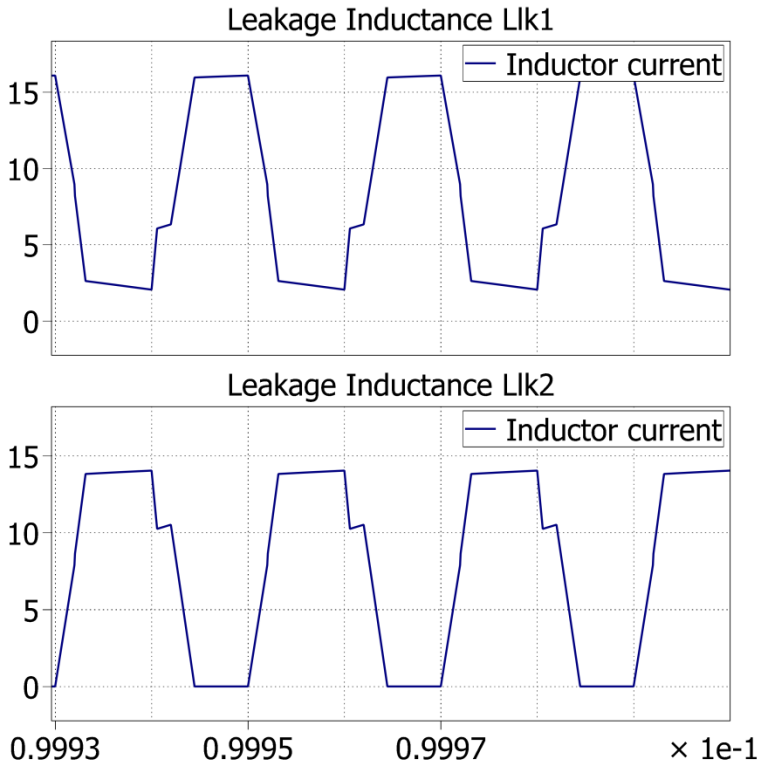

Figure 4.21. Leakage inductance Llk1 and Llk2 currents

The clamp appears to be working as expected. The currents through Dc1 and Dc2 are slightly different with the current of Dc1 having a lower peak and lower average current when compared to Dc2. This is due to the interaction of the leakage inductances when switch S2 turns to the OFF state. Since more windings are interacted with when the S2 turns off compared to when S1 turns off it takes longer for the leakage inductances to equalize. Additionally, leakage inductance Llk2 must reduce its current to zero before Dc2 can turn to the OFF state, increasing the average ON-time and current of Dc2.

Capacitor Cc has an useful waveform as it effectively shows all eight modes of operation. The two positive current spikes are the currents from clamp diodes and the negative currents in the capacitor are from the modes of operation which charge capacitor C1.

Overall these figures show what was expected of our clamped converter, not revealing anything unexpected or additional converter challenges.

5. CONCLUSION

In this thesis a solar microconverter for use in a DC Microgrid was discussed. This proposed topology demonstrated several desirable attributes necessary for a solar converter. These include the high gains this converter can achieve as well as the continuous input current necessary for use with solar panels. The proposed topology also achieved switch stresses which would allow low voltage and high current MOSFETs to be used. While the diodes in the system have a high voltage stress, the current through these components is low. Additionally, the proposed clamp worked well. With less than two additional components per stage this clamp is the most basic that can be sought. The clamping circuit effectively limits the leakage inductance induced switch voltage spikes, alleviating this converter's challenge. At the same time, the clamping circuit does not drastically interfere with the general operation of the converter, keeping the converter waveforms and operating modes very similar to the ideal converter.

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