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On-die sensors for transient events

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by

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ABSTRACT

Failures caused by transient electromagnetic events like Electrostatic Discharge (ESD) are a major concern for embedded systems. The component often failing is an integrated circuit (IC). Determining which IC is affected in a multi-device system is a challenging task. Debugging errors often requires sophisticated lab setups which require intentionally disturbing and probing various parts of the system which might not be easily accessible. Opening the system and adding probes may change its response to the transient event, which further compounds the problem.

On-die transient event sensors were developed that require relatively little area on die, making them inexpensive, they consume negligible static current, and do not interfere with normal operation of the IC. These circuits can be used to determine the pin involved and the level of the event in the event of a transient event affecting the IC, thus allowing the user to debug system-level transient events without modifying the system.

The circuit and detection scheme design has been completed and verified in simulations with Cadence Virtuoso environment. Simulations accounted for the impact of the ESD protection circuits, parasitics from the I/O pin, package and I/O ring, and included a model of an ESD gun to test the circuit's response to an ESD pulse as specified in IEC 61000-4-2. Multiple detection schemes are proposed. The final detection scheme consists of an event detector and a level sensor. The event detector latches on the presence of an event at a pad, to determine on which pin an event occurred. The level sensor generates current proportional to the level of the event. This current is converted to a voltage and digitized at the A/D converter to be read by the microprocessor. Detection scheme shows good performance in simulations when checked against process variations and different kind of events.

ACKNOWLEDGEMENTS

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1 INTRODUCTION

Immunity to transient events like ESD is a growing concern for electromagnetic compatibility (EMC) engineers in industry today. Isolating the component responsible for the error and debugging the error is a time intensive process which is becoming increasingly difficult with the shrinking size of embedded systems. This report presents the design of a set of circuits that can be implemented on-die to determine the I/O pin/pad affected by the transient event as well as approximate the level of transient event affecting the IC. The circuit was built to be relatively inexpensive (i.e. consume little area) and consume negligible static power. Such a detection scheme can allow: determination of specific (on-die) failure points and levels, reduced testing and debugging time and cost for both the IC manufacturer and customers, identification of the path taken by transient events on a system level, ESD protection circuit characterization, in-application event capture, error mitigation through defensive programming in response to an event, and prediction of IC lifespan and maintenance intervals based on the number and size of transient events encountered.

Section 1.1 discusses general need of a transient event detection scheme on ICs and previous work done on this. Section 1.2 describes technical details of research and simulation methods used throughout the project. Some designs developed in early part of the project are discussed in Section 2. These designs have few known shortcomings, discussed at the end of Section 2. To overcome shortcomings of circuits in Section 2, improved designs were developed which are discussed in Section 3.

1.1 BACKGROUND

The increasing in complexity of circuits on an integrated circuit (IC), the decreasing size of transistors, and the decreasing supply voltage and associated noise margins makes the ICs increasingly susceptible to failures from transient events like electrostatic discharge (ESD) [1]. Typical problems include temporary disruption of the IC, semi-permanent failures that can be solved by resetting the IC or re-powering the IC, and permanent failures like transistor burnout due to latch-up, leading to lower production yields, lower product reliability and higher manufacturing cost.

ICs are generally equipped with ESD protection which is designed to route the current away from I/O transistors to power rails and out of the IC. These circuits are solely designed for preventing damage to the IC and give no direct information to the user about a transient event and how it affects the IC. If a system with multiple ICs is affected by an ESD event it is often difficult to isolate which IC caused the system to fail. The debugging procedure might require special setups and measurements to determine which IC was affected and how was it affected, so that necessary steps can be taken to protect against future failures. These measurements can be time consuming and expensive and, in some systems, impossible to perform since the presence of the test equipment itself modifies the system's response to the transient event.

The idea behind the work presented here is to enable the IC itself to record information about the transient disturbance. Few techniques exist in the literature for providing a similar measurement. Methods were suggested in [2] to determine the presence of an electromagnetic-induced error using software which monitors critical registers in a programmable IC. This method, though elegant, only gives information

about particular soft-errors and depends upon the software to work perfectly to give out an error indication. The software method gives limited information to help in root cause analysis of the ESD disturbance.

Some techniques for reporting the presence of a transient disturbance of the power supply have also been reported. For example the technique presented in [3][4] monitors the power distribution network (PDN) for noise and gives an indication of an irregular supply. The peak noise level can be saved using a sample and hold circuit. In [5], a voltage monitor circuit is developed which stores the peak voltage of the event on a capacitor, which is later measured externally through a pin on the IC. Circuits in [6][7] measure the level of the voltage disturbance on the PDN to approximate the level of the transient event.

All these circuits give information regarding some aspect of the transient event but do not give information about which I/O pins were affected by a particular event. They also provide very limited information about the level of disturbance entering the IC. The sensors designed in the following report are intended to give both pieces of information. There is no need for the user to measure anything. The measurements are made on-die. Software only has to be built to read the information and use it. Since the information is easily obtainable in software, corrective measures can also be taken to defend against soft-errors caused by a transient event in the field – for example, by performing a memory check or restoring the code to a known safe state after the event has occurred. The circuits developed here were designed to give consistent readings for a variety of transient events. The level of the reading does not depend upon the rise time or

duration of the transient disturbance seen by the IC, only the peak value of the input voltage.

1.2 METHODOLOGY

The transient event sensors were developed using a simulate and verify approach. Simulations were done in Cadence Virtuoso custom IC design software. Models used for simulations were chosen so as to approximate actual IC and test hardware as closely as possible. Models include approximations of PCB components, pin and package parasitics, on-die ESD protection circuits, load on the IC, on-die decoupling capacitors and as ESD gun model which is used to inject I/O pads with ESD events in order to test the working of the detector circuits. During the initial phase of the project, a publicly available technology library (AMI06 from NCSU) was used for design and proof of concept simulations. This technology library was used for “Initial designs” in Section 2. Later designs, discussed in Section 3, used a 90 nm technology from Freescale that will be used in a future test IC. Since a test IC will be developed from this work and much of the technology library is available for this technology, the simulations include technology and IC specific models of ESD protection structures. These simulations provide a comprehensive idea of how these circuits will perform in the final implementation.

2 INTIAL DESIGNS

During the development of the measurement scheme for transient events, several detection and measurement strategies were explored which did not make it to the final test IC. These initial designs are discussed in the following section. Section 2.1 describes out-of-range voltage detectors which can measure transient events based on voltages on I/O pads. The measurement of the event is based on the voltage on an I/O pad going above or below the power supply voltage. Section 2.2 discusses oscillators for measuring the level of transient events. The number of output oscillations depends upon the level of the transient event. Counting the number of oscillations can be used to determine the level of the transient events. At the end of Sections 2.1 and 2.2 some known or foreseen issues are discussed. The circuits ultimately making it to the hardware testing phase, described in Section 3, were developed, in part, to get around these known issues.

2.1 OUT-OF-RANGE VOLTAGE DETECTORS

When an I/O pad is affected by an ESD event, the voltage on the I/O pad either goes higher than Vdd and current is injected into the pad (positive event) or the voltage on the pad goes below Vss and current is drawn from the pad (negative event). Detectors in this section are designed to react to such abnormal voltages on the I/O pad.

2.1.1 Concept and Schematics. Transistor M1 in Fig. 2-1 performs the essential detection of an overvoltage event. During a positive transient event the I/O pad voltage goes higher than the Vdd voltage and current flows through the ESD protection diode. If the voltage drop from the pad to Vdd is above a threshold voltage, the P-channel

MOSFET (PFET – transistor M1) between the I/O pad and Vdd net will be turned on, thus supplying current to the FET drain.

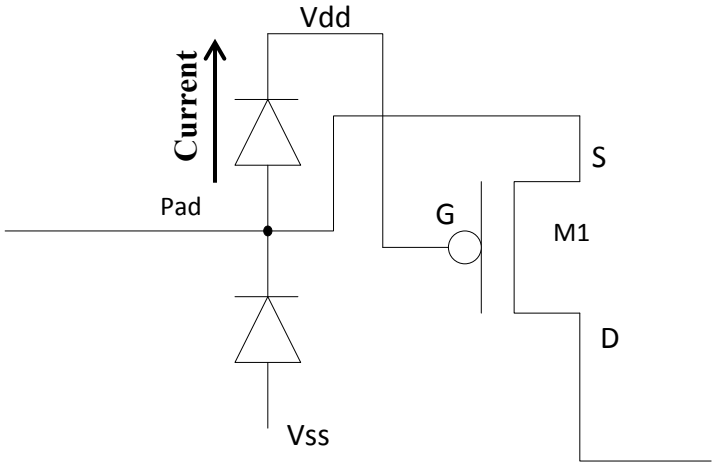


Figure 2-1. ESD protection at I/O pads and "Driving FET" M1

Transistor M1drives a latch circuit as shown in Fig. 2-2. The current driven by M1 is directly related to the voltage across the diode (i.e. V_{GS}), which is directly related to the current through the ESD protection diode. Accordingly, the node connected to the drain of M1 is being pulled up towards Vdd. This node will remain high only during the event, while current flows through the diode. The passing of this event can be saved in a latch and read out later.

Transistor M1 has to pull the node “A” high when M2 is “on” and weakly pulls down the node. The amount of current required to flip the latch depends on the pull-down strength of M2 compared to the pull-up strength of M1. By varying the size of M1 and M2, as well as the switching threshold of the inverter formed by M4 and M5, the

threshold of the latch can be controlled. This theory can be explained mathematically as shown below in equation (2.1).

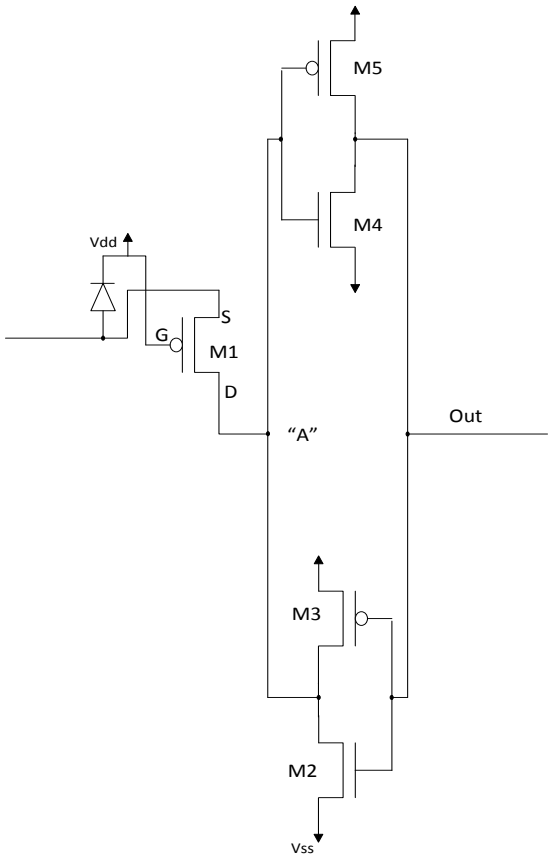


Figure 2-2. Positive event indicator

At the point where the latch switches state, node "A" has to reach the switching threshold of inverter M4-M5. This voltage will be called $V_{"A",SW}$. Since only M1 and M2 drive node "A", their drain currents are equal. At the switching point, M1 will be in saturation and M2 will be in linear mode. Equating the drain currents of M1 and M2 gives:

$$k'_p\left(\frac{W}{L}\right)_{M1}\left[\left(V_{dd}-V_{pad}-V_{t,p}\right)V_{dsat}-\frac{V_{dsat}{}^2}{2}\right]= \\ k'_n\left(\frac{W}{L}\right)_{M2}\left[\left(V_{op}-V_{ss}-V_{t,n}\right)\left(V_{"A"}-V_{ss}\right)-\frac{\left(V_{"A"}-V_{ss}\right)^2}{2}\right] \tag{2.1}$$

where k'_p and k'_n are the process trans-conductance for the PFET and NFET, respectively, $(W/L)_{M1}$ and $(W/L)_{M2}$ are the width to length ratios of M1 and M2, respectively, V_{pad} is the voltage at the pad, $V_{"A"}$ is the voltage at node "A", and $V_{t,p}$ and $V_{t,n}$ are the threshold voltages for the PFET and NFET, respectively.

Solving (2-1), the latch switching voltage at the pad, $V_{pad,sw}$, where $V_{"A"}$ reaches $V_{"A",sw}$ is given by:

$$-V_{pad}=V_{t,p}+\frac{V_{dsat}}{2}-V_{dd}+ \\ \left\{\frac{k'_n}{k'_p}\left(\frac{W}{L}\right)_{M2}\left(\frac{L}{W}\right)_{M1}\frac{1}{V_{dsat}}\left[\left(V_{op}-V_{ss}-V_{t,n}\right)\left(V_{"A",sw}-V_{ss}\right)-\frac{\left(V_{"A",sw}-V_{ss}\right)^2}{2}\right]\right\} \tag{2.2}$$

The parameters on the right hand side of the equation, except $(W/L)_{M2}$ and $(L/W)_{M1}$, are process parameters which are constants. Hence, the pad voltage at which the latch triggers can be controlled by changing the widths and lengths of M1 and M2.

Detecting the presence of the event can be done by creating a relatively low trigger voltage. The level of the event can be determined using multiple instances of such circuits with different trigger thresholds (e.g. one for 1 V above Vdd, one for 2 V above Vdd, etc.). The level of the ESD event can be estimated from which of the latches were triggered.

A similar circuit can be built for negative events, as shown in Fig. 2-3. In this case the pad voltage drops below V_{ss}.

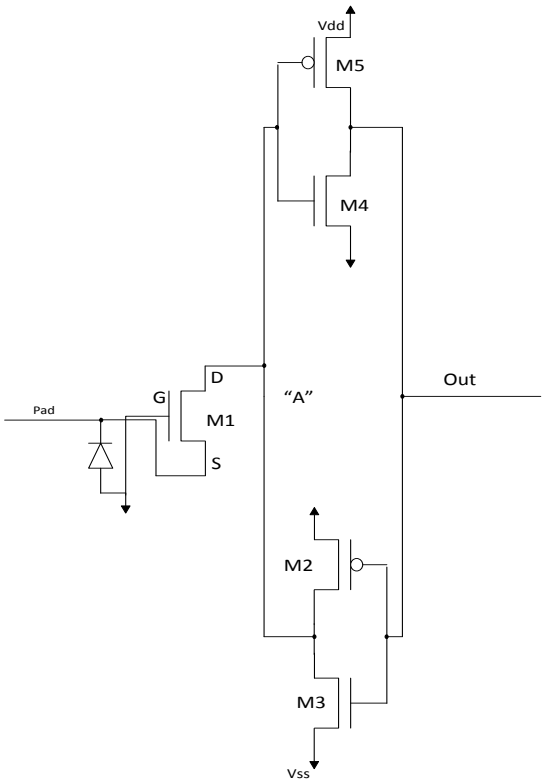


Figure 2-3. Negative event indicator

The corresponding equation for switching threshold of the negative event indicator in Fig. 2-3 is:

$$-V_{pad} = V_{t,n} + \frac{V_{dsat}}{2} - V_{ss} + \left\{ \frac{k'_p}{k'_n} \left(\frac{W}{L} \right)_{M2} \left(\frac{L}{W} \right)_{M1} \frac{1}{V_{dsat}} \left[\left(V_{op} - V_{dd} - V_{t,p} \right) \left(V_{"A",sw} - V_{dd} \right) - \frac{\left(V_{"A",sw} - V_{dd} \right)^2}{2} \right] \right\} \quad (2.3)$$

A reset transistor should be added to these latches as shown in Fig. 2-4 and Fig. 2-5 to ensure the correct state of the latch at power-up and to allow detection of multiple events.

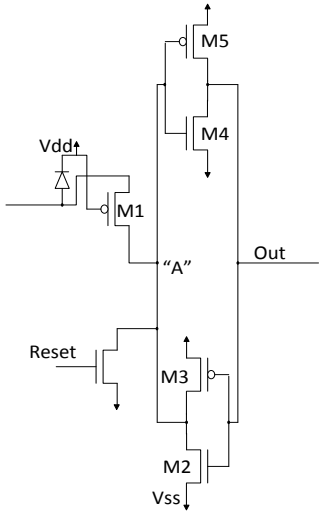


Figure 2-4. Positive event indicator with reset functionality

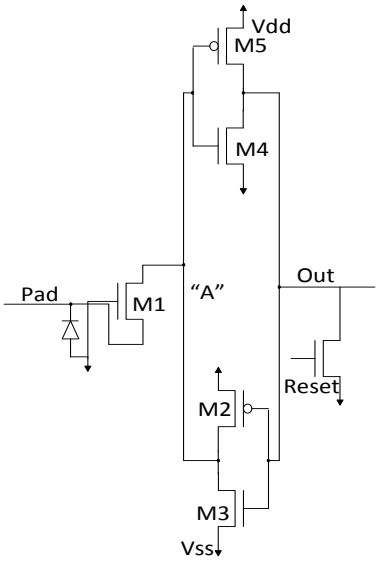


Figure 2-5. Negative event indicator with reset functionality

2.1.2 Simulation Models. A simulation model was constructed to provide a realistic representation of the voltage and current that would be experienced at the pad and across the on-die PDN during a transient event. Initial simulations excluded the PDN bus resistances and the characteristics of the on-die power clamps. These circuit elements, though important, were not required to test the basic functionality of this circuit.

The ESD gun model use to inject the test circuit with ESD events is shown in Fig. 2-6. This model is similar to one developed in [8]. This circuit gives a good approximation of IEC-61000-4-2 ESD pulse. IO pin and pad parasitics are approximated using a lumped element model as shown in Fig. 2-7. The approximation includes bond-wire and pin inductance, the capacitance of pins to ground, and the series resistance of the pin. This model is based on the package model developed from measurements of a Freescale microcontroller in [9]. The entire IC model used in the initial simulations is shown in Fig. 2-8.

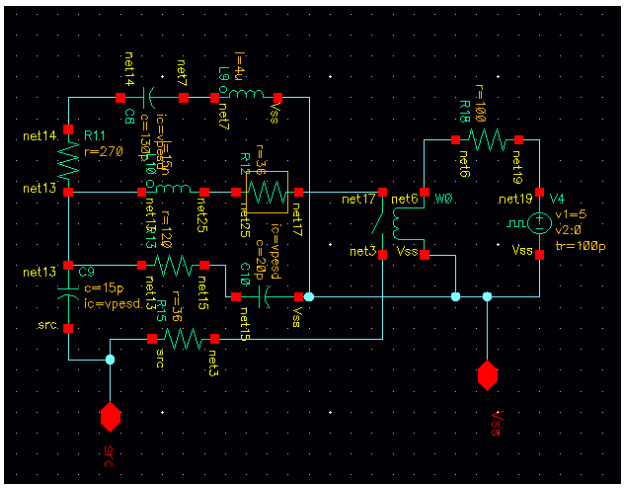


Figure 2-6. ESD gun model in Cadence Virtuoso used to generate IEC-6100-4-2 type pulses

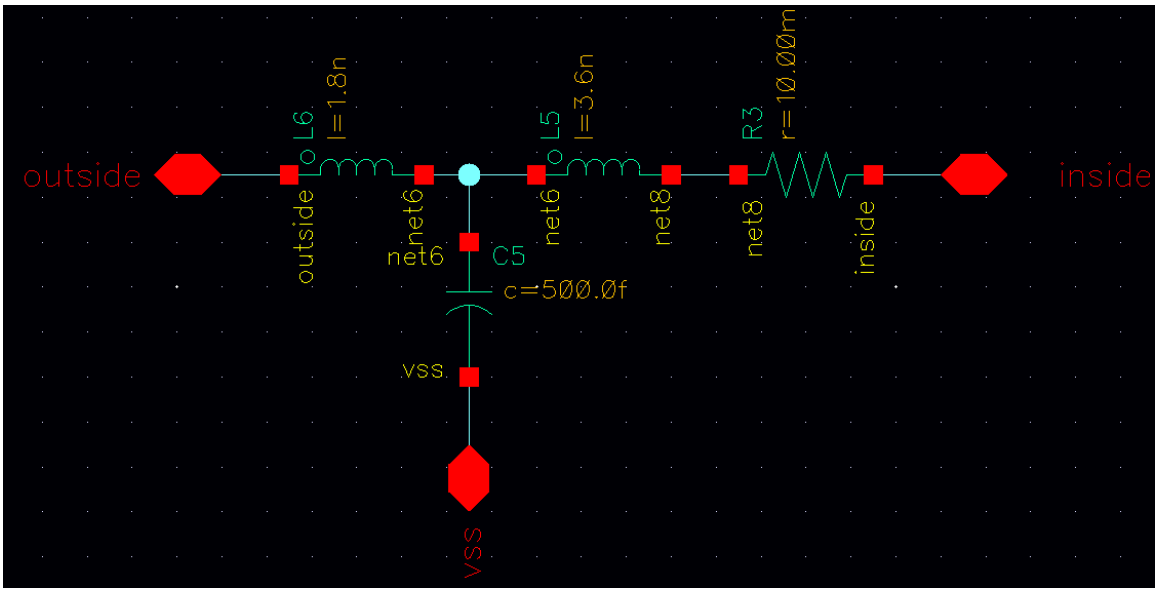


Figure 2-7. Pin parasitic model in Cadence Virtuoso

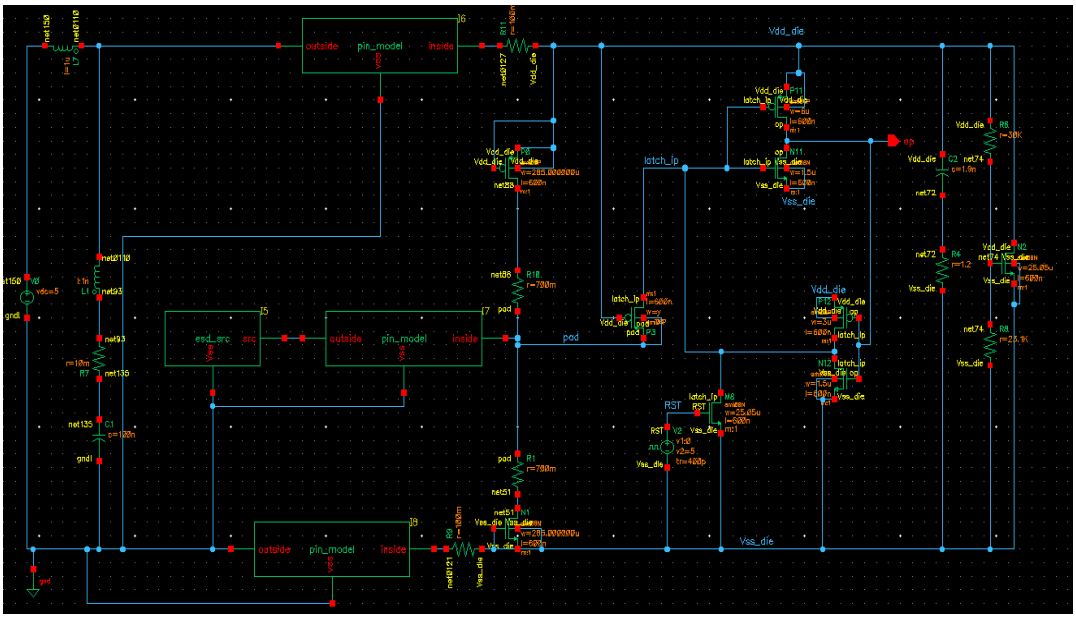


Figure 2-8. Complete simulation model formed in Cadence Virtuoso for testing different circuits

The simulation model is described in a block diagram in Fig. 2-9. The parts of the simulation, starting from the left, are: the on-board 5 V supply, decoupling capacitance

100 nF, ESD protection diodes, test circuit and finally, on the right, the on die decoupling capacitance and a current load approximating the IC current consumption. The behavior of PDN voltages is different on-board than on-die due to the pin parasitics. In this paper, discussions of Vdd/Vss refer to the Vdd/Vss on die since those are the supplies affecting the circuit under study.

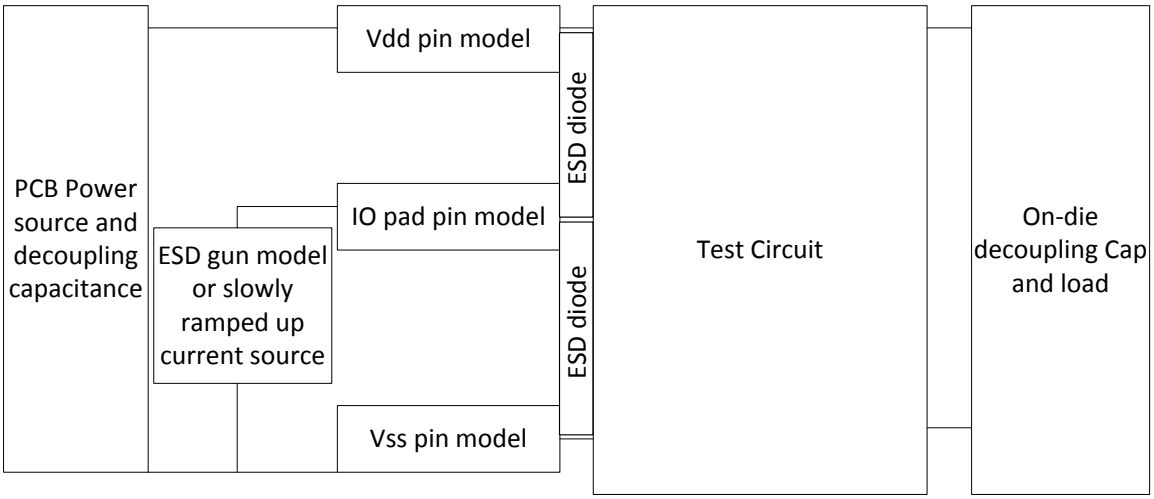


Figure 2-9. General simulation model for any test circuit

2.1.3 Simulation Results and Analysis. The positive event detector, shown in Fig. 2-10, was tested first. The size of the transistors was:

M1: 9 um/0.6 um
M2: 1.5 um/0.6 um
M3: 3 um/0.6 um
M4: 1.5 um/0.6 um
M5: 6 um/0.6 um
(Note: Sizes are specified as width/length.)

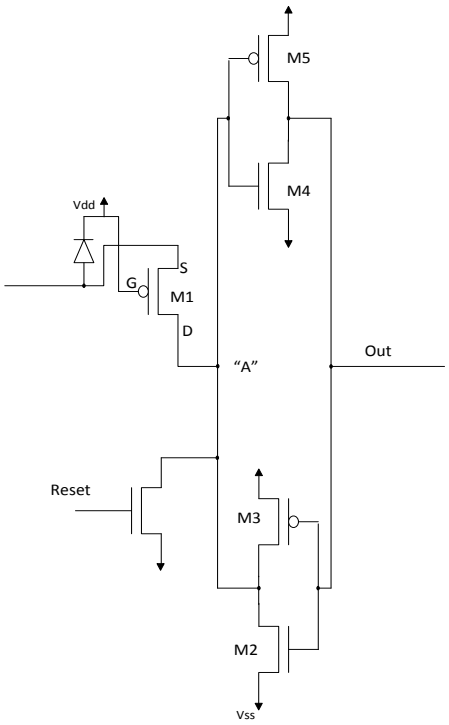


Figure 2-10. Positive event detector used for simulations

Figure 2-11 shows an example simulation when the I/O pad was injected with a 700 V event (i.e. the ESD gun capacitor was charged to 700 V before discharge). A 700 V event injects about 2.5A of current into the IO pad. Event capture is successful since the output of the detector switches from a high (5 V) to a low (0 V) when the ESD event disturbs the I/O pad. The PDN on the IC, depicted by Vdd_die and Vss_die, is disturbed momentarily during the ESD event due to current routed from the I/O pad to Vdd_die through the ESD diodes. Whether the device triggers depends on the peak voltage on the pad with respect to Vdd on die (Vdd_die). For this configuration, the threshold for triggering was found to be about 2 V. So long as the peak pad voltage is 2 V or more above Vdd_die, the event should be latched by the detector.

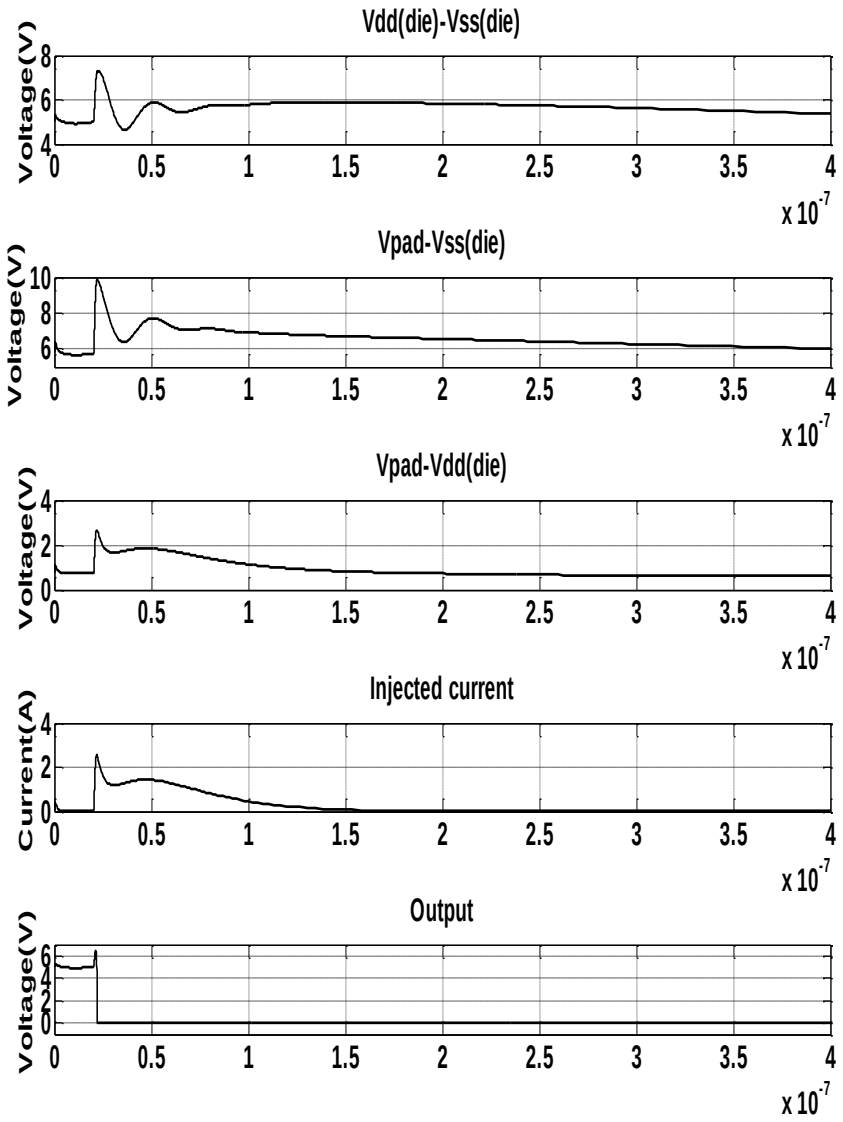


Figure 2-11. Response of positive detector to 700V ESD event

The trigger threshold is determined by the relative sizes of the transistors. Figure 2-12 shows the trigger threshold when the width of M1 was varied from 2 to 9 u. The trigger voltage varies from 5 to 2 V. Thus, it may be possible to measure the level of the ESD event using a group of such circuits and observing which of them triggered.

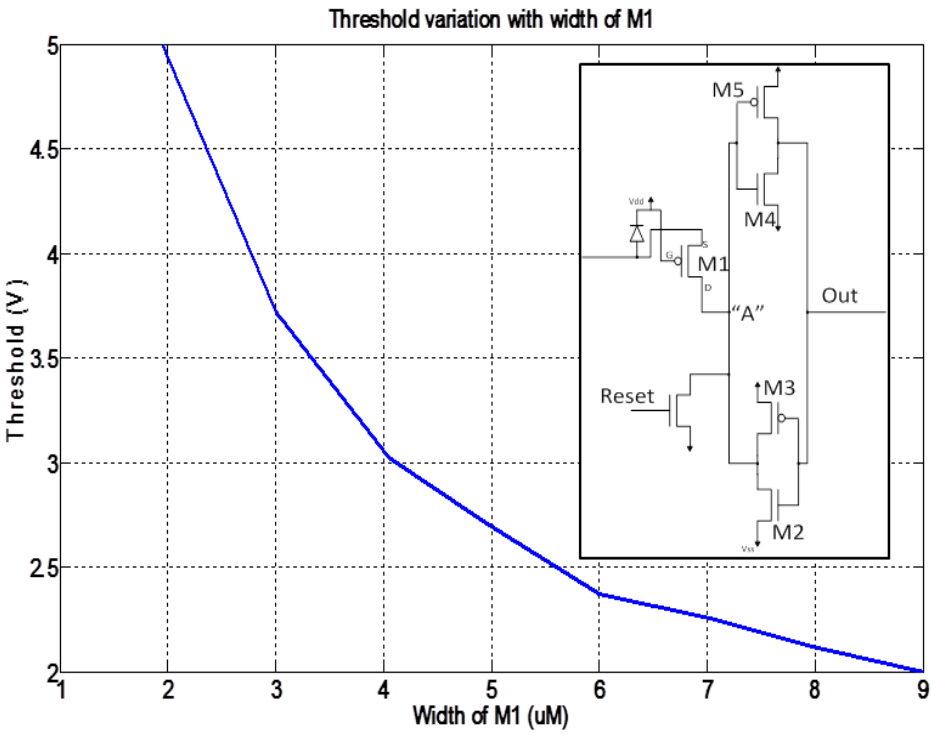


Figure 2-12. Threshold variation for positive event detector as width of M1 is varied

The trigger threshold can be determined analytically from the configuration of the detector. As described before, the equation governing the trigger of the positive event detector is:

$$-V_{pad} = V_{t,p} + \frac{V_{dsat}}{2} - V_{dd} + \left\{ \frac{k'_n}{k'_p} \left(\frac{W}{L} \right)_{M2} \left(\frac{L}{W} \right)_{M1} \frac{1}{V_{dsat}} \left[\left(V_{op} - V_{ss} - V_{t,n} \right) \left(V_{"A",sw} - V_{ss} \right) - \frac{\left(V_{"A",sw} - V_{ss} \right)^2}{2} \right] \right\} \quad (2.4)$$

This equation is derived using a simple MOSFET algebraic model suggested by Shichman and Hodges [10]. This model is based on curve fitting and is insufficient to predict the behavior for modern processes [11]. Modern models like BSIM models take into account variation of parameters with bias and temperature and the interdependence

among various parameters. Using such models here makes prediction of thresholds more complicated than needed.

A simpler model called the Alpha-power model introduced in [11] gives a set of parametric equations which are simple to use. Since curve fitting is done for this particular application, parameters and behavior of equations have more reliability. The Alpha-power law equations are as follows:

$$\begin{aligned} I_{Drain} &= 0 && \left(V_{gs} \le V_{th} : cutoff\right) \\ &= \left(I'_{Drain} / V'_{Drain}\right) V_{ds} && (V_{ds} < V'_{Drain} : Linear\,\mathrm{Re}\,gion) \\ &= (I'_{Drain}) && (V_{ds} \ge V'_{Drain} : Saturation) \end{aligned} \tag{2.5}$$

where:

$$I'_{Drain} = W * K(V_{gs} - V_t)^{\alpha}$$
$$V'_{Drain} = P_v(V_{gs} - V_t)^{\alpha/2}$$

where W is width of the MOSFET, and the length is factored into "K" since length is assumed to be constant. The parameters V_{th}, K, P_v and α are found from curve fitting to V-I curves of MOSFETs in simulation.

Following the earlier development, the equation for threshold for the positive event detector using the alpha power law is:

$$V_{pad,sw} = \left|V_{t,M1}\right| + \left(\frac{K_{M2} * W_{M2}}{K_{M1} * W_{M1} * P_{v,M2}} \left(\left|V_{dd}\right| - \left|V_{t,M2}\right|\right)^{\alpha_{M2}/2} * (V_{"A",sw})\right)^{1/\alpha_{M1}} \tag{2.6}$$

where $V_{"A",SW}$ is the voltage at node "A" at which inverter M4-M5 switches, found to be 2.9 V for the sizes of M4 and M5 used in simulations.

To match theoretical triggers to those found experimentally, the parameter values for the MOSFETs had to be found through simulation. Since M1 is assumed to be in

saturation mode when the latch triggers, simulations were performed with M1 in saturation. The simulation schematic is shown in Fig. 2-13.

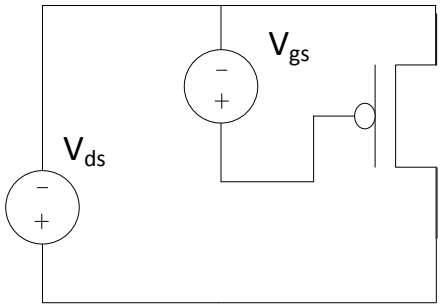


Figure 2-13. Simulation schematic for getting characteristic curves for the PFET

V_{ds} was kept to -10 V while V_{gs} was swept from 0 to -5 V. Since $V_{ds}>V_{gs}-V_t$ the FET would be in saturation for the entire sweep. Parameter values were determined to match the resulting curve with the following equation:

$$(I_{Drain}) = W * K(V_{gs} - V_t)^{\alpha} \tag{2.7}$$

The resulting parameters were: Vt= -0.5 V, α = 1.315 and K = 41.4022 A/m for a W=9 um PFET. The measured and simulated V_{gs} Vs I_{drain} curve is shown in Fig. 2-14.

Simulations for M2 (the NFET) were done for a W=1.5 um FET. The simulation schematic is shown in Fig. 2-15. The FET was simulated with V_{ds} = 10 V while sweeping V_{gs} from 0-5 V. The parameters found from curve fitting are: V_t= 0.95 V, α = 1.1469 and K = 67.35 A/m. Figure 2-16 shows the comparison between the simulated and calculated I-V curve.

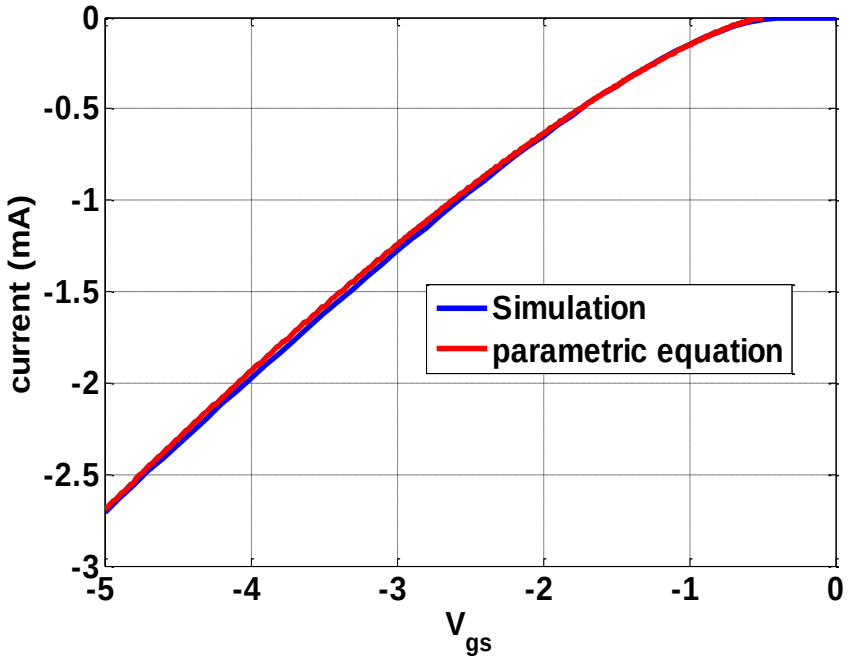


Figure 2-14. Comparison of Vgs-Idrain curve from simulations and parametric equation for 9u/0.6u PFET

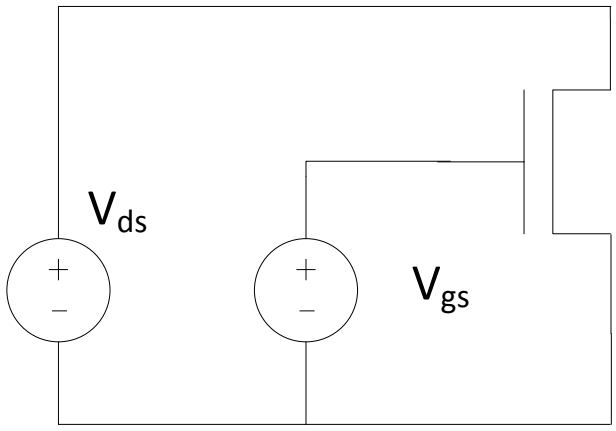


Figure 2-15. Simulation schematic for getting V-I curves for the NFET

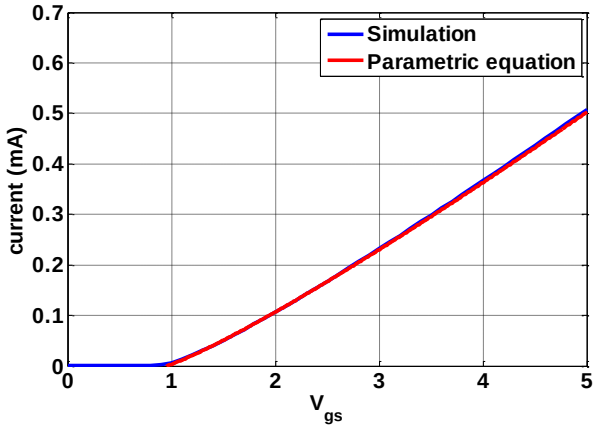


Figure 2-16. NFET drain current comparison in saturation region with equation and simulation results for 1.5u/0.6u NFET

The simulation above gives the value of Idrain during saturation. The values for I'drain and V'drain for linear operation are also needed. The equations for linear operation of the FET are:

$$(I_{Drain}) = \left(I'_{Drain} / V'_{Drain}\right) V_{ds}$$

$$I'_{Drain} = W * K(V_{gs} - V_t)^{\alpha} \qquad (2.8)$$

$$V'_{Drain} = P_v (V_{gs} - V_t)^{\alpha/2}$$

The parameter left to be found is P_v. Simulations and curve fitting for Vds sweep from 0-10 V while keeping Vgs= 5 V gave $P_v = 1.4$. The resulting curves are shown in Fig. 2-17. Notice how curve is fitted for linear region. This is done to have a close approximation around Vds = 3 V since that is the region this FET will be in during triggering. Similar curve fitting was performed to find P_v for PFETs, which was found to be 1.4.

New simulations were performed to find thresholds while slowly varying the pad voltage. Thresholds for various combinations of M1 and M2 sizes were found while injecting a triangular "pulse" with very slow rise time into the IO pad. The slowly

varying input was used to avoid bandwidth being a factor in the results since static conditions are assumed in the analytic equations. A 5 V DC source was connected between Vdd(die) and Vss(die) since this voltage is assumed in the equations. An example simulation result is shown in Fig. 2-18.

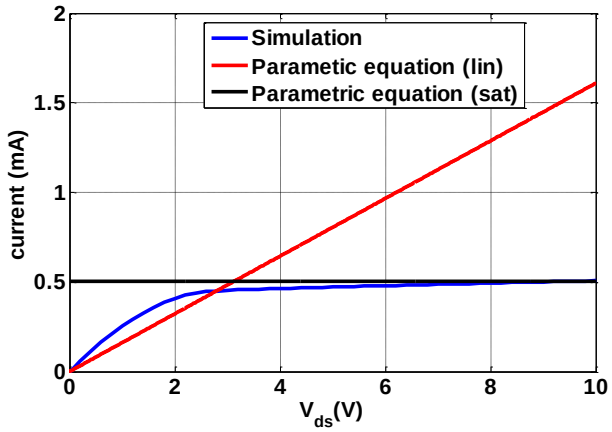


Figure 2-17. Comparison for NFET V_{ds} Vs I_{drain} curve and approximations from Alpha-power model

The thresholds for various sizes of M1 were found by recording the Pad-V_{dd}(die) voltages which made the circuit trigger. Corresponding thresholds were also found by solving the equation:

$$V_{pad,sw} - V_{dd} = |V_{t,M1}| + \left(\frac{K_{M2} * W_{M2}}{K_{M1} * W_{M1} * P_{v,M2}} \left(|V_{dd}| - |V_{t,M2}|\right)^{\alpha_{M2}/2} * (V_{"A",sw})\right)^{1/\alpha_{M1}} \qquad (2.9)$$

Both the results are plotted together in Fig. 2-19. The predicted and measured thresholds match to within about 0.2 V.

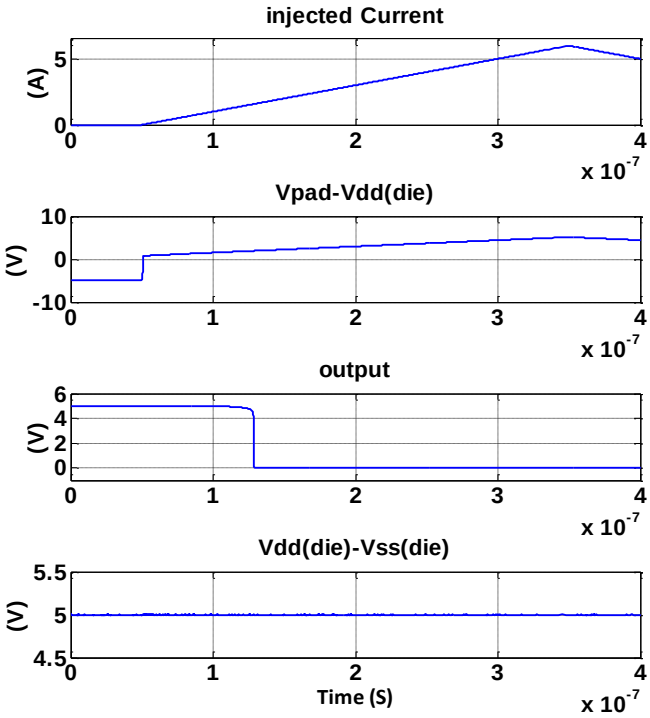


Figure 2-18. Response of positive event detector to slow event with 300 ns rise time while Vdd(die) and Vss(die) are held at a constant 5 V

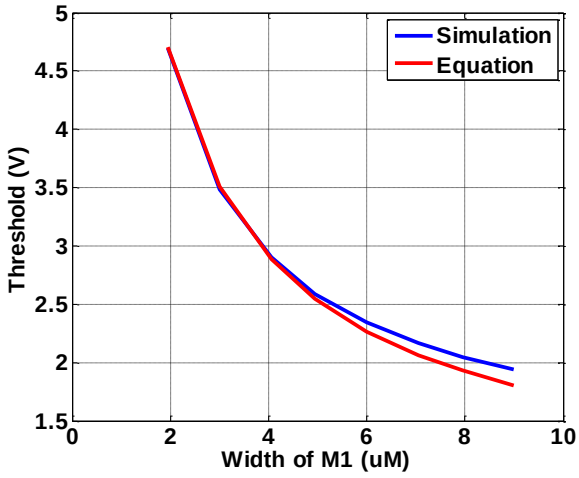


Figure 2-19. Comparison of thresholds for positive indicators from simulations and Alpha-power law when Vdd(die)-Vss(die)=constant

If Vdd(die) is not held constant with respect to Vss(die) during the ESD event, then the match is not as good as is shown in Fig. 2-20. This mismatch happens because the change in Vdd during the event changes the threshold of the M4-M5 inverter and this changes the $V_{"A",sw}$ term in the equations. This issue will be addressed later in the discussion.

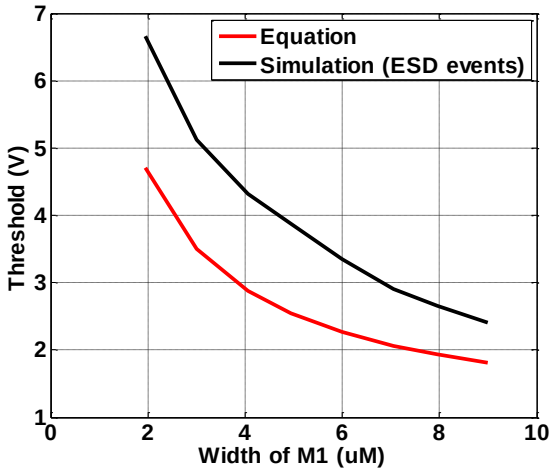


Figure 2-20. Comparison of thresholds for positive event indicators from simulations and Alpha power law when Vdd(die)-Vss(die) is not constant

A similar analysis was done for the negative event detectors, like the one shown in Fig. 2-21. Simulations were done with a slowly ramped current injected into the pin, while the power supply voltages were held constant with respect to each other. The thresholds were recorded during these simulations.

The equation for the trigger of a negative event detector is similar to that for a positive detector:

$$-V_{pad,sw} = \left|V_{t,M1}\right| + \left(\frac{K_{M2} * W_{M2}}{K_{M1} * W_{M1} * P_{v,M2}} \left(\left|V_{dd}\right| - \left|V_{t,M2}\right|\right)^{\alpha_{M2}/2} * \left(\left|V_{"A",sw} - V_{dd}\right|\right)\right)^{1/\alpha_{M1}} \quad (2.10)$$

A comparison of the calculated and simulated thresholds is shown in Fig. 2-22. When the power supply voltage is held constant, the theoretical and simulated values of trigger voltage match within less than 0.2 V.

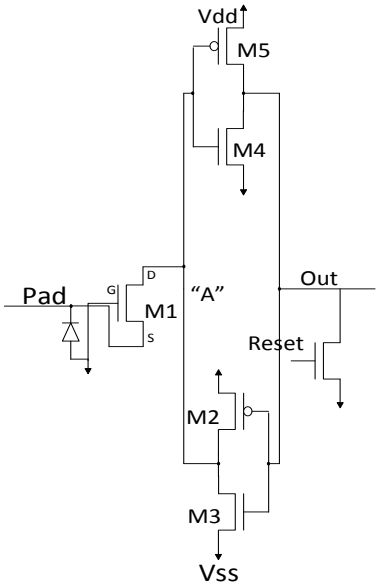


Figure 2-21. Negative event indicator

When Vdd is not noisy the thresholds of the out-of-range voltage detectors can be predicted well. Vdd will not be constant, however, for real application. The ESD events will cause significant changes in the power supply voltage (Vdd-Vss). This disturbance depends on the rise time and duration of the ESD event, which can have a wide range of rise times and durations when they affect a pin of an IC. This uncertainty in power supply voltage causes the thresholds for the detector circuits to be dependent on the type of the

event, since dependence of voltage at node “A” is different compared to dependence of M4-M5 inverter threshold on power supply.

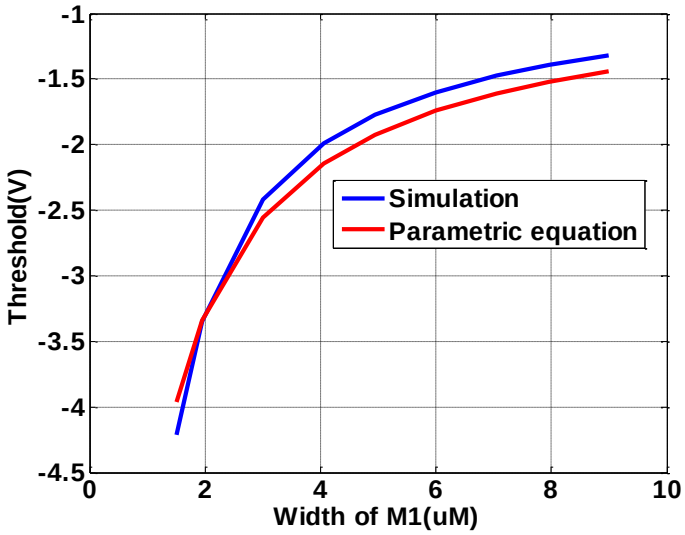


Figure 2-22. Comparison of thresholds for negative event indicators from simulations and Alpha power law when Vdd(die)-Vss(die)=constant

During switching of the latch in positive event detector (refer Fig. 2-10), M2 can be assumed as a pull-down resistor of value R while M1, which is in saturation, can be assumed to be to be a voltage controlled current source of current say I, hence voltage at node “A” can be given by equation 2.11

$$V_{"A"} = V_{ss} + I * R \tag{2.11}$$

Since, the latch switches when $V_{"A"}$ reaches switching threshold of M4-M5 ($V_{"A",sw}$), if the threshold for M4-M5 could be made proportional to power supply (V_{ss} in this case), in a similar manner to $V_{"A"}$, then the detector thresholds would become almost

independent from type of ESD events. This independence is required if the detector is to be used like an A/D converter.

Methods suggested to achieve desired proportionality between Vdd and M4-M5 inverter threshold (referred to as $V_{"A",sw}$ from now on) are shown in Fig. 2-23. One possibility is to make M4 very wide. Another is to make is to make the M4-M5 inverter a current-source-load inverter. Each of these options will be discussed in detail below.

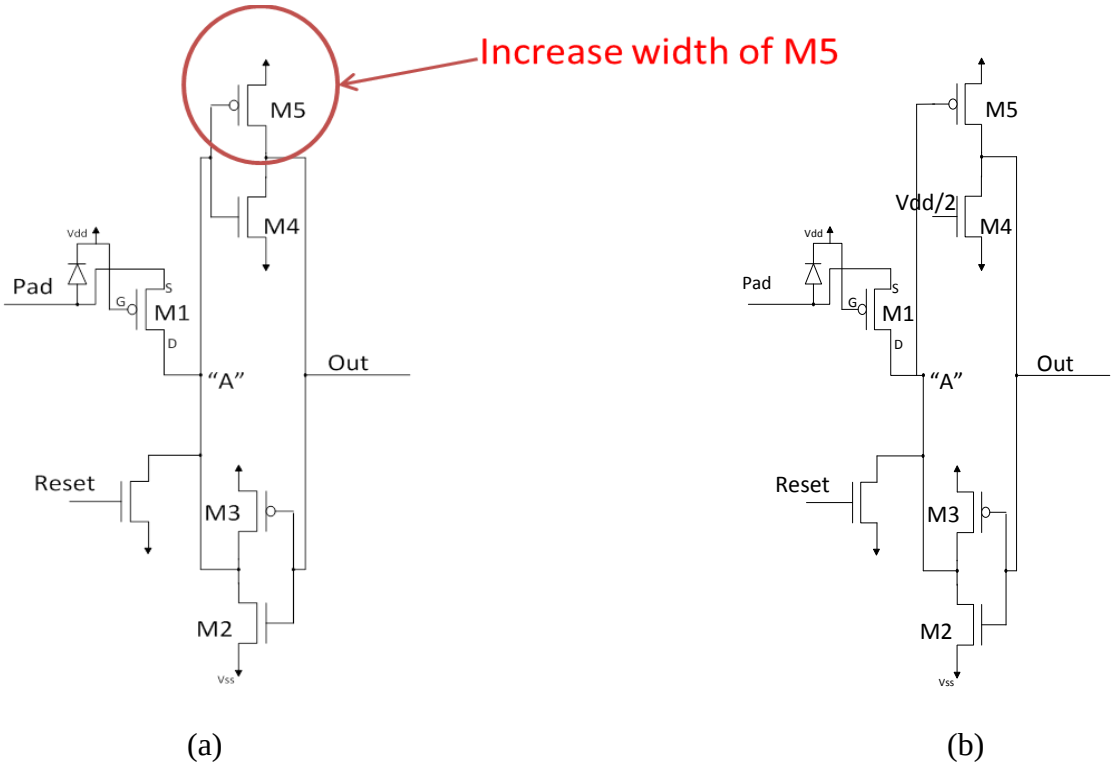


Figure 2-23. Methods to achieve proportionality between switching threshold of M4-M5 inverter and Vdd(die) (a) Increase width of M5 to be much larger compared to that of M4 (b) Make M4-M5 a current source load inverter

2.1.3.1 Increasing size of M5. The equation for the switching threshold of M4-M5 inverter is given as [12]:

$$k'_{M4} * V_{dsat,M4}(V_{"A",sw} - V_{ss} - V_{t,M4} - \frac{V_{dsat,M4}}{2}) + k'_{M5} * V_{dsat,M5}(V_{"A",sw} - V_{dd} - V_{t,M5} - \frac{V_{dsat,M5}}{2}) = 0$$

Giving

$$V_{"A",sw} = C + \frac{r}{r+1}\left(V_{dd} - V_{ss} + V_{t,M5} + \frac{V_{dsat,M5}}{2}\right) \quad (2.12)$$

where:

$$r = \frac{k'_{M5} * V_{dsat,M5}}{k'_{M4} * V_{dsat,M4}} = \frac{v_{sat,M5} * W_{M5}}{v_{sat,M4} * W_{M4}},$$

the term "C" is independent of Vdd, and W_{M5} and W_{M4} are channel widths of M5 and M4 respectively. If $W_{M5} >> W_{M4}$ then $(r/r+1) \rightarrow 1$ which will allow $V_{"A",sw}$ to change directly with V_{dd} or V_{ss}.

Simulated results for positive event thresholds are shown in Fig. 2-24 and 2-25. For Fig. 2-24, the sizes of the FETs were:

M1: 9 um/0.6 um
M2: 1.5 um/0.6 um
M3: 3 um/0.6 um
M4: 1.5 um/0.6 um
M5: 6 um/0.6 um

As discussed before, thresholds were found for both slow events and ESD events and compared. The difference between the thresholds for a slow and fast event in Fig. 2-24 was up to about 0.87 V when M5 was 6 um wide. Figure 2-25 shows the results when M5 was 20 um wide. Surprisingly, changing the size of M5 did not give the expected improvement in the threshold match for slow and fast events, the difference in thresholds of slow and ESD events is still up to 0.86 V.

2.1.3.2 Current-source load inverter. In this configuration, the M4-M5 inverter is converted to a current-source load inverter with M4 held in saturation with a gate-to-source voltage $V_{gs}=V_{dd}/2$, as shown in Fig. 2-26. The gate voltage of M4 is specifically set to follow changes in Vdd.

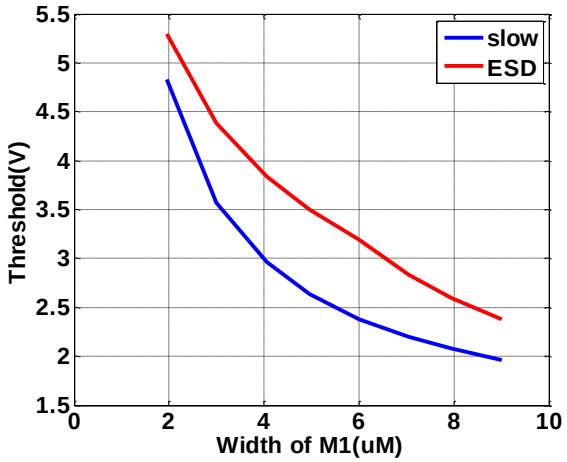


Figure 2-24. Comparison between positive event thresholds for slow and ESD events when M5=6u wide

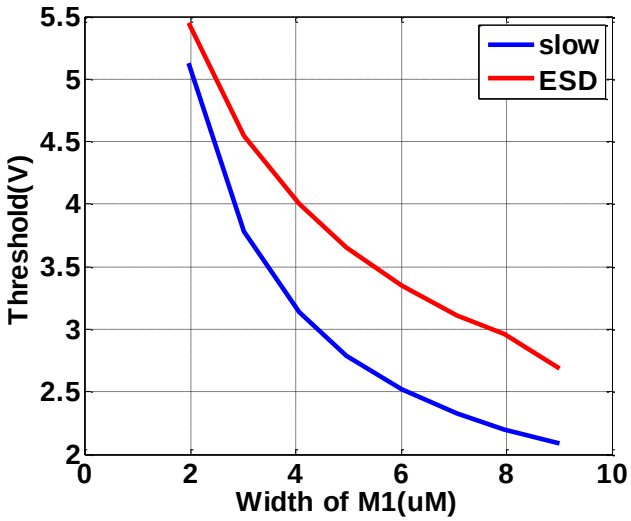


Figure 2-25. Comparison between positive event thresholds for slow and ESD events when M5=20u wide

At the point of switching, $V_{"A"}=V_{out.}$ and both M5 and M4 are in saturation. Equating currents in M5 and M4:

$$K'_{M5}*(\frac{W}{L})_{M5}*(V_{"A",sw}-V_{dd}-V_{t,M5})^2 = K'_{M4}*(\frac{W}{L})_{M4}*(\frac{V_{dd}-V_{ss}}{2}-V_{ss}-V_{t,M4})^2$$
$$\sqrt{\frac{K'_{M4}*(\frac{W}{L})_{M4}}{K'_{M5}*(\frac{W}{L})_{M5}}}*(\frac{V_{dd}}{2}-\frac{3V_{ss}}{2}-V_{t,M4})+C=V_{"A",sw} \quad (2.13)$$

K'_{M4} is roughly twice of K'_{M5} , if $L_{M4}=L_{M5}$ then WM4 and WM5 can be selected such that $V_{"A",sw}$ changes directly with power supply. For example if linearity with V_{dd} has to be achieved then setting $W_{M4}=2*W_{M5}$ gives relation as shown by equation 2.14.. The resulting match between the thresholds for slow and fast events is shown in Fig. 2-27. The match in this case is within less than 100 mV.

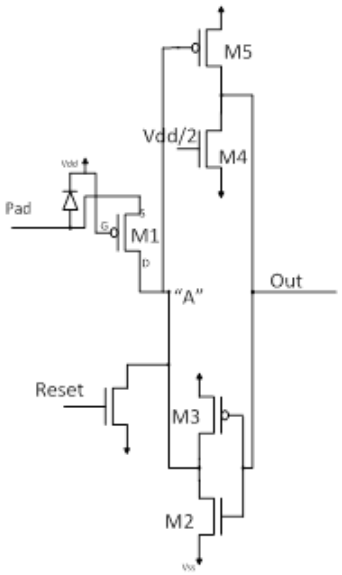


Figure 2-26. Positive event indicator with M4-M5 inverter with current source load

$$V_{"A",sw}=2*(\frac{V_{dd}}{2}-V_{t,M4})+C$$
$$V_{"A",sw}=V_{dd}+(2*V_{t,M4})+C \quad (2.14)$$

Note that theoretically the gate bias of M4 has to be kept at $V_{dd}/2$ and M4 width should be double to that of M5 but practically these conditions overpower M5 and circuit is always latched. For this reason gate bias of M4 is reduced from $V_{dd}/2$ to $(1.5/5)*V_{dd}$ and its size changed to accommodate change in gate bias. Simulations for results shown in Fig. 2-27 include these modifications.

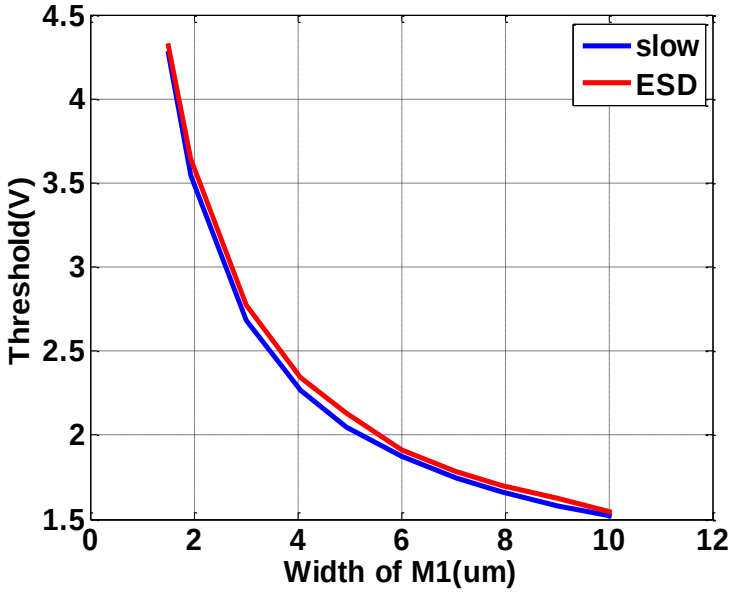


Figure 2-27. Comparison of positive event indicator thresholds for slow and ESD events for M4-M5 inverter having M4 as current source load

One possible issue with the circuit is that M4-M5 always consumes current – at least until an event is detected and the output is low. For some applications this static current might be acceptable and others not. To minimize static current, it is possible to only turn on the M4 during testing conditions, when static current is acceptable, and turn it off otherwise, for example by controlling the gate voltage at M4. Another possibility is to turn M4 on using a sensor circuit, like the one in Fig. 2-28. A second detector is added

which will turn on only during the transient event. This inverter will turn on the M4/M5 inverter and allow it to detect the event. Only one such "detector" is needed for all latches at a pad, so does not add significant cost/complexity to the design. Since M4 will be turned off after the event has passed, an additional weak pull-down is added to the output keep the output latched after the event has passed.

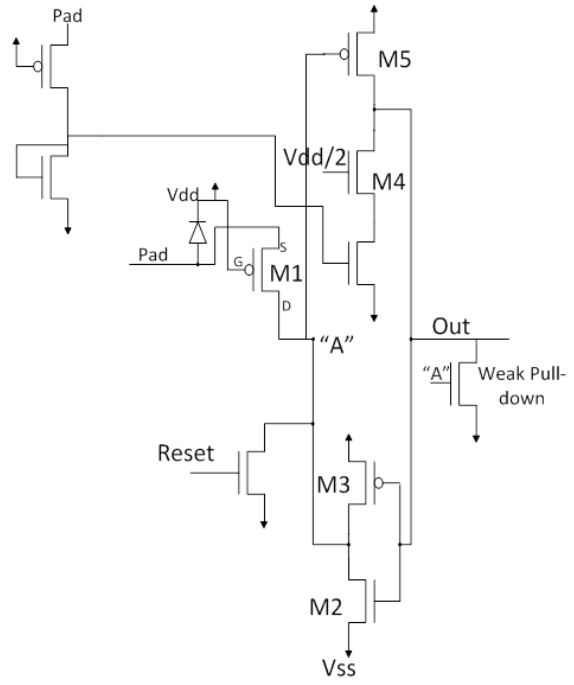
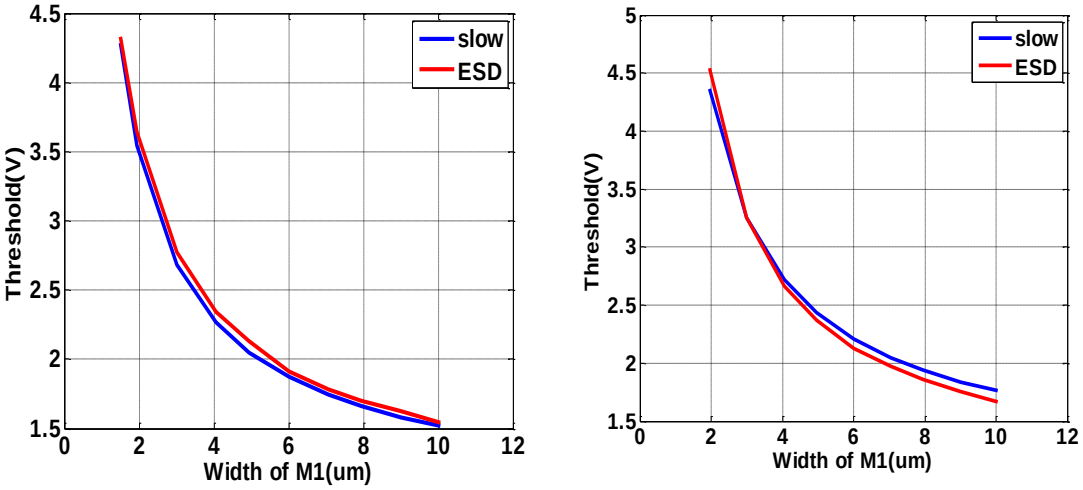


Figure 2-28. Positive event indicator with M4 as current source load and optimizations to have minimal static current consumption

Figure 2-29 shows comparison of thresholds for slow and ESD events (Figure 2-29(a) for current source load inverter configuration, Fig. 2-29(b) for modified version of the configuration as shown in Fig. 2-28). Comparing the results of Fig. 2-29(b) with Fig. 2-29(a), results with non-modified current-source load inverter configuration, notice that not only the thresholds for both slow and ESD events change by themselves (less than

9%) but also the match between slow and ESD events changes. For un-modified circuit the thresholds for slow and ESD events were less than 0.1 V apart throughout, while with modifications they are at 0.2 V maximum difference. Note that this result can be improved by changing size of M4 as needed, but with 0.5 um technology only this level of tuning could be achieved.



(a) (b)

Figure 2-29. Comparison of thresholds for slow and ESD events with (a) current source load inverter configuration (b) modified current source load inverter configuration

2.2 OSCILLATORS

The last section presented a possible instantaneous A/D converter that converts the peak voltage at the input to a digital level based on triggering one or more voltage-sensitive latch circuits. Another possibility for converting the input level to a digital reading is using an oscillator-based A/D. The basic idea is to use an oscillator configuration where the number of oscillations over a given time will vary with the pad

voltage during the event. By counting the number of oscillations, a digital level can be obtained.

2.2.1 Concepts and Schematics. Multiple methods of implementing an oscillator-based A/D for a transient event are possible. One scheme presented in this section is self-triggered and is automatically triggered during the transient event. The others require an out-of-range voltage detector with very small threshold to trigger the oscillator when a transient event occurs. For the windowed oscillator, the oscillator counts the number of oscillations over a fixed window of time to determine the level of the event to determine the energy in the event. In yet another approach, the trigger starts the oscillator after the event has passed. A capacitor is charge to the peak level of the event, and the number of oscillations is dependent on the time it takes to discharge the capacitor through a resistor.

2.2.1.1 Self-triggered oscillator. The self-triggered oscillator in Fig. 2-30 will oscillate whenever the pad voltage goes above Vdd (for a positive event). The frequency of oscillation depends on the pad voltage. The total number of oscillations depend both on the voltage over the event as well as its duration, given a rough measure of the energy in the event. The number of oscillations is counted using an asynchronous counter.

2.2.1.2 Windowed oscillator. Two windowed oscillator circuits were investigated. The first is shown in Fig. 2-31.

Each I/O pad will need an out-of-range voltage detector, like those discussed in Section 2.1, with a very low trigger threshold so that it will trigger for any ESD event that the I/O pad receives. When the pad goes above Vdd (for a positive event) the ring oscillator will oscillate. The frequency of oscillations for the ring-oscillator is dependent

upon the pad voltage. The length of time over which the oscillator is active depends on a built-in delay in the circuit. This option allows the oscillator to only count for a short, fixed duration. If the measurement window is kept long enough to capture the whole event, then the energy of the event is measured as with the self-triggered oscillator. If the window is short, then the energy is only measured within a small window, which may or may not capture the peak of the event.

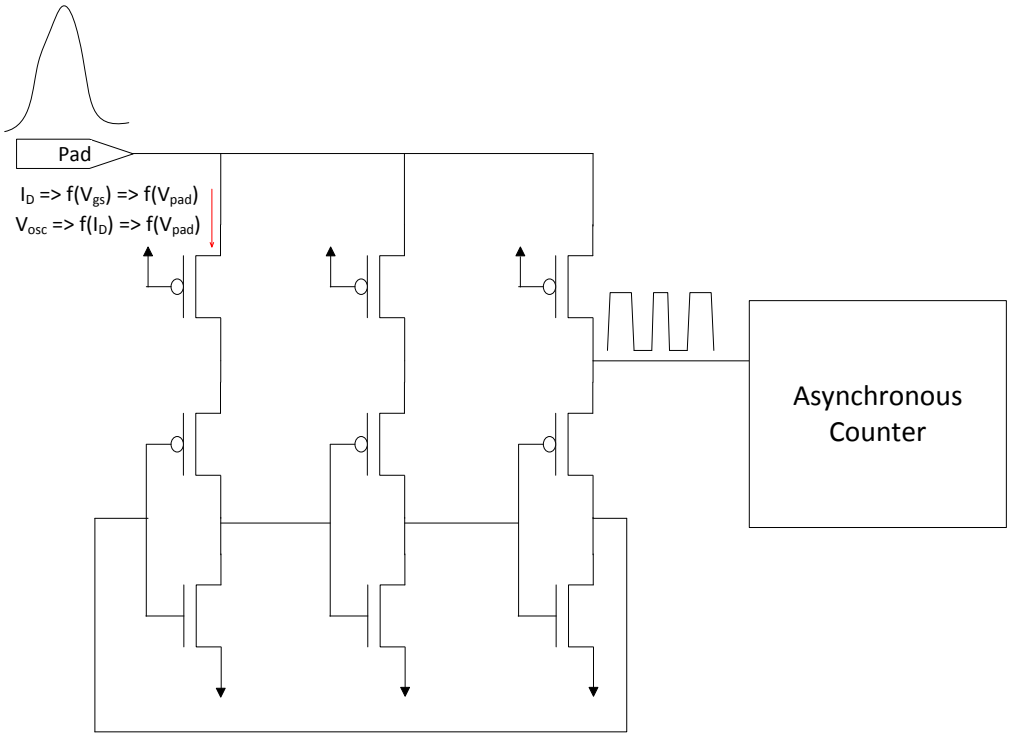


Figure 2-30. Self-triggered oscillator for measuring energy in a transient event

2.2.1.3 RC-based oscillator. The windowed oscillator in Fig. 2-31 can capture a voltage, but that voltage may or may not occur at the peak. To capture the voltage at the peak of the event, a diode and capacitor were added as shown in Fig. 2-32.

Theoretically the capacitor can only be discharged by leakage from the diode or leakage from M1. A voltage detect signal is used to trigger the oscillator. The voltage detect signal is generated from an out-of-range voltage detector but is delayed by some time to allow the disturbance on the power deliver network to pass (e.g. 200 ns) and to ensure the capacitor is charged to the peak level of the event. The voltage detect signal activates the ring oscillator and turns on M1 to discharge the capacitor. The oscillator frequency is controlled by the voltage on the capacitor. The length of time the oscillator runs depends on the time to discharge the capacitor through M1. Thus, the number of oscillations depends upon peak voltage stored on capacitor. The peak level of the ESD can be approximated from the count.

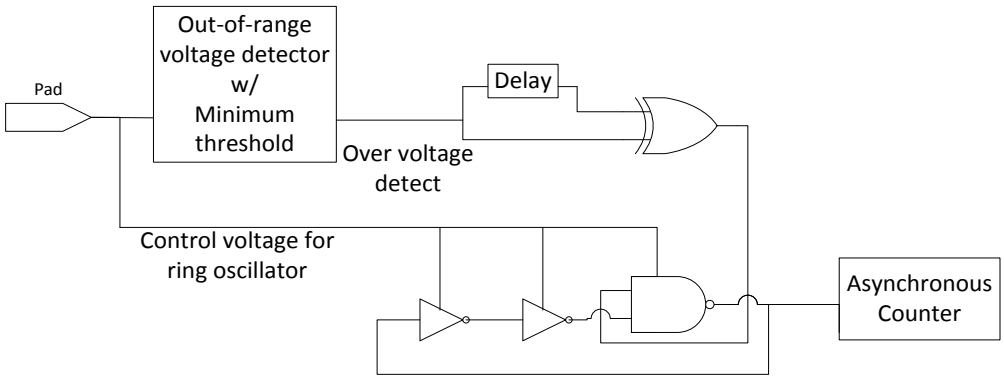


Figure 2-31. Windowed oscillator for measuring voltage of transient events

2.2.2 Simulation Models. The simulations for the oscillator-based level sensors were similar to the simulations for the out-of range voltage detectors. The basic

simulation setup for both sets of simulations is shown in Fig. 2-33. In this case, the test circuit is the oscillator-based level sensor.

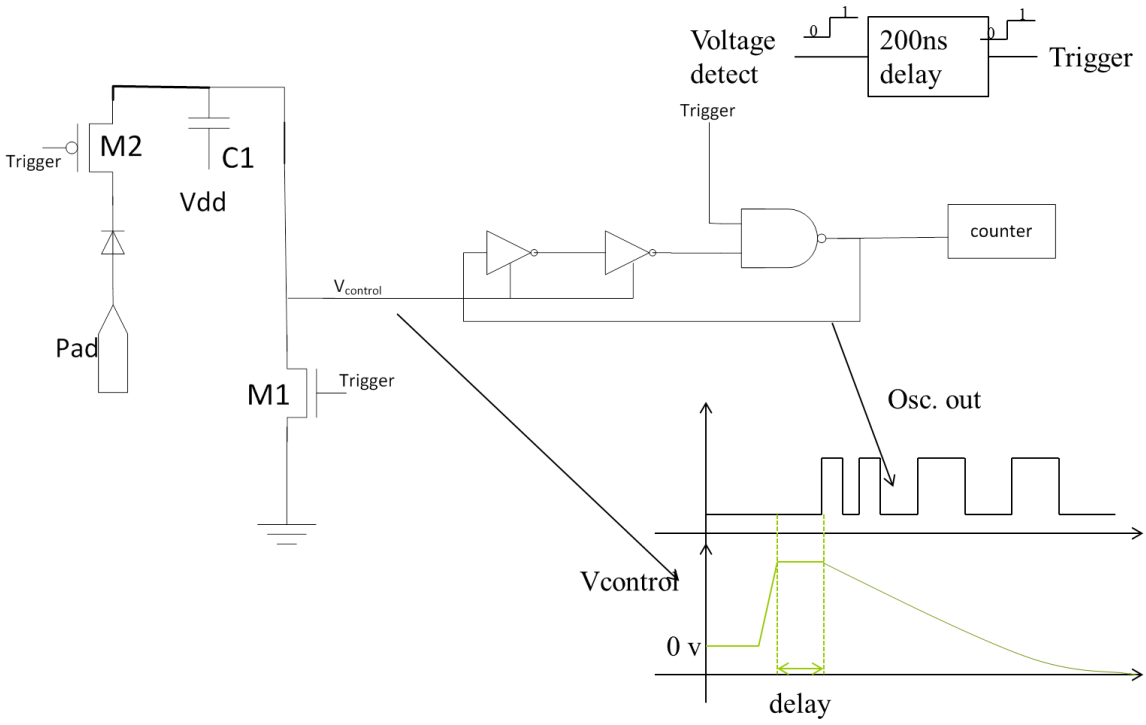


Figure 2-32. The RC-based oscillator stores the maximum pad voltage on a capacitor and then counts the number of oscillations while the capacitor is discharged

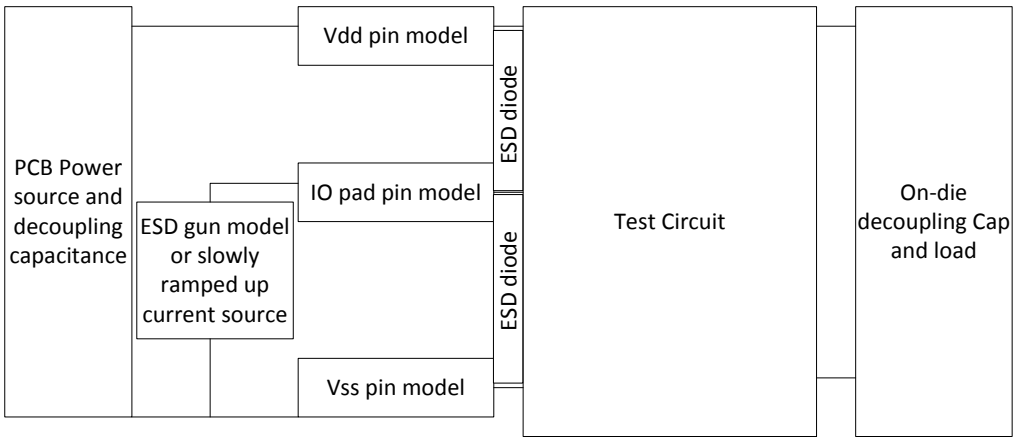


Figure 2-33. General simulation model for testing different circuits

2.2.3 Simulation Results and Analysis. Simulations were performed for each oscillator-based sensor as discussed in the following sub-sections.

2.2.3.1 Self-triggered oscillator. Simulations with the self-triggered oscillator were performed with positive events. Schematic for simulations is shown in Fig. 2-34 The circuit was tested for both ESD and slow events. ESD events were simulated using the ESD source model and slow events were created using an ideal current source in Virtuoso which injects slowly ramped currents into the test pin.

Initial tests were done by holding V_{dd}(die) and V_{ss}(die) constant with respect to each other. Results when injecting a slow event with a 3.5 A peak are shown in Fig. 2-35. Results when injecting an ESD event with a 3.5 A peak are shown in Fig. 2-36. The number of oscillations is determined by the number of rising edges. This count will be used as a measure of the level of the event. Figure 2-37 shows the variation in the output count with the level of current injected to the pin. It is clear from Fig. 2-37 that this circuit implementation gives a measure of energy in the event rather than the peak of the event. This measure of energy gives a larger count for a slow event with the same peak current as an ESD event, which passes relatively quickly.

Simulations with a noisy PDN i.e. V_{dd}(die) and V_{ss}(die) not held constant w.r.t. each other are done. Figure 2-38 shows such a simulation for slow events and Fig. 2-39 shows the simulation for ESD event.

Figure 2-40 shows that the self-triggered oscillator is not resistant to PDN noise and hence will give a different measure of level for different kinds of events depending upon their rise times, even if they have same amount of energy. As mentioned earlier, this method gives a measure of energy and not the peak disturbance.

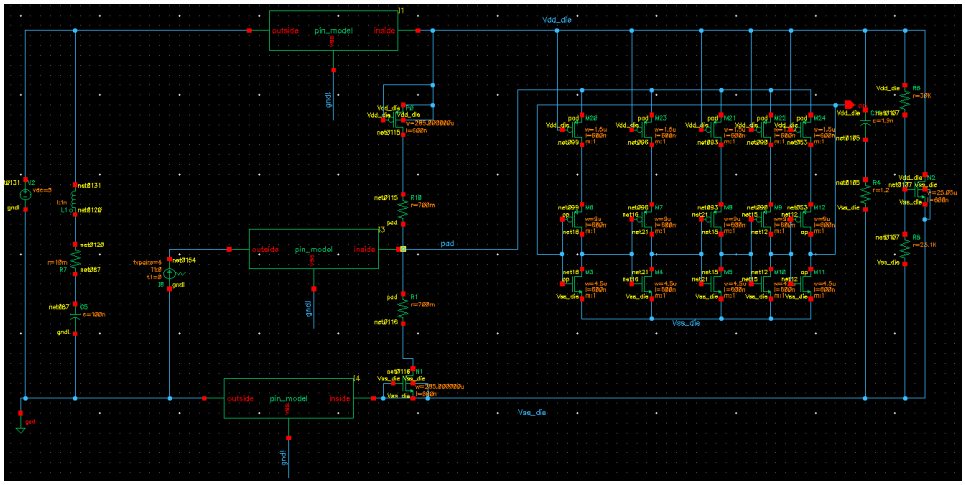


Figure 2-34. Simulation setup for self-triggered oscillator

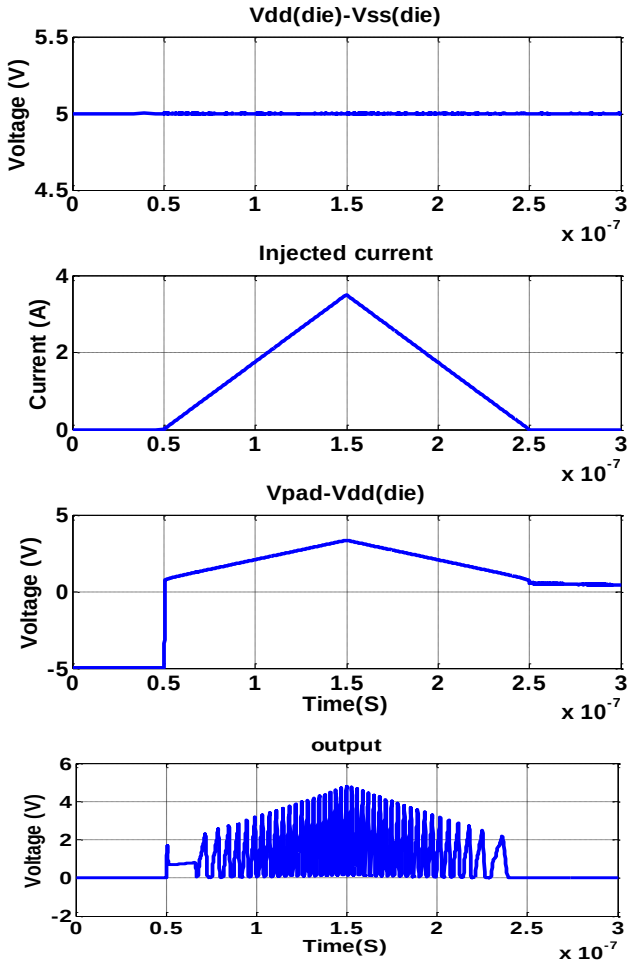


Figure 2-35. Response of self-triggered oscillator to slow events with Vdd(die)-Vss(die) = constant

2.2.3.2 Windowed oscillator. The windowed oscillator was implemented as shown in Fig. 2-41. The out of range voltage detector is the same detector discussed in Section 2.1 with a very low threshold so it can trigger on almost all transient events on the pad. The implementation used here is shown in Fig. 2-42.

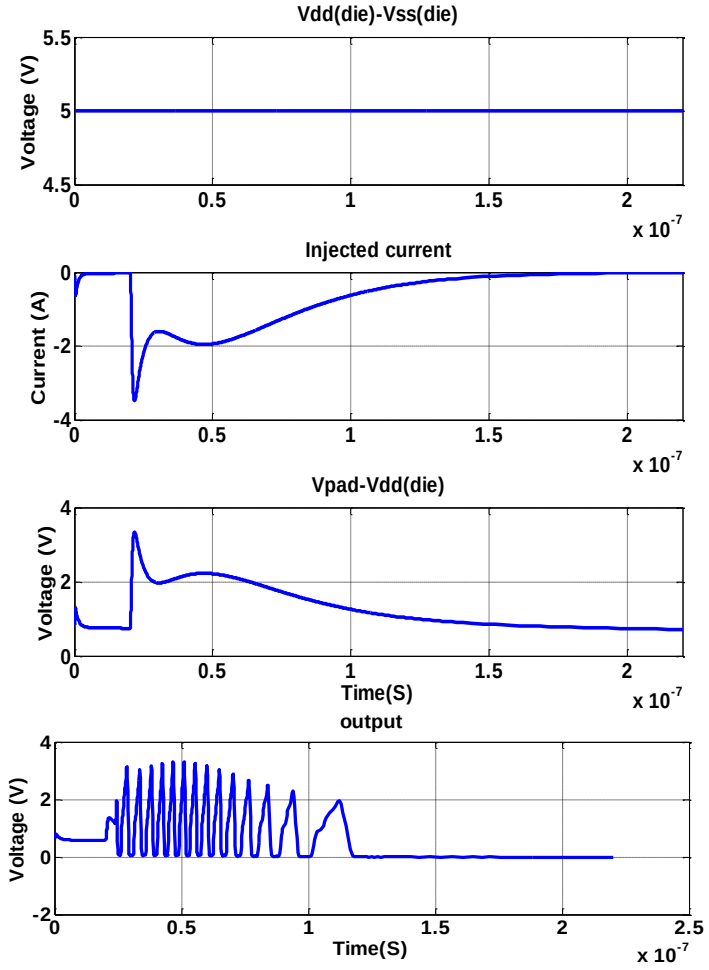


Figure 2-36. Response of self-triggered oscillator with Vdd(die)-Vss(die)=constant

For the proof-of-concept implementation, the delay line was implemented using inverters and capacitors as shown below in Fig. 2-43. This delay line gives approximately

a 115 ns delay between a transition of the input and a transition of the output as shown in Fig. 2-44.

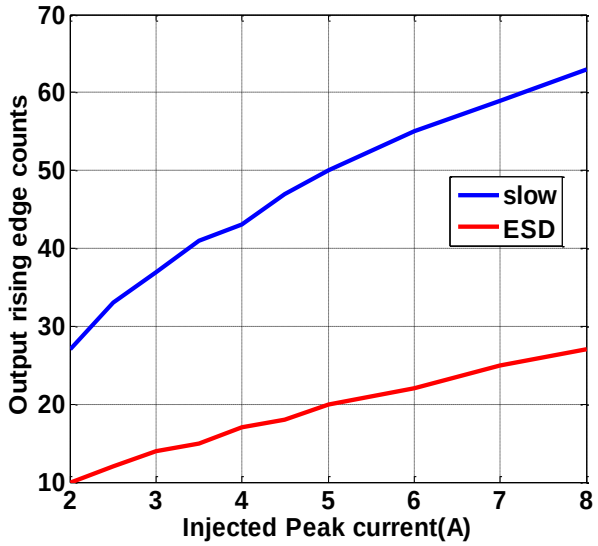


Figure 2-37. Comparison of output counts for self-triggered oscillator for slow rise/fall time and for positive ESD events when Vdd(die)-Vss(die)=constant

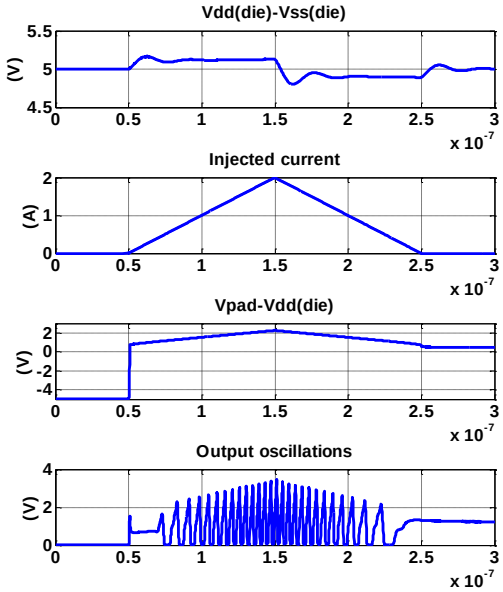


Figure 2-38. Response of self-triggered oscillator during a slow event when Vdd(die)-Vss(die) is not constant

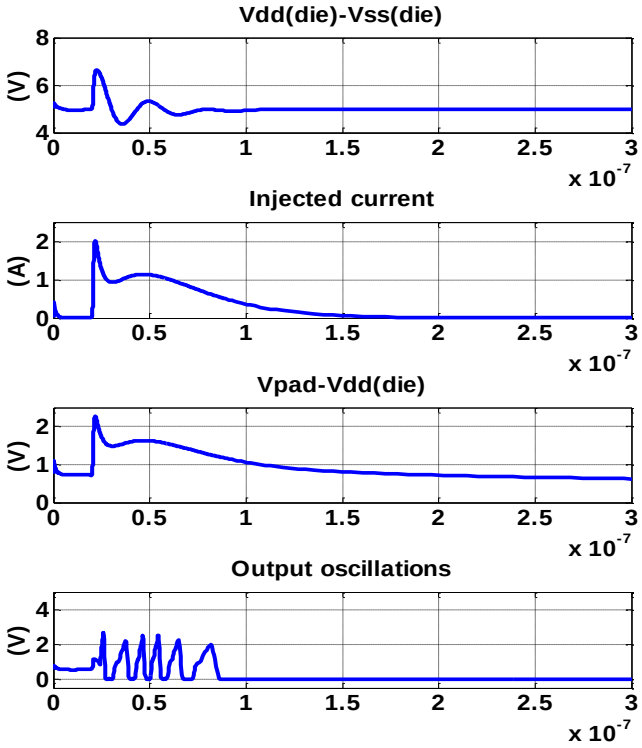
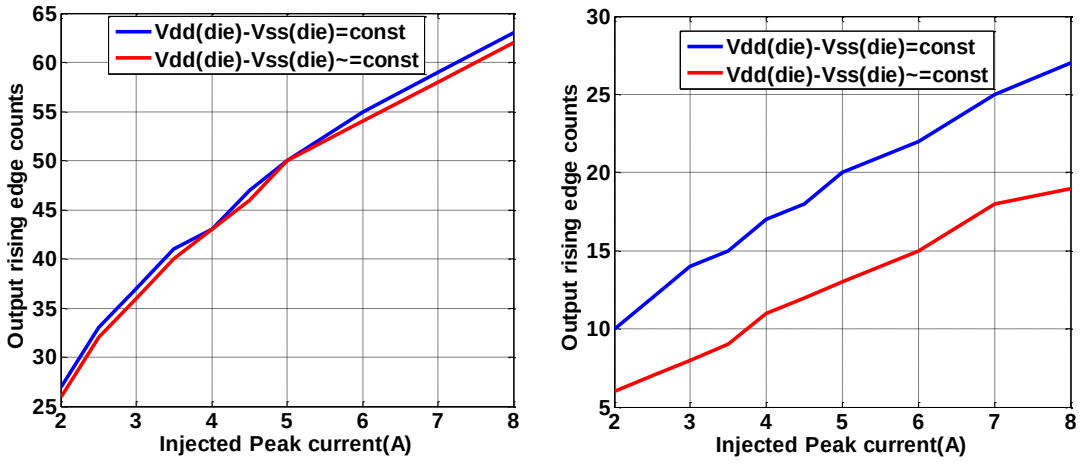


Figure 2-39. Response of self-triggered oscillator during an ESD event when Vdd(die)-Vss(die) is not constant



(a) (b)

Figure 2-40. Comparison of output counts for cases with and without Vdd(die)-Vss(die)=constant (a) for slow events (b) for ESD events

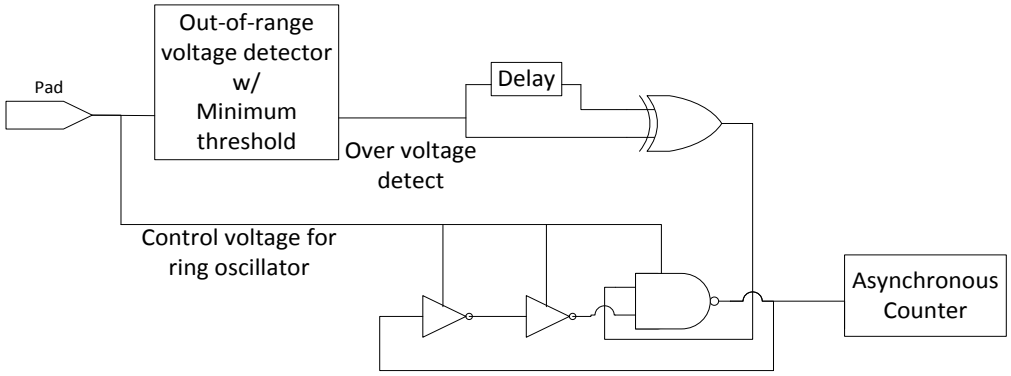


Figure 2-41. Windowed oscillator level sensor

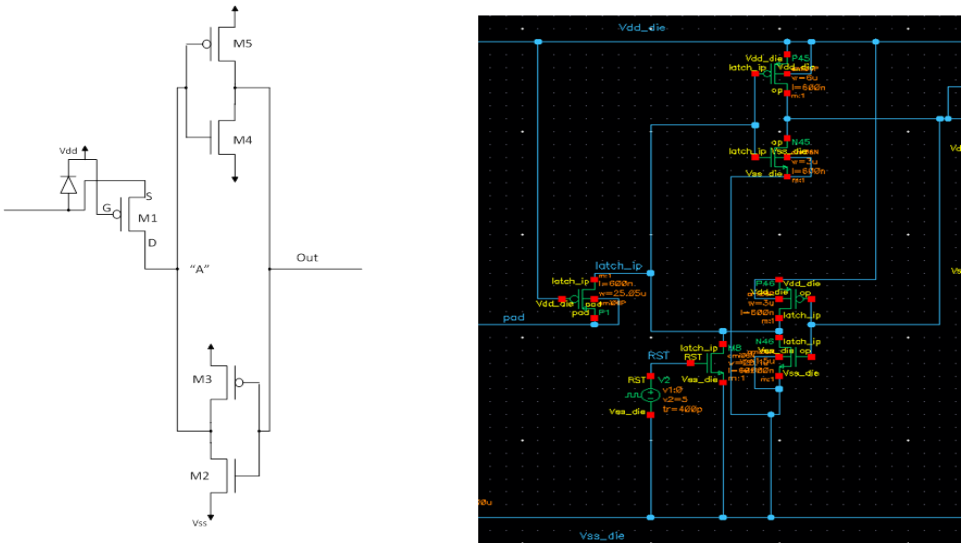


Figure 2-42. Implementation of the out-of-range voltage detector

The XOR gate implementation is shown in Fig. 2-45. The XOR gate is used to generate a window of operation for the oscillator to measure the level of the event.

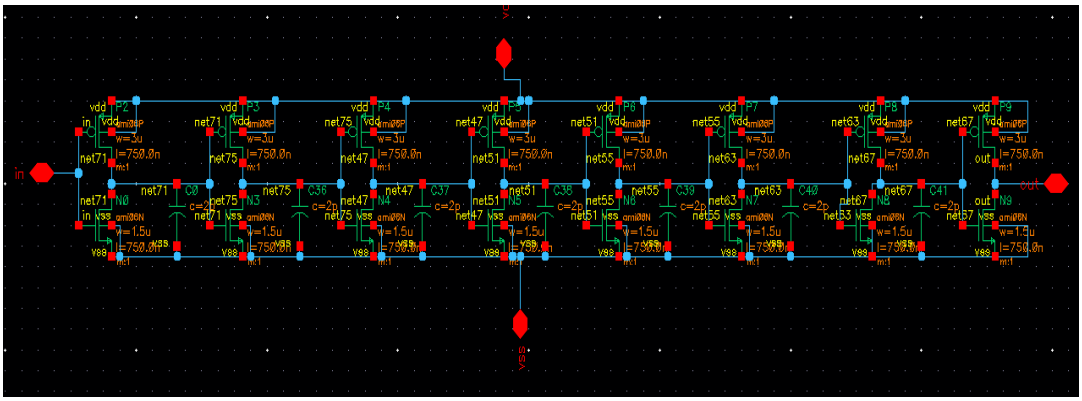


Figure 2-43. Implementation of delay line

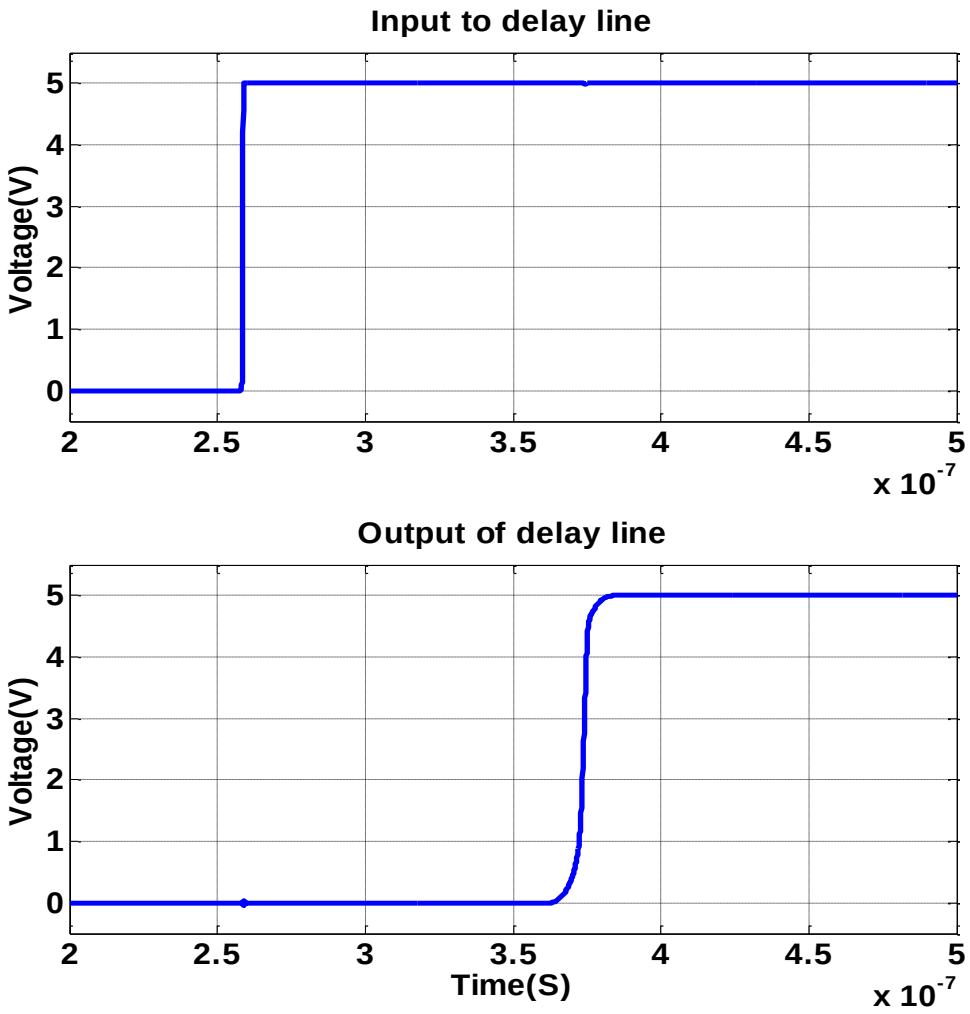


Figure 2-44. The delay line has a 115ns delay from input to output

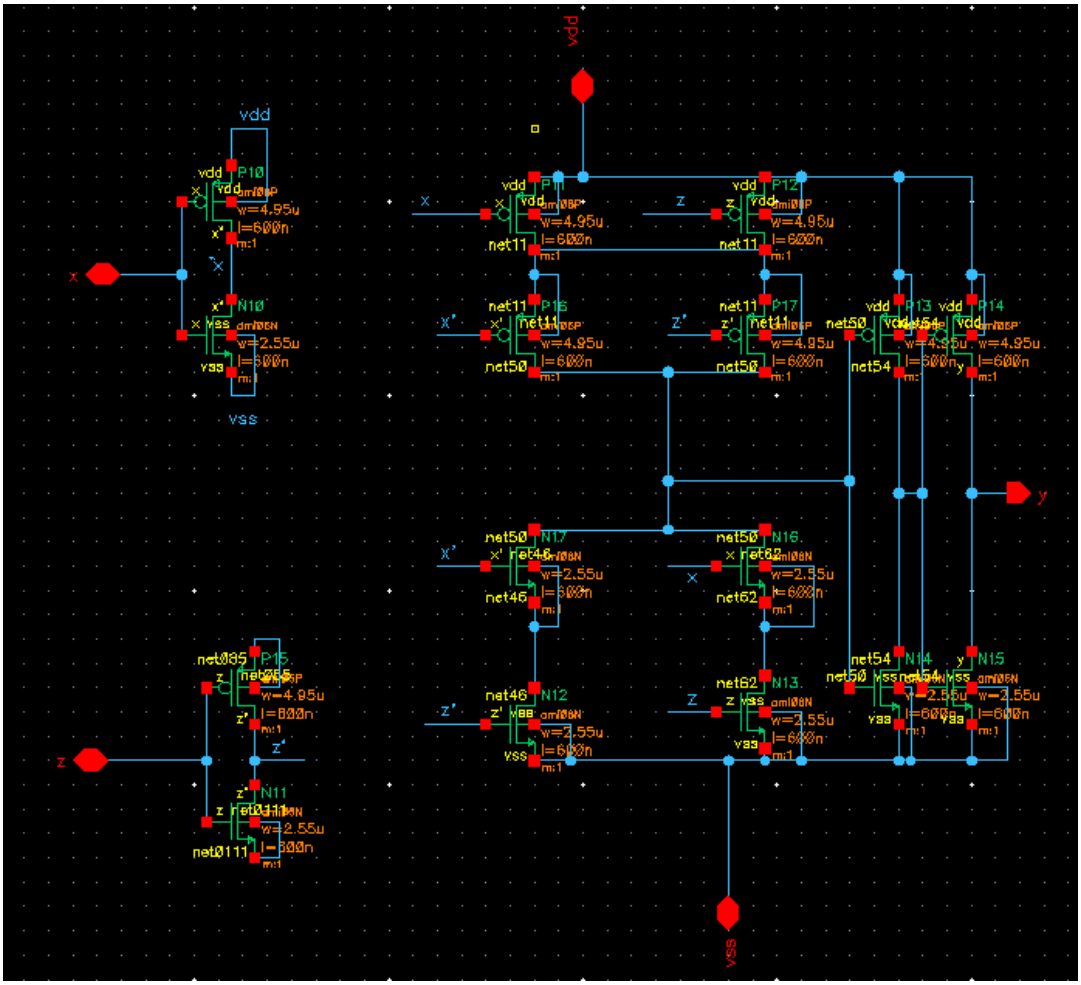


Figure 2-45. XOR gate implementation

The oscillator was implemented as shown in Fig. 2-46. The frequency response of this oscillator to the control voltage (pad voltage) is shown in Fig. 2-47. The relation is close to linear when the pad voltage is at least diode voltage above Vdd(die). The output frequency varies from 100 MHz to 750 MHz

Testing was first done with Vdd(die) and Vss(die) kept constant with respect to each other. Fig. 2-48 shows the response of the oscillator to a slow pulse with a 3 A peak. Figure 2-49 shows the response to an ESD event with a 3 A peak event.

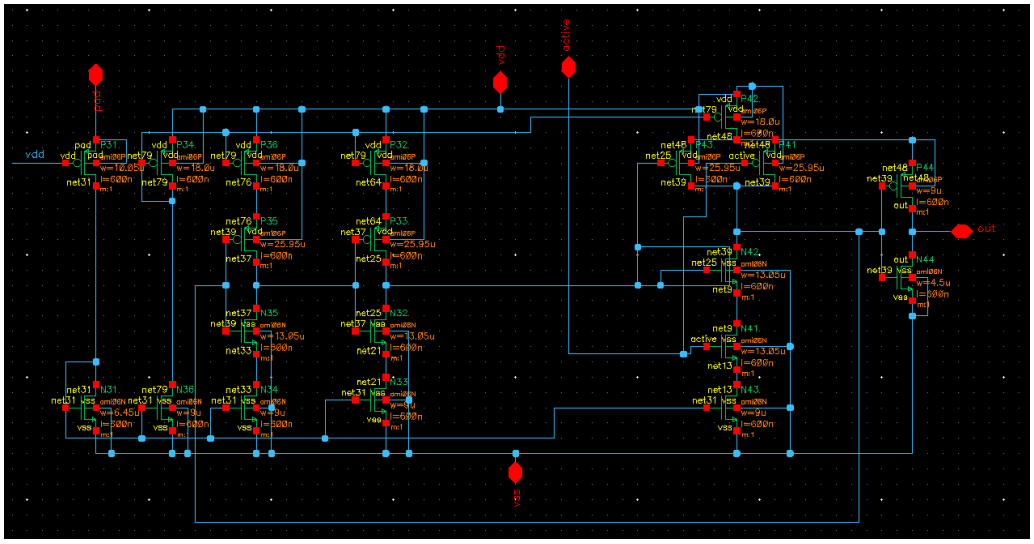


Figure 2-46. Oscillator implementation

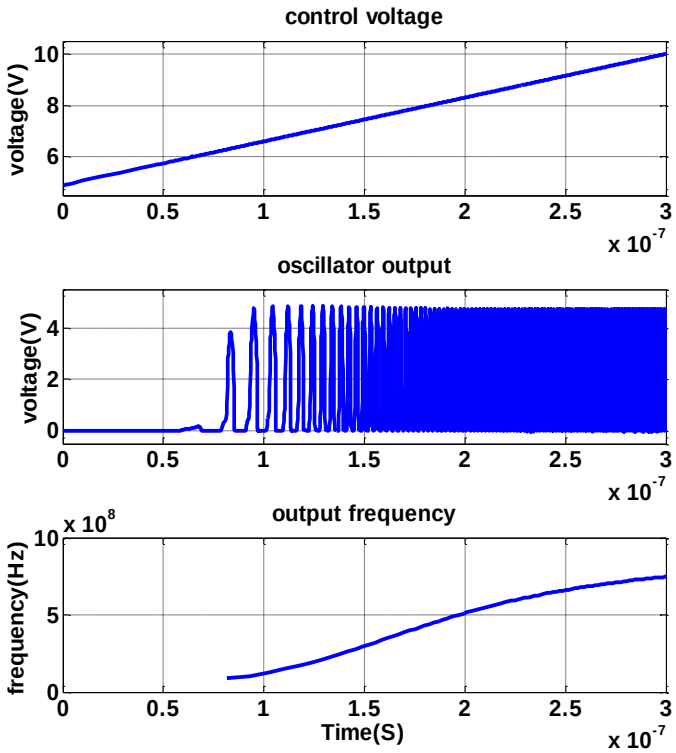


Figure 2-47. Variation of ocillator output frequency with the control voltage

One fact that is evident from the plot is that the portion of the input waveform captured by the event depends much on the waveform. For a very slow event, the count may entirely miss the peak. This mismatch causes different parts of slow event to be captured. For and ESD event, the window can be constructed to reliably capture nearly the entire event.

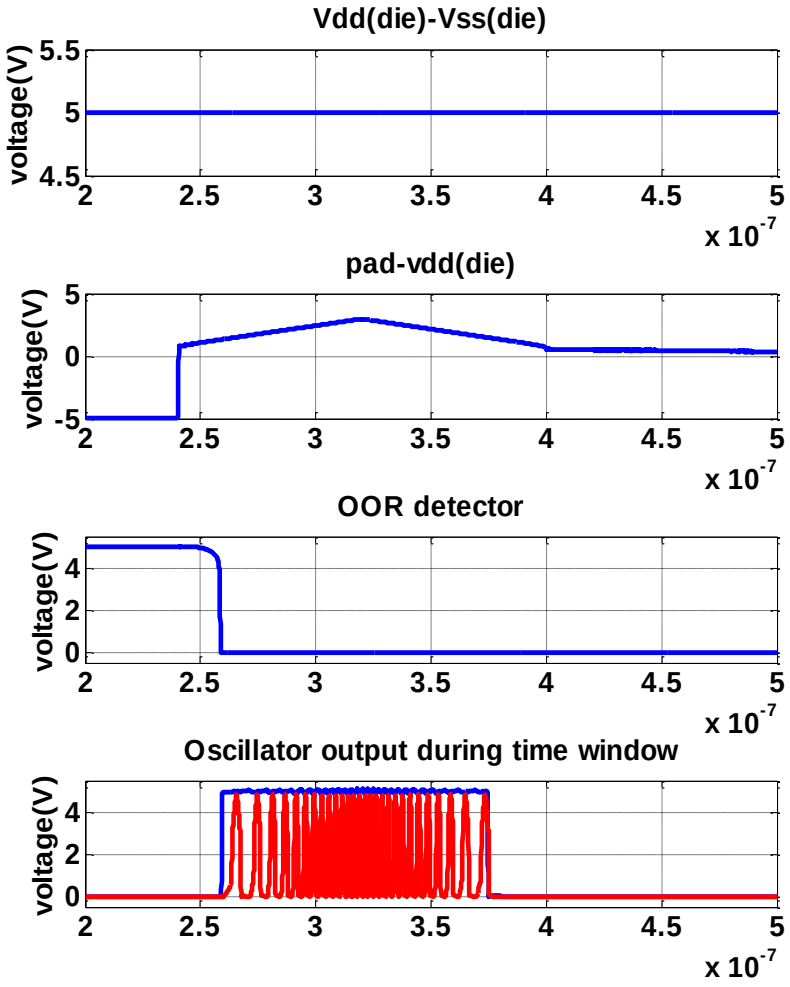


Figure 2-48. Response of windowed oscillator to slow event when Vdd(die)-Vss(die)=constant

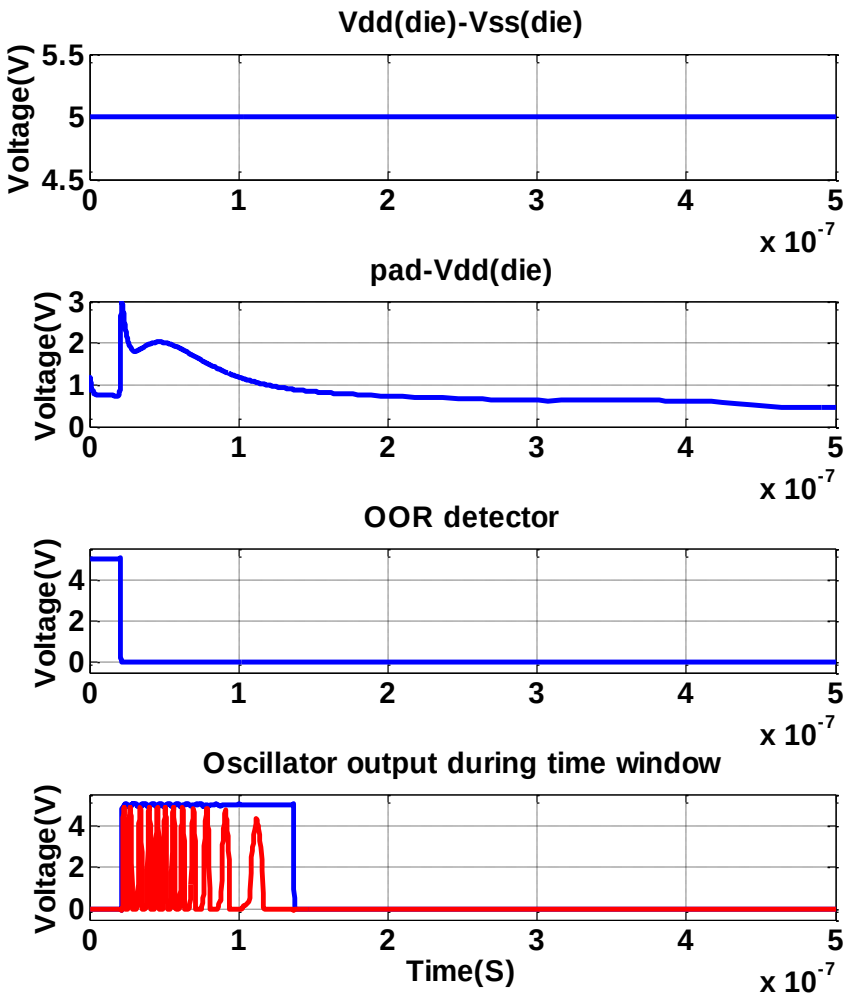


Figure 2-49. Response of windowed oscillator to ESD events when Vdd(die)-Vss(die)=constant

Fig. 2-50 shows a comparison of the output count for slow and ESD events when Vdd(die) and Vss(die) were held constant with respect to each other. Since the measurement window is long, the energy in the event is captured rather than peak of the event. This measure of energy results in higher count for slow events that have the same peak as an ESD event, since the area under the curve may be smaller with the ESD event.

Figure 2-51 shows a comparison of counts in cases with and without Vdd(die) and Vss(die) noise (Figure 2-51(a) shows comparison for slow events and Fig. 2-51(b) for ESD events). The results demonstrate that the count for the windowed oscillator is not significantly affected by the Vdd noise caused by the ESD event. The results differ by a maximum of 10% for large events. This result indicates that the output count is a reliable measure of the energy in the event, even in the presence of power supply noise.

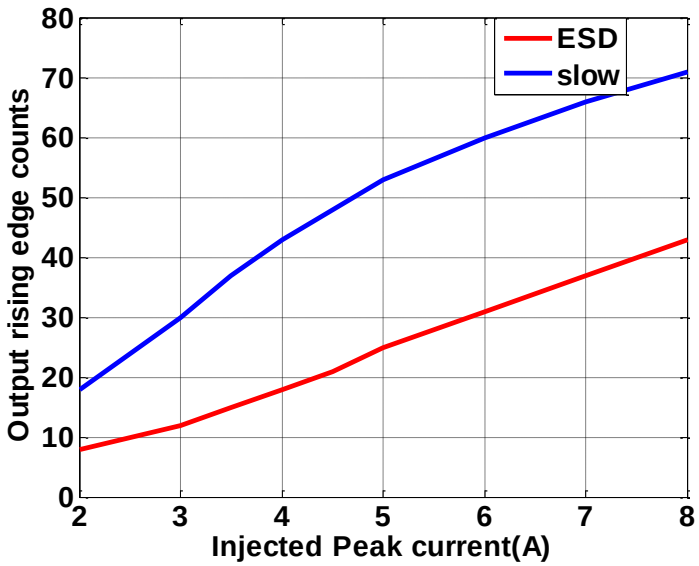
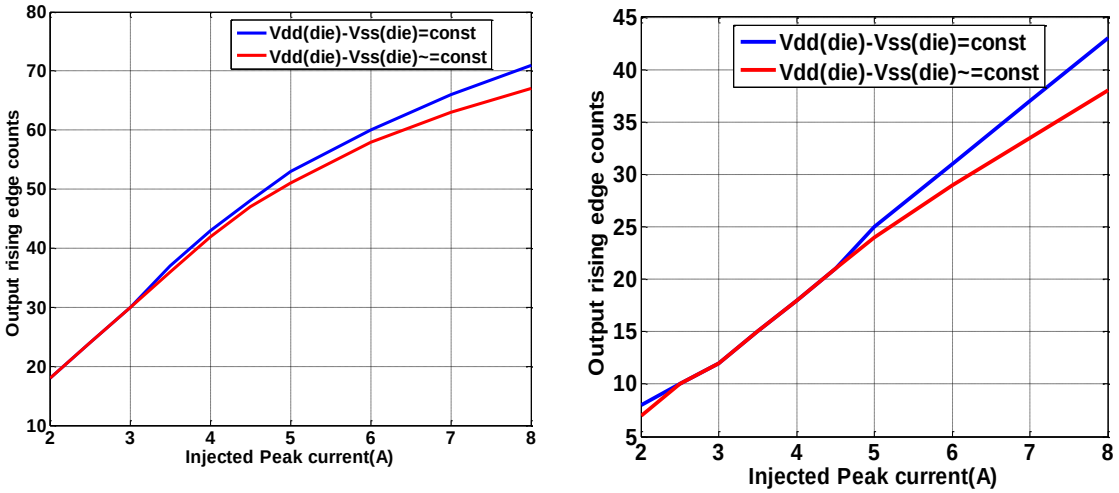


Figure 2-50. Comparison of output counts of windowed oscillator for slow and ESD events while Vdd(die)-Vss(die)=constant

If the window of measurement is made over a small window, then the peak of ESD events with fast rise time can be captured, but this small window will only capture the initial portion of a slow event waveform and may entirely miss the peak. One possible resolution to this issue is to record the number of oscillation over multiple, consecutive small windows one after another and saving the maximum count. This method will

require additional circuit and logic to save multiple counts and compare them. If memory allowed one to save all the counts, one could construct an approximation of the waveform at the pad.



(a) (b)

Figure 2-51. Comparison of windowed oscillator output counts with and without having Vdd(die)-Vss(die)=constant for (a) slow events (b) ESD events

2.2.3.3 RC-based oscillator. Figure 2-52 outlines the basic method for determining the peak level of the event using an RC-based oscillator.

The diode at the pad allows capacitor C1 to charge to within a diode voltage drop of the pad voltage and then keep that charge. Capacitor C1 is referenced to Vdd so that is accurately captures the voltage difference between the pad and Vdd. If C1 were referenced to Vss, the voltage across C1 would be impacted by changes in Vss as well as the voltage at the pad. During normal operation M2 is turned on and M1 is turned off. When an overvoltage event occurs, C1 is charged to within a voltage drop of the peak pad voltage. 200 ns after the event, M2 is turned off, M1 is turned on, and the ring

oscillator is turned on. Waiting until after the event has passed to determine the level mitigates the impact of power supply noise on results. When M1 is turned on, C1 begins to discharge to VSS. M2 is turned off so that C1 can be discharged all the way to VSS, independent of the voltage at the pad. The frequency of oscillation is dependent on the voltage on C1. The period of time the oscillations occur depend on the time it takes for C1 to discharge to VSS. By counting the number of oscillations, one can obtain a measure related to the peak voltage on the pad. A lookup table can be used to correlate the resulting count with the specific voltage value.

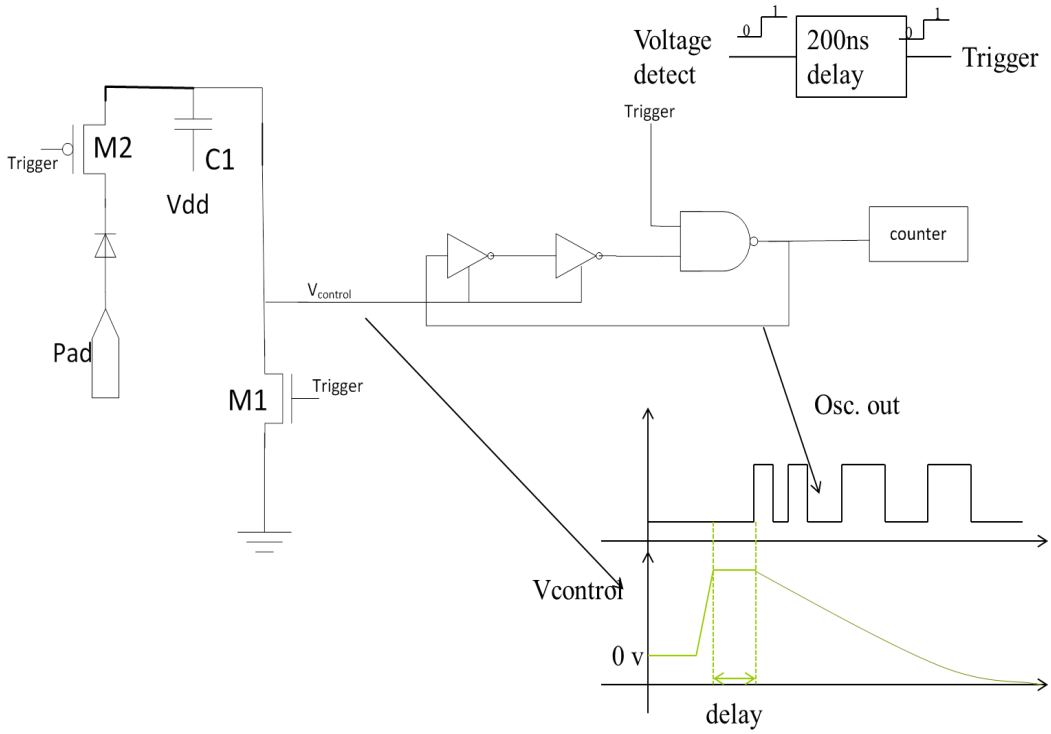


Figure 2-52. Basic concept for determining peak level of the event using the RC-based oscillator

Figure 2-53 shows the behavior of the RC-based oscillator for a slow triangular waveform with a peak current of 3 A and while holding Vdd(die) - Vss(die) constant. Figure 2-54 shows the behavior of the oscillator for an ESD event with a 3 A peak current. Figure 2-55 compares the output count measured for slow and ESD events for different peak levels of the event. Figure 2-56 compares output counts for slow events (Fig. 2-56(a)) and ESD events (Fig. 2-56(b)) with and without a constant power supply. These results demonstrate that the oscillator is largely unaffected by power supply noise. There is, however, a difference in the count for slow and ESD events. For this design, the slow events had a count roughly 20% higher than the ESD events for an 8A event. This difference results because the voltage stored on the capacitor is dependent upon the rise time of the event, due to the resistance between the pad and capacitor C1. In the initial tests, the size of M2 was 10 um/0.6 um. Making M2 wider can reduce the difference, as shown in Fig. 2-57 where the size of M2 was doubled roughly cutting the difference in half. If using a large M2 is unreasonable, the area impact of this large FET could be minimized by using a shared storage (or boost) bus, where multiple pads were connected to the bus through a diode. The peak voltage on any of the I/O connected to the bus would determine the voltage on the capacitor. Only one capacitor and one transistor M1 would be required for the whole bus.

2.2.4 Limitations. The oscillator designs are generally large and may be too large to be implemented for each I/O pad. One option is to implement them only on the most critical pads. Another is to implement a single oscillator for a group of I/O or perhaps for an entire IC, when the IC is small. In this case, the pads would be connected to a “boost” bus through a diode, which would isolate the pads from one another.

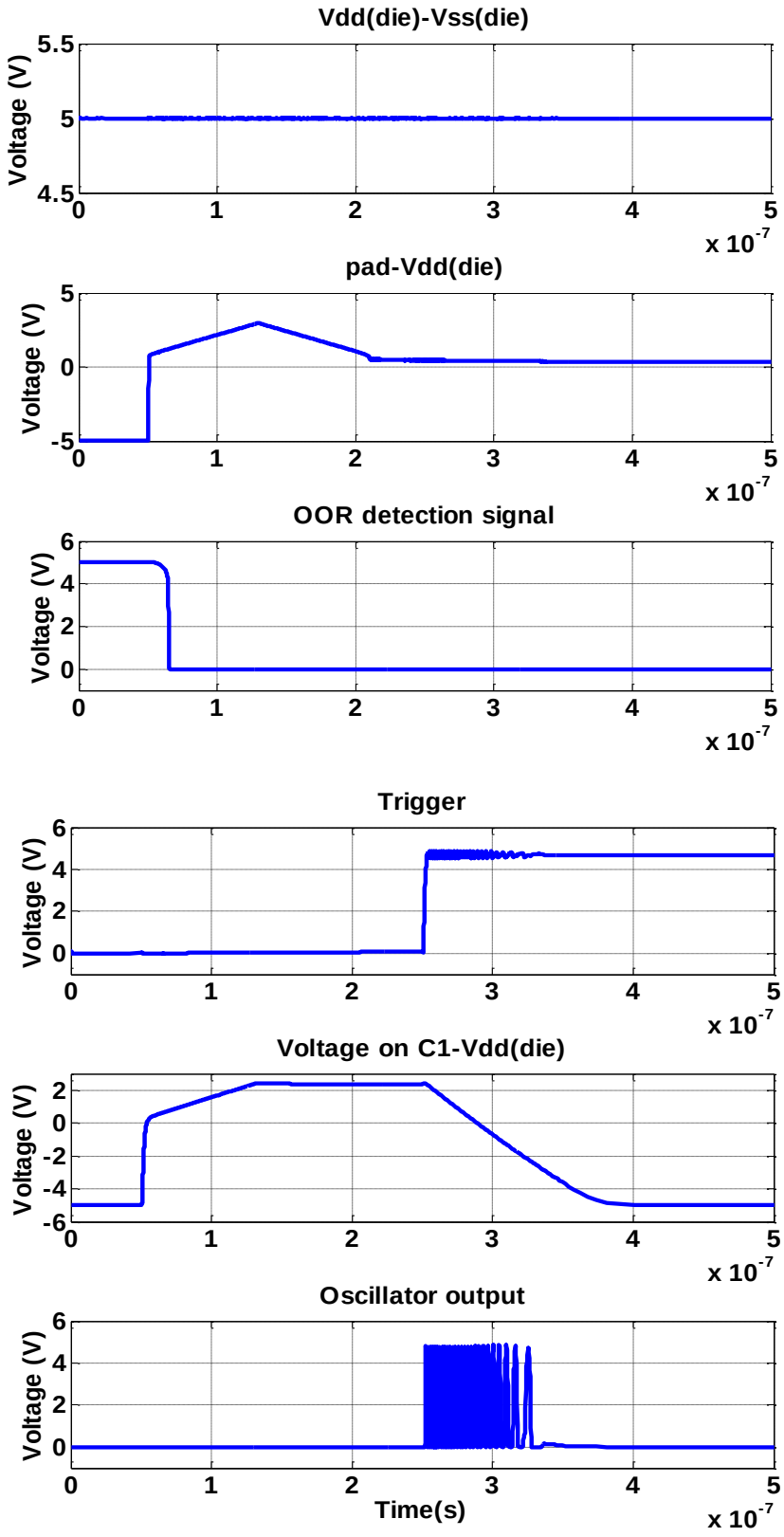


Figure 2-53. Response of RC-based oscillator to slow transient events

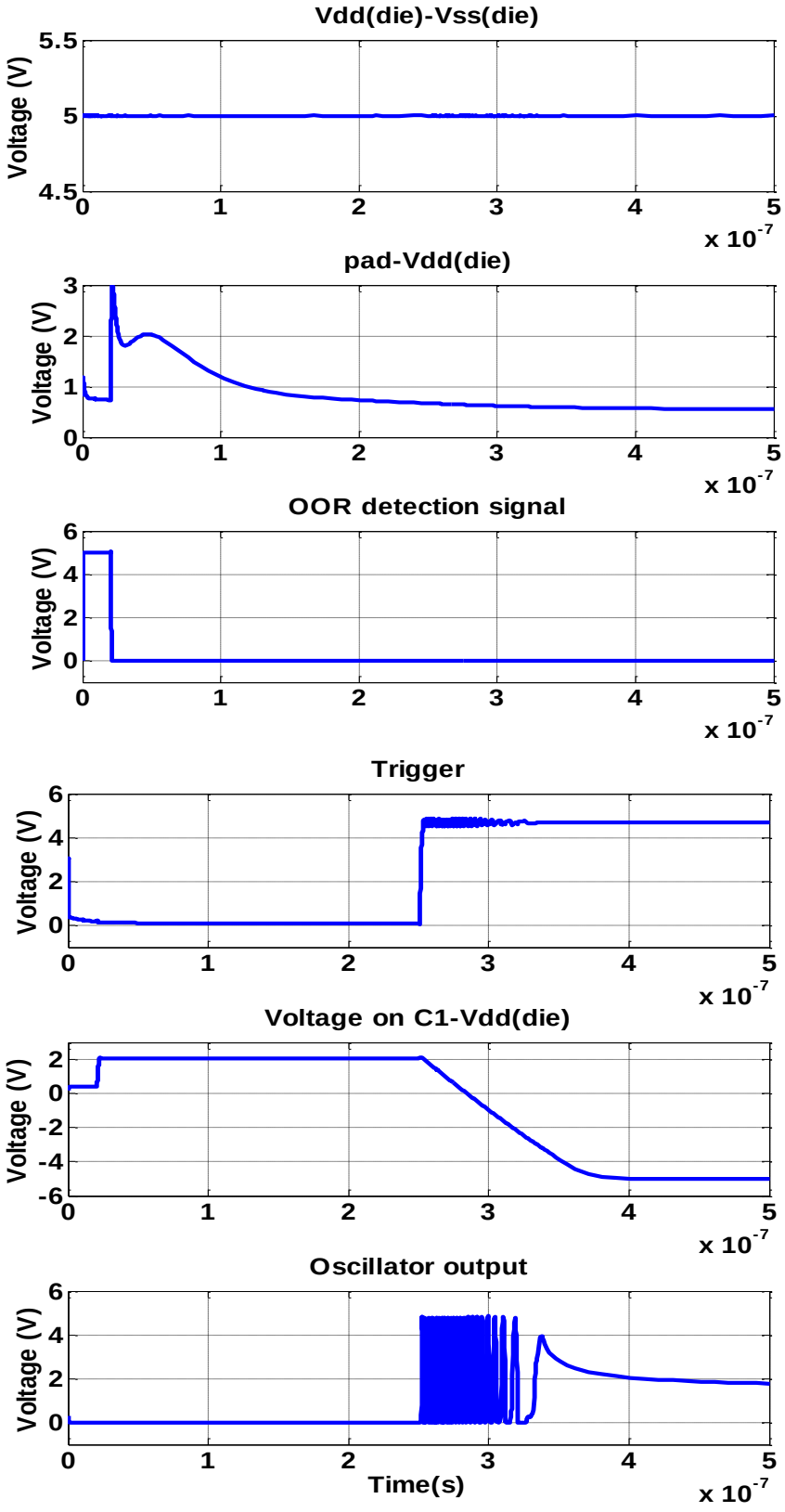


Figure 2-54. Response of RC-based oscillator to ESD event

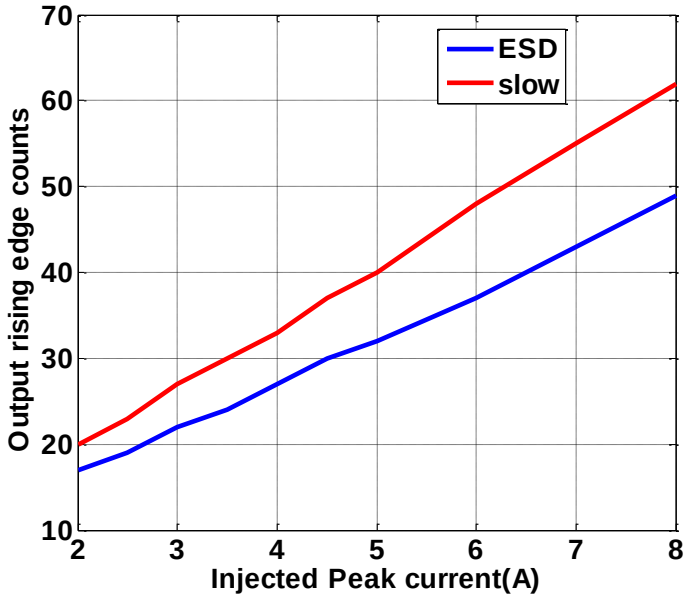
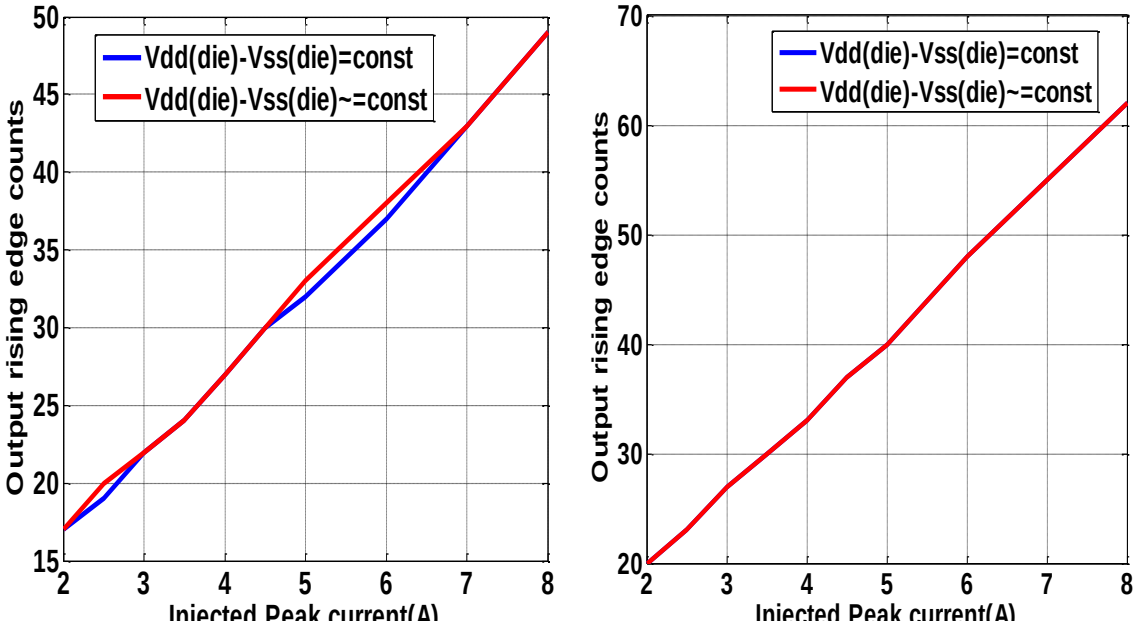


Figure 2-55. Comparison of output counts for RC-based oscillator for slow and ESD events (M2=10u/0.6u)



(a) (b)

Figure 2-56. Comparison of output counts for cases with and without Vdd(die)-Vss(die)=constant for RC-based oscillator (a) slow events (b) ESD events

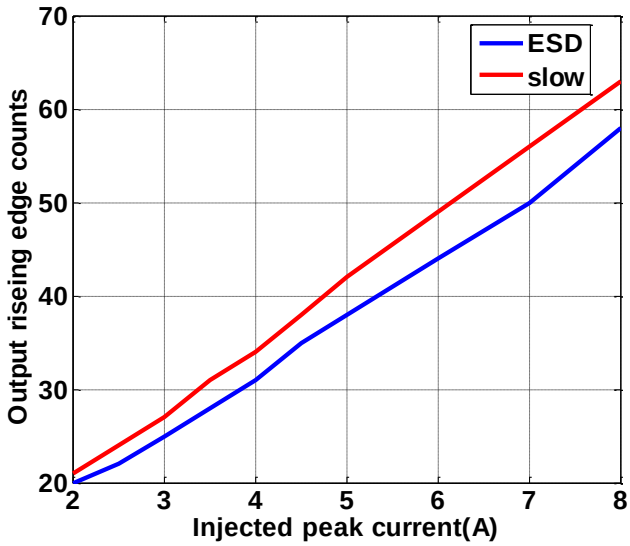


Figure 2-57. Comparison of output counts for RC-based oscillator for slow and ESD evemts when Vdd(die)-Vss(die) =constant (M2=20u/0.6u)

A transient event at any pad in the group would cause a measurement by the oscillator for the group. This would allow measurement of the level of the event seen by one of the pads within the group. Out-range-voltage detectors could be implemented at each I/O pad to determine on which pad (or pads) the event occurred. One problem with a boost bus is that there may be a voltage drop across the bus or the power supply between the location of the pad where the transient event occurred and the location of the oscillator where the event is measured. This voltage drop may reduce the accuracy of the measured level among the pads and make the measured level vary more with the strength and rise/fall time of the event.

The storage capacitance for the RC-based oscillator could potentially be implemented from the boost-bus wiring itself, as a wire running around an IC will not have an insubstantial capacitance. The problem, however, is that this capacitance may be referenced to Vss in some locations and to Vdd in other locations. The inability to control

the reference of this capacitance may cause additional noise in the measurement. More than likely, this parasitic capacitance must be supplemented with added FET-based capacitance with a known reference to maximize accuracy of results.

3 CENTRALIZED A/D BASED DETECTION METHODS

Measurement of the level of an event at each pad requires substantial area and may be subject to errors from process variation. Using a single level detector for several pads can potentially reduce area, but must consume minimal static current and must be able to handle a large voltage drop across the IC during a transient event.

This section discusses methods which send a current proportional to the level of the event around the IC where the level is measured by a single A/D converter. Currents are transmitted rather than voltage because they are less likely to be corrupted than voltages, particularly as a result of large voltage drops across the IC during a transient event. The first detector investigated, as described in Section 3.1, attempts to instantaneously convert the level of the event as it occurs. This sort of approach does not require storage of the event level on a capacitor, whose charge can be altered by minority carrier injection to the substrate during the event [5], but is highly susceptible to voltage drops across the IC. To get around the power supply noise issues, the second approach uses a diode and capacitor to store the peak level of the event on the capacitor until after the disturbance has passed. One passed, the level of the event can be read by an A/D converter. This sample and hold method is described in Section 3.2.

3.1 INSTANTANEOUS DETECTION

To avoid problems with voltage drops on buses around the I/O pad ring, as information related to the magnitude of the transient event is communicated from one end of IC to the A/D converter on the other side, information is communicated in the form of

a current. In this section a scheme where current related to the magnitude of event is sent instantaneously to a designated spot on the IC for level measurement is discussed. Since transient events have relatively fast peaks, this method requires separate circuits to rapidly digitize each level of the event.

3.1.1 Concept. A current proportional to the I/O pad voltage and hence to the level of the transient event is generated at each I/O pad by place the gate and source of a FET across the ESD protection diode as introduced in Section 1 and shown in Fig. 3-1. The drain current of M1 will be directly proportional to V_{gs} when the FET is in linear mode, hence resulting in a close to linear relationship between the drain current and injected transient event. The voltage across the ESD diode depends on the injected current and the design of the diode. If the voltage drop is linear with current (as it roughly is for high injection levels), the drain current would be roughly proportional to the current injected to the I/O pad. The final measurement of the level of the transient event will be based on the drain current of M1, thus making final measurement have roughly linear relationship with injected current. Here, results are conveniently about linearly related to injected current, even if that was not the case a look-up table can be formed for the end result with respect to injected current and this table can be used to estimate the level of the transient event.

The drain current from drain of such M1s connected to each I/O pad of the IC can be used to measure the level of transient event affecting the I/O pads. A common rail has to be created to carry the current from each I/O pad to the A/D converter. Since a current, rather than a voltage, is being sent, voltage drops across bus resistances or noise becomes a smaller issue.

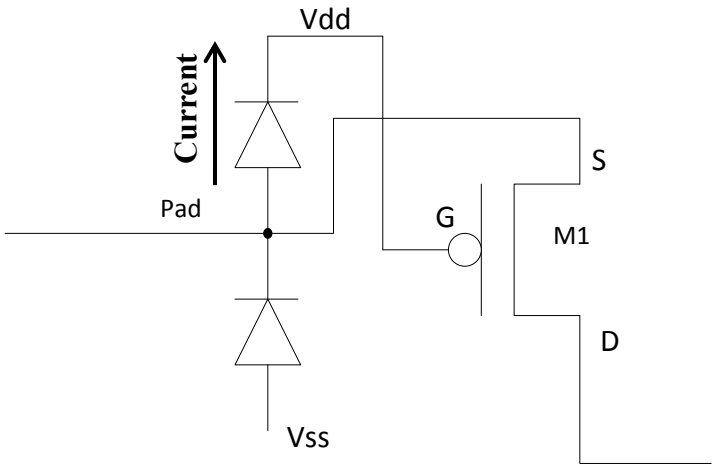
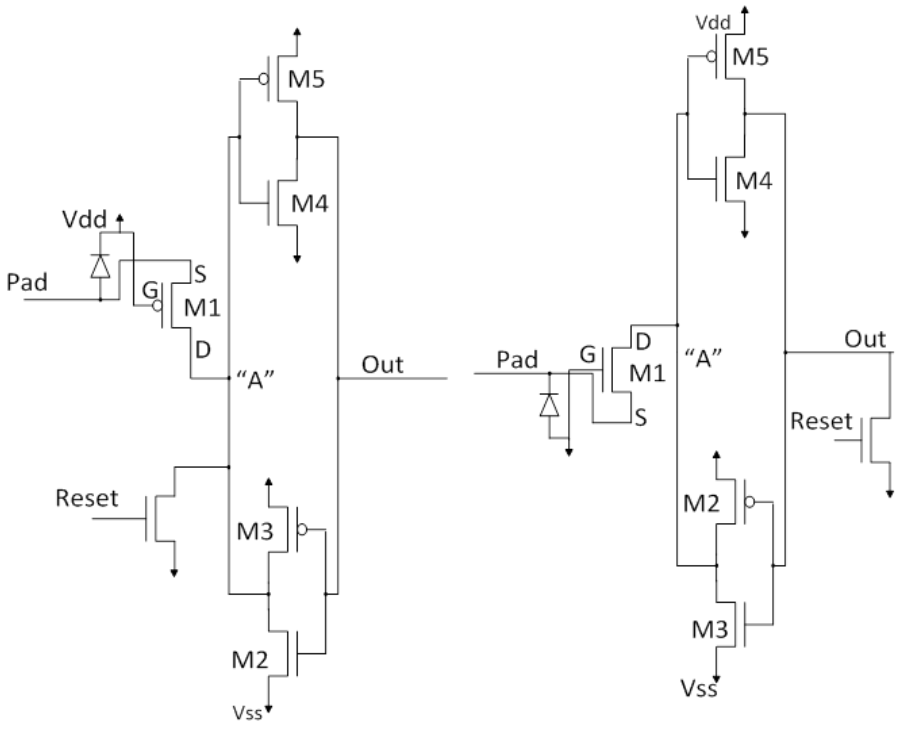


Figure 3-1. ESD protection diodes on I/O pad and PFET connected across positive event diode

3.1.2 Detection Scheme. The detection scheme has two circuits: one for detecting which I/O pad(s) was affected by the transient event and one for measuring the level of the transient event.

Out-of-range voltage detectors are used to detect the event, one for each polarity of transient events, as discussed in Section 2.1 and shown again in Fig. 3-2. The thresholds of such detectors should be low enough to detect the smallest of transient events which might be of interest. The level of the event can be detected at a central location using one of the A/D converter schemes discussed in the previous section, though a more robust measurement technique has been built, as discussed below.

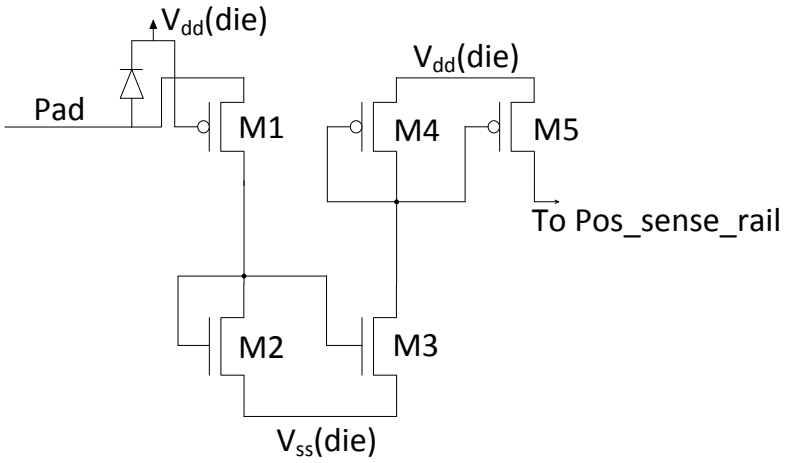
The circuits in Fig. 3-3 are used to direct the current measured by FET M1 to a common rail. The rail is named pos_sense_rail for positive events and neg_sense_rail for negative events.



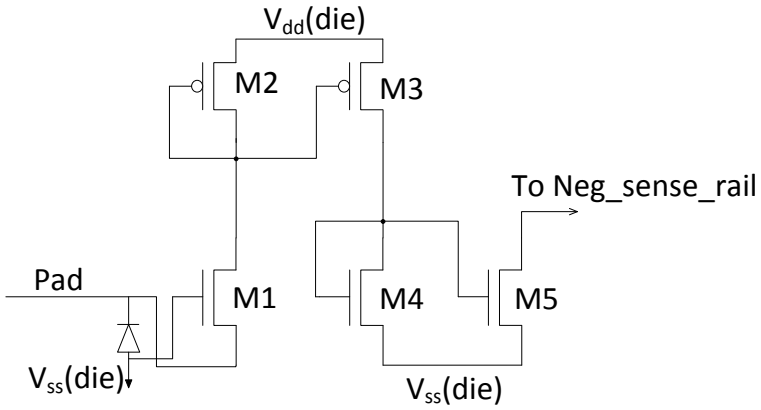
(a) (b)

Figure 3-2. Event indicators based on out-of-range voltage detector (a) Positive event indicator (b) Negative event indicator

The current is transmitted across the IC via the sense rail to a central location. Circuits for reading the level of the transient event are shown in Fig. 3-4. The circuits in Fig. 3-4(a) and (b) are simple current mirrors that mirror the event to the level detectors. The circuit in Fig. 3-4(c) is the level detector, and can be set to trigger the latch at different levels of current, similar to the detectors described in Section 2.1. Multiple instances of the circuits in Fig. 3-4(c) can be placed to measure different levels of current from the sense rail. The output of these circuits goes high when current coming from sense rails is higher than a reference current set on these circuits.



(a)



(b)

Figure 3-3. Sensors for level measurement at each I/O pad (a) Sensor for positive events (b) Sensor for negative events

These circuits for determining the level of the transient events use the core supply. The reason for such an implementation is two-fold: 1) the core voltage is generally cleaner than the I/O supply, particularly during an ESD event; and 2) multiple instances of the level sensing element may take up more area than is reasonable in the I/O pad ring. Routing of reference currents around the I/O pad ring is also avoided.

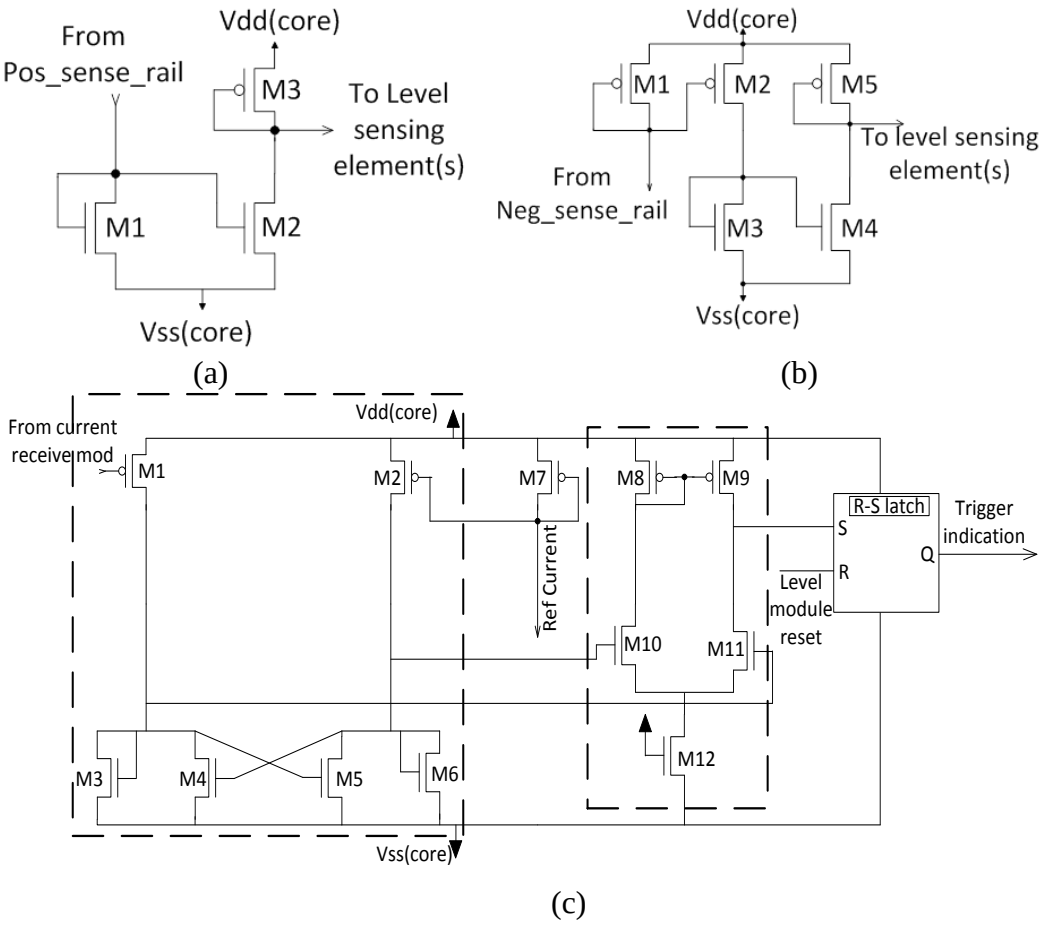


Figure 3-4. Parts of level detection module (a) Positive current receive modeule (b) Negative current receive module (c) Level sensing element

Notice the difference between positive current receive module and negative current receive module in Fig. 3-4(a) and Fig. 3-4(b). In Fig. 3-4(b), the extra mirror stages are used to step down the current coming from neg_sense_rail. In Fig. 3-4(a) M1-M2 current mirror stage is required to feed the sensing element, and also allow room to step down current coming from pos_sense_rail. Because of these mirror stages, the same sense circuit can be used for both positive and negative events.

The level sensing module is based around a decision circuit adopted from [13]. Current in two branches formed by M1 and M2 in Fig. 3-4(c) are compared and control

the differential output of the decision circuit. The differential output is given to a differential amplifier with high gain and hence quick response of the level sensing element. Finally, the output of the differential amplifier is given to an RS latch to save when the output goes high.

The drain of M1 in Fig. 3-4(c) supplies current proportional to the sense rail current (positive or negative depending upon which receiving module precedes level sensing element). The drain of M2 supplies current proportional to a constant reference current. As soon as current from M1 goes higher than the reference current from M2, the differential amplifier output goes high until the M1 drain current is higher than the M2 drain current. The RS latch is set high when the differential amplifier goes high, thus a "1" on RS latch output shows the current on the sense rail went higher than a set reference. Multiple decision circuits can be used to compare the level of the event to multiple thresholds. Depending on which outputs are set, the level of the transient event can be approximated. The plan is to have a minimum of three level sensing elements each for both positive and negative polarity of the transient events. Thus the transient events can be classified as small, medium, or large.

One drawback with this method is that it consumes DC current in in current mirrors associated with reference currents. This drawback may limit the application of the detection scheme to a testing environment if these circuits cannot be kept "always on". It is possible to turn off the reference current when not in use, limiting the DC power draw.

3.1.3 Need of Repeaters in I/O Pad Ring. Figure 3-5 shows the IC-level distribution of the detection scheme for the positive level sensors. Suppose the I/O pad at

the far end of the IC from the level sensing module is zapped with a positive ESD event. The local PDN voltage would rise above the voltage at the level sensing module.

Referring to Fig. 3-3(a), M5 transfers current from Vdd at pad 12 to Vss at the level sensing module. The difference between Vdd at pad 12 and Vss at the level sensing module becomes larger with the magnitude of event. This difference in PDN voltages across the IC during the ESD event can cause a large Vds voltage across M5 in Fig. 3-3(a). These large voltages can cause snapback of the device. Even if the devices are protected using current limiting resistors, the current on the pos_sense_rail is no longer proportional to the ESD event level when the FET is in snapback. This snapback makes the detection scheme fail for large events. To prevent snapback the level sensing module was changed as shown in Fig. 3-6 to use repeaters across the IC as shown in Fig. 3-7.

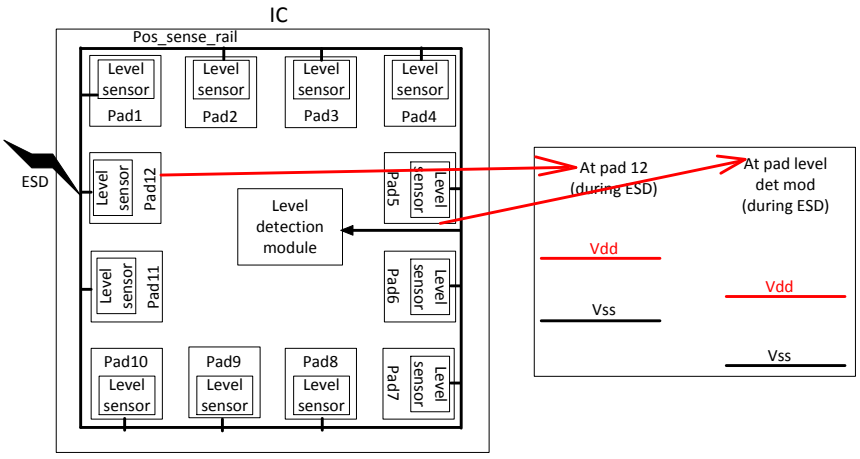
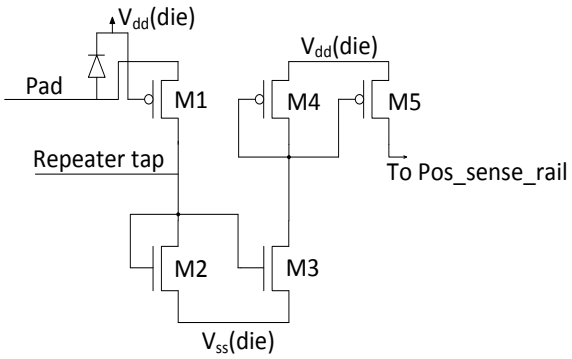
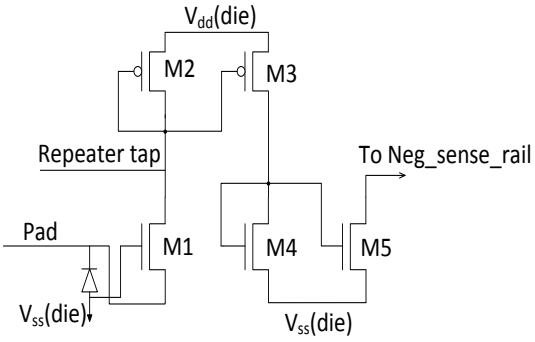


Figure 3-5. Scenario of positive ESD event and behavior of local PDN at different points on IC



(a)



(b)

Figure 3-6. Modified level sensors (a) Modified positive level sensor (b) Modified negative level sensor

The detection scheme uses 2 types of level sensors, either with or without repeater taps. The level sensor without tap is shown in Fig. 3-3 and with repeater taps are shown in Fig. 3-6. As shown in Fig. 3-7 the pos_sense_rail and neg_sense_rail are broken intermittently to feed rail currents into the repeater taps in level sensor modules in the I/O pad. The current in the repeater taps is then mirrored twice in the level sensor circuit, for example in Fig. 3-6(a) the current from repeater tap is mirrored through M2-M3 and M4-M5 mirrors to be relayed on to next section of pos_sense_rail. The mirror ratios are kept 1:1 to preserve the current being fed into the repeater tap. Breaking the sense rails allows the current to be delivered a shorter distance across the IC, ensuring smaller Vds voltages

on devices like M5 in Fig. 3-6(a) compared to the previous strategy where current is delivered across the IC. FETs M2-M3 and M4-M5 in the level sensors of Fig. 3-3 and the level sensors in Fig. 3-6 have a ratio of 1:1 to ensure the current is mirrored without change to the level sensor.

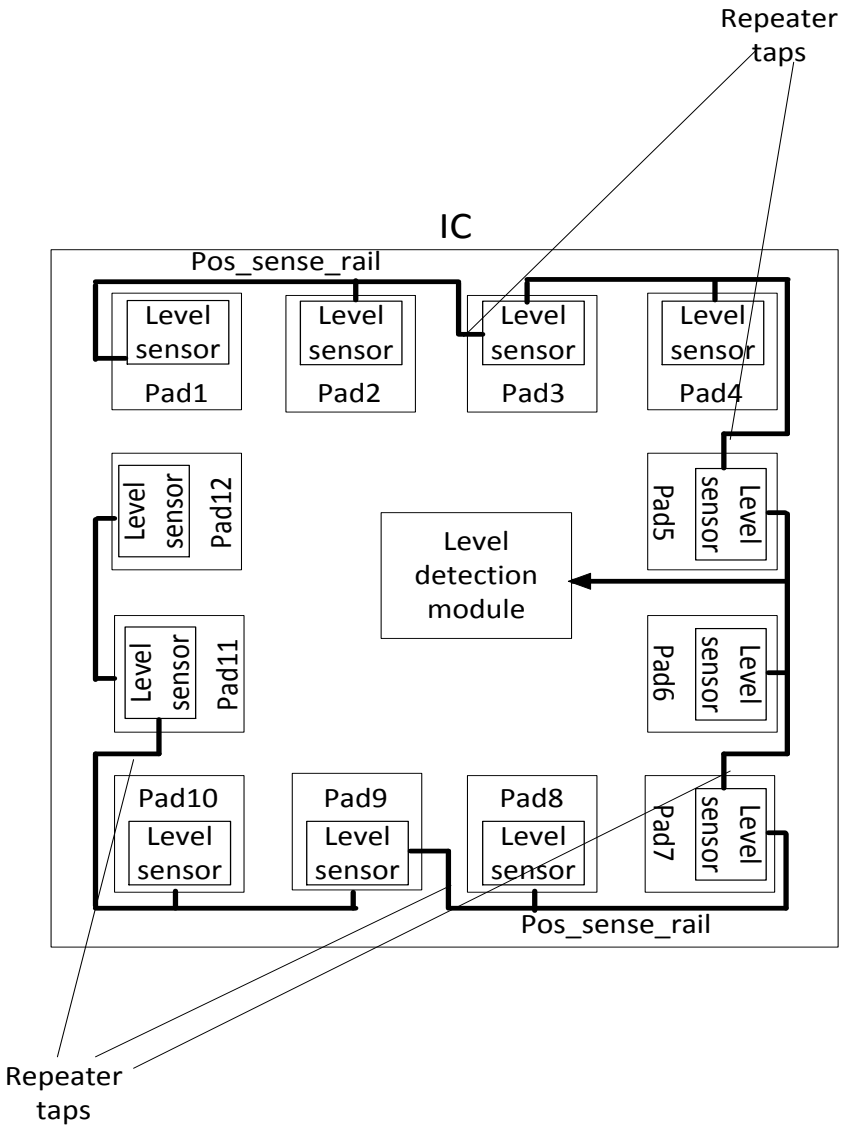


Figure 3-7. Detection scheme with repeater strategy

3.1.4 Simulation Models. A high-level view of the simulation model is shown in Fig. 3-8. The simulation model contains of a pad-ring of 80 pads. The pad ring contains one Vdd pad which is connected to the PCB through pin parasitics. The PCB model contains a decoupling capacitor, an I/O supply with parasitics, and a load on the supply. All the other pads are I/O pads. Only one pad is zapped (i.e. the I/O pad on which the ESD event occurs).

The zapped pad is connected to the outside world through pin parasitics to an ESD gun model used to inject current onto the I/O pad. ESD trigger circuits and power-on-reset (POR) circuits are placed at regular intervals across the pad-ring. ESD trigger circuits are used to trigger the power clamps in event of an I/O pad being affected by transient event, leading the distributed power clamps in I/O pads to route the injected current to V_{ss}. Power on reset (POR) circuit is used to keep IC in a pre-determined (reset) state while the IC is being powered up. This is done to have various important circuits in the IC, in this case the ESD protection circuit, to be booted up in a finite known state to guarantee expected working.

Each I/O pad contains ESD protection diodes, distributed power clamps and bus resistances, as shown in Fig. 3-9. The ESD protection circuits were designed for the target IC which will house the transient detection scheme. Hence, these ESD protection circuits are not discussed in detail in this report, though they follow the approach outlined in [14]. The zapped and some other I/O pads will contain the detection circuits. The relative location of the power and return pads, the zapped pad, and the level detection module was varied to comprehensively test the impact of the voltage drop across the IC during the ESD event.

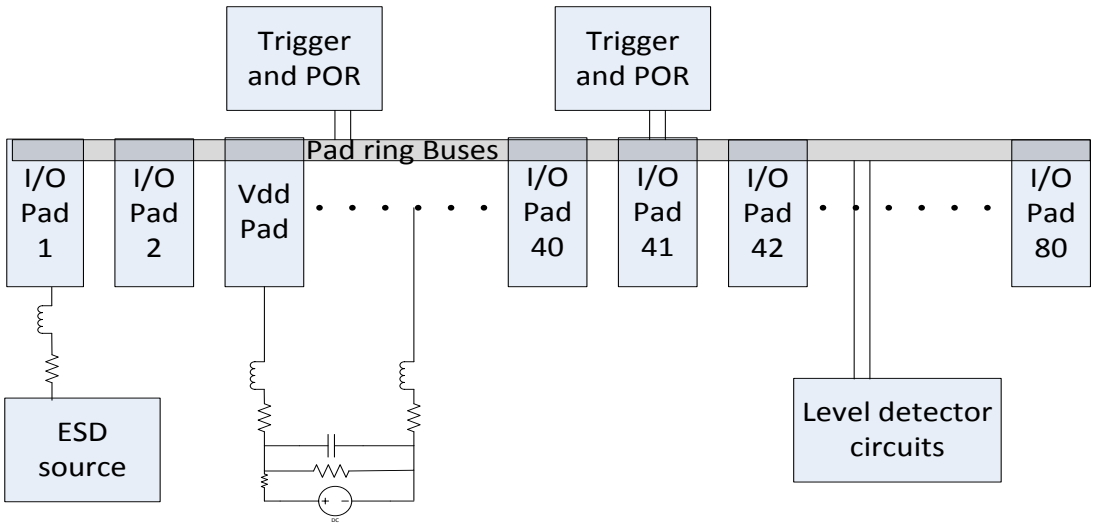


Figure 3-8. Full simulation model

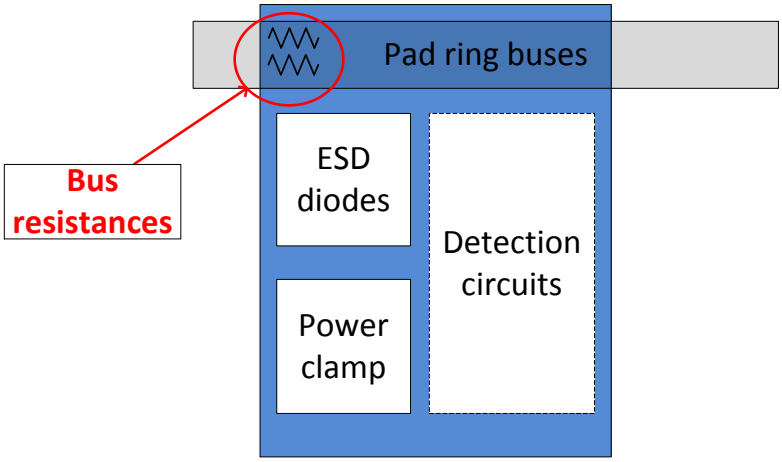


Figure 3-9. I/O pad contents in the simulation model

3.1.5 Simulation Results and Drawbacks. The detection circuits described in Section 3.1.3 were verified using the simulation models described in Section 3.1.4. The

first objective was to verify the proper operation of the event indicators. The event indicators should be triggered at very low injections.

Hence, positive and negative ESD events of 500 V or 1.5 A were injected into the I/O pad during the first tests. Figure 3-10 shows that the event indicators were triggered, as desired, for these relatively small events when the zapped pad was next to the Vdd pad as shown in Fig. 3-11.

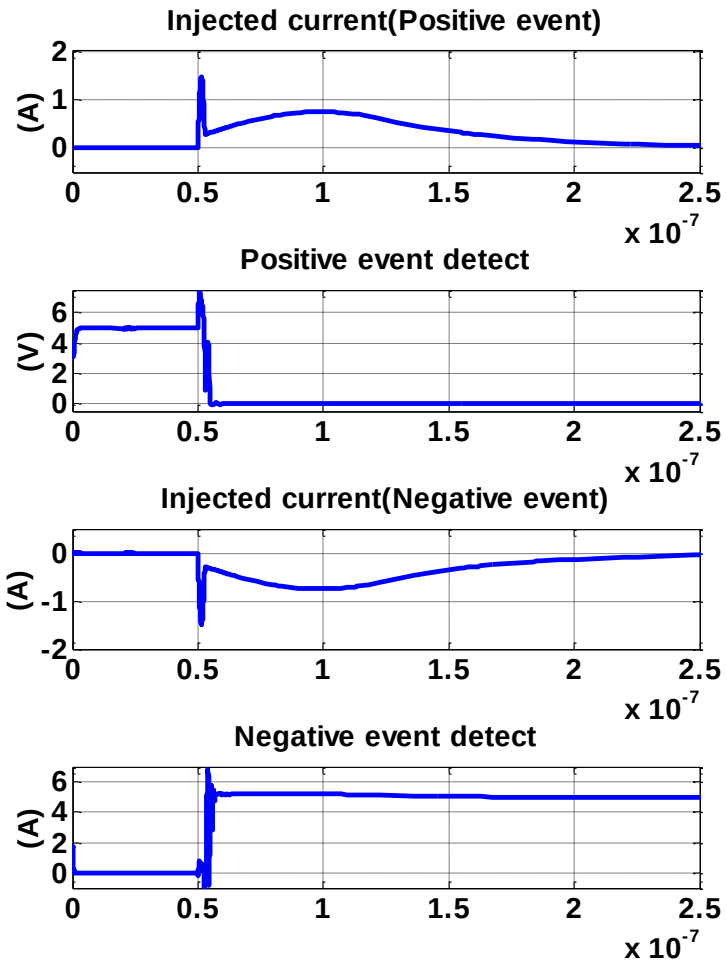


Figure 3-10. Detection signals for positive and negative 500 V ESD events

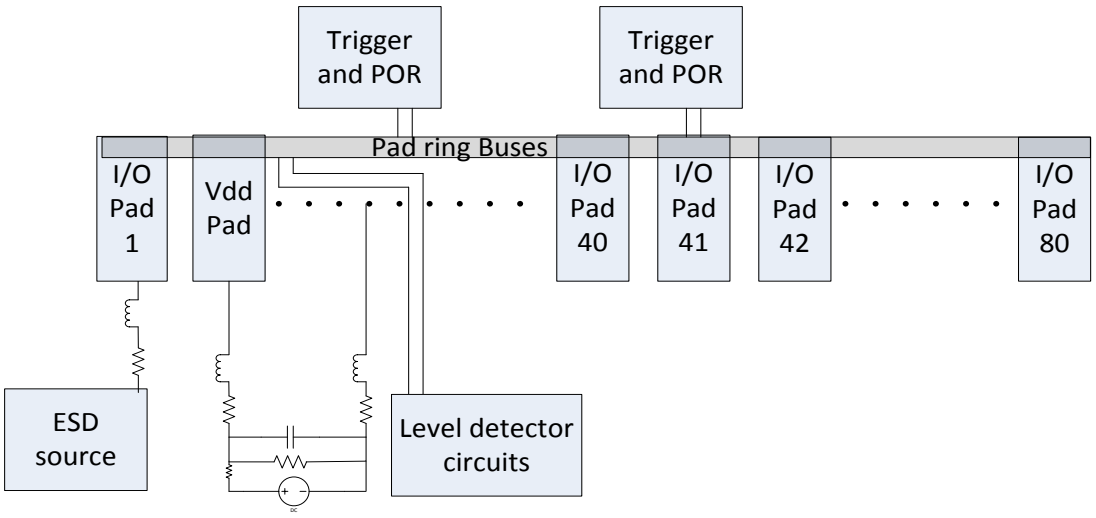


Figure 3-11. Initial tests of level sensors placed zapped pad, level detector, and Vdd pad next to one another

Figure 3-13 shows the plot of injected current for a 4 kV event and currents produced at drain of M1 and M5 of the level sensor (a positive level sensor circuit is shown in Fig. 3-12 for reference). The current produced at the drain of M5 is fed to pos_sense_rail. The current on M5 drain is different from that on M1 because of PDN noise – in particular at the peak of the event. This difference must be factored into the error margins.

At the level detector, current from pos_sense_rail is given to the level sensing element after stepping down the current. This stepped down current related to the ESD event is then compared to a reference current in the level sensing element. In the example in Fig. 3-14, the reference current shown in red is set to the equivalent injected current of approximately a 4 kV event. Although the current at the decision circuit for the 4 kV event was above the reference current, the level sensor did not trigger because of the setup time of the level sensing element. The current inside the decision circuit must stay

higher than the reference current for a couple of nanoseconds for the event to be registered. For example, as is shown in Fig. 3-15. In this case, a 4.5 kV event was properly detected. This limitation must also be accounted for when using this level detecting scheme. None-the-less, these initial tests demonstrate the feasibility of the approach.

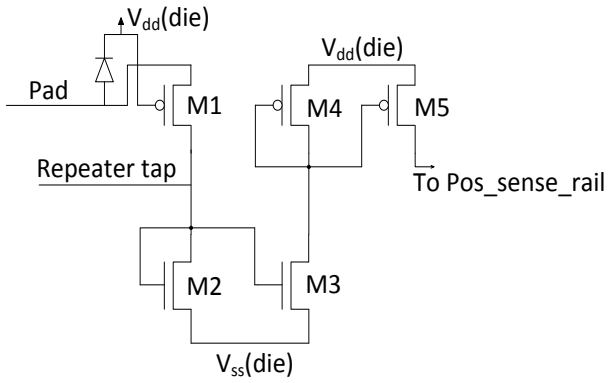


Figure 3-12. Positive event level sensor schematic

A more challenging case was considered next, where the zapped I/O pad was 40 pads away from the level sensing module and the V_{dd} pad, as suggested in Fig. 3-16. No changes were made to the event indicator circuits, except that repeaters were added around the I/O pad ring to carry current on the pos_sense_rail. For tests discussed here, repeaters were put at every 4^{th} I/O pad. For example, if pad 1 was zapped pad then the current would be repeated at the 5^{th}, 9^{th}, 13^{th} I/O pads and so on. Fig. 3-17 shows the simulated output current from the repeaters during a 4 kV event. The current levels, between 75 ns and 150 ns, drop drastically near the 17^{th} I/O pad and width of the first peak reduces compared to previous pads. This drop occurs because the V_{dd}(die) and

V_{ss}(die) voltages are very low at these I/O pads as shown by Fig. 3-18. At some points the PDN supply voltage drops to as low as 2 volts. The drop in the power supply voltage is caused by the amperes of ESD current flowing through the PDN bus resistance, causing volts of drop.

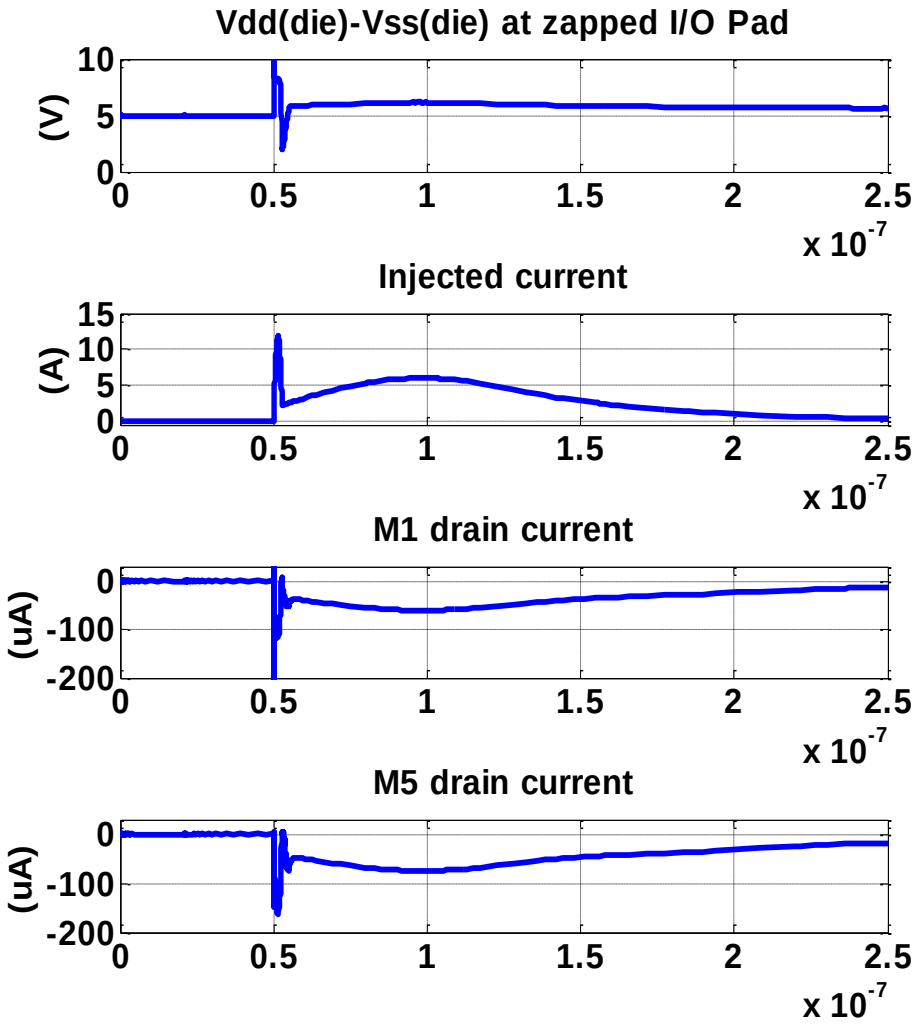


Figure 3-13. Response of level sensor to a 4 kV ESD event

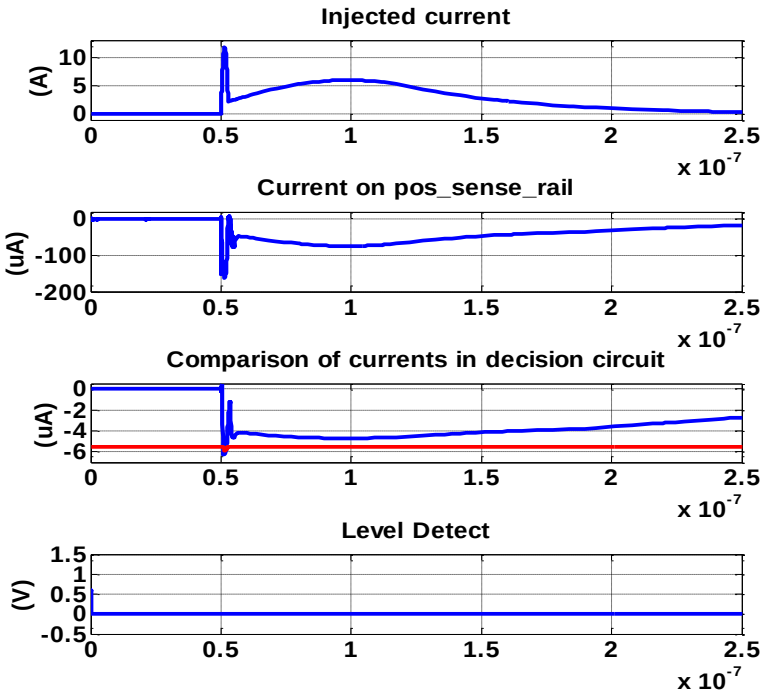


Figure 3-14. Response of level detector module to a 4 kV ESD event

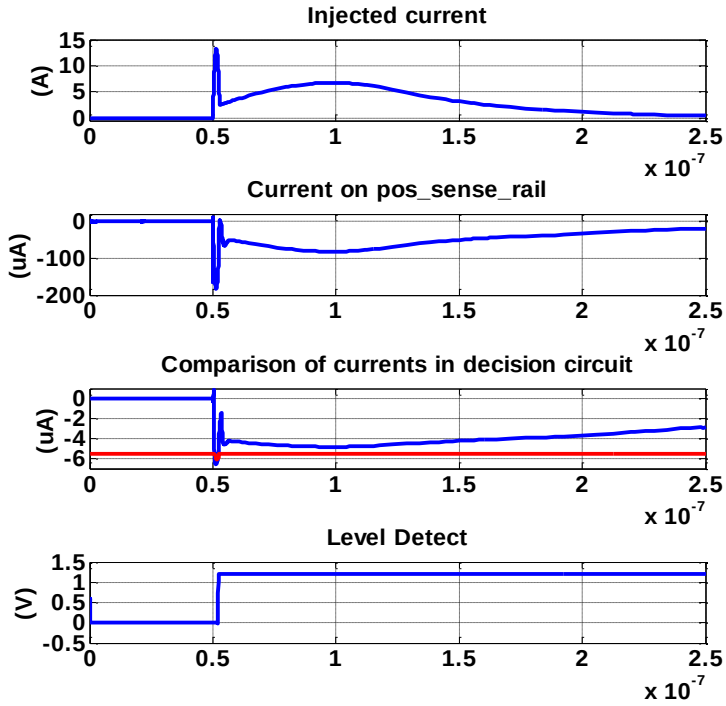


Figure 3-15. Response of level detector module to a 4.5 kV ESD event

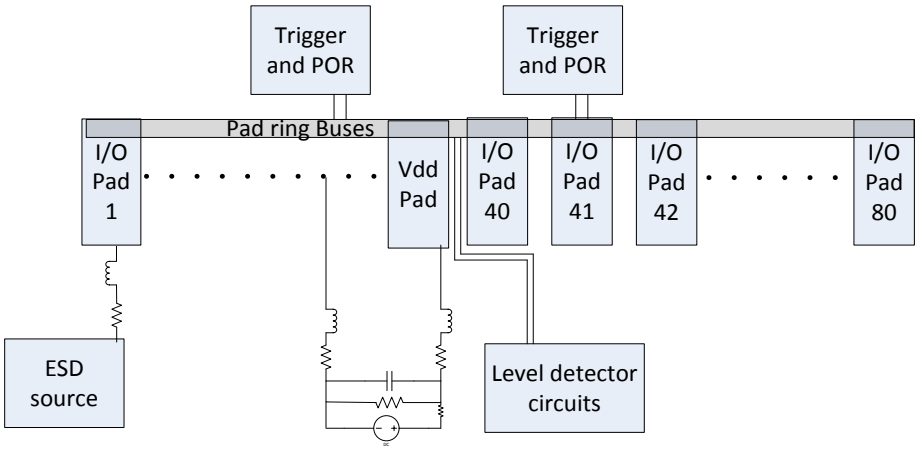


Figure 3-16. Simulation model when the zapped I/O pad was 40 pads away from Vdd and the level detector circuits

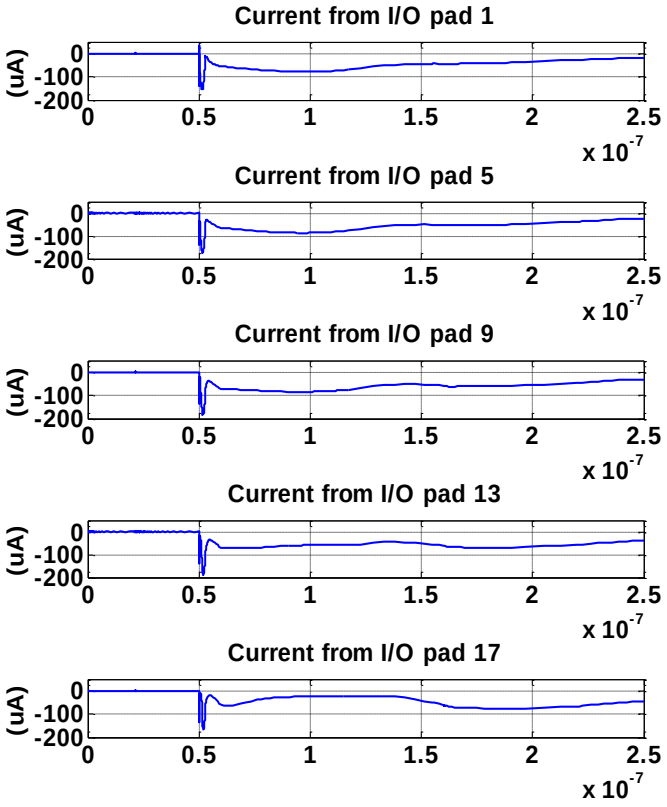


Figure 3-17. Currents at output of repeaters during a 4 kV ESD event

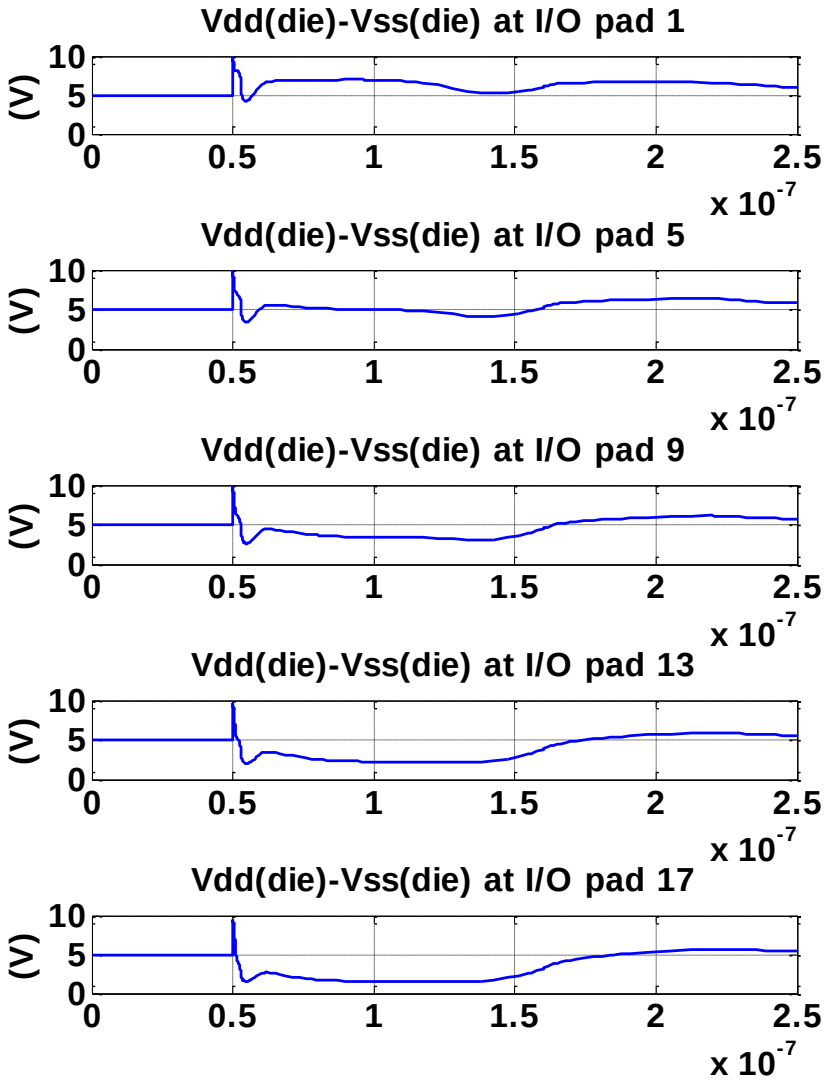


Figure 3-18. Vdd(die)- Vss(die) at the repeater locations during an ESD event

The amount of PDN voltage drop can be controlled by adding more V_{dd} and V_{ss} pads and by adding more level detector modules, so that the level detector module is never "too far" away from zapped pad. Both solutions, of course, have their drawbacks. Some variation in the behavior of the PDN voltage is also expected, as the behavior depends on the design of the ESD protection circuits and the bus resistance of the IC

design. These limitations make this design infeasible for large ICs where multiple V_{dd} and V_{ss} pads are not present. Even if IC is allowed to have multiple supply pads, the supplies might not be placed around the IC as needed by the detection scheme.

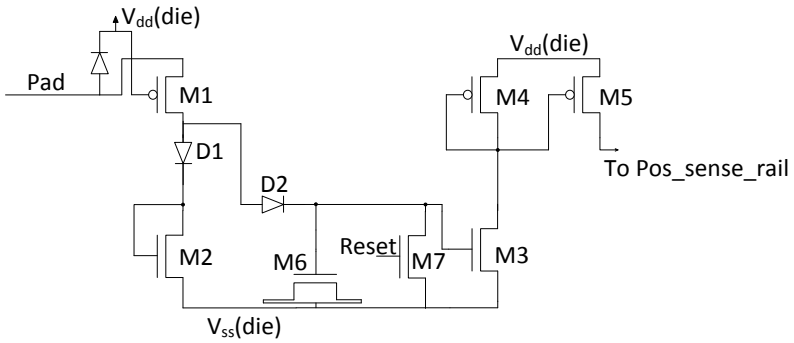
3.2 "SAMPLE AND HOLD" METHOD

Instantaneous detection fails because of the power supply disturbance on the PDN and boost rails during ESD. A workaround for this problem is discussed in this section. The main idea is to save the information related to the peak of the transient event on a capacitor in the I/O pad, and read the value on the capacitor later, after the transient event has passed and power supply noise is minimal. The detectors used to determine at which pin the event occurs remains the same as in Section 3.1

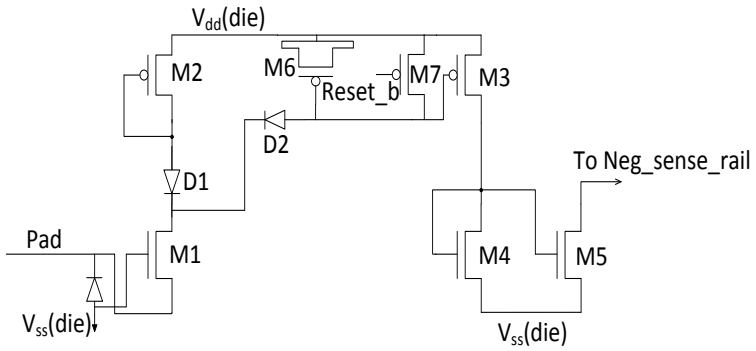
3.2.1 Concept Derivation from Instantaneous Detectors. Figure 3-19 shows the modified level sensors which store the level of the event before transmitting. Information about the peak disturbance is saved as a voltage on a capacitor with help of diodes. The capacitor then drives the gate of a FET to deliver current to pos_sense_rail/neg_sense_rail. This enables reading of the peak disturbance information at later in time when disturbance has settled down on PDN.

The level sensors contain two diodes. Diode D2 is used to allow the capacitor, M6, to charge up to the peak level of the event and stay there. Diode D1 is used to compensate for diode drop across D2 when peak voltage across M2 is saved on capacitor M6, so that M3 will properly mirror the current in M2. The voltage on M6 drives the gate of M3 to give out a constant current dependent on peak disturbance on the I/O pad. Theoretically the capacitor M6 should not discharge very quickly since it is only driving

a gate. FET M7 is inserted to reset the voltage on M6 after the level of the transient event level has been read out. M7 is a long-channel device to minimize charge leakage which may discharge capacitor M6.



(a)



(b)

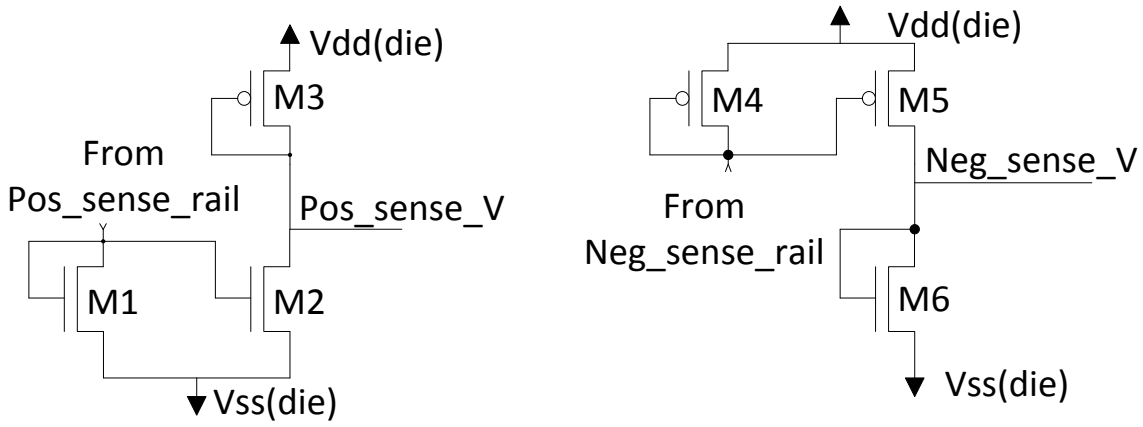
Figure 3-19. Sample and hold level sensors (a) for positive events (b) for negative events

Repeater taps are not required since the level measurement is done after the PDN is back to normal and PDN noise is minimal. Snapback of M5 is still a possibility during the transient event hence current limiting resistors have to be used which will be discussed later in this report.

Since the information about the peak transient disturbance is available for a long time, instantaneous analog-to-digital conversion of the level is not required and an on-chip ADC can be used for level measurement. Using an on-chip ADC can reduce static current consumption of the detection, scheme since no part of the scheme then has to consume DC current continuously, allows greatest re-use of components, and allows use of a much more sophisticated converter design. Since the scheme does not consume DC current, it can be “always on”, even in low power modes. When a transient event is detected, the on-chip ADC can be “woken up” and the level of the transient event can be read.

The on-chip ADC typically has multiple channels multiplexed to its inputs. Two additional channels can be added to read the level of positive or negative events from pos_sense_rail or neg_sense_rail respectively. Since the ADC reads voltages and not currents, the currents on pos_sense_rail and neg_sense_rail are converted to voltages in a separate I->V converter module as shown in Fig. 3-20.

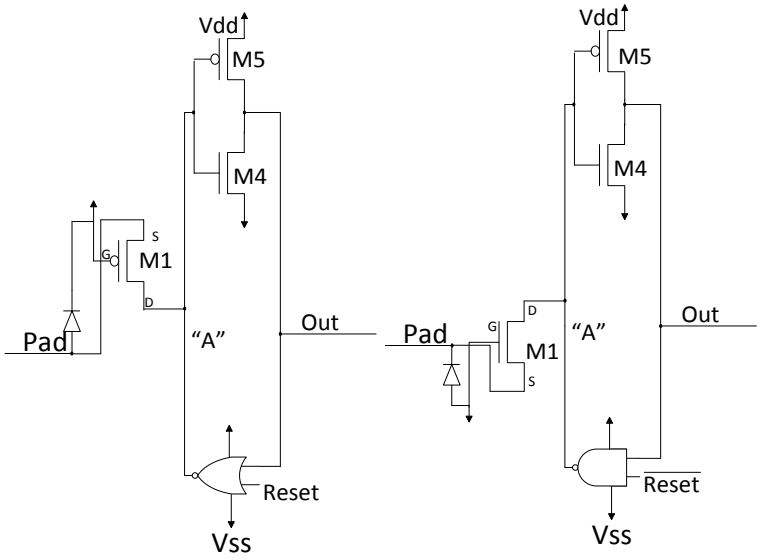
The circuits shown in Fig.3-9 drop the currents coming from Pos_sense_rail (Fig. 3-9a) or neg_sense_rail (Fig. 3-9b) across a PMOS or a NMOS load respectively. The voltage rails pos_sense_v and neg_sense_v are fed to inputs of the ADC. While fewer components could be used by dropping the pos_sense_rail current, for example, across an NFET, dropping the current across a PFET is required for optimal matching with PFET M1 in Fig. 3-19(a) which generated the current. This matching is done to minimize the effect of process variation on the output voltage. The current must similarly be dropped across an NFET for the converter for negative events.



(a)

Figure 3-20. Current to voltage converter circuits (a) I-V for positive events (b) I-V for negative events

The event indicator designs are also changed, as shown in Fig. 3-21, compared to previous design to have a better reset functionality.



(a) (b)

Figure 3-21. Event indicators (a) Positive event indicator (b) Negative event indicator

Reset functionality is added by replacing M2-M3 in previous designs with a NOR and NAND gates in positive and negative event indicators respectively. This is done so that inverter M4-M5 has a minimal effect on the latch when a reset is asserted.

The complete detection scheme is illustrated at a high level in Fig. 3-22 and Fig. 3-23. Figure 3-22 shows the contents of each I/O pad cell. Figure 3-23 shows how currents are passed around the I/O ring, though the sense rails, to an A/D converter at one side of the IC.

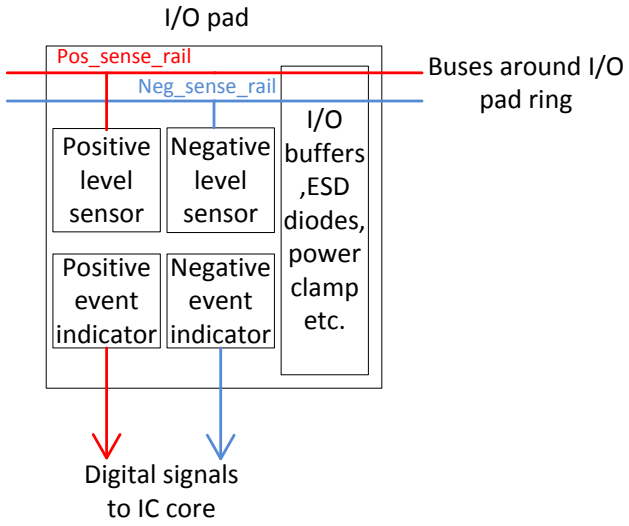


Figure 3-22. Circuit components in I/O pad for sample and hold detection scheme

Each I/O pad contains 4 sensors. Two sensors are event indicators, one for each polarity of the transient event. Two sensors are level sensors which transmit the level of the current back to the A/D converter. Two sensors are required for each polarity of the event. The event indicators produce digital signals i.e. a “1” or “0” which can be directly

given to registers in the core of the IC to save the information and allow access by the microcontroller.

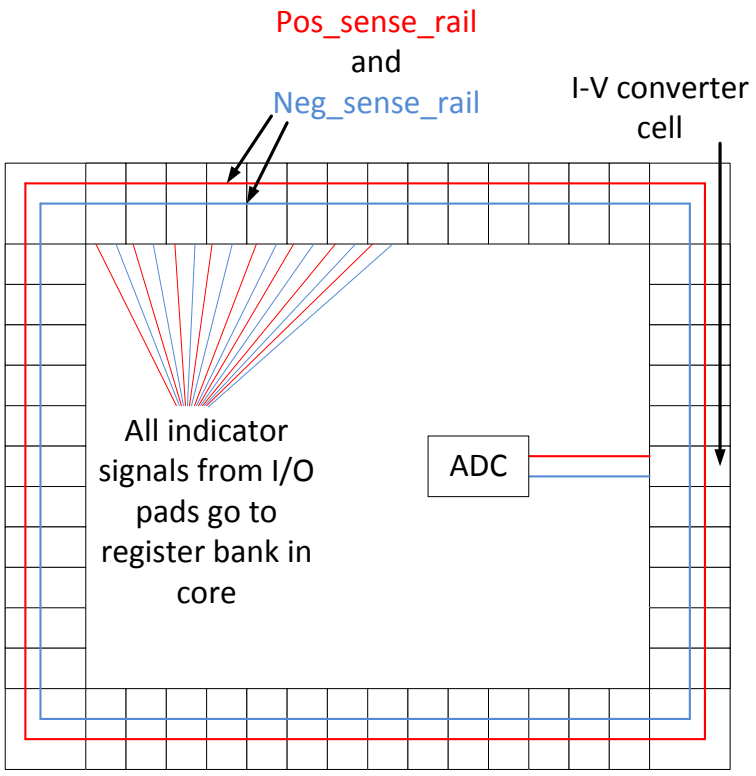


Figure 3-23. I/O pad ring for sample and hold detection scheme

The level sensors give out currents proportional to the peak magnitude of the transient events and are carried by pos_sense_rail and neg_sense_rail around the whole IC. The pos_sense_rail and neg_sense_rail currents are converted to voltages at I->V converter cells (Fig. 3-20) which is located near to the ADC. The voltages at the output of

the I-> V converter cell are given to the ADC to read out the level of the transient events. Figure 3-24 shows a rough flow of events when the IC is disturbed by a transient event.

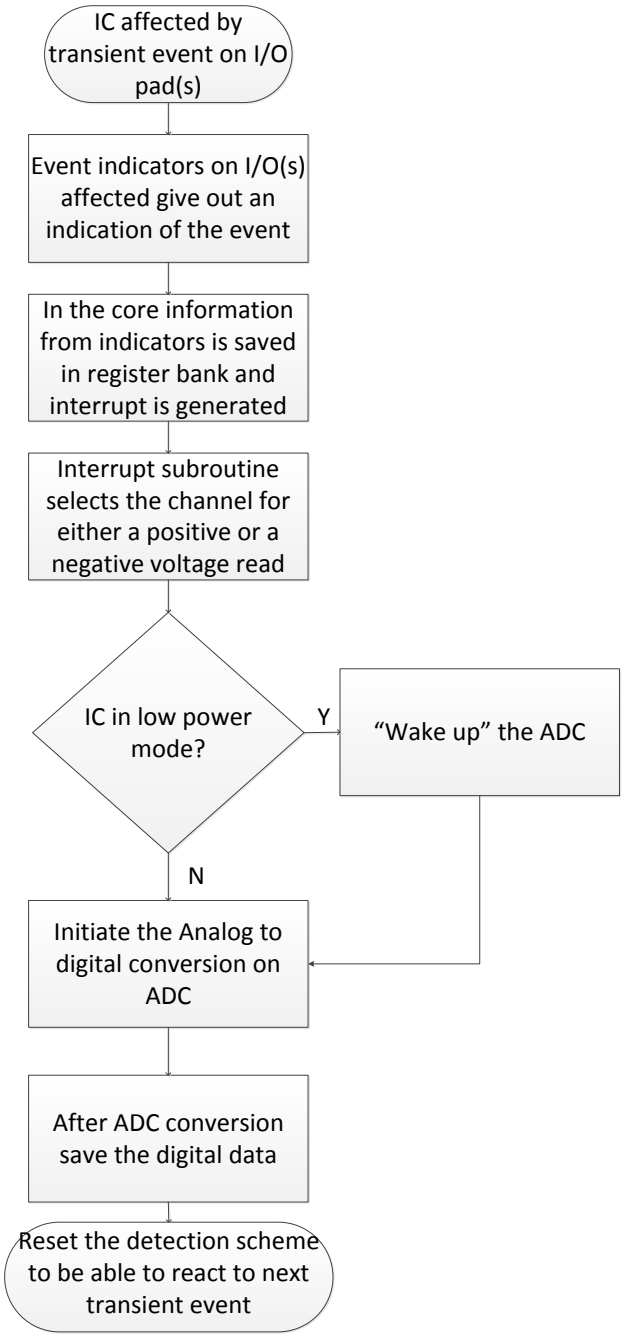


Figure 3-24. Flow of events when IC is affected by a transient event

3.2.2 Simulation Models. The model used for simulating the sample-and-hold method is similar to that used for simulating the instantaneous detection method, as shown in Fig. 3-25. The level detector module is replaced by the current-voltage converter cell. The sense rails are ran all around the IC, without repeaters. The simulations were generally done with the V_{dd} pad and current-voltage converter cell next to the zapped pad, since the PDN noise during the transient event does not affect the measurements in this detection scheme. In the case that it does, the PDN noise is greatest for this configuration.

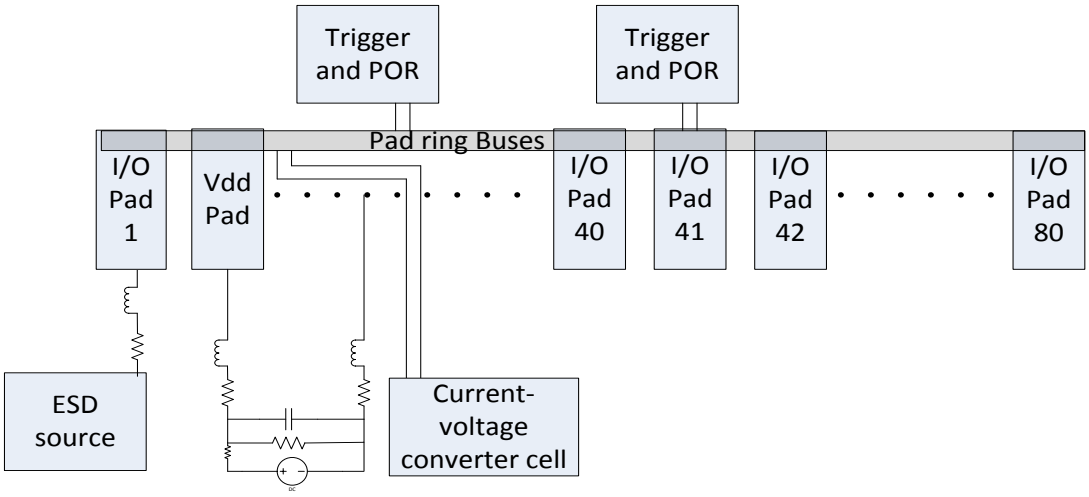


Figure 3-25. Simulation setup for testing sample and hold detection scheme

3.2.3 Simulation Results and Analysis. The event indicators were tested first. Since the design changed from that compared to the event indicators in Section 3.1, the sizes of FETs were decided so that event indicators can trigger on relatively small

transient events, but at the same time have no false triggers. Figure 3-26 shows response of the positive event indicator to an ESD type event with model of the gun charged to 500 V. The event indicators trigger as desired for relatively small events.

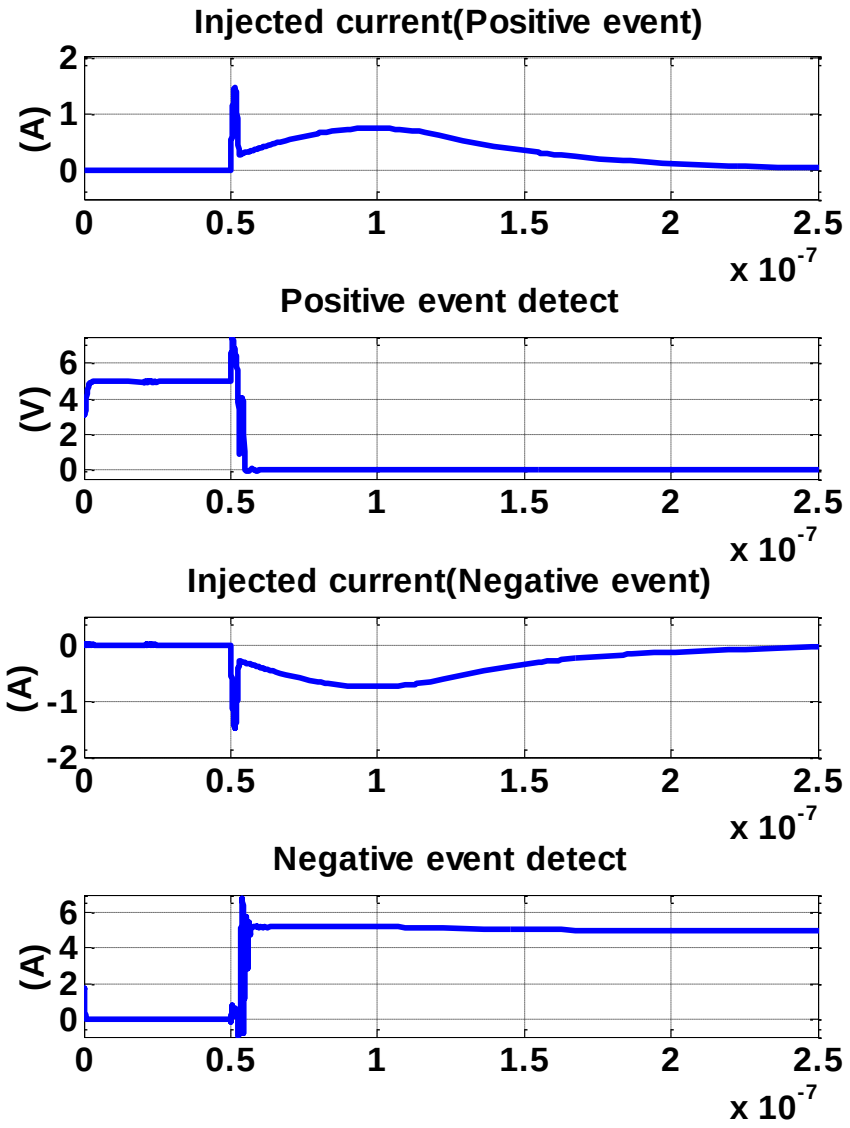


Figure 3-26. Positive and negative events injected on I/O pad and detected by the respective indicators

One concern is how small of an event will trigger the event indicators. There can be overshoots and undershoots on the I/O pad due to high speed signals and false indications should not be generated due to these signals on I/O pads. To test this possibility a slowly ramped current was injected on the I/O pad and the current and voltage values which triggered the event indicators was recorded. Figure 3-27 shows the slowly injected current and the detection of a positive event on I/O pad. In this case, the indicator does not trigger until nearly 1 A of current was injected.

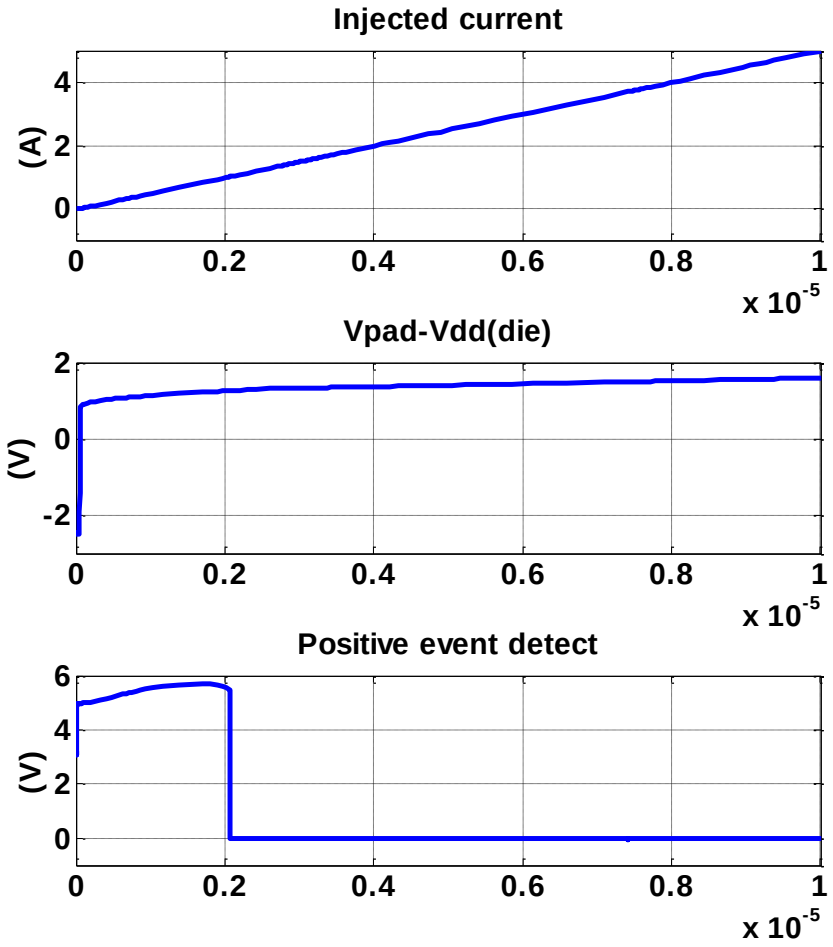


Figure 3-27. Simulation of event indicators with slow events to get quantitative measure of switching threshold

The voltage and currents at which the level detect triggers was recorded while performing Monte Carlo simulations which included process variations. Fig. 3-28 and Fig. 3-29 show histograms of the injected currents and pad voltages, respectively, that caused the event detector to trigger. For 2-sigma variations i.e. about 95% cases, injected current from 0.5 A – 2.5 A (voltages 1.15 – 1.4 V above Vdd) caused the detector to trigger. A modest 500 V ESD event is expected to cause up to 1.5 A of peak current in the standard ESD gun model. The trigger level is sufficiently high that false triggers are unlikely, but sufficiently low to capture even small ESD events. The event detectors triggered below 4 A in all cases, which is roughly equivalent to the peak current in a 1.5 kV ESD gun event.

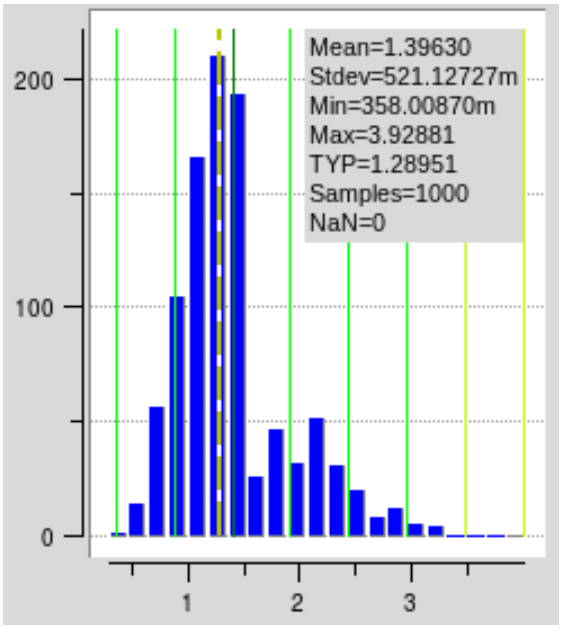


Figure 3-28. Switching threshold of positive event indicator in terms of injected current

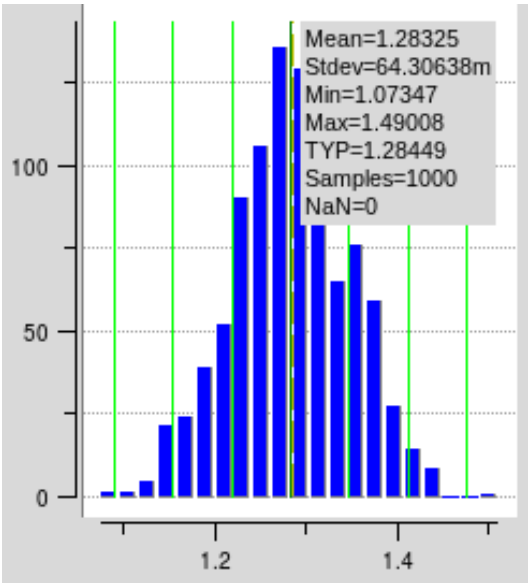


Figure 3-29. Switching threshold of positive event indicator in terms of pad voltage relative to Vdd

Similar Monte Carlo simulations were done using negative events applied to the negative event indicator. The resulting histograms of the trigger current and voltage are shown in Fig. 3-30 and Fig. 3-31, respectively. For 2-sigma cases, the injected current causing the negative event detector to trigger lies between -0.5 A to -1.37 A and the voltage drop on the I/O pad voltage lies between 1.2 V – 1.275 V below Vss(die).

The level sensors were tested next. The positive level sensor is shown again in Fig. 3-32 for reference. Figure 3-33 shows the currents and voltages in the level sensor for a 4 kV ESD event. As discussed before, the goal is for the drain current out of M3 to be fairly constant and proportional to the peak of the event, and for this current to be mirrored through the drain of M5 to pos_sense_rail. The plots show that the capacitor is able to capture voltage corresponding to peak of the event and even after the event has

passed a constant current, proportional to peak of the event, is supplied from drain of M5 to pos_sense_rail.

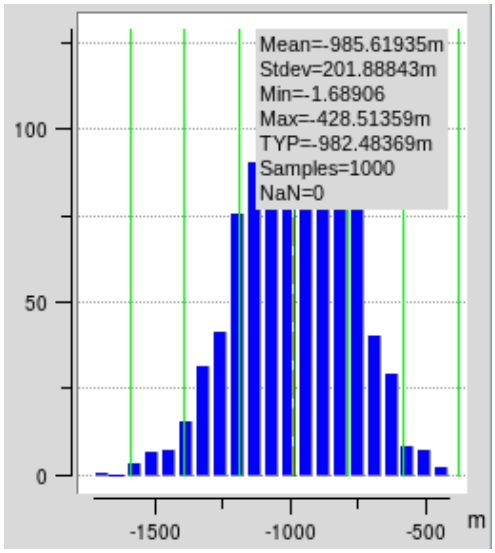


Figure 3-30. Switching threshold of negative event indicator in terms of injected current

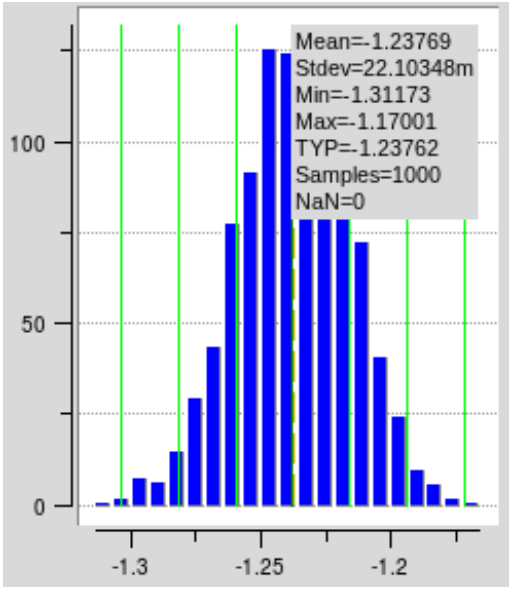


Figure 3-31. Switching threshold of negative event indicator in terms of pad voltage relative to Vdd

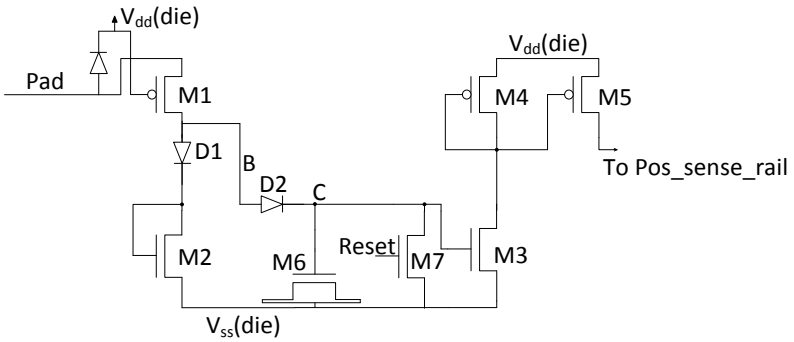


Figure 3-32. Positive event level sensor

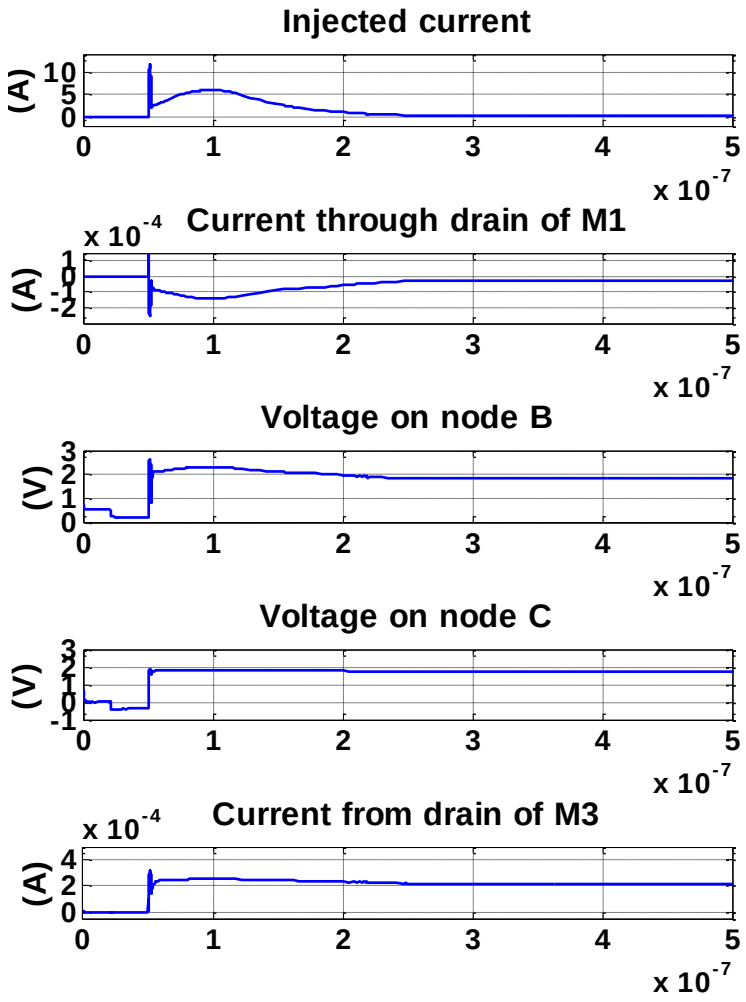


Figure 3-33. Important currents and voltages related to level sensor when the I/O pad is subjected to a 4kV event

The current at the output of M3 does not precisely mirror the peak current through M1, but it is close. The level sensor output currents can be calibrated to the simulation results from the ESD events but it is critical first to ensure that the output levels are independent of the type of the event. That is, irrespective of the rise time and duration of the event, the current coming of the level sensors should have the same proportionality to the peak current injected into the I/O pad. Simulations with trapezoidal pulses were performed to test this independence as shown in Fig. 3-34 for a 12 A pulse. The rise time and duration if the trapezoidal pulse was varied from 2 ns – 10 ns and the output current was recorded 50 us after the event passed. The peak output currents 50 ns after injection of 12 A pulses with different rise times and pulse widths are shown in Fig. 3-35. A 13% variation in the output current was observed when rise time was varied from 2 ns -10 ns and pulse width was varied from 2 ns-100 ns

If process variation is considered along with the trapezoidal pulse variation then the total variation of the output current is about 50%. This variation, although large, is not a problem in the overall circuit, since the process variation is compensated at the current-voltage converter, shown in Fig. 3-36. As discussed earlier, most of the variation in the output current results from the FET that generates the initial current at the diode (e.g. M1 in Fig. 3-19) rather than from other FETs which are matched within current mirrors. The variation in this FET is roughly matched by variations in the load FET at the current-to-voltage converter (e.g. M3 in Fig. 3-36).

Simulations of the level detector and voltage converter, combined, were performed first without process variations. A simulation of the current to voltage converter alone is shown in Fig. 3-37. The output of the level detector and voltage

converter as a result of trapezoidal pulses with different rise and fall times and different width (2 ns – 100 ns) applied to the I/O pad is shown in Fig. 3-38 for 12 A peak injections. The voltage on the output is shown by pos_sense_V. The variation in the output voltage from the level detector and voltage converter due to rise time and pulse width is 8%.

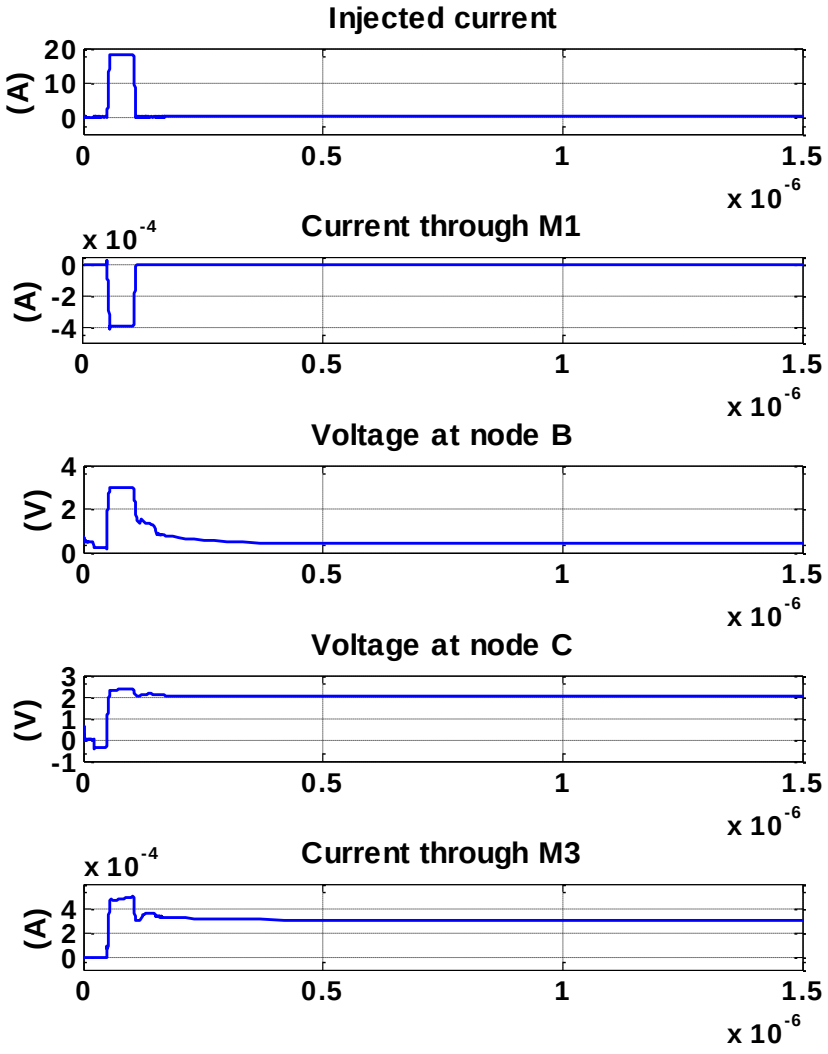


Figure 3-34. Important current and voltages in level sensor when I/O pad was injected with 12 A peak trapezoidal pulse

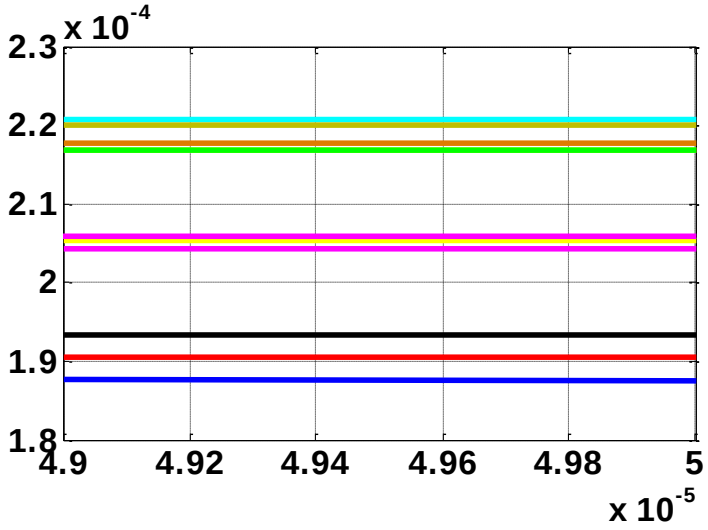


Figure 3-35. pos_sense_rail current 50 us after event when I/O pad injected with 12 A pulses with different rise times and pulse widths

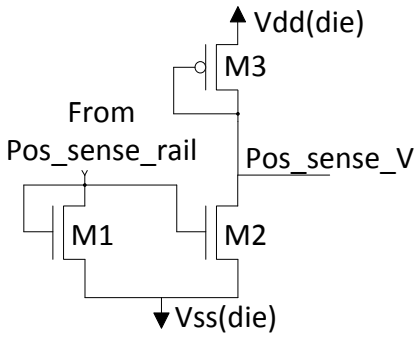


Figure 3-36. Current-voltage converter circuit for positive events

Monte Carlo simulations were done to include the effect of process variations on the output voltages. Simulations were performed with both trapezoidal pulses with varying rise and fall times and pulse width and with different sized ESD pulses. Fig. 3-39 – Fig. 3-41 show the histograms of output voltages when varying process parameters and trapezoidal pulse shapes, for peak currents of 6 A, 12 A, and 18 A.

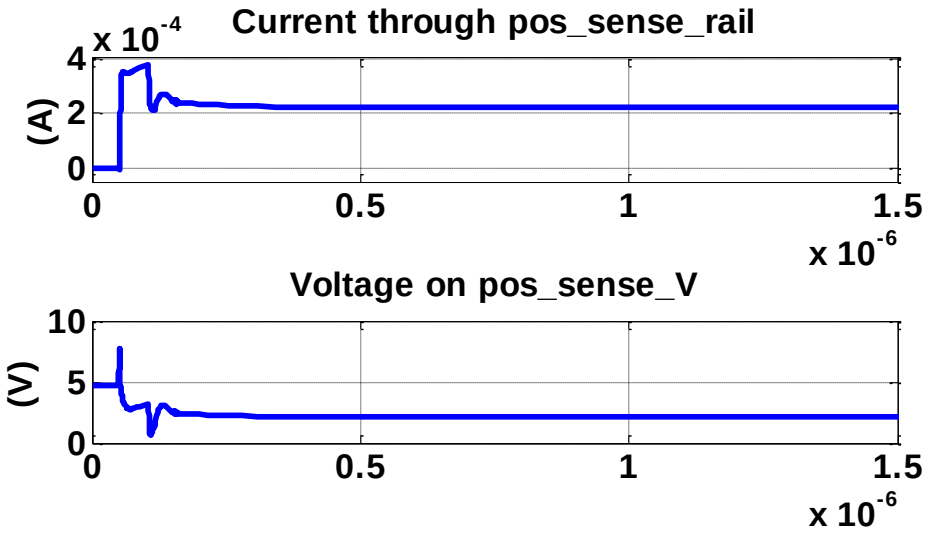


Figure 3-37. Operation of current-voltage converter for a 12 A peak trapezoidal injection

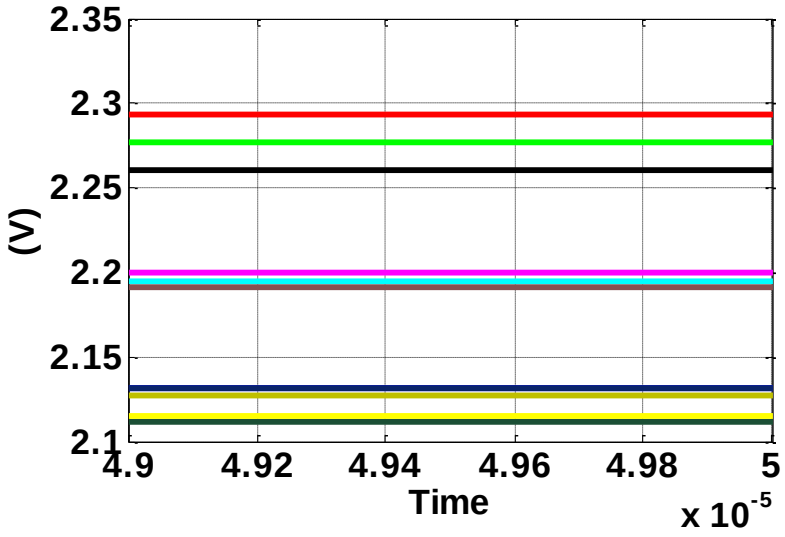


Figure 3-38. Variation of output voltage from level detector and voltage converter at pos_sens_v due to rise time and pulse width variation of 12 A peak injection

The total variation on the output voltage, including process variation and pulse variation, comes to around 16% for 12 A peak injections. Fig. 3-42 – Fig. 3-44 show

histograms of the output voltage for ESD events. These sized events were used with the intent to show the scheme could effectively differentiate between small, medium, and large events without any calibration. The results in Fig. 3-39 – Fig. 3-44 show no overlap between these sized events, illustrating that the detector can function effectively without calibration.

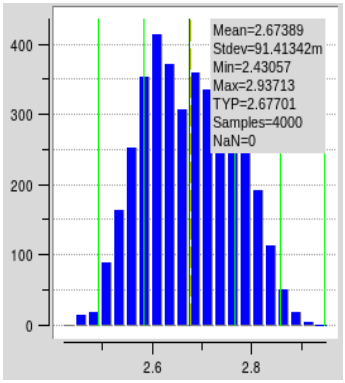


Figure 3-39. Monte Carlo simulation results for output voltage variations from detector and converter due to process variations as well as rise time and pulse width variations of 6 A peak events

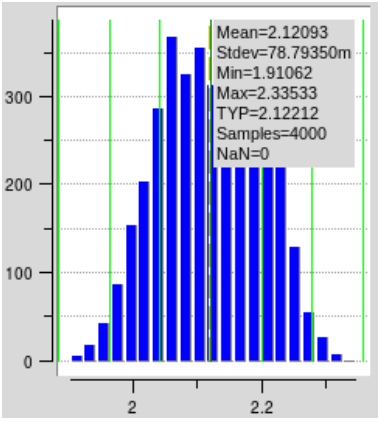


Figure 3-40. Monte Carlo simulation results for output voltage variations from detector and converter due to process variations as well as rise time and pulse width variations of 12 A peak events

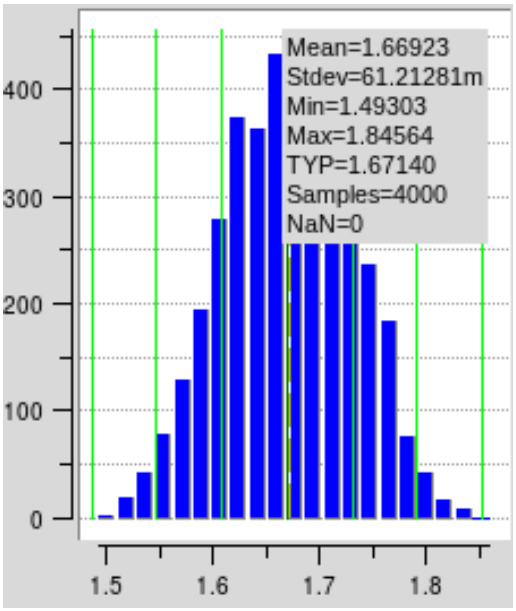


Figure 3-41. Monte Carlo simulation results for output voltage variations from detector and converter due to process variations as well as rise time and pulse width variations of 18 A peak events

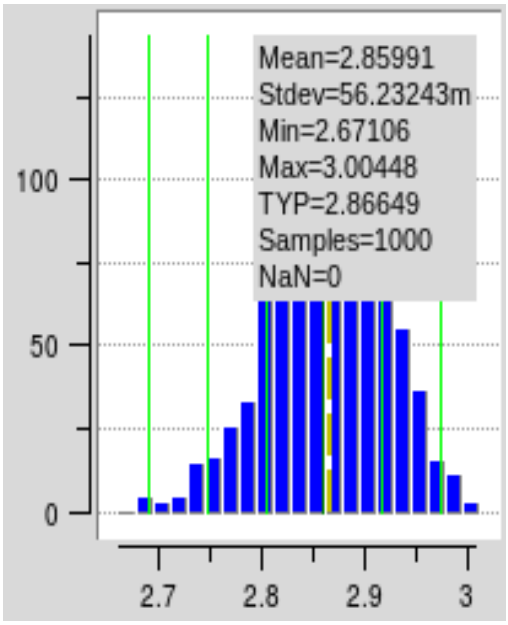


Figure 3-42. Monte Carlo simulation results for output voltage variations from detector and converter due to process variations as well as rise time and pulse width variations of 2kV ESD events

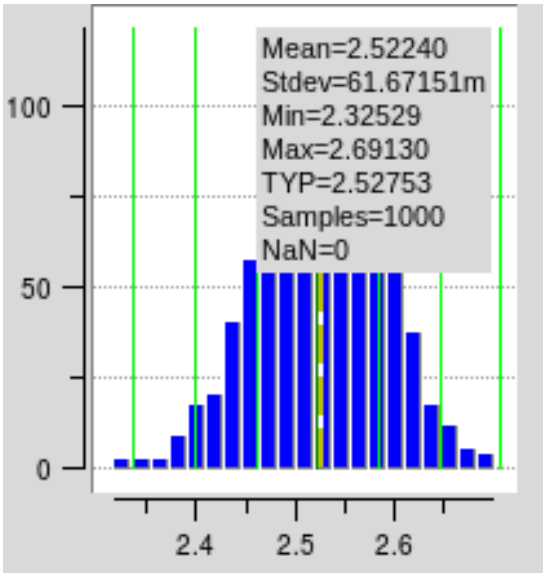


Figure 3-43. Monte Carlo simulation results for output voltage variations from detector and converter due to process variations as well as rise time and pulse width variations of 4kV ESD events

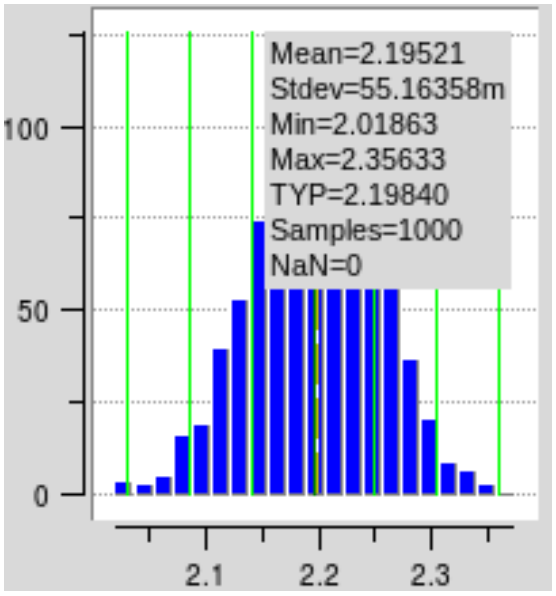


Figure 3-44. Monte Carlo simulation results for output voltage variations from detector and converter due to process variations as well as rise time and pulse width variations of 6kV ESD events

Earlier results clearly demonstrate that the level detection circuit can effectively discriminate between rough levels of events without calibration. If one is willing and able to calibrate an IC to a specific level of event, even better results are possible. Fig. 3-45 is a plot of the output voltage as a function of the peak injection current, when the I/O pad was injected with positive trapezoidal pulses with 10 ns rise time and 100 ns pulse width. Such a curve can directly tell the user the peak input current for a particular measured voltage at the A/D. The output voltage curve changes with process corners as shown in Fig. 3-46. The maximum variation of output voltage due to the process corners is +/- 100 mV, or less than 10%. This variation could potentially be eliminated by calibrating one or two points on the curve, and accounting for the estimated shift in the curve in future measurements. Variations due to the rise and fall time of the curve may still be an issue, though earlier results demonstrate the effective shift due only to pulse shape is less than 10%. Figure 3-47 shows simulations of the output with variations in the temperature of the IC from 10-40 degrees C. The maximum variation in the output over this temperature range is +/- 20 mV, or about 1% maximum.

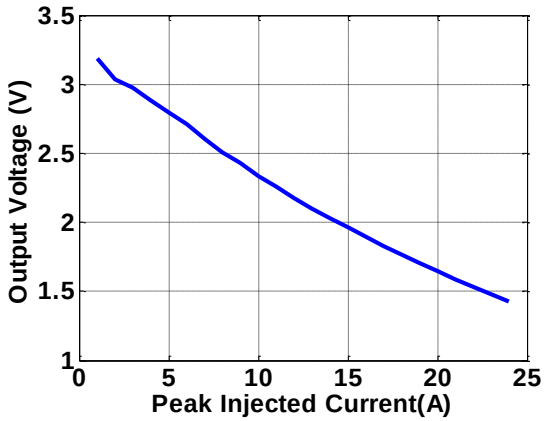


Figure 3-45. Output voltage for positive events as injected peak current is varied

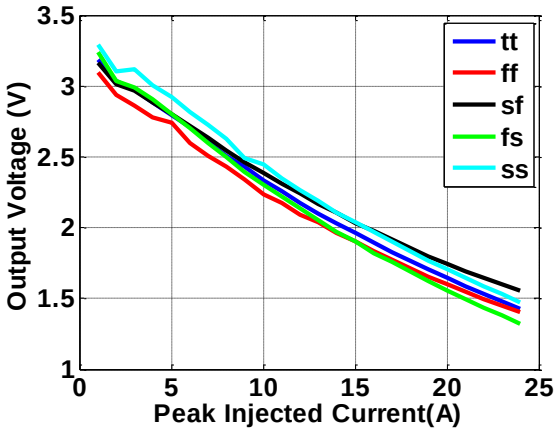


Figure 3-46. Output voltage curve variation with process corners

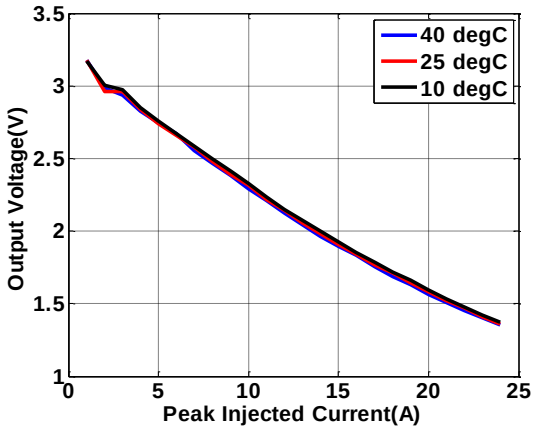


Figure 3-47. Output voltage curve variation with testing lab temperature

The previous analysis was performed for positive events. An analysis was also performed for negative events. Figure 3-48 through Fig. 3-50 show the variation of the output voltage of the level detector and voltage detector while accounting for process variation and variation in the rise time and pulse width of the input pulse. The total variation on the output voltage, including process variation and pulse variation, comes to around +/- 15% for -12 A peak injections. Figure 3-51 through Fig. 3-53 show variation

of output voltage for ESD events of different magnitudes. The results of this analysis demonstrate that, as with positive events, the level detectors are able to effectively differentiate between small, medium, and large events without calibration.

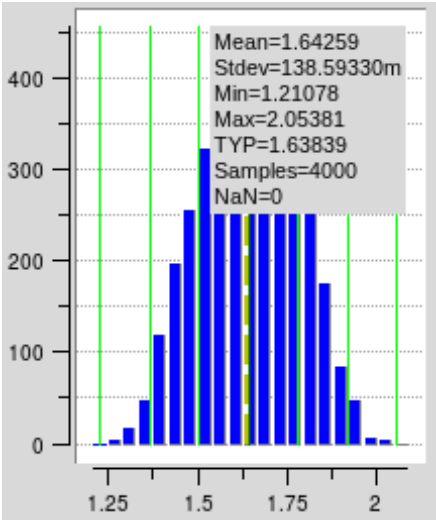


Figure 3-48. Monte Carlo simulation results for output voltage variations due to process variations as well as rise time and pulse width variations of -6 A peak events

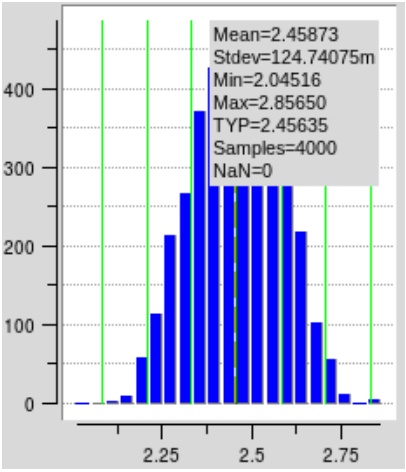


Figure 3-49. Monte Carlo simulation results for output voltage variations due to process variations as well as rise time and pulse width variations of -12 A peak events

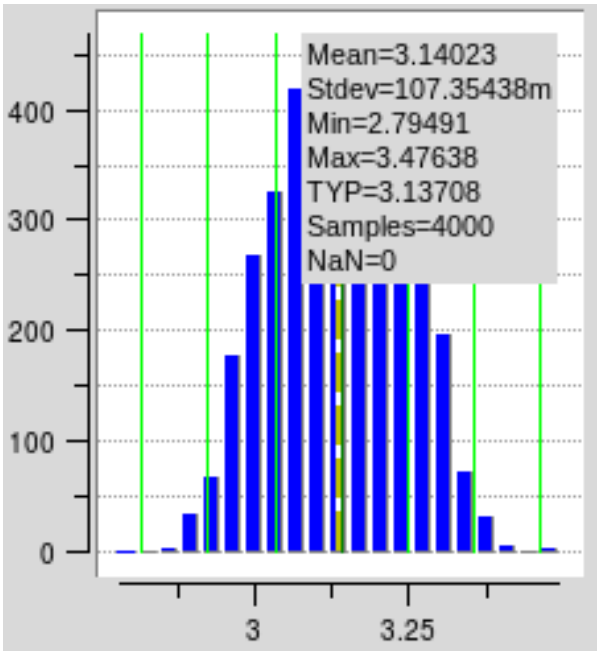


Figure 3-50. Monte Carlo simulation results for output voltage variations due to process variations as well as rise time and pulse width variations of -18 A peak events

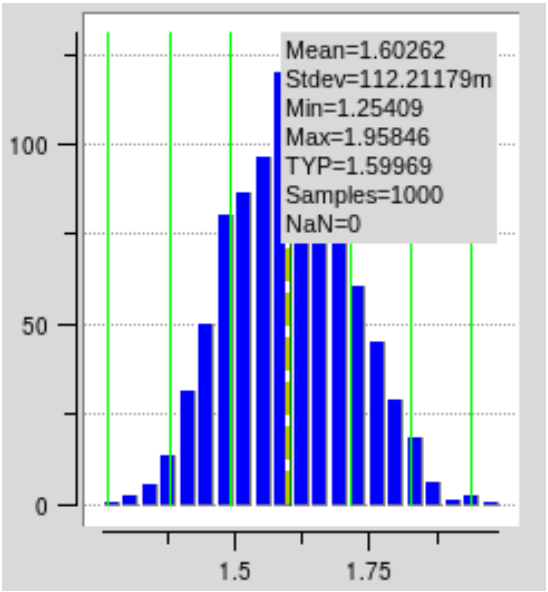


Figure 3-51. Monte Carlo simulation results for output voltage variations due to process variations as well as rise time and pulse width variations of -2 kV ESD events

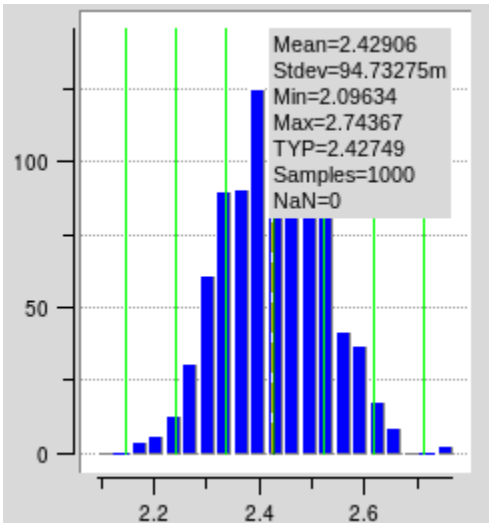


Figure 3-52. Monte Carlo simulation results for output voltage variations due to process variations as well as rise time and pulse width variations of -4 kV ESD events

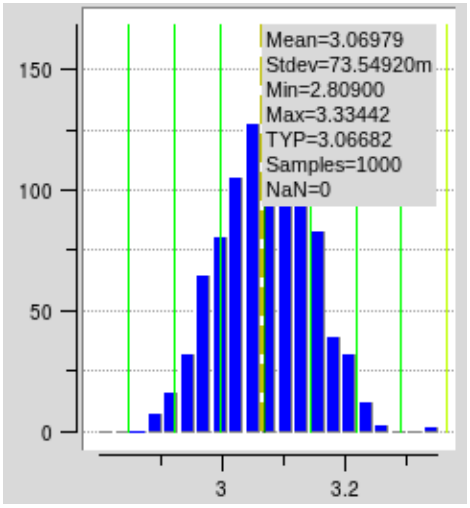


Figure 3-53. Monte Carlo simulation results for output voltage variations due to process variations as well as rise time and pulse width variations of -6 kV ESD events

Curves showing the relationship between peak injected current and the output voltage for negative injection are shown in Fig. 3-54 through Fig. 3-56. The curves for

negative injection differ from positive injection in the sense that the output voltage increases as the level of injection increases. The variation of the output voltage with the process corner is a maximum of +/- 110 mV (less than +/- 12%) as shown in Fig. 3-55 for injections from 1 to 24 A. The maximum variation in in output voltage with temperatures from 10-40 degrees C is +/- 55 mV (less than +/- 7%).

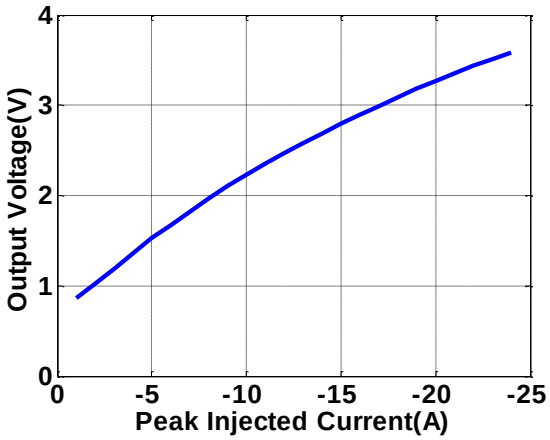


Figure 3-54. Output voltage for negative events as injected peak current is varied

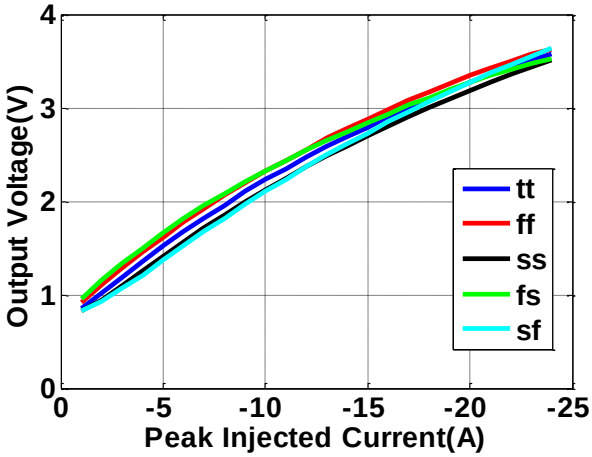


Figure 3-55. Negative events output voltage curve variation for with process corners

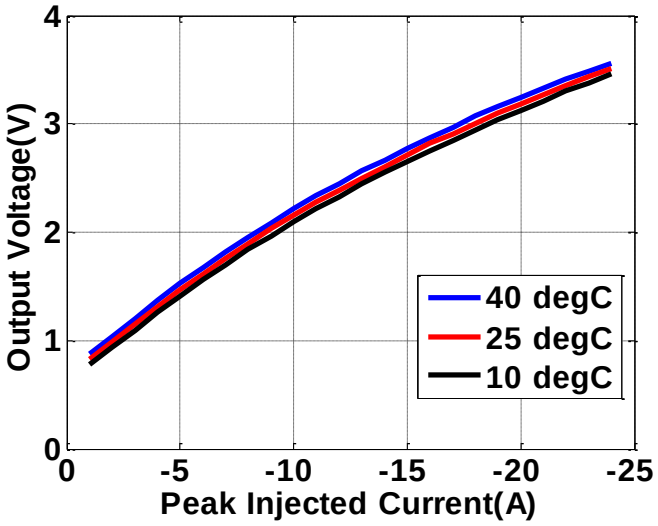


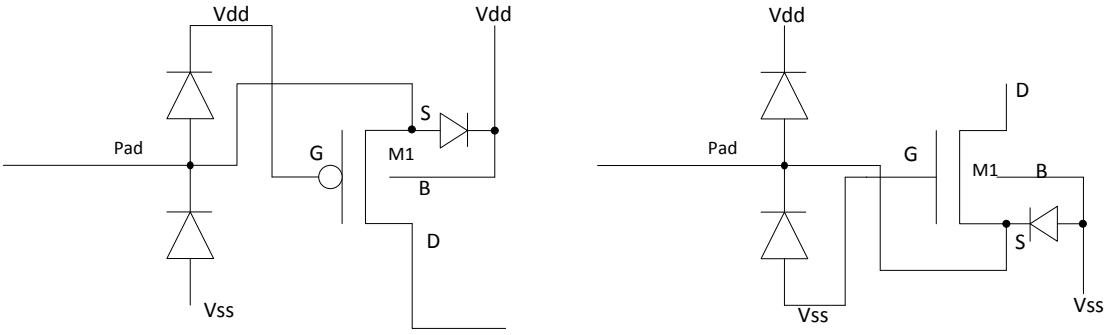
Figure 3-56. Negative events output voltage curve variation for with lab temperature

3.2.4 Implementation Details. The basic functionality of the event detectors and level sensors was demonstrated in the tests presented in previous sections.

Implementation of the detection scheme in a real CMOS IC, however, will require some additional design overhead. The next section will discuss methods to bias the body (the well) of the detection FET, for preventing damage from snapback across the sense rail, for limiting the impact of minority carrier injection on the voltage stored by the capacitor, for resetting the stored capacitance and event detectors, for level shifting signals between the pads and the core, and for dealing with a power on reset. All the modifications to the circuits discussed in next section were part of the simulations discussed in the report and will also be implemented in the test IC.

3.2.4.1 N-well and p-well biasing circuits. It is generally assumed that the body connections of PFETs are made to V_{dd}(die) and NFETs are made to V_{ss}(die). As shown in Fig. 3-57, if these connections are used then parasitic diodes from the source to body of

the detection FET will turn on during a under/over voltage event and this parasitic diode may thus prevent the circuit from working according to design.



(a) (b)

Figure 3-57. Parasitic diodes between body and substrate for PFETs and NFETs connected to I/O pads

The reason for connecting the body of a PFET to Vdd is to have the body at the highest potential in the circuit and thus prevent the parasitic diode from turning on. During an overvoltage event, the I/O pad would be at the highest potential so one option would be to connect the body to the I/O pad (i.e. short the source and body of the PFET). This works when the I/O pad voltage is high, but fails when the pad voltage goes low. If the pad voltage goes more than a diode drop below the drain voltage (e.g. after an ESD event), the parasitic diode between the drain and body could turn on and "reset" the detector or interfere with level measurement. Even if the parasitic drain-body diode is not an issue, the dependence of the PFET threshold voltage on the level of the event (i.e. the level of the body-source voltage) complicates interpretation of the results. Circuit solutions are shown in Fig. 3-58. The circuit shown in Fig. 3-58(a) and (c) fixes this issue

by biasing the N-well (body) of the PFET to the highest potential from either Vdd(die) or V_{pad}. A similar problem occurs when connecting the body of the NFET of the negative event detectors or sensors to VSS, as shown in Fig. 3-57(b). This problem is solved by using isolated P-wells and using the well biasing circuit shown in Fig. 3-58(b) and (d).

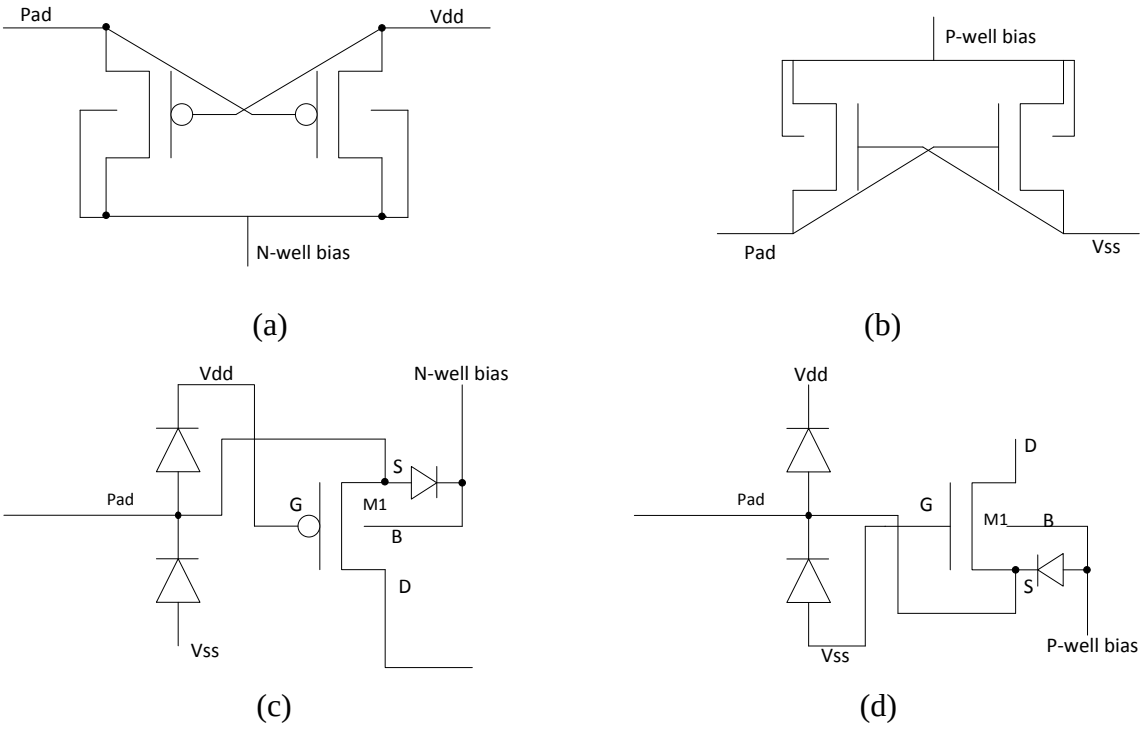


Figure 3-58. Solution circuits to body biasing problem (a) N-well biasing circuit (b) P-well biasing circuit (c),(d) Modified connections for FETs source conencted to I/O pads to avoid problems with parasitic diodes

The PFETs in Fig. 3-58(a) and (c) should all lie in a single N-well. The N-well containing these 3 FETs should be separate from the N-wells used by other PFETs that are part of the design. Similarly, the NFETs in Fig. 3-58(b) and Fig. 3-58(d) should be placed together in an isolated P-well, which is separated from other NFETs in the design.

3.2.4.2 Snapback current limiting resistors. For the level sensor circuits, the FETs connected to the pos_sense_rail or neg_sense_rail (M5 in Fig. 3-59) may be connected through the sense rail and I-V converter to a power rail all the way on the other side of the IC.

During a large magnitude transient event, the voltage drop across the power supply rail across the IC may be large enough to cause M5 (and the equivalent FET in the I-V converter) to go into snapback. While this snapback does not necessarily disturb the level measurement (since the peak level is stored on a capacitor and read later) the FETs should be protected to ensure they will not fail. Current limiting resistors as shown in Fig. 3-59 should be added to both the positive and negative event level sensors. The value of the current limiting resistors can be determined from the width of M5 devices, the secondary breakdown current for M5, and the worst case voltage that can be seen from Vdd(die) at one end of the IC to Vss(die) at another end of the IC, as determined from simulations of the ESD event. This resistance should generally be too small to impact the performance of the bus during normal operation. This resistance could be implemented with short segments of polysilicon along the bus or by using silicide block at the drain of M5 and an appropriately long drain connection.

3.2.4.3 Different p-wells and n-wells. The diodes in level sensors should not be implemented in the same well as the capacitor in the level sensor. For example in Fig. 3-59(a), the positive event level sensor, the diodes D1 and D2 should be constructed in an isolated P-well, different than other N-devices.. The capacitor and diodes must be implemented in different isolated P-wells to minimize the possibility that minority carrier injection into the substrate during a transient event can be captured by these devices and

discharge the capacitor. For a similar reason, the diodes D1 and D2 in Fig. 3-59(b) should be constructed in an N-well isolated from other P-devices.

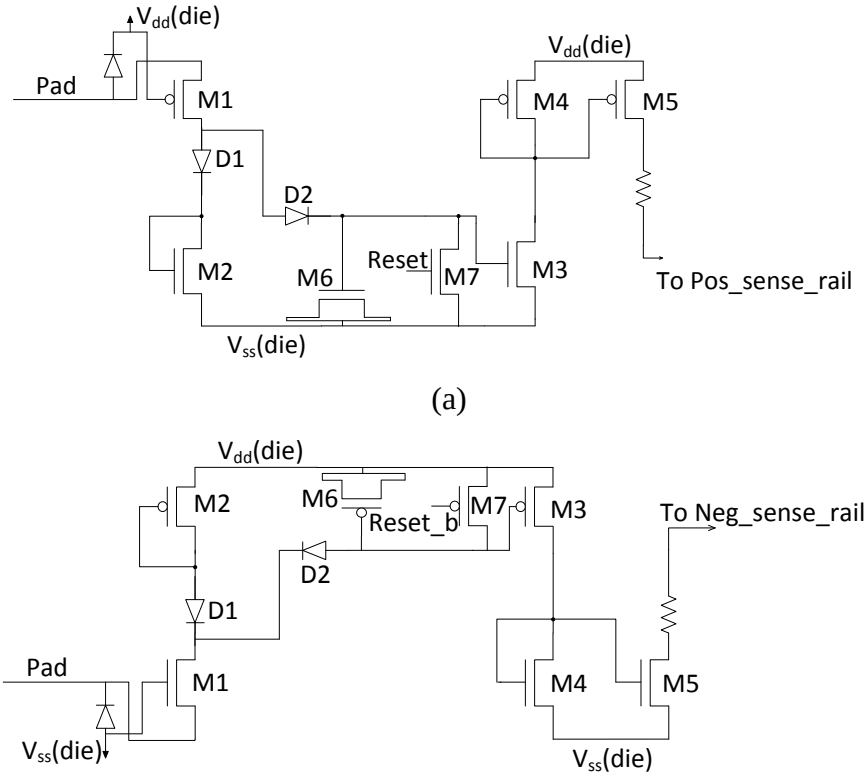


Figure 3-59. Level sensors with current limiting resistor (a) Positive level sensor (b) Negative level sensor

3.2.4.4 Reset and reset_b. As shown in Fig. 3-18. and Fig. 3-19, the positive event indicator and level sensor use the "reset" signal to reset the event detector and clear the charge on the capacitor, while the negative event indicator and level sensor use the "Reset_b" signal, which is the inverted form of reset. The reset and Reset_b signals are generated by the core and these 2 signals are routed to all the I/O pads by a minimum width bus on I/O pad ring.

While the Reset_b signal could be generated from reset using an inverter (or vice-versa), such a scheme could cause a false reset during a transient event. During a positive event the Vdd(die) and Vss(die) at the I/O pad affected by transient event will be at higher than at other locations on the IC. Hence, if reset is "0" and referenced to Vss(die) at some other part of the IC, reset will certainly be lower than Vdd at the pad location and there is no chance of a false reset to the positive event sensors. Similarly for negative events the Vdd(die) and Vss(die) at the I/O pad are lower than that at other locations on the IC. A Reset_b set to "1" and referenced to Vdd(die) at some other place in the IC is guaranteed to be higher than Vss at the pad, and there is no chance of a false Reset_b signal at the pad. If the Reset_b had been generated by an inverter from the reset signal, a "0" on reset would be referenced to Vss at another location at the die, and this value may be sufficiently higher than the Vss at the pad to be interpreted as a "1" – thus causing Reset_b to be activated during the negative event and preventing proper registration of the negative transient event.

3.2.4.5 Level shifters. The output from the event indicators will be sent to the IC core, where they can be accessed by the microcontroller, and the reset and reset_b signals will be generated by the IC core so the user may exercise control over the transient event detectors/sensors through software.

Level shifters are needed to shift between the voltage levels of the I/O to the levels of the core and vice versa. The level shifting for the event indicators is done at the indicator output using inverters constructed from high voltage devices but supplied from the core supply. This method of level shifting results in the positive event indicator giving an output "high" to the core when it detects an event and causes a "low" from the

core to be seen as a “1” at the event detector/sensor. Similarly, the negative event indicator shows a “low” at the core when it detects a transient event and “high” otherwise, and the reset_b signal of “1” at the core is seen as a “0” at the sensor. A special level shifting cell is created for the reset and reset_b signals which contains the level shifters for both signals. This cell should be placed as close to the location where reset and reset_b are generated as possible. The level shifter circuits are adopted from previous designs.

3.2.4.6 Padrst_mv and close signals. Two additional signals called padrst_mv and close_mv are used by the level sensors to handle power on reset (POR). The padrst_mv signal is generated on a power on reset signal.

The circuits generating the POR signals hold the IC circuits in a predefined state while the IC is powering up. It is possible, however, that there can be a false triggering of POR circuits due to a transient event. Hence, the design is made such that the POR signal, using padrst_mv, will hold the reset signal to a “0” and reset_b signal to a “1”, specifically preventing a POR from causing any information loss. The POR signal will, however, initiate an IC boot-up code. A software check can be placed at the end of this code to check if any event indicators are set and, if set, to read the level of the event. Once the event indicators and the level of the transient event are read the detection scheme can be reset in software. This scheme does cause potential garbage data from detection scheme during an actual power-up of the IC, but this data can be ignored by the user.

The close_mv signal is asserted when the IC core powers down i.e. in low-power modes. Detection of transient events during the low-power mode is desired. Hence, the

close_mv signal also causes the reset signal to default to “0” and reset_b to default to “1”. A detected event can be used to wake up the processor or, when woken up, the processor can check the state of the detector circuits. The detection scheme can be reset after the level of event is measured.

3.3 FUTURE WORK: TEST PLAN FOR SAMPLE AND HOLD METHOD

Test Plan for Sample and Hold Method. Freescale is driving the project towards implementing the detection circuits on a test-chip. The IC is planned for completion by mid-2015. A detailed plan to specifically test the detection circuits designed in this work is presented.

Different aspects of detection scheme that would be tested/determined include:

- **Threshold for triggering event indicators:** These thresholds are an important aspect of the detection scheme as false triggers on event indicators due to overshoots/undershoots on IO pads during normal operation are not desirable. The indicator should trigger, however, on a true ESD event.
- Functioning of **Interrupt subroutine**: The subroutine should be executed whenever one of the event indicators is triggered. The ADC should be initiated as needed and a useful reading should be produced.
- **Level readings:** An initial goal of the design was to categorize events as small, medium and large. Tests should be done to show that 2kV, 4kV and 6kV powered ESD (PESD) pulses fall in separate bins consistently. 2kV, 4kV and 6kV (corresponding to 6A, 12A and 18A peak currents) are just initial approximations where boundaries for small, medium and large level bins fall.

- **Consistency and resolution**: The resolution of the level detection is likely better than just 3 levels (small, medium, and large) if a calibration step is performed first. Tests should be performed after calibration to demonstrate ability to determine the relatively level of the event. Repeated injections of a particular level should be done on each test pin to see the consistency of level readings. The consistency needs to be checked from pin-pin as well as on the same pin for one particular level of injections. The consistency of these test results will determine the resolution between different levels of events. Test should also be performed to ensure consistency among I/O at different locations.
- **Operation under multiple event conditions.** Situations of interest include positive events, negative events, event at a single pin, event at multiple pins, high-speed event (e.g. ESD), low-speed event (e.g. EFT). ESD events which enter through one I/O pin and leave through another will not be tested, as it is expected that the return pin will typically be a power pin (which does not include a sensor).
- **"Hold time" of capacitor**. While the voltage is expected to remain on the capacitor for sufficient time to take a reading, tests should be performed to demonstrate the voltage level is not changing quickly after the event. An approximate upper limit on the amount of time between the event and an A/D reading is also useful.
- **Limits:** After operation of circuits has been tested for recommended limits, circuits can be can tested for higher and lower limits, in the sense of how high

or low of an event can useful ADC readings be achieved. At what point do the level or event detectors fail?

3.3.1 Transient Sources. There are three ways at the EMC lab in which inputs can be provided to test the detection circuits:

1) IEC type injections using ESD gun

Tests using the ESD gun would be comparable to tests done at Freescale for ESD compliance. The simulations are done for IEC shape pulses hence simulation results should be available for comparison. The measurement results, though, would be subject to the variation inherent to ESD gun testing.

2) Arbitrary waveform generator w/ 100 W, 1 GHz power amplifier (largest gain available in the lab)

This method gives flexibility to test many kinds of pulse shapes on a pin by pin basis. Rise times, polarity, duration of pulses, shape of the pulse, etc., can be configured. The problem with this test is the achievable magnitude of the pulse. The arbitrary waveform generator only gives a 700 mv peak to peak output, which when combined with the 100 W power amplifier and other methods can result in injected currents up to 6-7A and a few 10s of volts at the pin. Other test methods must be used for peak currents of 20A or above.

3) Transmission Line Pulser (TLP)

Both industrial and handmade TLPs are available in the lab. These TLPs are configurable in terms of rise times and pulse widths of the output trapezoidal pulse. The

TLPs can easily generate currents of the needed magnitude. Flexibility of waveform shapes and the rise times and pulse widths can be controlled only in particular steps.

Among all the three possibilities, the TLP method seems good for initial tests to prove the function and capabilities of the detector circuits. Initial testing with the TLP can be followed up with tests using the other sources.

3.3.2 Test Board. Proper test board needs to be planned for injections and related measurements. One such example is given in Fig. 3-60.

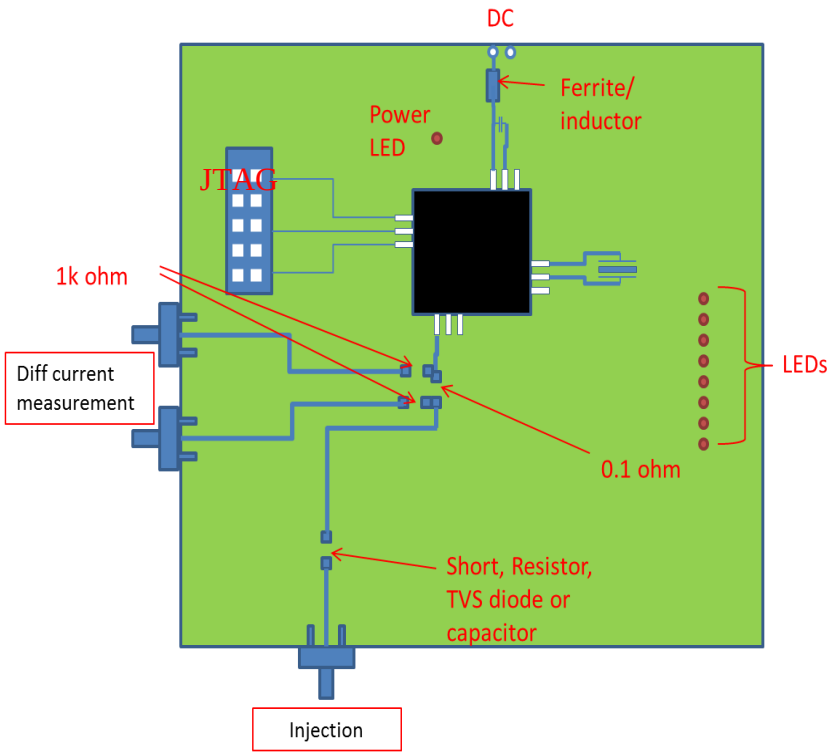


Figure 3-60. Example of a PCB board for measurement setup

The components of this test board include:

- The IC: The pin-out or package style of the test IC is not known, but whichever package is used, it would be better to put a socket on the board rather than the IC

itself. ESD tests would be conducted on these ICs so expectation is that some ICs will be destroyed. Having sockets helps avoid damage to board/pads because of frequent soldering/de-soldering of the IC.

- DC supply: DC supply is isolated from board supply using a ferrite or an inductor. A decoupling capacitor is also placed between Vdd and Vss close to the IC. Additionally, a protection circuit can be placed on board to protect the IC from latch-up current.
- Clock: A crystal oscillator should be placed on the board and connected to the XTAL pins. Injection and measurement traces: The example shows a setup where one can easily measure the injected current and the voltage on the pin and also has a variety of injection methods. This setup requires space on the board and three connectors/pins. This might be ok if only 4-5 pins on the board are going to be tested but may be too many connectors if many pins are to be tested. If more pins are to be tested then current probes can be used instead of having on board current measurements. One voltage measurement point still needs to be embedded on the board close to the IC pin. A lot of space can be saved by using connectors like MMCX connectors rather than SMA connectors for example. The trace between the connector and the pin should be reasonably short and should have a characteristic impedance of 50 ohms. If sufficient space is not available putting test pads near to each pin and injecting current using a probe can be considered.
- Current measurement: The injected current is made to pass through a 0.1 ohm resistor. The voltage on both the sides of this resistor is measured. The injected current can be derived from the difference of two voltages. The trace lengths for

both voltage measurement points must be the same. Out of the two voltage measurements, the one closer to the pin is the voltage at the pin.

- Injection methods: for a non-operational pin one can use direct injection or resistive injection. For an operational pin, a diode is suggested since it provides good isolation to the pin otherwise a resistor as large as 500 ohms might also serve the job depending on the impedance of the pin during operation. A capacitor can be used to create very narrow pulses using a TLP. A capacitor does attenuate the TLP pulse but it helps to get a very narrow pulse.
- JTAG: JTAG needs to be present, not only so that the IC can be programmed in place but also to read register status during injection to see the working of the detection circuit. Optionally series of LEDs (8 LEDs) connected to GPIOs from the microcontroller can be used. If access to the Interrupt sub-routine for the detection circuits is available, then data being sent to these LEDs can be controlled. Having LEDs is suggested particularly if safety/reliability of the debugger connected to the board while doing ESD tests is not guaranteed.

3.3.3 Measurements. The plan is to have automated measurements on each pin, in the sense that the TLP will be connected to a particular injection connector and then an automated program will control injections and measurements using Matlab/Labview.

For all the tests discussed below, the TLP magnitude should not exceed 8 A peak when pulse widths of 10ns or higher are used (up to 50 ns). For higher current injections pulse width should be reduced to 2 ns if possible. With 2 ns pulse width, injections of up to 20 A can be made. A 5 ns pulse width should have a current limit of15 A.

Before series of tests are performed a sample from all of the below mentioned tests should be performed to get a good idea of delay to set in interrupt routine and how interrupt and ADC are behaving during the tests. Then the tests can be performed in the order they appear in this report.

3.3.4 Event Indication Thresholds. Event indication thresholds should be determined, both to confirm simulation results and to ensure that the device will not generate a false trigger. The test setup is shown in Fig. 3-61.

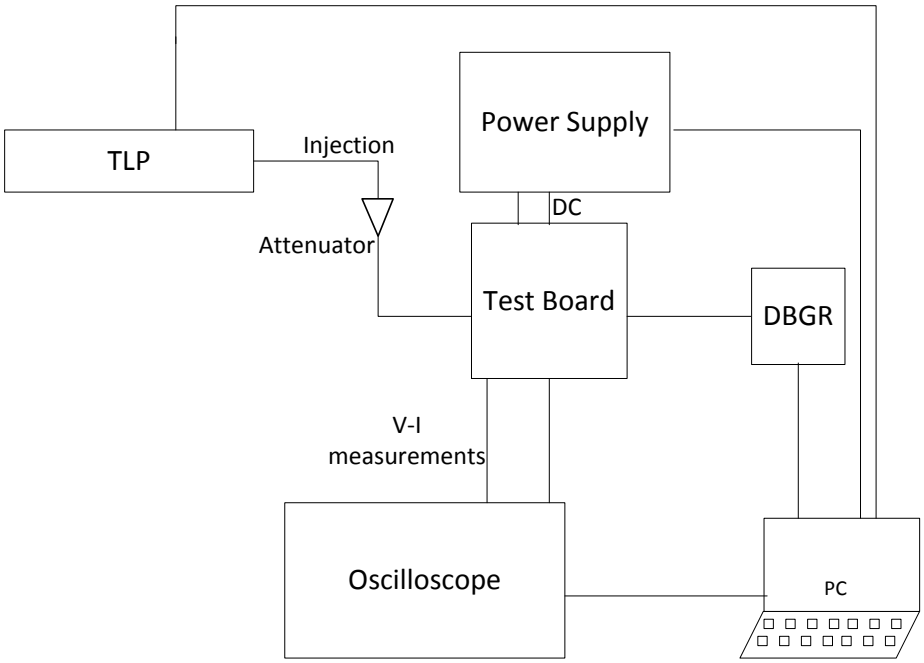


Figure 3-61. Example setup for testing detector circuits on test board

Important aspects of the test setup include:

- Microcontroller should be configured with appropriate software. At a minimum, the microcontroller should configure the pins and the detectors and then loop continuously. If an RS232 or LED interface will be used to read the state (e.g.

whether an event occurred), then code must be included (e.g. an interrupt service routine to detect event or trigger RS232 comm.). Using the interrupt here to light an LED allows easier reading of the event and dual testing of both the event detection and the use of the interrupt to do so.

- The TLP should be set for the fastest rise time possible and a pulse width of around 10 ns. The attenuation for TLP should be set high enough to get injections of 100's of mAs on the IC pin. The level of the injection can be determined from the oscilloscope reading of the voltage across a resistor in series with the pin under test. The TLP should be injected between the pin and the PCB reference plane.
- The I/O pin under test should be tri-stated (e.g. set as an input), to ensure all current is routed through the ESD protection structures. Other pins are unimportant.
- Start injecting to the board with low magnitude pulses (approx. 50mA). The magnitude should be sufficiently low that it does not initially trigger the event indicator. The board should be reset before every injection by turning the power supply on-off.
- The IC should be checked for triggering of event indicators either through debugger interface as shown in setup or through on-board LEDs. If the debugger interface is used, the interface must remain connected during the test. An optical RS232 interface is also a possibility.
- The IC should be injected with at least 25 pulses for each magnitude to provide a statistical measure of results.

- For each test, the IC should be queried to determine on which pin the event was detected. It is expected that only an event detection will be found on the pin under test.
- The magnitude of the injection should be increased until the event indicators trigger consistently. The current should be increased in steps of roughly 50 mA, though smaller steps can be used to better determine the true threshold.
- Consistent triggering would mean 80-90% of injections cause trigger of the indicators.
- Record the injected current and pin voltage for such injections by recording data from oscilloscope. The threshold should be based on injected current**.** If the current cannot be reasonably measured on-board, one might consider measuring the current using a current probe in line with the board.
- Repeat this process to find thresholds for event indicators at multiple test pins
- Map of thresholds can be created as shown in Fig. 3-62. All the pads will have same design implemented so the curve is expected to be close to a straight line.
- Repeat the above test while varying the rise times and duration of injected pulses. The threshold should remain roughly constant.

- **Level Readouts.** The setup for this test remains similar to previous test for event indication thresholds.

- Software should be loaded in the microcontroller to allow readout of the A/D detector, to read the level either using the debugger or by writing the level to the

LEDs or the serial interface. The event detection interrupt can be used if appropriate.

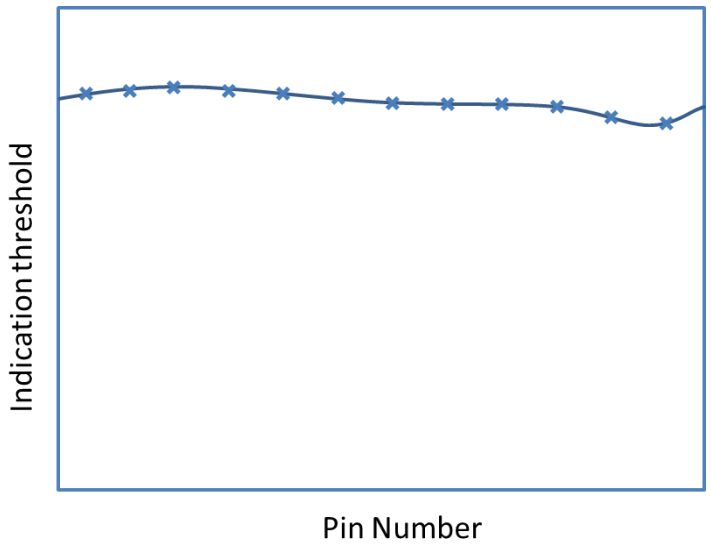


Figure 3-62. Example pin number to indication threshold map

- The test pin where injections are to be performed should be high impedance (example: set as an inputs)
- At first, a test will be performed to ensure the event is detected, the correct pin is indicated, the interrupt is triggered, and a result can be read from the A/D converter.
- Attenuation on TLP will need to be decreased so as to have Amperes of current injected.
- Fix the TLP to positive polarity, rise time to fastest available and as narrow pulse width as possible.

- Start injections from magnitude just above the highest event indication threshold observed in previous tests. Repeat injections with one magnitude while resetting the board before each injection
- Enough injections should be done at one particular level so as to have good statistical data. For each injection ADC reading representing magnitude of event should be recorded from debugger or LED interface. Histogram for each level of injection can be created as shown in Fig. 3-63.

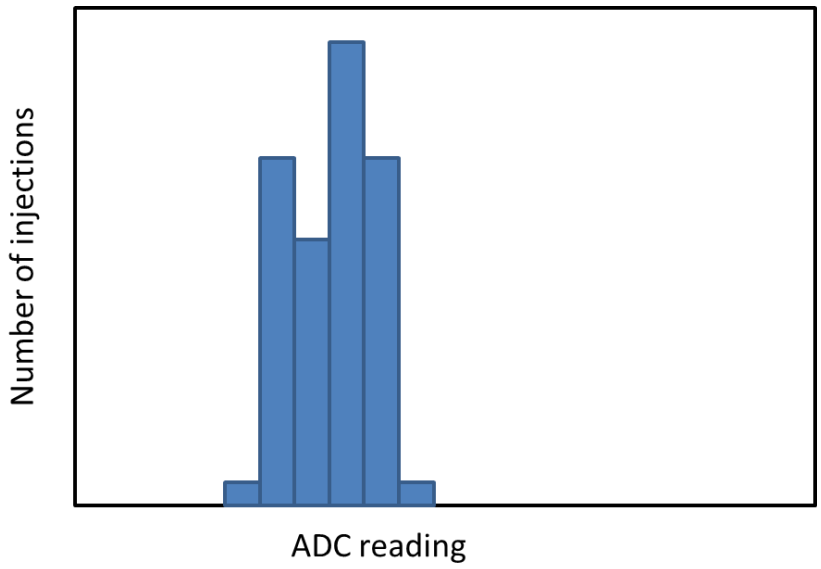


Figure 3-63. Example histogram created for a particular level of injection on a particular test pin

- The injection levels might be increased in steps of around 500 mA and similar histograms for each injection level should be created.
- Histograms for each level of injection also help us to know how different the levels of event have to be in order to clearly differentiate between them

(Resolution). This knowledge can be derived by knowing mean and variance of histograms for different event levels.

- After histograms and statistical data for each pin is obtained, each pin can be calibrated by creating injected current Vs mean ADC reading plot as shown in Fig. 3-64 and Fig. 3-65. For each level, error bars can be added as shown in figures below to aid the analysis.

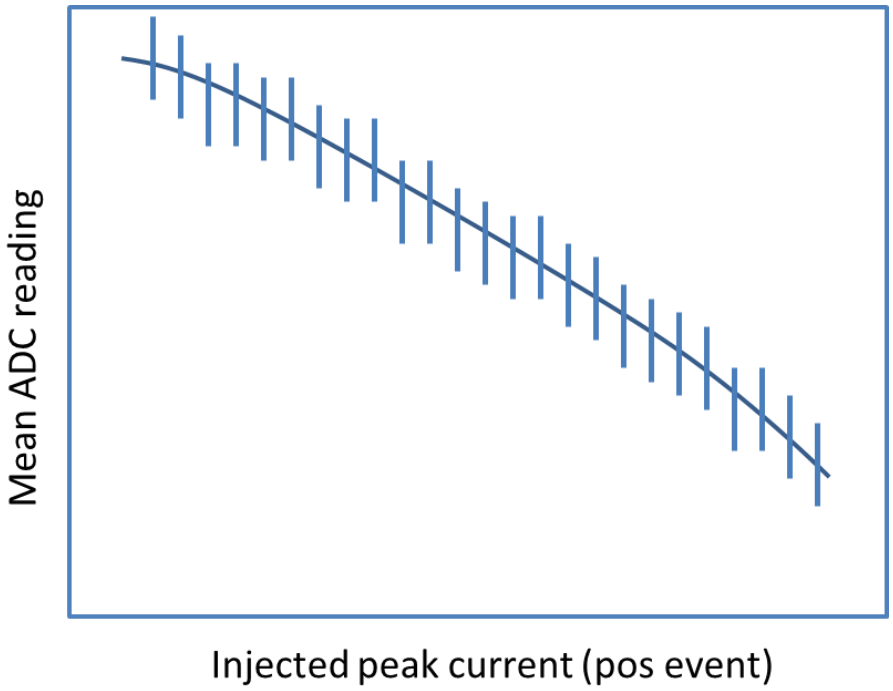


Figure 3-64. Example plot of ADC reading vs injected peak current with error bars included (positive events)

- The plots in Fig. 3-64 and Fig. 3-65 will then be useful to know magnitude of injected disturbance during system level ESD.

- Injections with different levels can be done on few other test pins and the level readouts from ADC can be compared or a map can be formed as shown in Fig. 3-66

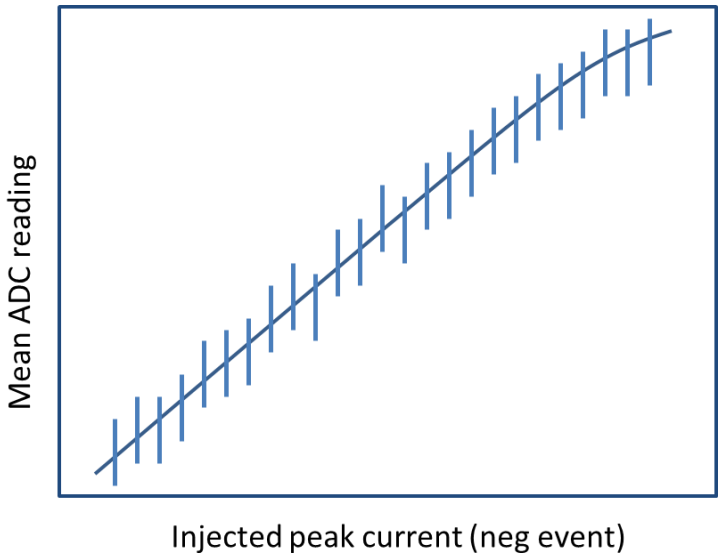


Figure 3-65. Example plot of ADC reading vs injected peak currents with error bars include (negative events)

- Plots as shown above are useful to know the consistency of detection circuit. These plots also help to decide absolute minimum and maximum ADC readouts for a particular level of injection anywhere on the IC.
- Dynamic range of ADC readings should also be noted to make sure ADC is being used close to full capacity at the same time data is not out of the range for ADC.
- The whole process should be repeated with different rise times, pulse widths and negative polarity and various thresholds and plots should be compared.

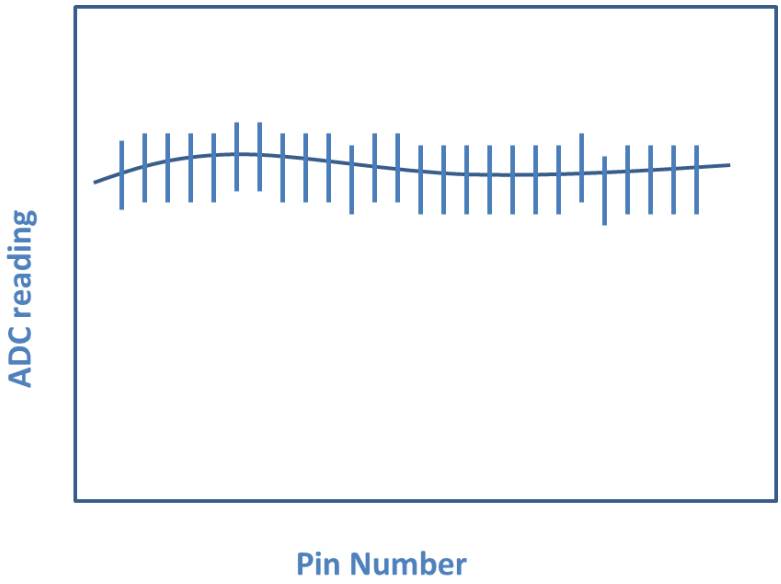


Figure 3-66. Example ADC reading vs pin number map created for a particular level of injection

3.3.5 Hold Time. For testing for hold time the setup would remain same as for other tests but the interrupt subroutine needs to be changed to have variable delay between when the interrupt occurs and when the ADC is activated.

- Setup the instruments and test board as shown in Fig. 3-67. Similar to previous tests, set the test pin to input
- The tests should be started from no delay in the interrupt sub-routine.
- Select one particular level of injection (say 5A peak current) with fixed rise time (1ns) and pulse width (5-10ns) on the TLP.
- Injections should be done on the board while resetting the board before every injection by turning the power supply on and off in the program. At every injection ADC reading corresponding to the detection should be recorded using

the debugger interface, or if LEDs or serial interface is used the interrupt subroutine should be configured to relay out the data.

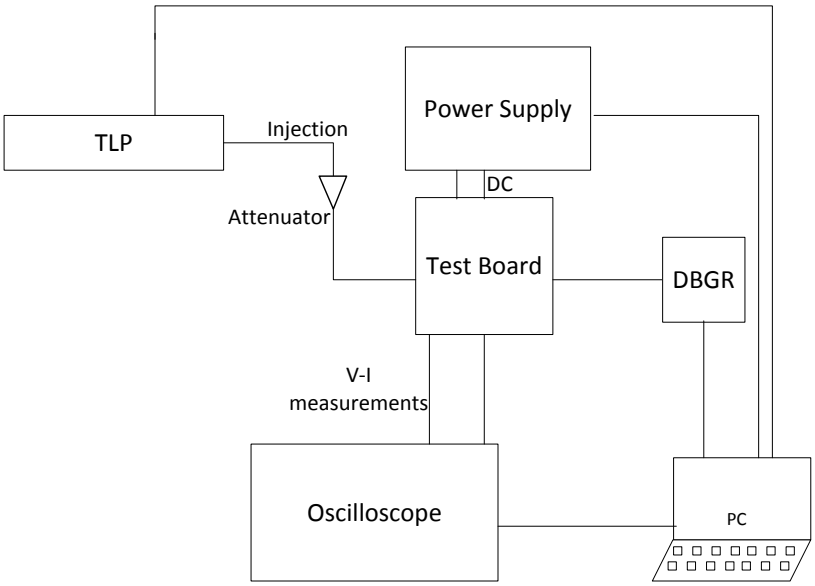


Figure 3-67. Example setup for testing detector circuits on the test board

- 25-50 injections at each hold time should be performed and histogram for such injection as well as mean value should be recorded
- After this 10s of microseconds of delay can be added to the interrupt subroutine, just before the ADC read is initiated
- Again multiple injections should be done with the setup and histogram should be recorded.
- The process can be repeated by increasing the delay before ADC read every time
- Finally a plot of ADC reading Vs delay time has to be created, for example as shown in Fig. 3-68.

- The point where reading starts to be more than 2-3% different then the initial reading should be considered as upper limit of the delay.
- The whole test process should be repeated with different levels of injections (example 5, 10 and 15A) and different pins should be tested to get an average usable value of delay.
- Negative polarity should also be tested with the same process as mentioned above.

3.3.6 ESD Gun Tests. After verification of working of the detection circuits using the TLP, ESD gun tests can be run. Individual pins can be tested as well as other tests like discharge on nearby ground plane, air discharge and so on can be conducted using ESD gun.

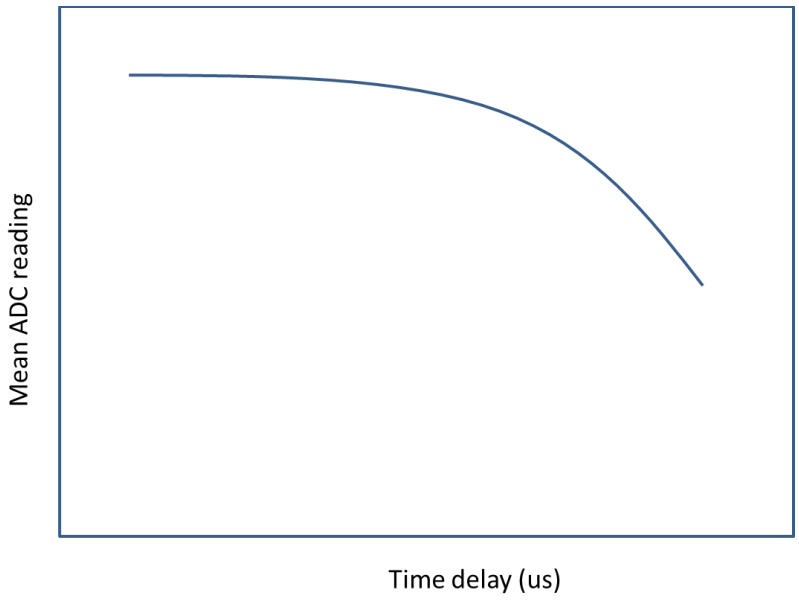


Figure 3-68. Example ADC reading vs time delay plot created for a particular level of injection on a particular test pin

4 FILTERING/INTEGRATION FOR DETAILED EVENT ANALYSIS

Detectors designed and discussed till this point will estimate the peak disturbance caused by a transient event. Peak level is one of the factors on which the errors or damage to the IC depends upon. Energy of the event is also important. A sustained event can cause more thermal damage to the IC compared to a brief event of same magnitude. The idea is to modify the level sensor designs so that with small added area on the detector circuits, user can get information regarding the peak disturbance as well as the energy in the event.

Two ideas thought of, to achieve the above said goals, are filtering and integration.

4.1 FILTERING

Filtering approach is developed with reference to IEC-6100-4-2 ESD pulse. Designs till this point will measure the highest disturbance caused by the event, either by the first, short peak or the later prolonged hump of the pulse. If first peak of the event is filtered out then it can be ensured that the measurement is reference to the prolonged hump of the event, where majority of the energy of the pulse is concentrated. Idea of the level sensor proposed is shown in Fig. 4-1. Transmission gate T1 will have to be very low resistance path, so as to let the measurement be unaffected by it but T2 will be more resistive compared to T1 to form a filter in conjunction with capacitor M6. This filter essentially would be a low pass filter to filter out the voltage corresponding to first peak

of the ESD event affecting the gate voltage of M3. Filtering can be turned on or off using a digital signal S1.

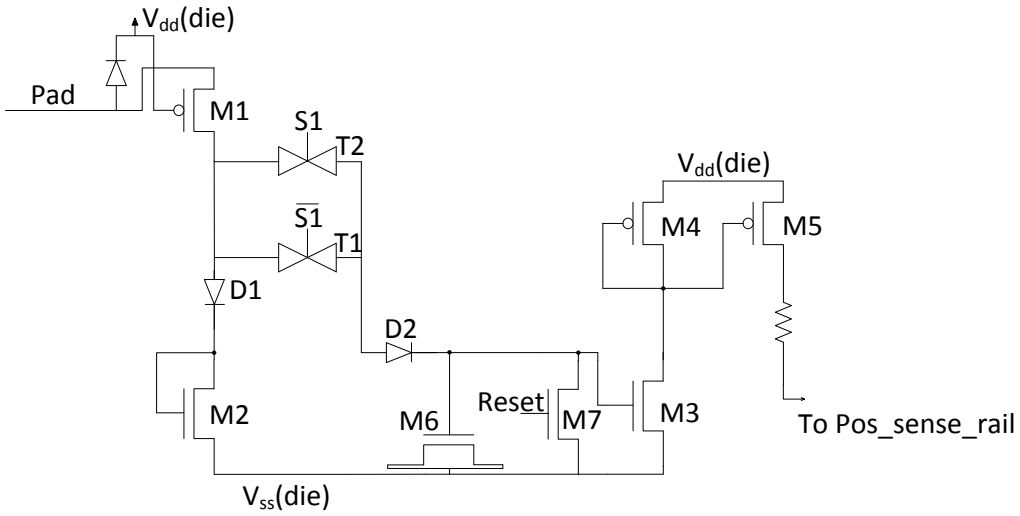


Figure 4-1. Positive event level sensor with filtering

4.2 INTEGRATION

Integration will directly give a measure of the energy of the event. Modified level sensor for positive events is shown in Fig. 4-2. The current from M3 is proportional to the instantaneous level of the event. Capacitor formed by M4 integrates the current from M3. Hence, final voltage on the capacitor is proportional to the energy in the event. This voltage on the capacitor is converted to a constant current by driving gate of M5. Thus different events can be compared in terms of energy by using such a level sensor. Drawback of such a sensor is that it has to be implemented separately than the sensor giving information regarding the peak disturbance, making it area expensive. This circuit

can still be used where user is willing to spend area on die to get more information about the transient events, for example, test ICs.

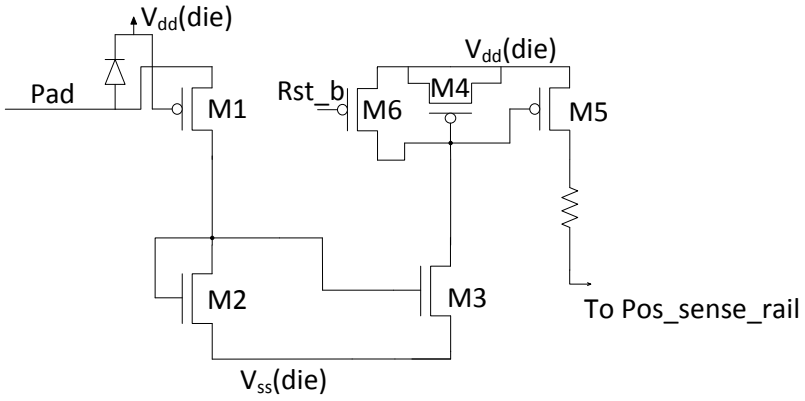


Figure 4-2. Positive event level sensor with integration

5 CONCLUSIONS

Many designs are proposed and tested in simulations, which can be implemented on an IC to give information about the transient event(s) affecting the IC. Out-of-range voltage detectors in Section 2.1 show good resistance to PDN noise with current-source load inverter configuration. An A/D converter of sorts can be implemented at each I/O pad using multiple out-of-range voltage detectors. This implementation can determine presence of disturbance at that I/O pad and approximate the level of event but will have comparatively large area overhead for the IC. If implemented as central A/D converter the voltage drops across buses around I/O pad ring will cause problems in accuracy. Also this design might have lot of variation in results when process variation is considered. Oscillators in Section 2.2 will have similar problems to out-of-range voltage detectors in terms of voltage drop across buses causing accuracy problems.

Centralized A/D based methods promise better accuracy compared to designs in Section 2, since the information about levels is sent to central location in form of current. Current is more resistant to corruption by bus resistance compared to voltage, hence good results. Instantaneous detection scheme shows good results but due to voltage drop on PDN, this scheme can possibly be used for small ICs or applications with V_{dd}/V_{ss} pairs at regular intervals in the IC pad ring.

Design proposed in Section 3.2 is found to be most feasible for present application and is verified, in simulations, to give satisfactory results with low error margins considering process variations, variation in rise time and duration of transient event affecting the IC and temperature of the test environment. A test IC is planned in

summer of 2015 with this design implemented and a test plan is proposed to test the performance of detection scheme. Modifications to the detection scheme are suggested in Section 4 to get more information on the transient event affecting the IC compared to designs in Section 3.2.

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