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Analysis and comparison of two high-gain interleaved coupled-inductor boost converters

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Department:

ANALYSIS AND COMPARISON OF TWO HIGH - GAIN INTERLEAVED COUPLED-INDUCTOR BOOST CONVERTERS

by

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ABSTRACT

The main objective of this thesis is to compare and analyze two different high-gain dc-dc power electronic converters based on coupled inductors and capacitor-diode multiplier cells. The idea of these converters is to integrate the solar energy with a 400V DC microgrid. DC microgrids are more efficient, less expensive, and more reliable compared to AC microgrids. They also favor the integration of renewable energy sources. With the growing need for the utilization of more renewable sources of energy, photovoltaic panels have become one of the trending technologies which convert the energy from the sun to a useable electrical power. But these panels produce a low dc output voltage which cannot directly be connected to the high voltage dc distribution of the grid. They require high-gain dc-dc converters suitable for converting the output voltage of the solar panels to the dc distribution grid voltage. The topologies studied in this thesis provide a high dc voltage gain suitable for this application. The other significant advantage of these topologies is a continuous input current which increases the effective utilization of the source. These converters can also be used in applications involving high gain dc-dc conversion such as fuel cells, and energy storage applications like ultracapacitors. In this thesis, the different operating modes of the two high-gain dc-dc converters are explained in detail. Also, the voltage and current stresses seen by the components have been derived and power loss analysis is carried out for both the topologies. Recently, GaN switches have gained popularity for their higher efficiencies at higher switching frequencies, so this thesis also makes an attempt to compare Si to GaN devices in terms of efficiency improvements for the studied converters.

ACKNOWLEDGMENTS

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NOMENCLATURE

Symbol	Description
V_{in}	Input Voltage
V_{out}	Output Voltage
D	Duty Cycle
N	Turns Ratio of the coupled inductors

1. INTRODUCTION

1.1. ROLE OF HIGH GAIN DC-DC CONVERTERS

With the growing interest in the field of DC microgrids and integration of renewable sources in power generation, the need for high gain DC-DC converters has become one of the most viable options as they would help in integrating solar energy. The main purpose of high gain DC-DC converters is to boost up the low voltage from the solar panel to high voltages which makes it feasible for connecting it to DC micro grids [1-3].

There have been many proposed topologies for high gain DC-DC converters in the literature [4-13]. But topologies with higher efficiency and lesser component stress is the optimal solution. In this regard, this thesis will focus on two high gain DC-DC converter topologies based on a coupled inductor boost converter with multiplier cells. The topologies discussed in this thesis are almost similar in operation except that one of them uses coupled inductors each with a core consisting of one primary winding and two secondary windings and the other with one primary winding and only one secondary winding. This thesis compares, explains various operating modes, and obtains voltage transfer ratio and component's stress for both topologies. It also shows simulation results and hardware results.

1.2. REVIEW OF HIGH-GAIN DC-DC CONVERTERS

With the growing applications of high gain dc-dc converter, there have been many proposed high gain dc-dc converters in the literature. This section reviews few topologies to achieve high voltage gain. Figure 1.1 shows a a parallel diode clamped coupled inductor based boost converter.

Topology shown in Figure 1.1 uses a center tapped coupled inductor. The primary winding is similar to a filter inductor and secondary winding acts as a voltage source in series with the power branch. Diode D_c is a clamp diode, which is used to dissipate leakage energy on to the output side.

The output to input voltage gain of this topology is $\frac{V_0}{V_{in}} = \frac{1+ND}{1-D}$, where N – is the secondary to primary turns ratio of coupled inductor, D- is the duty ratio of switch.

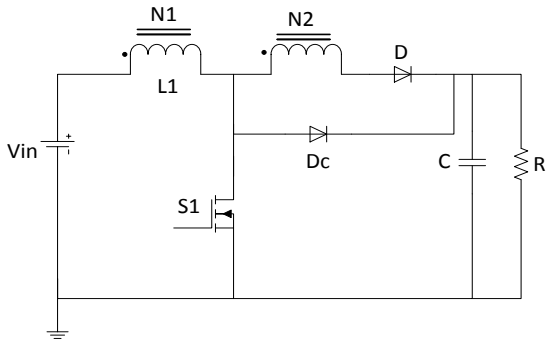

Figure 1.1 Parallel diode clamped coupled inductor boost converter [14]

The voltage stress across switch in this topology is same as the output voltage which is a major disadvantage for applications involving high voltage gain. Figure 1.2 shows another topology based on winding-coupled inductor.

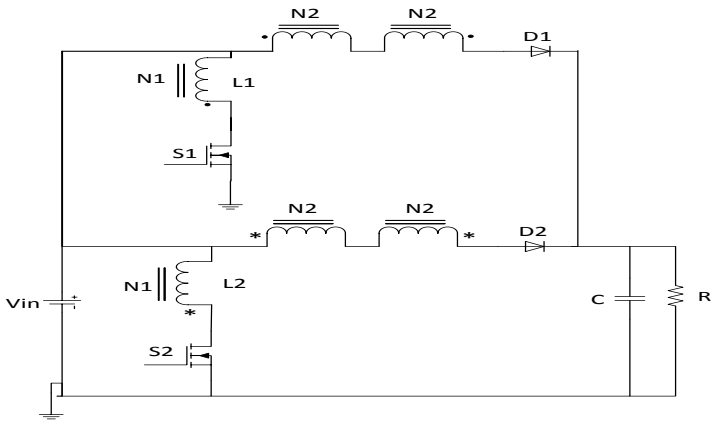

Figure 1.2 Boost converter with winding-coupled inductor [15]

Topology shown in Figure 1.2 consists of a coupled inductor based interleaved boost converter with three windings on the coupled inductors. The voltage transfer ratio of this topology is $\frac{V_o}{V_{in}} = \frac{N}{1-D}$, where N – is the secondary to primary turns ratio of coupled inductor, D- is the duty ratio of switches. Because of interleaving of two boost converters, the input current in this topology is smooth and voltage stress across switches is $\frac{V_o}{N}$. High-gain DC-DC converters can also be designed by adding voltage lift cells to a basic boost converter to achieve high output voltage. By using an elementary Luo converter [16] and connecting two such cells in series a higher voltage transfer ratio can be achieved. A two-cells in series circuit is shown in Figure 1.3.

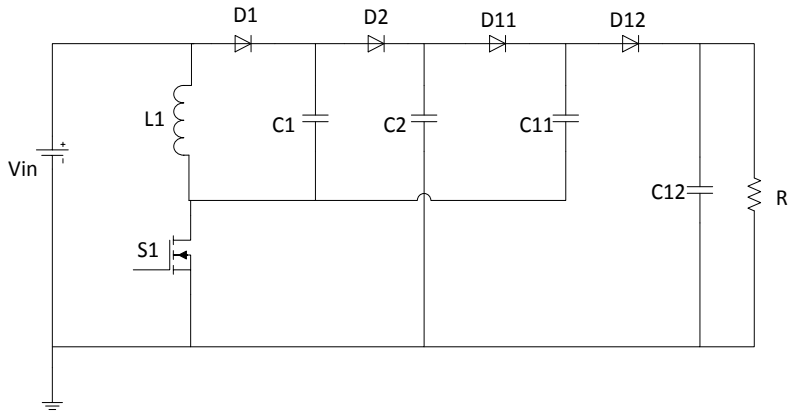

Figure 1.3 Elementary additional circuit

The principle of operation of this topology is charging capacitors in parallel and discharging them in series to achieve a higher voltage gain at the output. The voltage transfer ratio is $\frac{V_o}{V_{in}} = \frac{3-D}{1-D}$. As there are lot of capacitors and diodes being used in this topology, it results in high cost and low efficiency. Another similar topology based on voltage lift cell is as depicted in Figure 1.4 [17]. The voltage transfer ratio of this topology is $\frac{V_o}{V_{in}} = \frac{1+D}{1-D}$.

One topology of interest based on voltage lift cell is as shown in Figure 1.5 [18]. In this, a voltage multiplier cell used in AC voltage lift applications is introduced. Small L_r in the multiplier cell helps in zero current switching (ZCS) of the diodes. The voltage transfer ratio of this topology is $\frac{V_o}{V_{in}} = \frac{1+M}{1-D}$, where M represents number of voltage multiplier cells. The efficiency of this topology is good according to [18]. But the efficiency is not good for high voltage applications. Other methods used to achieve a high voltage gain are based on a coupled inductor based boost converter interleaving which is reported in [19].

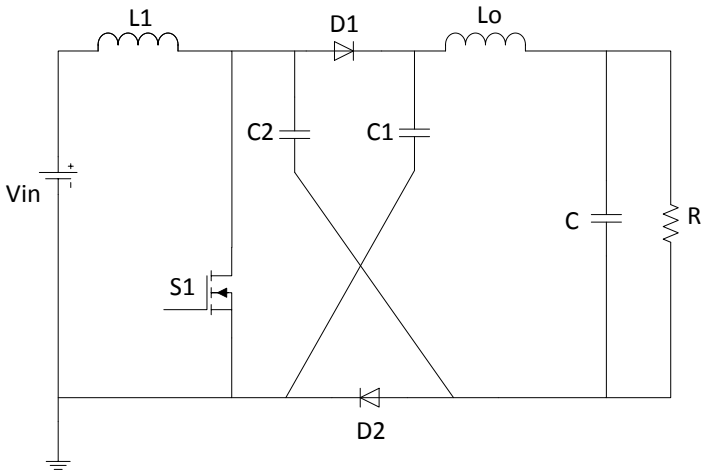

Figure 1.4 Hybrid Step up converter switching structure

Figure 1.6 shows another edition of voltage multipliers for boost converters. This topology has an interleaved coupled inductor based boost converter on the front end and a capacitor diode multiplier cell on rear end which is charged and discharged to achieve high voltage gain at the output. Voltage gain of this topology is $\frac{V_o}{V_{in}} = \frac{2N+1}{1-D}$, where N is the secondary to primary turns ratio of the coupled inductor and D is the duty ratio of the switches. The voltage stress across switches in this topology is very less $\frac{V_{in}}{1-D}$. This topology has a high potential for applications involving high voltage gain.

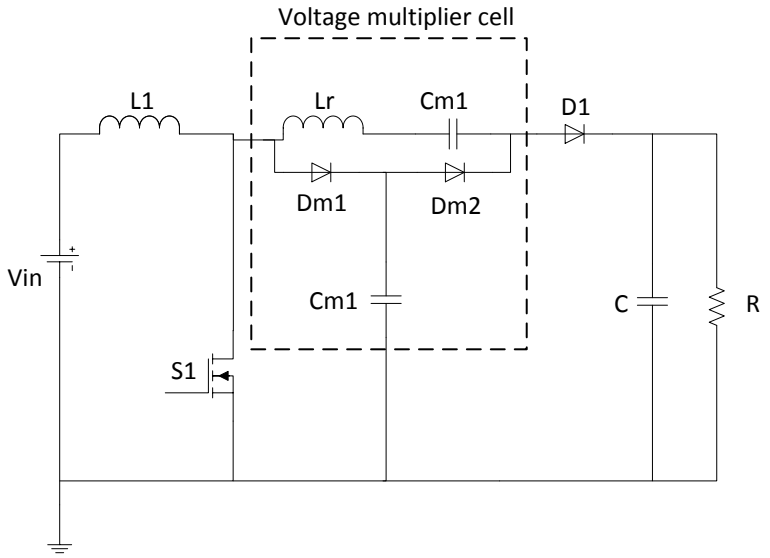

Figure 1.5 Boost converter with voltage multiplier cell

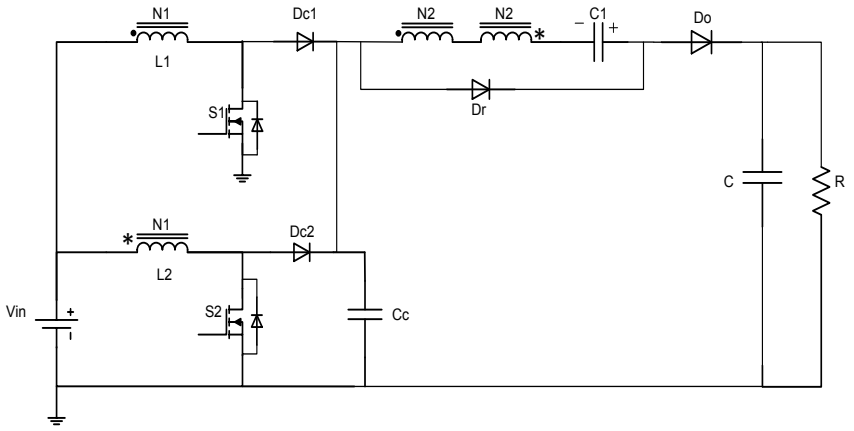

Figure 1.6 Interleaved boost converter with voltage multiplier cell

The schematic of an interleaved coupled inductor boost converter [4] is as shown in Figure 1.7. The voltage gain for this topology is $\frac{V_o}{V_i} = \frac{N+1}{1-D}$. Because of interleaving of two boost converters, input current of this topology is continuous. The voltage stress

across switches is $\frac{V_{in}}{1-D}$. The coupled inductor secondary windings on the rear end produce a voltage boost on the output side.

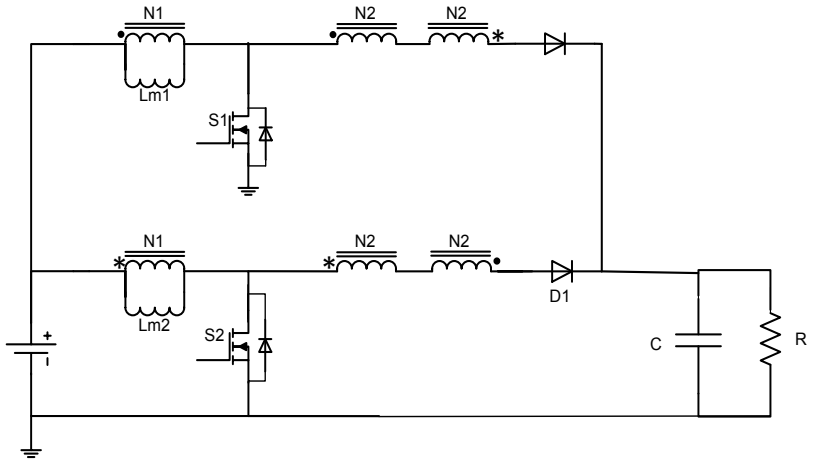

Figure 1.7 Interleaved coupled inductor boost converter

An interleaved boost converter with intrinsic voltage-doubler characteristic [20] topology works on the principle of charging and discharging capacitor C1 as one of the switches is always ON over a switching cycle. There is a 180 degrees phase displacement between the pulses given to active switches. This creates a doubling effect of boost converter output voltage in the system. The voltage gain is of this topology is $\frac{V_o}{V_i} = \frac{2}{1-D}$. This voltage gain of the converter is not suitable for high voltage gain applications. The schematic of this topology is as shown in Figure 1.8.

The focus of application in this thesis is integration of solar energy to a 400V DC microgrid. In this regard, two new topologies were proposed based on a coupled inductor based interleaved boost converter concept. These topologies have higher voltage gain, continuous input current and less voltage stress across switches when compared to other topologies in existing literature as discussed above.

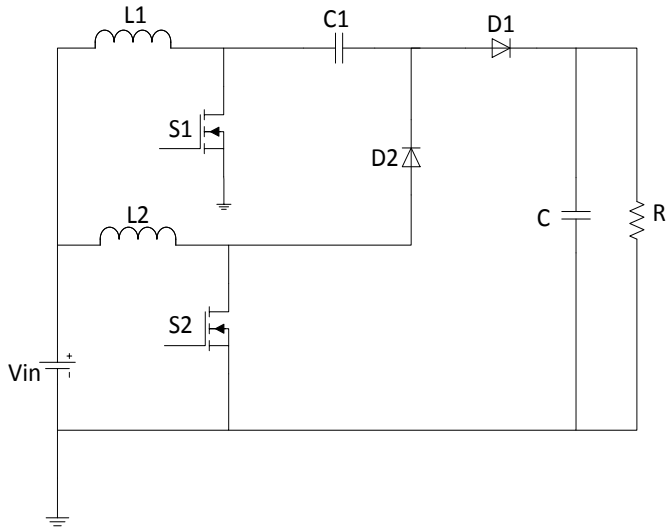

Figure 1.8 Interleaved boost converter with intrinsic voltage-doubler characteristics

Because of these features, they are the best topologies that can be used in the focus of application being discussed in this thesis. So, this thesis performs analysis and comparison of these two proposed topologies.

1.3. INTERLEAVED COUPLED INDUCTOR BASED BOOST CONVERTER WITH TWO SECONDARY WINDINGS (TOPOLOGY 1)

Figure 1.9 is an interleaved coupled inductor based boost converter with a multiplier cell. It basically consists of an interleaved boost converter at the front end that boosts up the input voltage with a gain $\left(\frac{1}{(1-D)}\right)$ and coupled inductor secondary windings that are connected in series with a capacitor. This capacitor is used to charge and discharge every switching cycle to boost up the interleaved boost converter output further. The other basic principle in switching pattern is that the pulses to switches S1 and S2 has a phase difference of 180 degrees. The voltage transfer ratio of this topology is $V_{out} = \left(\frac{3N+2}{1-D}\right) \times V_{in}$, where N is the turns ratio of coupled inductors. The operating

modes, component's stress, simulation and hardware results are discussed in the latter part of the thesis.

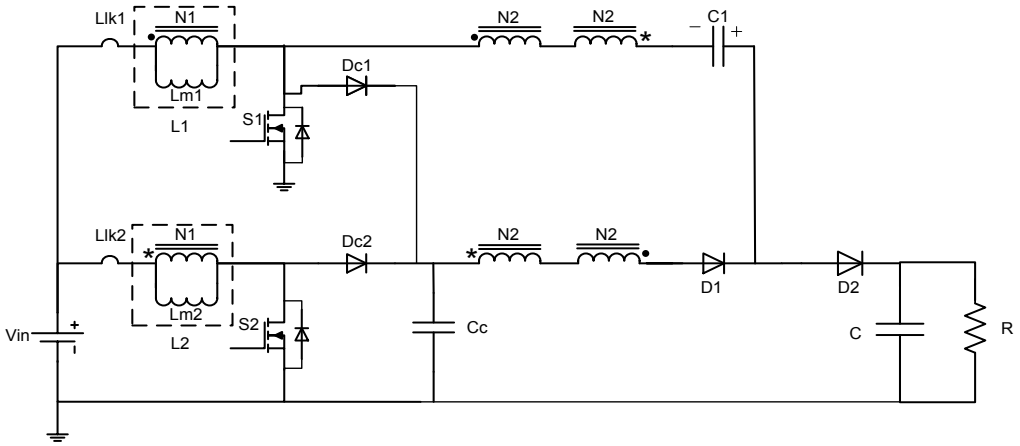

Figure 1.9. Schematic diagram of topology1

1.4. INTERLEAVED COUPLED INDUCTOR BASED BOOST CONVERTER WITH ONE SECONDARY WINDING (TOPOLOGY 2)

The schematic of topology 2 is almost similar to that of topology 1 except that the coupled inductors have only one secondary winding. Even operating principle of this topology is the same as topology 1 but the transfer ratio of this is less when compared to topology 1 for a particular duty cycle. The voltage transfer ratio of this topology is $V_{out} = \left(\frac{2N+2}{1-D}\right) \times V_{in}$, where N is the turns ratio of coupled inductor. Figure 1.10 shows the schematic of topology 2.

In Figures 1.9 and 1.10, a body diode of the MOSFET is shown but it will not be shown in future schematics as there is no participation of this diode in operating modes of the circuit.

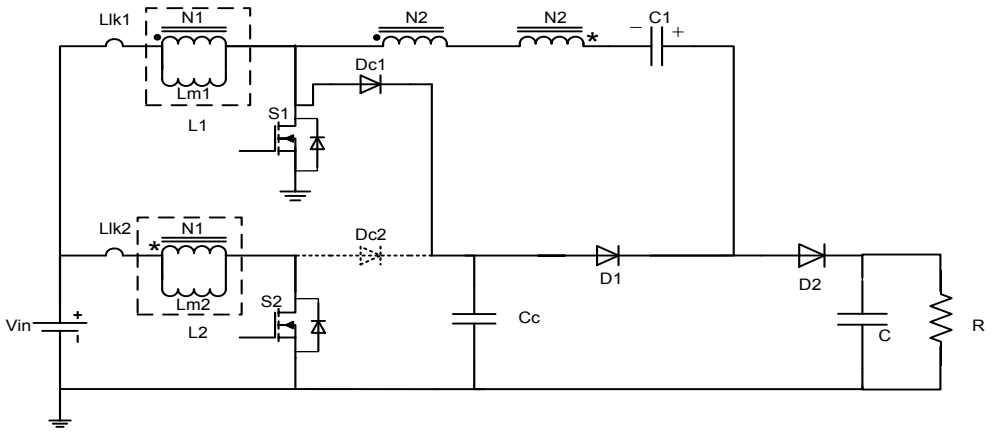

Figure 1.10. Schematic diagram of topology 2

1.5. OPERATING MODES

1.5.1. Operating modes of Topology 1. The basic operating modes are explained in this section for topology 1. The other operating modes includes only the transient dissipation of leakage energy in to the clamp circuit. The clamp circuit consists of D_{C1}, D_{C2} , C_c components

Mode 1

In this mode, both switches S_1 and S_2 are ON, this charges inductors L_1 and L_2 respectively. This is similar to the boost converter operation when switch is ON. During this mode, the load is supplied by the output capacitor. Figure 1.11 shows the circuit operation in Mode 1.

Mode 2

This mode starts when switch S_1 is turned OFF while S_2 remains ON. The current through L_2 keeps increasing but the current through L_1 starts decreasing and charges the output capacitor through C_1 and D_2. Figure 1.12 shows the circuit operation in Mode 2.

Mode 3

This mode starts when switch S_1 is ON and S_2 is OFF. During this mode, inductor L_1 charges and L_2 discharges to charge capacitor C_1 through lower and upper secondary windings of coupled inductor. Figure 1.13 shows the circuit operation in Mode 3.

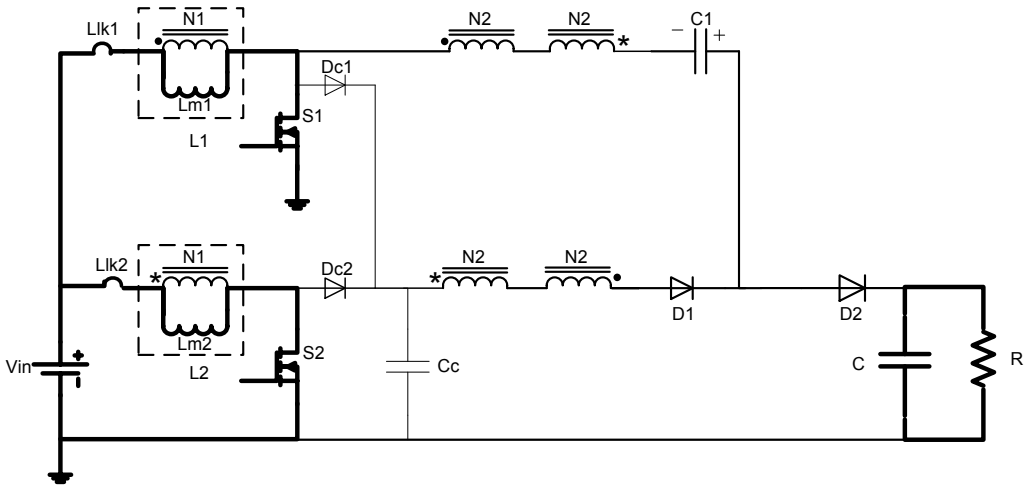

Figure 1.11. Topology 1 operating mode 1

1.5.2. Operating Modes of topology 2. Mode 1.This mode is similar to mode 1 of topology 1, both inductors L_1 & L_2 are charged through S_1, S_2 respectively. Figure 1.14 shows the circuit operation in Mode 1.

Mode 2

In this mode, S_1 is OFF and S_2 is ON. The current through inductor L_2 increases and the current through L_1 discharges through C_1 and diode D_2 to charge the output capacitor. The stored energy in inductor L_1 and capacitor C_1 is used to boost up the output voltage. Figure 1.15 shows the circuit operation in Mode 2. Capacitor C_c is charged through input source through D_{c1}.

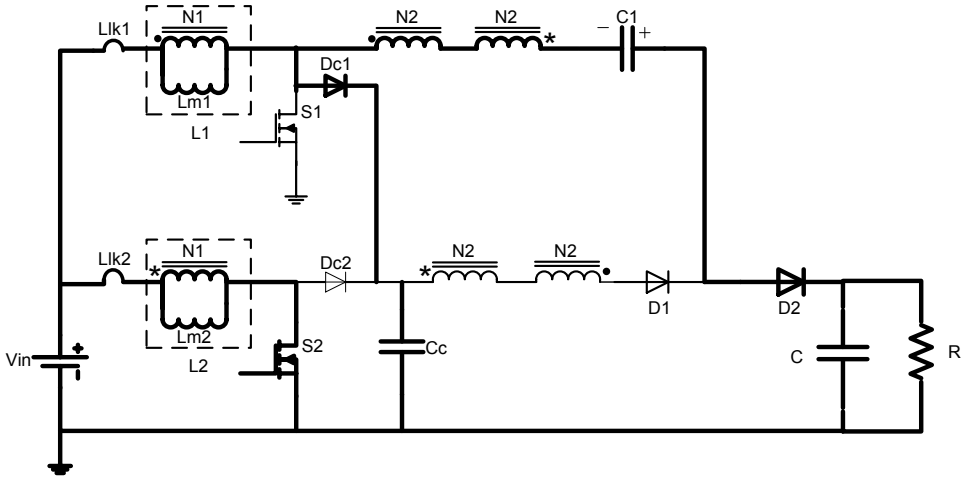

Figure 1.12. Topology 1 operating mode 2

Mode 3

This mode starts when S_1 is ON & S_2 is OFF. In this mode, capacitor C_c discharges through the darkened path and charges capacitor C_1. During the same, the load is supplied by the output capacitor. Figure 1.16 shows the circuit operation in Mode 3.

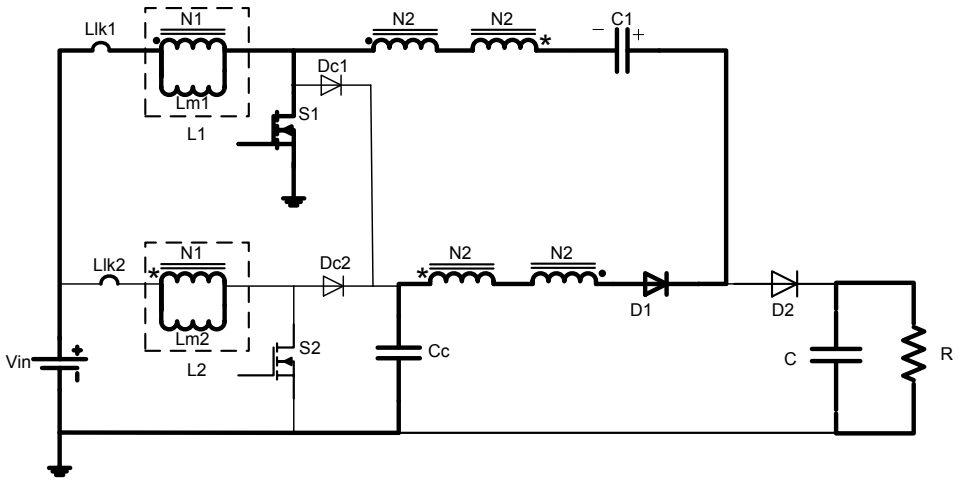

Figure 1.13. Topology 1 operating mode 3

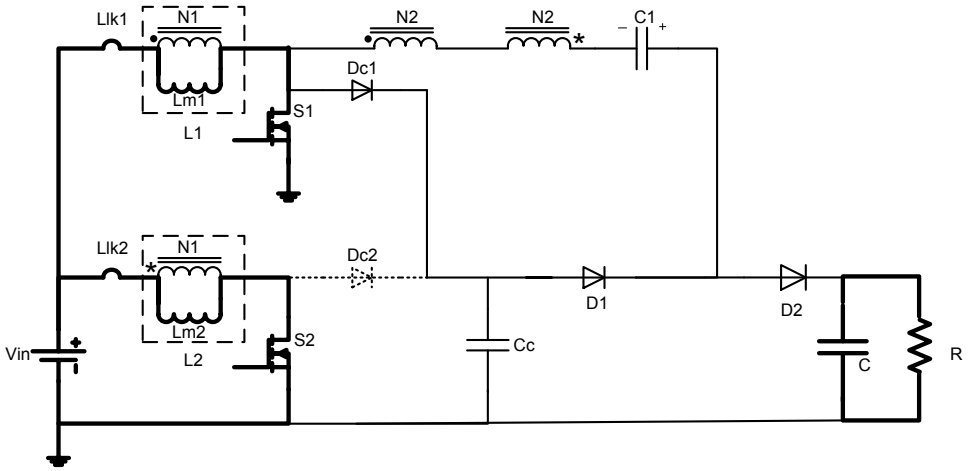

Figure 1.14. Topology 2 operating mode 1

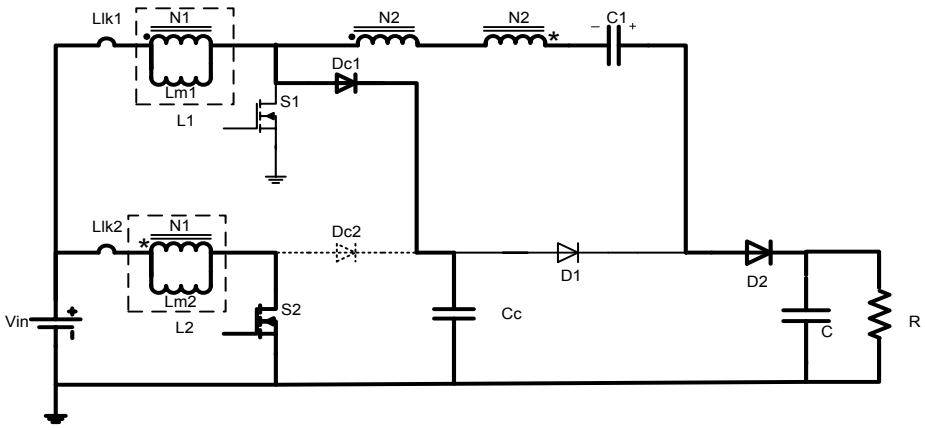

Figure 1.15. Topology 2 operating mode 2

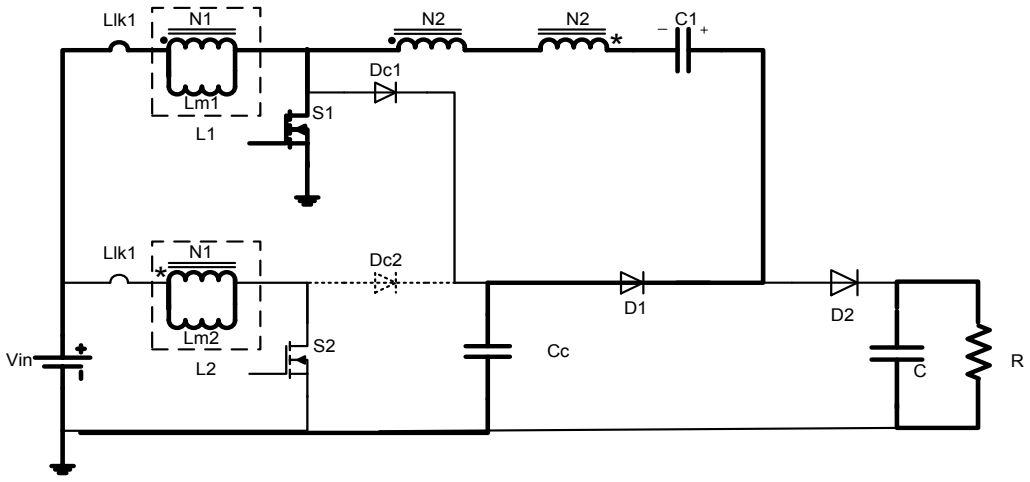

Figure 1.16. Topology 2 operating mode 3

2. COMPONENT'S STRESS IN TOPOLOGIES 1 & 2

2.1. THEORETICAL ANALYSIS

For theoretical analysis of components stress, the analysis is carried out on topology 1 as both the topologies are almost similar except that in topology 2, there is only one secondary winding for coupled inductors. While deducing the equations for topology 2 from topology 1 the windings from C_c to anode of diode D_1 are considered not to exist. Figure 2.1 shows the schematic of topology 1.

2.2. VOLTAGE STRESS OF COMPONENTS IN TOPOLOGY 1

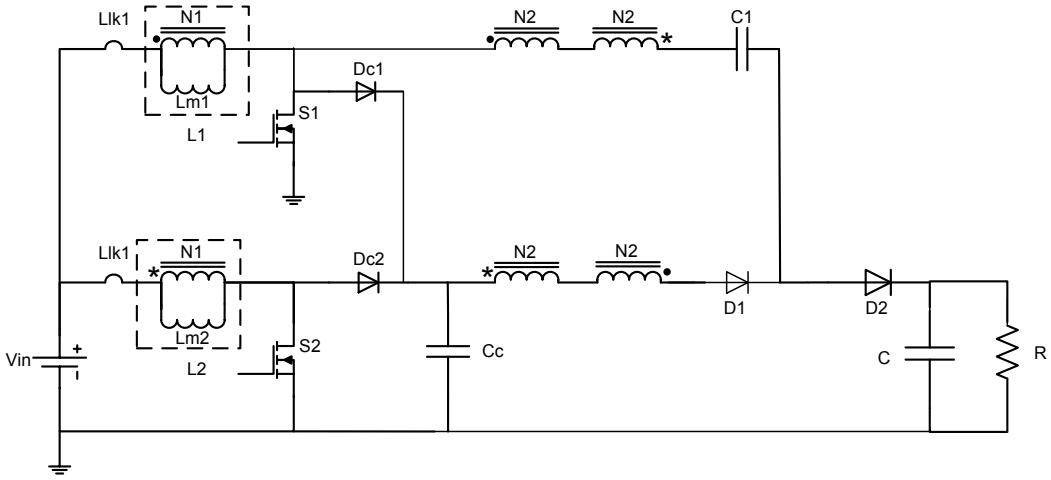

Figure 2.1. Schematic diagram of topology1

Topology above has various components as show in the circuit diagram. In designing a power converter sizing of components is one of the main requirements which require components stress in selecting the optimal device. The stress across components can be found by analysis of topology during various modes of operation.

2.2.1. Voltage Across Capacitor C_1 : The voltage across C_1 can be analyzed by using mode 3 of topology. Figure 2.2 shows the operation of topology 1 in mode 3.

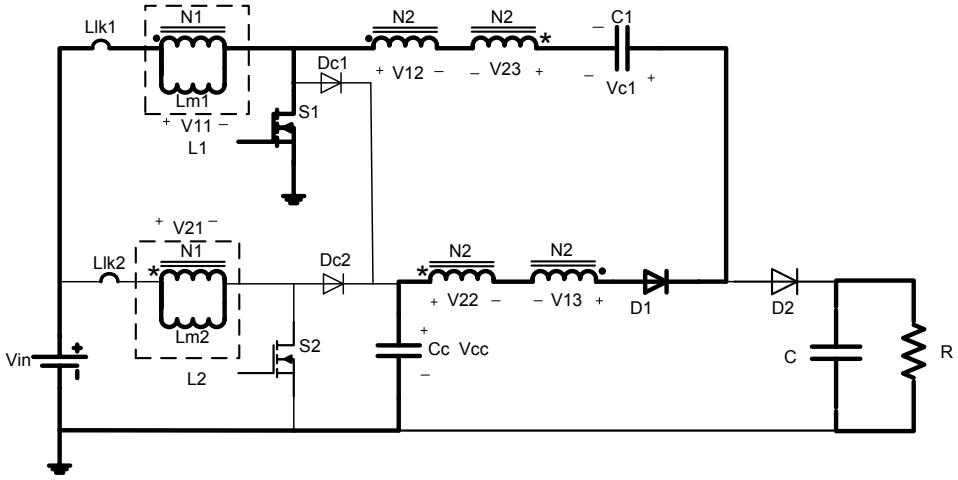

Figure 2.2. Topology 1 operating mode 3

In the above loop, by applying KVL ,

$$V_{c1} = V_{cc} - V_{22} + V_{13} - V_{23} + V_{12} \tag{2.1}$$

$V_{cc} = \left(\frac{V_{in}}{1-D} \right)$, as it is the output of a interleaved boost converter

$$\begin{aligned} V_{23} = V_{22} &= N \times (V_{in} - V_{cc}), N = \frac{N_2}{N_1} \\ &= N \times \left(V_{in} - \frac{V_{in}}{(1-D)} \right) \end{aligned} \tag{2.2}$$

Voltage across the top inductor with dotted representation in the circuit is V_{in} as inductor L_1 is charging.

$$V_{12} = V_{13} = N \times V_{in} \tag{2.3}$$

Substituting equations (2.2) and (2.3) in (2.1),

$$V_{c1} = \left(\frac{V_{in}}{1-D}\right) - N \times \left(V_{in} - \left(\frac{V_{in}}{1-D}\right)\right) + (N \times V_{in}) - N \times \left(V_{in} - \left(\frac{V_{in}}{1-D}\right)\right) + N \times V_{in}$$

$$= 2 \times N \times \left(\frac{V_{in}}{1-D}\right) + \left(\frac{V_{in}}{1-D}\right)$$

$$V_{c1} = \left(\frac{(2N+1) \times V_{in}}{1-D}\right)$$

$$V_{c1} = \left(\frac{V_{in}}{1-D}\right) - N \times \left(V_{in} - \frac{V_{in}}{1-D}\right) + (N \times V_{in}) - N \times \left(V_{in} - \frac{V_{in}}{1-D}\right) + N \times V_{in}$$

$$= 2 \times N \times \left(\frac{V_{in}}{1-D}\right) + \left(\frac{V_{in}}{1-D}\right)$$

$$V_{c1} = \left(\frac{(2N+1)V_{in}}{1-D}\right) \quad (2.4)$$

2.2.2. Voltage Across Capacitor C. The voltage across C can be analyzed by using mode 2 of topology 1. This is also the voltage transfer ratio of the converter. Figure 2.3 shows the operation of topology 1 in mode 2.

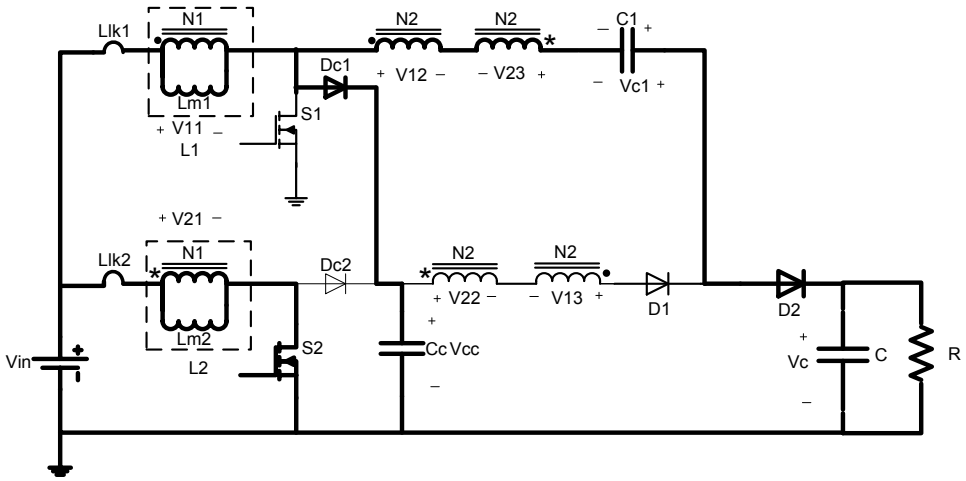

Figure 2.3. Topology 1 operating mode 2

Applying KVL in the above loop,

$$V_c = V_{cc} - V_{12} + V_{23} + V_{c1}$$

$$V_{cc} = \frac{V_{in}}{1-D}$$

$$V_{23} = N \times V_{in}, N = \frac{N2}{N1}$$

$$V_{12} = N \times \left(V_{in} - \frac{V_{in}}{1-D} \right)$$

Substituting above values and (2.4),

$$V_c = \left(\frac{V_{in}}{1-D} \right) - N \times \left(V_{in} - \frac{V_{in}}{1-D} \right) + N \times V_{in} + \left(\frac{2N+1}{1-D} \right) \times V_{in}$$

$$V_c = \left(\frac{3N+2}{1-D} \right) \times V_{in}$$

Hence, the gain or transfer ratio of the converter is $V_c = \left(\frac{3N+2}{1-D} \right) \times V_{in}$

2.2.3. Voltage Across MOSFET. The voltage across switches when they are OFF will be equal to the boost converter output voltage, i.e., $\left(\frac{V_{in}}{1-D} \right)$.

2.2.4. Voltage Across Diode D2. The voltage across diode D2 is maximum in operation mode 3. The voltage stress can be analyzed from Figure 2.4 which shows the operation of topology 1 in mode 3.

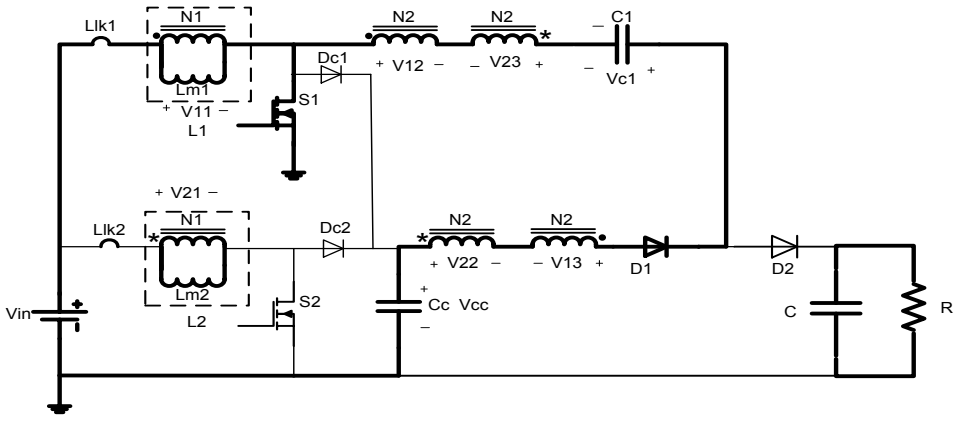

Figure 2.4. Topology 1 operating mode 3

V_{d2} = (Voltage at the node where C1, D1 are connected – output voltage)

$$V_{d2} = (V_{c1} + V_{23} - V_{12}) - Vc$$

$$= \left(\frac{(2N+1)\times V_{in}}{1-D}\right) + N\times\left(V_{in} - \frac{V_{in}}{1-D}\right) - N\times V_{in} - \left(\frac{(3N+2)\times V_{in}}{1-D}\right)$$

$$= -\left(\frac{(2N+1)\times V_{in}}{1-D}\right)$$

2.2.5. Voltage Across Diode D1 . Diode D1 experiences maximum stress in mode 2. The analysis in mode 2 is as shown in Figure 2.5.

$$V_{d1} = (V_{22} - V_{13} - V_{cc}) - V_c$$

$$V_{d1} = (V_{22} - V_{13} - V_{cc}) - V_c$$

$$= N\times V_{in} - N\times\left(V_{in} - \frac{V_{in}}{1-D}\right) - \left(\frac{V_{in}}{1-D}\right) - \left(\frac{(3N+2)\times V_{in}}{1-D}\right)$$

$$= -\left(\frac{(4N+1)\times V_{in}}{1-D}\right)$$

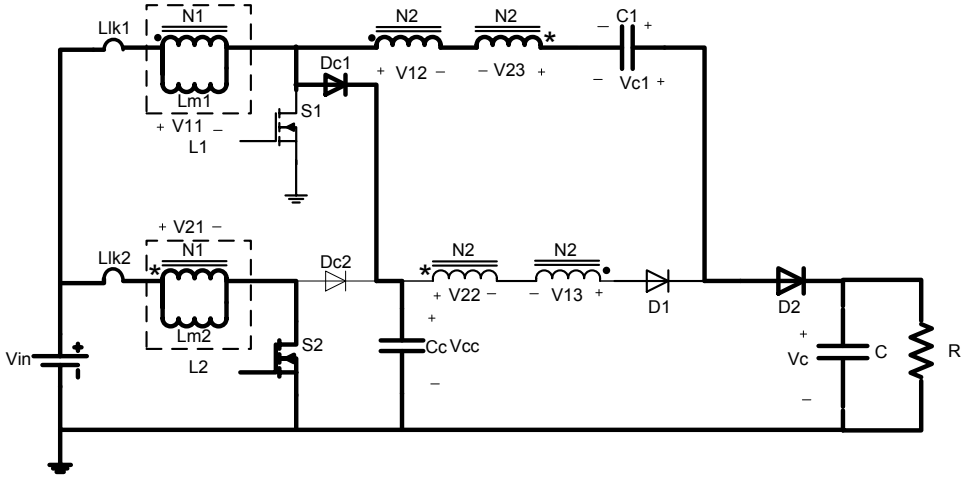

Figure 2.5. Topology 1 operating mode 2

2.3. VOLTAGE STRESS OF COMPONENTS IN TOPOLOGY 2

Topology 2 is almost similar to topology 1 in analysis. The following section shows the derivation of the voltage stress for various components in the circuit.

2.3.1. Voltage Across Capacitor C1. The voltage across capacitor C1 can be analyzed from mode 3 operation of topology 2 as shown in Figure 2.6.

In the below loop, by applying KVL ,

$V_{c1} = V_{cc} - V_{22} + V_{12}$

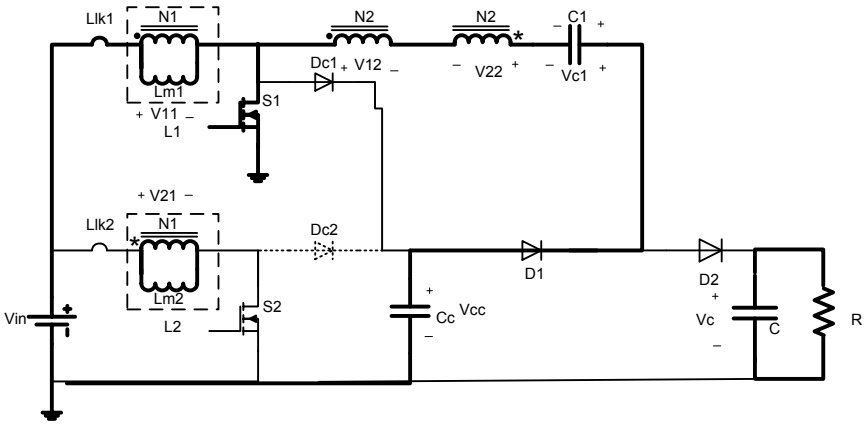

Figure 2.6. Topology 2 operating mode 3

$V_{cc} = \left(\frac{V_{in}}{1-D} \right)$, as it is the output of a interleaved boost converter

$$V_{22} = N \times (V_{in} - V_{cc}), N = \left(\frac{N_2}{N_1} \right) = N \times \left(V_{in} - \frac{V_{in}}{1-D} \right)$$

$$V_{12} = N \times V_{in}$$

Substituting the above values in equation

$$V_{c1} = \left(\frac{V_{in}}{1-D} \right) - N \times \left(V_{in} - \frac{V_{in}}{1-D} \right) + N \times V_{in}$$

$$= \left(\frac{(N+1) \times V_{in}}{1-D} \right)$$

2.3.2. Voltage Across Capacitor C. Mode 2 of topology 2 is used to analyze voltage across capacitor C as shown in Figure 2.7.

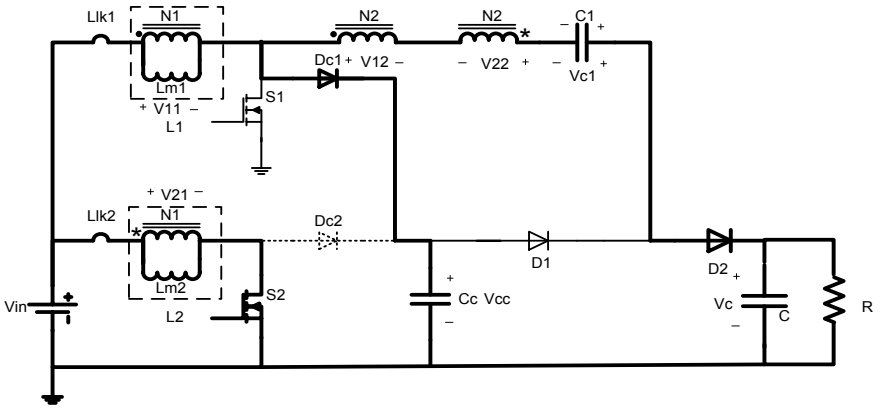

Figure 2.7. Topology 2 operating mode 2

$$V_c = V_{cc} - V_{12} + V_{22} + V_{c1}$$

$$V_{cc} = \left(\frac{V_{in}}{1-D} \right)$$

$$V_{22} = N \times V_{in}, N = \frac{N2}{N1}$$

$$V_{12} = N \times \left(V_{in} - \frac{V_{in}}{1-D} \right)$$

Substituting the above values in equation for Vc,

$$V_c = \left(\frac{V_{in}}{1-D} \right) - N \times \left(V_{in} - \frac{V_{in}}{1-D} \right) + N \times V_{in} + \left(\frac{(N+1) \times V_{in}}{1-D} \right)$$

$$V_c = \left(\frac{(2N+2) \times V_{in}}{1-D} \right)$$

Hence, the gain of topology 2 is $\left(\frac{(2N+2) \times V_{in}}{1-D} \right)$

2.3.3. Voltage Across MOSFET. The voltage across switches when they are OFF will be equal to the boost converter output voltage, i.e., $\left(\frac{V_{in}}{1-D}\right)$.

2.3.4. Voltage Across Diode D2. Mode 3 of topology 2 is used to analyze the voltage across D_2 as shown in Figure 2.8.

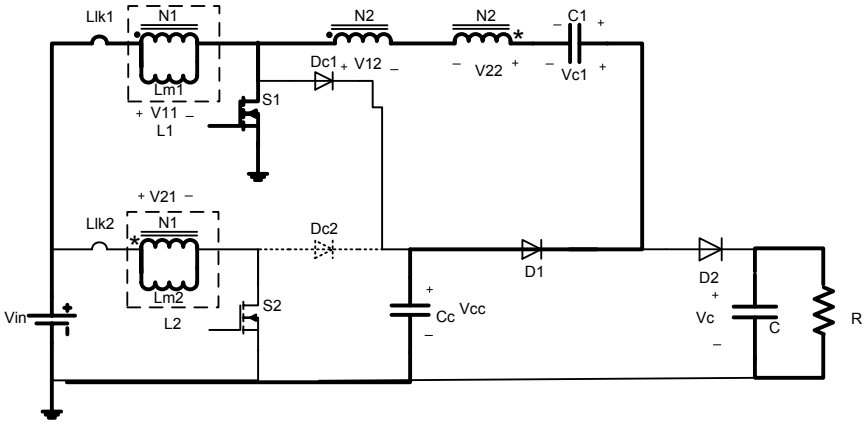

Figure 2.8. Topology 2 operating mode 3

V_{d2} = (Voltage at the node where C_1, D_1 are connected – output voltage)

$$V_{d2} = (V_{c1} + V_{22} - V_{12}) - V_c$$

$$= \left(\frac{(N+1)\times V_{in}}{1-D}\right) + N \times \left(V_{in} - \frac{V_{in}}{1-D}\right) - \left(N \times V_{in} - \frac{(2\times N+2)\times V_{in}}{1-D}\right)$$

$$= -\left(\frac{(2N+1)\times V_{in}}{1-D}\right)$$

2.3.5. Voltage Across Diode D1. Mode 2 of topology 2 is used to analyze voltage across diode D_1 as shown in Figure 2.9.

$$V_{d1} = V_{cc} - V_c$$
$$= \left(\frac{V_{in}}{1-D}\right) - \left(\frac{(2N+2)\times V_{in})}{1-D}\right)$$
$$= -\left(\frac{(2N+1)\times V_{in})}{1-D}\right)$$

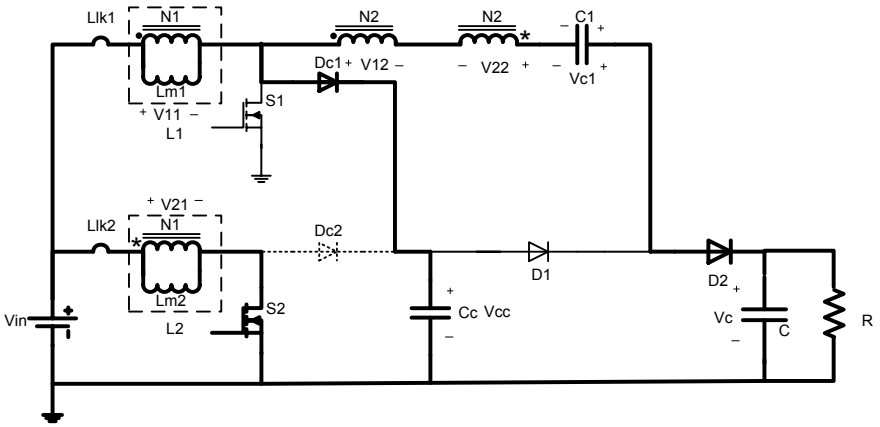

Figure 2.9. Topology 2 operating mode 2

2.4. COMPARISON OF VOLTAGE STRESS IN BOTH TOPOLOGIES 1 AND 2

Based on the analysis shown in before sections, a comparison of voltage stress across various components is tabulated as shown below in Table 2.1.

Table 2.1 Voltage stress comparison

S.No	Component	Voltage Stress	
		Topology 1	Topology 2
1	Capacitor C1	$\left(\frac{(2N+1)\times V_{in}}{1-D}\right)$	$\left(\frac{(N+1)\times V_{in}}{1-D}\right)$

Table 2.1 Voltage stress comparison (Contd.)

2	Output Capacitor C	$\left(\frac{(3N+2)\times V_{in}}{1-D}\right)$	$\left(\frac{(2N+2)\times V_{in}}{1-D}\right)$
3	Switch	$\left(\frac{V_{in}}{1-D}\right)$	$\left(\frac{V_{in}}{1-D}\right)$
4	Diode D1	$\left(\frac{(4N+1)\times V_{in}}{1-D}\right)$	$\left(\frac{(2N+1)\times V_{in}}{1-D}\right)$
5	Diode D2	$\left(\frac{(2N+1)\times V_{in}}{1-D}\right)$	$\left(\frac{(2N+1)\times V_{in}}{1-D}\right)$

2.5. CURRENT STRESS OF COMPONENTS IN TOPOLOGY 1

This section describes some work about current equations of components in topology 1 which is one of the main requirements of component selection. The rms and average current equations are analyzed. In analysis of current equations for both the topologies 1 and 2, it is assumed that there is no leakage inductance (without clamp) and the duty ratios of both the upper and lower switches as the same.

2.5.1. Magnetizing Currents of Inductors. (L_{m1} and L_{m2}) : Mode 3 is used to explain the derivation of these currents. In this mode of operation, when S_1 is ON and S_2 is OFF, the value of the current flowing through I_{lm2} will be $\frac{<I_{d1}>}{(1\text{-}D)}$, because of this current flowing through two secondary windings there is a reflected current of $\left(\frac{2\times N\times I_o}{1-D}\right)$, therefore the average value of inductor 2 magnetizing current is $I_{lm2}=\left(\frac{I_o}{1-D}\right)+\left(\frac{2\times N\times I_o}{1-D}\right)=\left(\frac{2N+1}{1-D}\right)\times I_o$. Based on the power balance equation of the converter, $I_{lm1}+I_{lm2}=\left(\frac{(3N+2)\times I_o}{1-D}\right)$. Hence, $I_{lm1}=\left(\frac{(N+1)\times I_o}{1-D}\right)$.

On assuming $L_1 = L_2 = L$ and $D_1 = D_2 = D$, in operating mode 1, the voltage across inductors L1 and L2 will be V_{in}, hence $\Delta i = \left(\frac{V_{in} \times D}{L \times f_{sw}} \right)$. The rms values of inductor magnetizing currents can be found from the equations as under

$$I_{lm1rms} = \sqrt{I_{lm1}^2 + \frac{\Delta i^2}{12}} \quad , \quad I_{lm2rms} = \sqrt{I_{lm2}^2 + \frac{\Delta i^2}{12}}$$

2.5.2. Inductor Coil Currents. $(L_1 \text{ and } L_2)$ Inductor coil average currents for various periods during the switching cycle is as shown below

$$I_{l1} = \begin{cases} \dfrac{I_{l1\,\min} + \left(\dfrac{(V \times (D - 0.5))}{L \times f_{sw}} \right) + I_{l1\,\min}}{2} & 0 < t < (D - 0.5)T \\ I_{lm1} + \left(\dfrac{(2 \times N \times I_o)}{(1 - D)} \right) & (D - 0.5)T < t < T/2 \\ \dfrac{I_{l1\,\min} + \left(\dfrac{(V \times 0.5)}{L \times f_{sw}} \right) + I_{l1\,\max}}{2} & T/2 < t < DT \\ \dfrac{I_o}{(1 - D)} & DT < t < T \end{cases}$$

$$I_{l2} = \begin{cases} \dfrac{I_{l2\,\min} + \left(\dfrac{(V \times (D - 0.5))}{L \times f_{sw}} \right) + I_{l2\,\min}}{2} & 0 < t < (D - 0.5)T \\ I_{in} - I_o / (1 - D) & (D - 0.5)T < t < T/2 \\ \dfrac{I_{l2\,\min} + \left(\dfrac{(V \times 0.5)}{L \times f_{sw}} \right) + I_{l2\,\max}}{2} & T/2 < t < DT \\ 0 & DT < t < T \end{cases}$$

$$I_{l1} = (2 \times D - 1) \times I_{lm1} + (3 \times N + 2) \times I_o$$

$$I_{l2} = (2 \times D - 1) \times I_{lm2} + (3 \times N + 2) \times I_o$$

The rms values of the above currents can be calculated by applying the rms equation in given periods over a switching period.

2.5.3. Switch Currents. (S_1 and S_2) Switch average currents for various periods during the switching cycle is as shown below

$$I_{s1} = \begin{cases} \dfrac{I_{l1\,\min} + \left(\dfrac{(V \times (D-0.5))}{L \times f_{sw}}\right) + I_{l1\,\min}}{2} & 0 < t < (D-0.5)T \\ I_{in} & (D-0.5)T < t < T/2 \\ \dfrac{I_{l1\,\min} + \left(\dfrac{(V \times 0.5)}{L \times f_{sw}}\right) + I_{l1\,\max}}{2} & T/2 < t < DT \end{cases}$$

$$I_{s2} = \begin{cases} \dfrac{I_{l2\,\min} + \left(\dfrac{(V \times (D-0.5))}{L \times f_{sw}}\right) + I_{l2\,\min}}{2} & 0 < t < (D-0.5)T \\ I_{in} - \dfrac{I_o}{(1-D)} & (D-0.5)T < t < T/2 \\ \dfrac{I_{l2\,\min} + \left(\dfrac{(V \times 0.5)}{L \times f_{sw}}\right) + I_{l2\,\max}}{2} & T/2 < t < DT \end{cases}$$

$$I_{s1} = (2 \times D - 1) \times I_{lm1} + (3 \times N + 1) \times I_o$$

$$I_{s2} = (2 \times D - 1) \times I_{lm2} + (3 \times N + 1) \times I_o$$

The rms values of the above currents can be calculated by applying the rms equation in the given periods over a switching period.

2.5.4. Diode Currents. (D_1 **&** D_2 **)** The average current values of diodes D_1 & D_2 is equal to the load current. From above, the peak value of diode current will be $\frac{I_o}{(1-D)}$, the rms value will be $\frac{I_o}{\sqrt{1-D}}$.

2.5.5. Capacitor C1 Current. Capacitor current is same as diode D_1 & D_2 currents while charging and discharging respectively, as capacitor discharges when diode D_1 conducts and charges when D_2 conducts. The rms can be found as shown below

$$I_{c1rms} = \sqrt{\left(\frac{1}{T}\right)\times((1-D)T)\times\left(\left(\frac{I_o}{(1\text{-}D)}\right)^2+\left(\frac{I_o}{(1\text{-}D)}\right)^2\right)}$$
$$= \sqrt{\frac{2}{(1-D)}}\times I_o$$

2.6. CURRENT STRESS OF COMPONENTS IN TOPOLOGY 2

Similar to the work shown in the above section, this section will describe about various current equations of the components in topology 2.

2.6.1. Magnetizing Currents of Inductors. (L_{m1} and L_{m2}) Mode 3 is used to explain the derivation of these currents**.** In this mode of operation when S_1 is ON and S_2 OFF, the average value of current flowing through I_{lm2} will be $\frac{<I_{d1}>}{(1\text{-}D)}$, because of this current flowing through the secondary winding there is a reflected current of $\left(\frac{N\times I_o}{1-D}\right)$, therefore the average value of inductor 2 magnetizing current is $I_{lm2}=\left(\frac{N\times I_o}{1-D}\right)$. Based on the power balance equation of the converter,

$$I_{lm1}+I_{lm2}=\left(\frac{(2N+2)\times I_o}{1-D}\right)$$

Hence, $I_{lm1}=\left(\frac{(N+2)\times I_o}{1-D}\right)$

On assuming $L_1 = L_2 = L$ and $D_1 = D_2 = D$, in operating mode 1, the voltage across inductors will be V_{in}, hence $\Delta i=\left(\frac{V_{in}\times D}{L\times f_{sw}}\right)$. The rms values of inductor magnetizing currents can be found from the equations as under

$$I_{lm1rms} = \sqrt{I_{lm1}^2+\frac{\Delta i^2}{12}}, \quad I_{lm2rms} = \sqrt{I_{lm2}^2+\frac{\Delta i^2}{12}}$$

2.6.2. Inductor Coil Currents. (L_1 and L_2) Inductor coil average currents for various periods during the switching cycle is as shown below

$$I_{l1}=\begin{cases}\dfrac{I_{l1\,\min}+\left(\dfrac{(V\times(D-0.5))}{L\times f_{sw}}\right)+I_{l1\,\min}}{2} & 0<t<(D-0.5)T\\ I_{lm1}+\left(\dfrac{(2\times N\times I_o)}{(1-D)}\right) & (D-0.5)T<t<T/2\\ \dfrac{I_{l1\,\min}+\left(\dfrac{(V\times 0.5)}{L\times f_{sw}}\right)+I_{l1\,\max}}{2} & T/2<t<DT\\ \dfrac{I_o}{(1-D)} & DT<t<T\end{cases}$$

$$I_{l2}=\begin{cases}\dfrac{I_{l2\,\min}+\left(\dfrac{(V\times(D-0.5))}{L\times f_{sw}}\right)+I_{l2\,\min}}{2} & 0<t<(D-0.5)T\\ I_{in}-I_o/(1-D) & (D-0.5)T<t<T/2\\ \dfrac{I_{l2\,\min}+\left(\dfrac{(V\times 0.5)}{L\times f_{sw}}\right)+I_{l2\,\max}}{2} & T/2<t<DT\\ 0 & DT<t<T\end{cases}$$

$$I_{l1}=(2\times D-1)\times I_{lm1}+(2\times N+3)\times I_o$$

$$I_{l2}=(2\times D-1)\times I_{lm2}+(2\times N\times I_o)$$

The rms values of the above currents can be calculated by applying the rms equation in the given periods over a switching period.

2.6.3. Switch Currents. (S_1 and S_2) Switch average currents for various periods during the switching cycle is as shown below

$$I_{s1}=\begin{cases}\dfrac{I_{l1\,\min}+\left(\dfrac{(V\times(D-0.5))}{L\times f_{sw}}\right)+I_{l1\,\min}}{2} & 0<t<(D-0.5)T\\ I_{in}-\dfrac{I_o}{(1-D)} & (D-0.5)T<t<T/2\\ \dfrac{I_{l1\,\min}+\left(\dfrac{(V\times 0.5)}{L\times f_{sw}}\right)+I_{l1\,\max}}{2} & T/2<t<DT\end{cases}$$

$$I_{s2}=\begin{cases}\dfrac{I_{l2\,\min}+\left(\dfrac{(V\times(D-0.5))}{L\times f_{sw}}\right)+I_{l2\,\min}}{2} & 0<t<(D-0.5)T\\ I_{in}-\dfrac{N\times I_o}{(1-D)} & (D-0.5)T<t<T/2\\ \dfrac{I_{l2\,\min}+\left(\dfrac{(V\times 0.5)}{L\times f_{sw}}\right)+I_{l2\,\max}}{2} & T/2<t<DT\end{cases}$$

$$I_{s1}=(2\times D-1)\times I_{lm1}+(2\times N+3)\times I_o$$

$$I_{s2}=(2\times D-1)\times I_{lm2}+(N+2)\times I_o$$

The rms values of the above currents can be calculated by applying the rms equation in the given periods over a switching period.

2.6.4. Diode Currents. $(D_1 \text{ and } D_2)$ The average current values of diodes D1 & D2 is equal to the load current. From above, the peak value of diode current will be $\frac{I_o}{(1-D)}$, the rms value will be $\frac{I_o}{\sqrt{1-D}}$.

2.6.5. Capacitor C_1 Current. Capacitor current is same as diode D_1 & D_2 currents while charging and discharging respectively, as capacitor discharges when diode D_1 conducts and charges when D_2 conducts. The rms can be found as shown below

$$I_{c1rms}=\sqrt{\left(\frac{1}{T}\right)\times((1-D)T)\times\left(\left(\frac{I_o}{(1-D)}\right)^2+\left(\frac{I_o}{(1-D)}\right)^2\right)}$$

$$=\sqrt{\frac{2}{(1-D)}}\times I_o$$

2.7. COMPARISON OF CURRENT STRESS IN BOTH THE TOPOLOGIES 1 & 2

Based on the analysis shown in before sections, a comparison of current stress across various components is tabulated as shown below in Table 2.2.

Table 2.2 Current stress comparison

S.No	Component	Current Stress	
		Topology 1	Topology 2

Table 2.2 Current stress comparison (Contd.)

1	I_{lm1}	$\left(\frac{(N+1)\times I_o}{1-D}\right)$	$\left(\frac{(N+2)\times I_o}{1-D}\right)$
2	I_{lm2}	$\left(\frac{(2N+1)\times I_o}{1-D}\right)$	$\left(\frac{N\times I_o}{1-D}\right)$
3	I_{s1}	$(2\times D-1)\times I_{lm1}+(3\times N+1)\times I_o$	$(2\times D-1)\times I_{lm1}+(2\times N+3)\times I_o$
4	I_{s2}	$(2\times D-1)\times I_{lm2}+(3\times N+1)\times I_o$	$(2\times D-1)\times I_{lm2}+(N+2)\times I_o$
5	I_{d1}, I_{d2}	I_o	I_o
6	I_{d1rms}, I_{d2rms}	$\frac{I_o}{\sqrt{1-D}}$	$\frac{I_o}{\sqrt{1-D}}$
7	I_{c1rms}	$\sqrt{\frac{2}{(1-D)}}\times I_o$	$\sqrt{\frac{2}{(1-D)}}\times I_o$

2.8. COMPARISON OF SIMULATION RESULTS WITH THEORETICAL ANALYSIS

To validate the theoretically analyzed voltage and current stress equations, a comparison study with simulated values is discussed in this section. The comparison is performed at two different output powers 400W and 200W to focus on derived equations validity for various conditions. The specifications used for output power 400W are as tabulated in Table 2.3. Also Table 2.4, Table 2.5, Table 2.7, and Table 2.8 shows the results of theoretical to simulation results of voltage and current stress of components at 400W and 200W respectively.

Table 2.3 Simulation inputs for output power 400W

	Topology 1	Topology 2
V_{in}	20V	20V
V_{out}	400V	400V
R_{out}	400Ω	400Ω
D	0.75	0.75

Table 2.3 Simulation inputs for output power 400W (Contd.)

f_{sw}	100kHz	100kHz
L	50µH	50µH
N	1	1.5
I_o	1A	1A
I_{in}	20A	20A

Table 2.4 Voltage stress comparison of theoretical to simulation results at 400W

	Voltage Stress (V) Topology1		Voltage Stress (V) Topology2	
	Theoretical	Simulated	Theoretical	Simulated
V_{c1}	240	240	200	199.9
V_{sw_pk}	80	80	80	80
V_{D1_pk}	400	400	320	320
V_{D2_pk}	240	240	320	320
V_o	400	400	400	400

Table 2.5 Current stress comparison of theoretical to simulation results at 400W

	Current Stress (A) Topology1		Current Stress (A) Topology2	
I_{lm1_avg}	8	8	14	13.93
I_{lm2_avg}	12	12	6	6.16

Table 2.5 Current stress comparison of theoretical to simulation results at 400W (Contd.)

I_{lm1rms}	8.05	8.05	14.03	13.95
I_{lm2rms}	12.03	12.03	6.06	6.16
I_{s1_avg}	9	9	13	13
I_{s2_avg}	10	10	6	5.96
I_{s1rms}	11.52	11.52	15.58	15.56
I_{s2rms}	11.68	11.68	7.38	7.4
I_{d1_avg}	1	1	1	1
I_{d2_avg}	1	1	1	1.02
I_{d1rms}	2	2	2	2.02
I_{d2rms}	2	2	2	2.1
I_{c1rms}	2.83	2.84	2.83	2.99
Δi_{l_ripple}	3	3	3	3
I_{l1_avg}	9	9	13	13.98
I_{l2_avg}	11	11	6	5.97
I_{l1rms}	10.03	10.03	14.23	14.65

The specifications for the second iteration i.e. at output power 200W is as shown in Table 2.6.

Table 2.6 Simulation inputs for output power 200W

	Topology 1	Topology 2
V_{in}	20V	20V
V_{out}	400V	400V
R_{out}	800Ω	800Ω
D	0.75	0.75
f_{sw}	100kHz	100kHz
L	50µH	50µH
N	1	1.5
I_o	1A	1A
I_{in}	10A	10A

Table 2.7 Voltage comparison of theoretical to simulation results at 200W

	Voltage Stress (V) Topology1		Voltage Stress (V) Topology2	
	Theoretical	Simulated	Theoretical	Simulated
V_{c1}	240	240	200	199.9
V_{sw_pk}	80	80	80	80
V_{D1_pk}	400	400	320	320
V_{D2_pk}	240	240	320	320
V_o	400	400	400	400

Table 2.8 Current stress comparison of theoretical to simulation results at 200W

	Current Stress (A) Topology1		Current Stress (A) Topology2	
I_{lm1_avg}	4	4	7	6.82
I_{lm2_avg}	6	6	3	2.89
I_{lm1rms}	4.09	4.1	7.05	6.87
I_{lm2rms}	6.06	6.06	3.12	3.03
I_{s1_avg}	4.5	4.5	6.5	6.53
I_{s2_avg}	5	5	3	2.93
I_{s1rms}	5.79	5.8	7.82	7.88
I_{s2rms}	5.87	5.87	3.74	3.68
I_{d1_avg}	0.5	0.5	0.5	0.49
I_{d2_avg}	0.5	0.5	0.5	0.43
I_{d1rms}	1	1	1	1.04
I_{d2rms}	1	1	1	0.98
I_{c1rms}	1.41	1.44	1.41	1.48
Δi_{l_ripple}	3	3	3	3
I_{l1_avg}	4.5	4.5	6.5	7.15
I_{l2_avg}	5.5	5.5	3	2.96
I_{l1rms}	5.05	5.06	7.15	7.5
I_{l2rms}	5.96	5.96	3.74	3.72

2.9. COMPARISON OF SIMULATION TO PRACTICAL WAVEFORMS IN BOTH THE TOPOLOGIES

This section shows various practical and simulated waveforms for both topologies 1 and 2. In order to perform practical testing, a hardware set up was built and various waveforms are captured.

2.9.1. Topology 1. This section shows practical and simulated waveforms for topology 1. The parameters of the hardware prototype to capture practical waveforms are as shown in Table 2.9.1.

Table 2.9.1 Hardware parameters for topology 1

V_{in} (V)	I_{in} (A)	V_o (V)	R_o (Ω)	I_o (A)	P_{in} (W)	P_o (W)	N	f_{sw} (kHz)
20	11.36	400.7	796	0.503	227.2	201.5	1.4	50

In Figure 2.10, each voltage division is 50V and total number of divisions is 8. So, the output voltage is $8 \times 50 = 400V$. Figure 2.10 and Figure 2.11 shows the practical and simulated output voltage waveforms for topology1.

In Figure 2.12, each voltage division is 50V and total number of divisions is around 4.8. So, capacitor C_1 voltage is $5 \times 50 = 250V$. Figure 2.12 and Figure 2.13 shows the practical and simulated voltage of capacitor C_1 for topology 1.

Practical

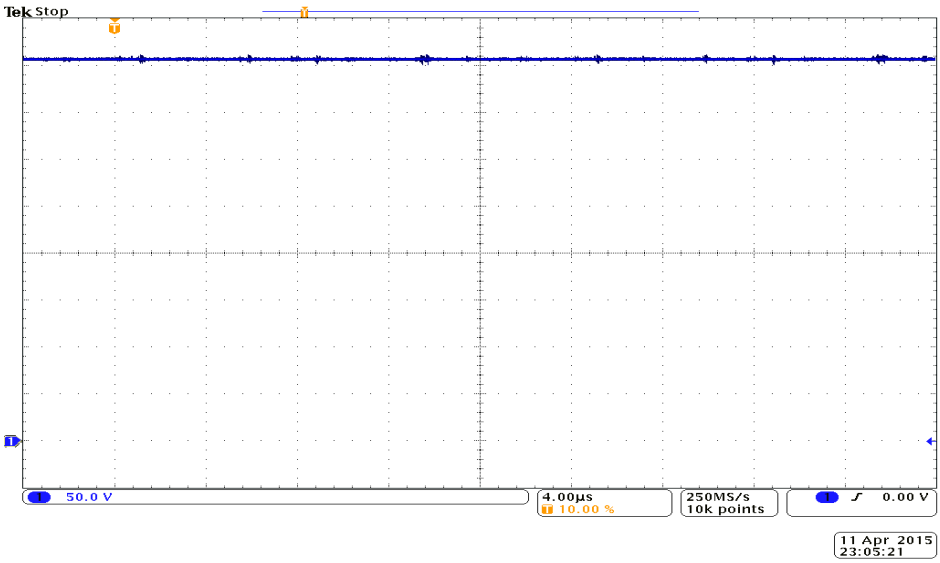

Figure 2.10. Practical waveform of Vout for topology 1

Simulated waveform

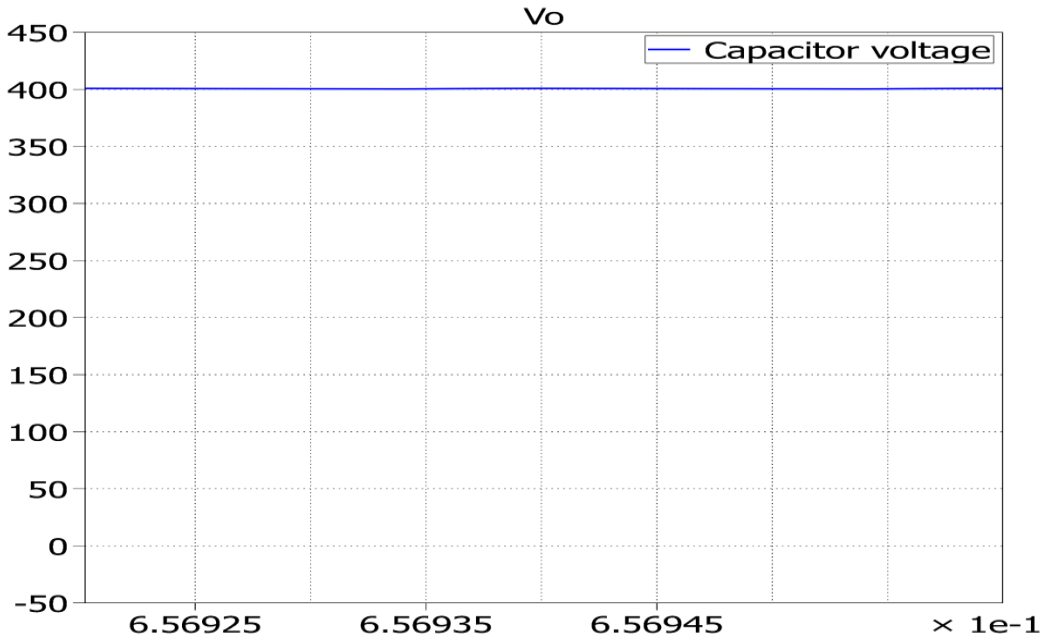

Figure 2.11. Simulated waveform of Vout for topology 1

Practical

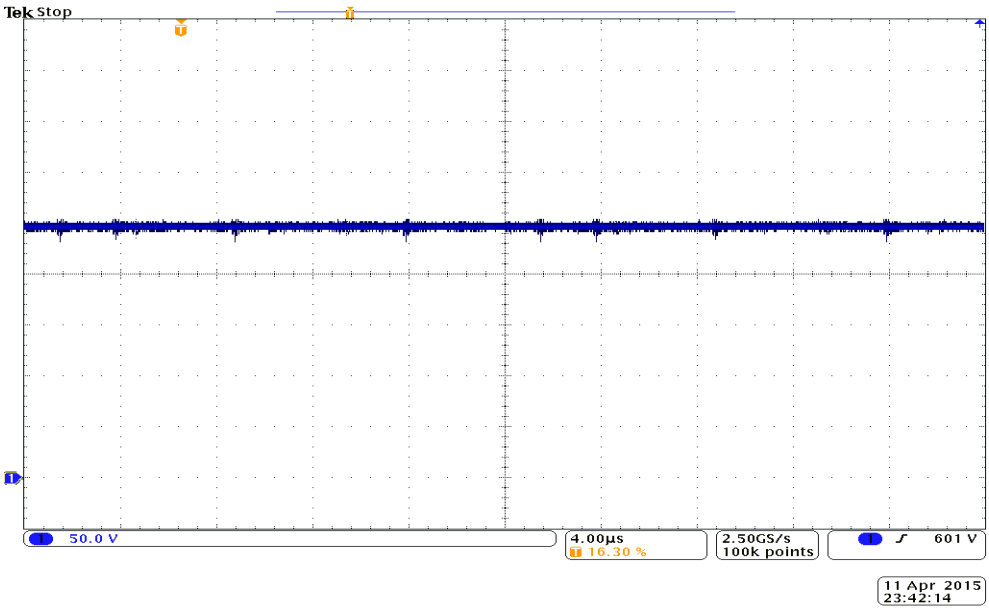

Figure 2.12. Practical waveform of V_{c1} for topology 1

Simulated waveform

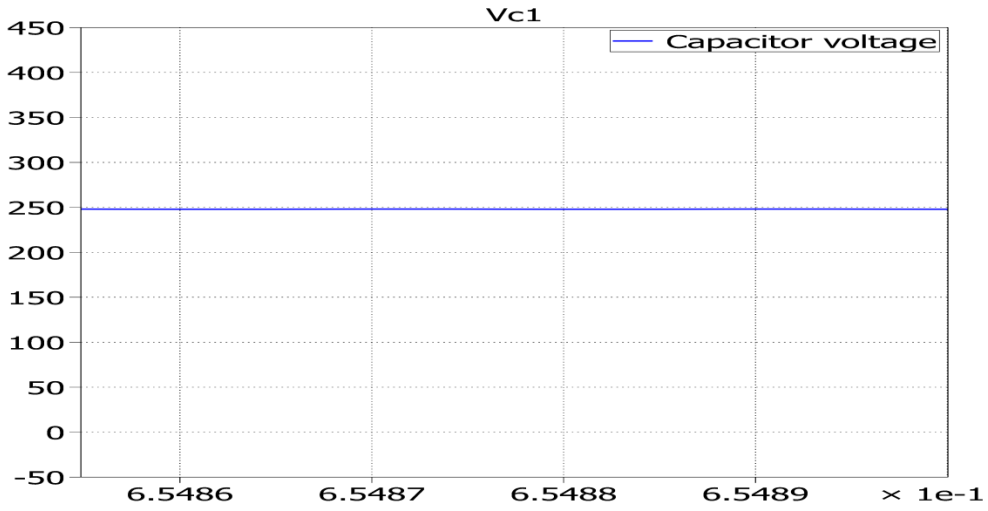

Figure 2.13. Simulated waveform of V_{c1} for topology 1

In Figure 2.14, each voltage division is 10V and total number of divisions is 7.2. So, capacitor C_c voltage is $7.2 \times 10 = 72V$. Figure 2.14 and Figure 2.15 shows the practical and simulated waveforms of voltage across capacitor C_c for topology 1.

Practical

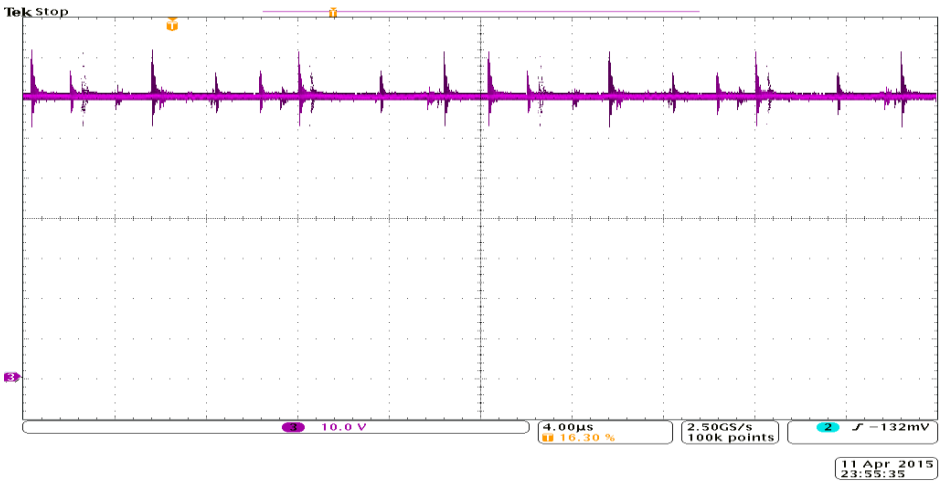

Figure 2.14. Practical waveform of V_{cc} for topology 1

Simulated waveform

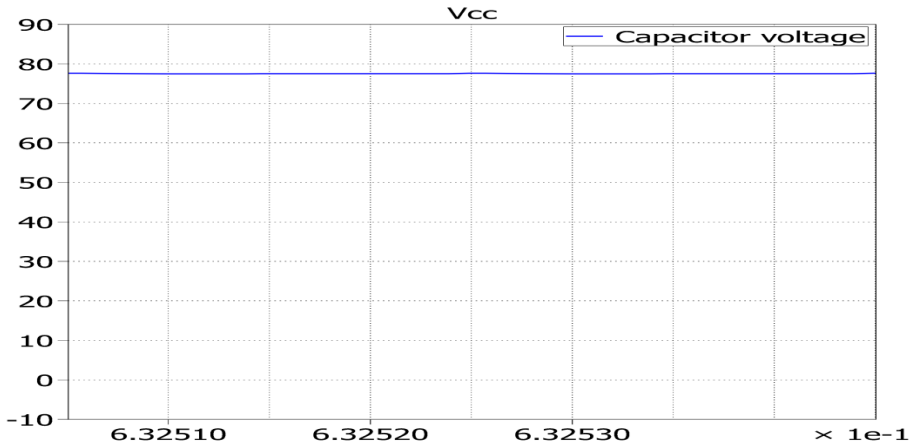

Figure 2.15. Practical waveform of V_{cc} for topology 1

The below waveform across diode D_1 was measured with positive terminal of the probe connected to cathode and negative to anode, hence the waveform above is positive. The ringing in the waveform is because of leakage inductance and parasitics and may also be because of loop inductance while measuring the waveform.

In Figure 2.16, each voltage division is 100V and total number of divisions is 4.5. So, diode D_1 peak voltage is $4.3 \times 100 = 430V$. Figure 2.16 and Figure 2.17 shows the practical and simulated waveforms for voltage across diode D_1 for topology 1.

Practical

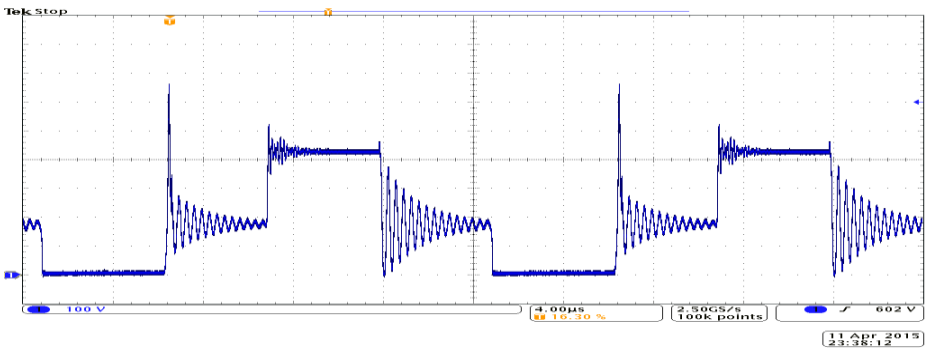

Figure 2.16. Practical waveform of V_{d1} for topology 1

Simulated waveform

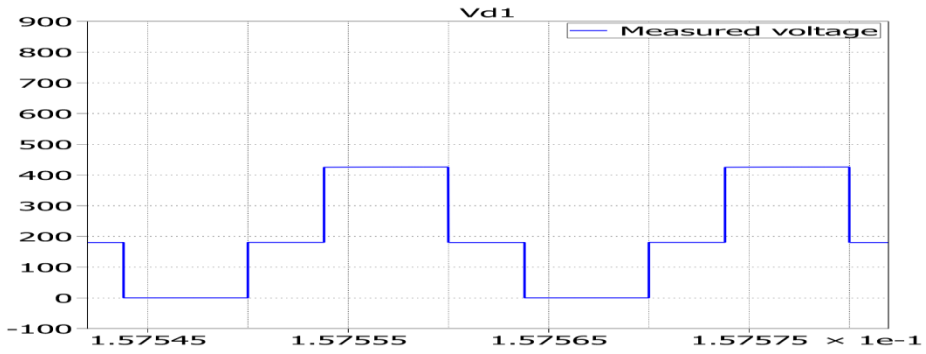

Figure 2.17. Simulated waveform of V_{d1} for topology 1

The below waveform across diode D_2 was measured with positive terminal of the probe connected to cathode and negative to anode, hence the waveform above is positive. The ringing in the waveform is because of leakage inductance and parasitics and may also be because of loop inductance while measuring the waveform.

In Figure 2.18, each voltage division is 50V and total number of divisions is 4.8. So, diode D_2 peak voltage is $4.8 \times 50 = 240V$. Figure 2.18 and Figure 2.19 shows the practical and simulated waveforms for voltage across diode D_2 for topology 1.

Practical

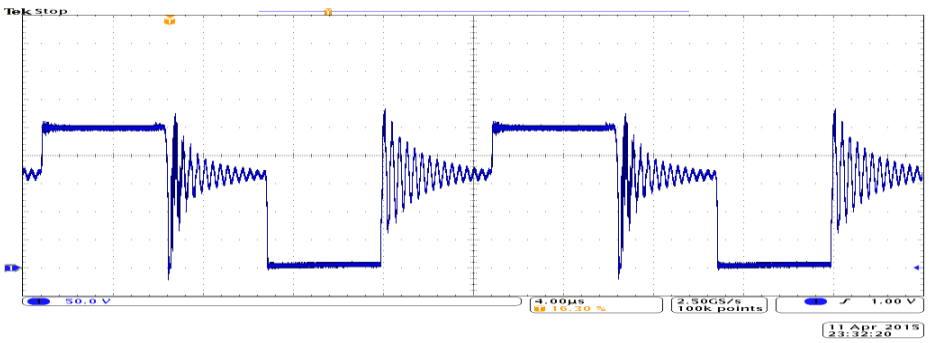

Figure 2.18. Practical waveform of V_{d2} for topology 1

Simulated waveform

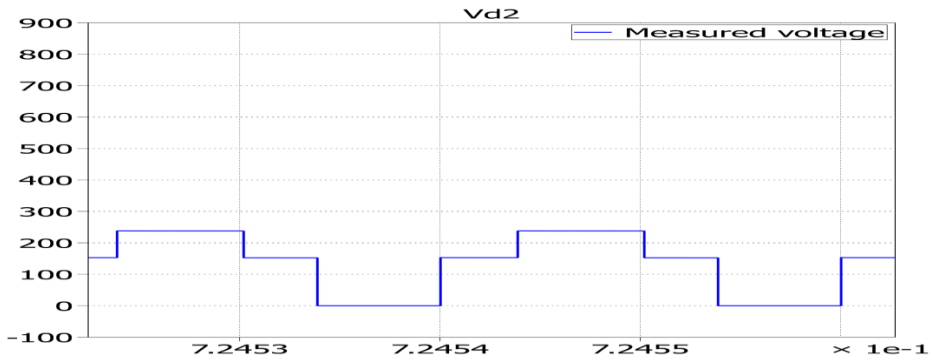

Figure 2.19. Simulated waveform of V_{d2} for topology 1

In Figure 2.20, each voltage division is 20V and total number of divisions is 3.2. So, switch peak voltage is $3.2 \times 20 = 64V$. The voltage spike is because of leakage inductance in the circuit during turn-off of switch. Figure 2.20 and Figure 2.21 shows the practical and simulated waveforms for voltage across switch S_1 for topology 1.

Practical

Figure 2.20. Practical waveform of V_{ds1} for topology 1

Simulated waveform

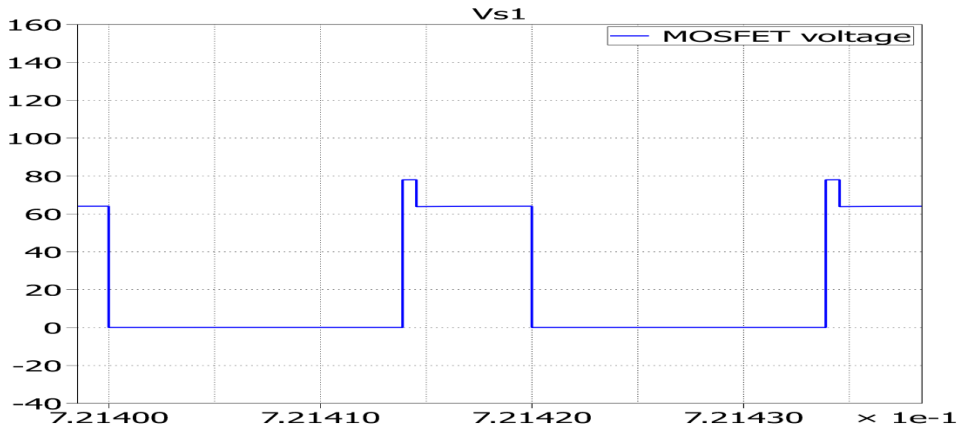

Figure 2.21. Simulated waveform of V_{ds1} for topology 1

In Figure 2.22, each voltage division is 20V and total number of divisions is 3.2. So, switch peak voltage is $3.2 \times 20 = 64V$. The voltage spike is because of leakage inductance in the circuit during turn-off of switch. Figure 2.22 and Figure 2.23 shows the practical and simulated waveforms for voltage across switch S_2 for topology 1.

Practical

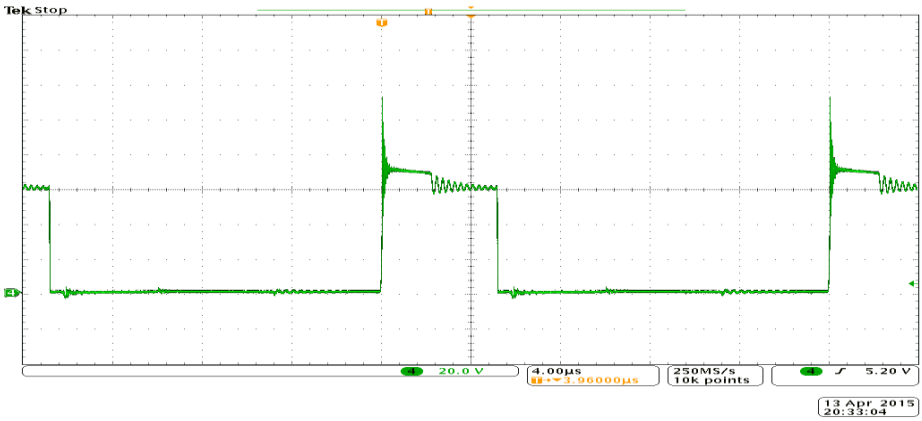

Figure 2.22. Practical waveform of V_{ds2} for topology 1

Simulated waveform

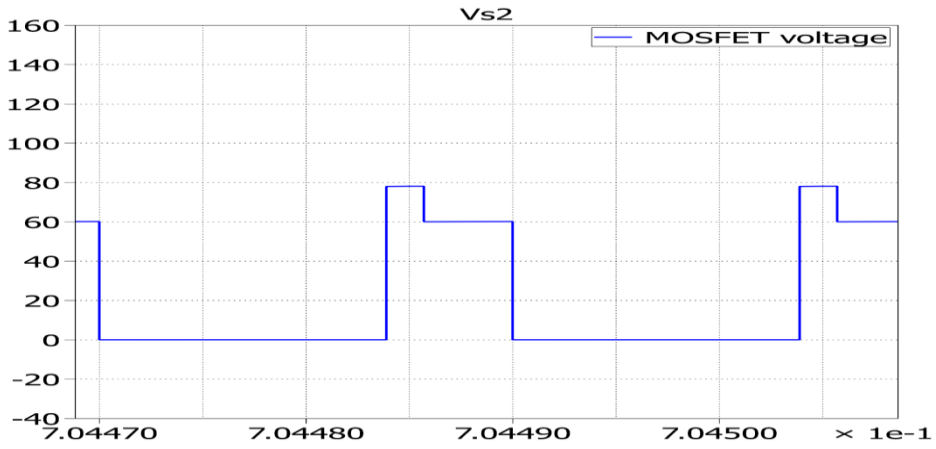

Figure 2.23. Simulated waveform of V_{ds2} for topology 1

In Figure 2.24, each voltage division is 2A and total number of divisions is 6.4. So, peak input current is $7 \times 2 = 14A$. Figure 2.24 and Figure 2.25 shows the practical and simulated waveforms for input current of topology 1.

Practical

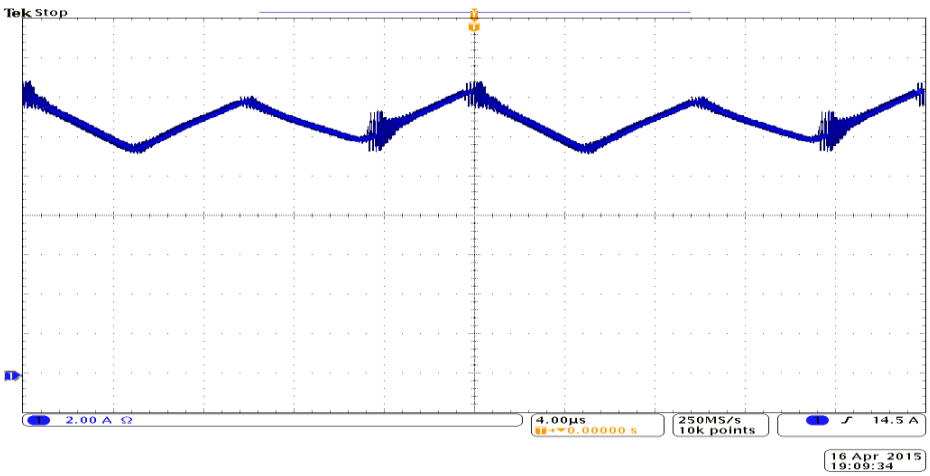

Figure 2.24. Practical waveform of I_{in} for topology 1

Simulated waveform

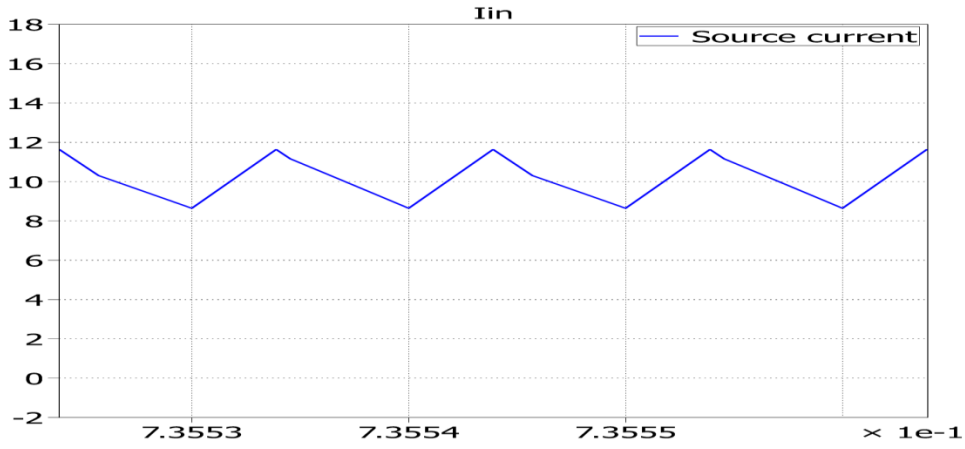

Figure 2.25. Simulated waveform of I_{in} for topology 1

The ringing in the circuit is mainly because of parasitics. In Figure 2.26, each voltage division is 2A and peak of above current is 5.6 divisions. So, L_2 peak primary inductor current is $5.6 \times 2 = 11.2A$. Figure 2.26 and Figure 2.27 shows the practical and simulated waveforms for inductor current I_{L2} of topology 1.

Practical

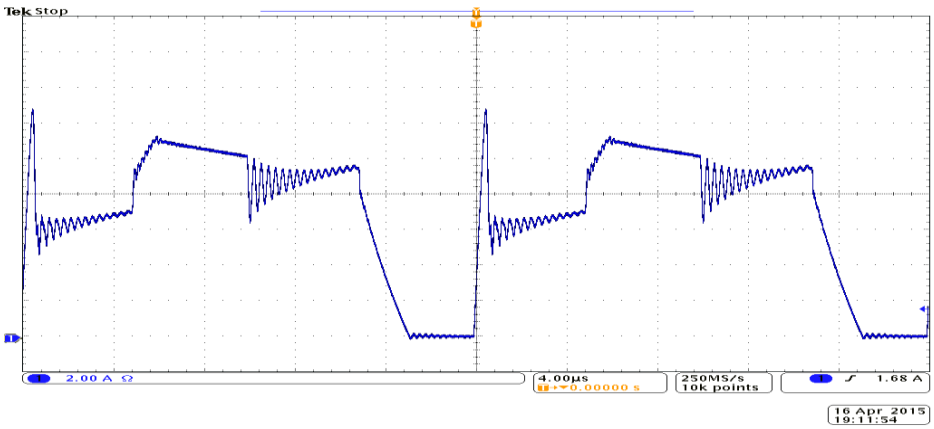

Figure 2.26. Practical waveform of I_{L2} for topology 1

Simulated waveform

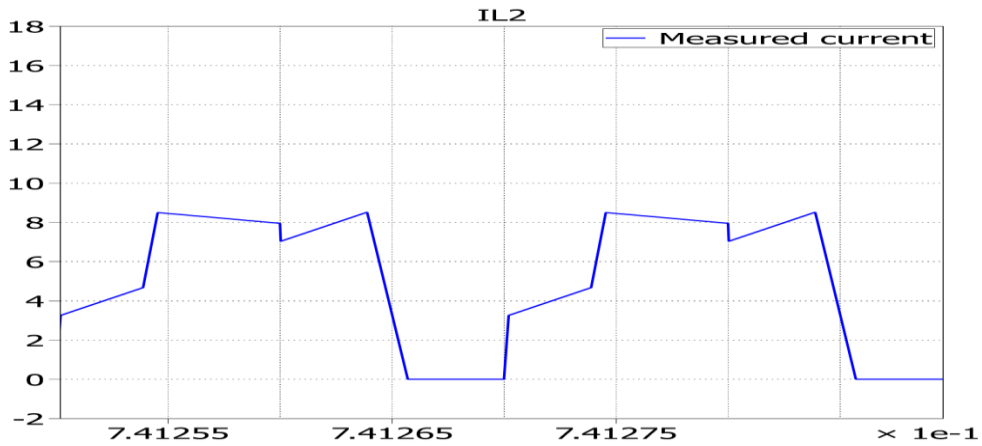

Figure 2.27. Simulated waveform of I_{L2} for topology 1

The ringing in the circuit is mainly because of parasitics. In Figure 2.28, each voltage division is 2A and peak of above current is 6.4 divisions. So, L_1 peak primary inductor current is $6.4 \times 2 = 12.8A$. Figure 2.28 and Figure 2.29 shows the practical and simulated waveforms for inductor current I_{L1} of topology 1.

Practical

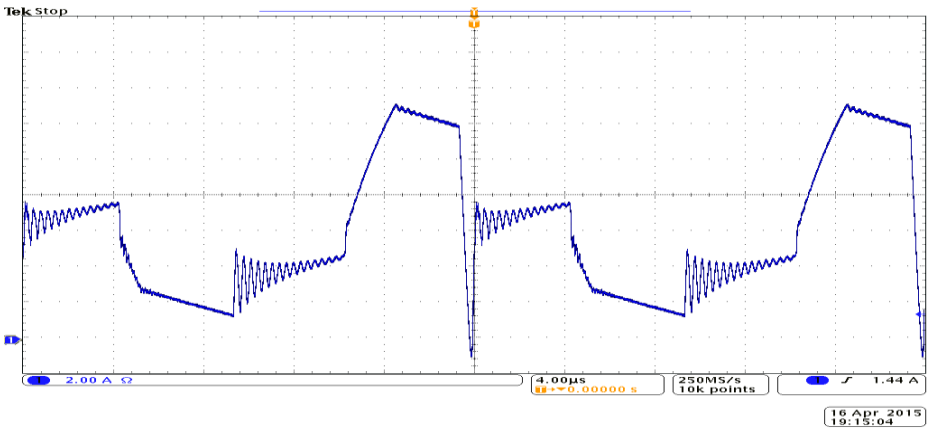

Figure 2.28. Practical waveform of I_{L1} for topology 1

Simulated waveform

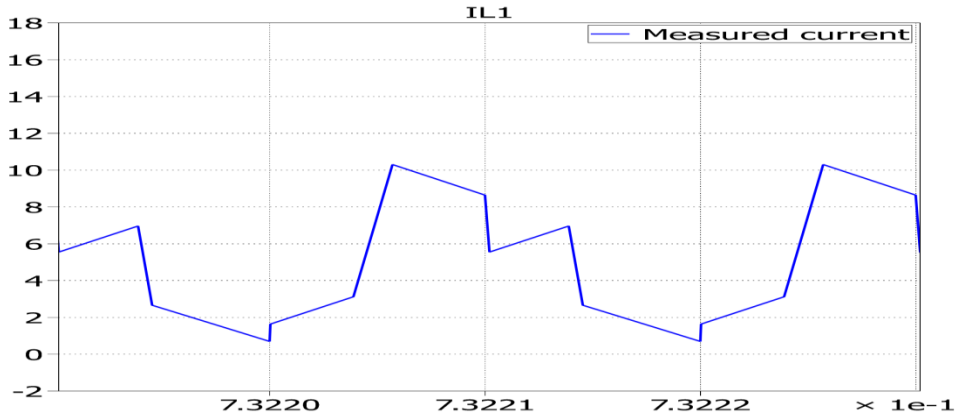

Figure 2.29. Simulated waveform of I_{L1} for topology 1

The ringing in the circuit is mainly because of parasitics. In Figure 2.30, each voltage division is 2A and peak of above current is 7.8 divisions. So, S_1 peak current is $7.8\times 2 = 15.6A$. Figure 2.30 and Figure 2.31 shows the practical and simulated waveforms for switch current I_{S1} of topology 1.

Practical

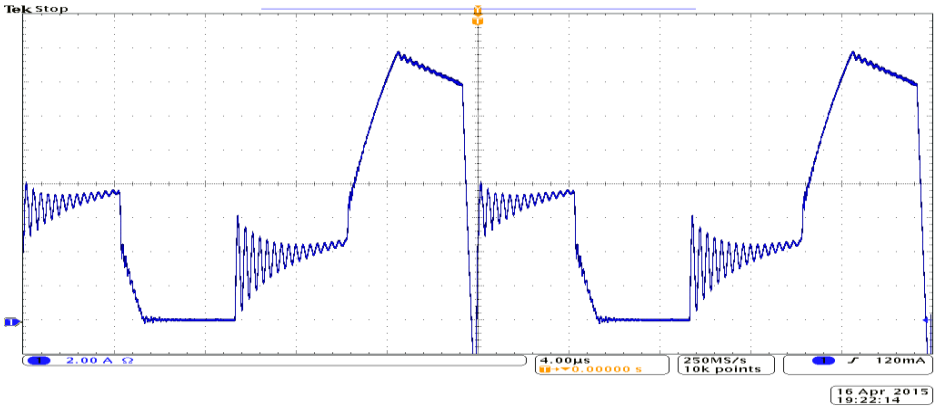

Figure 2.30. Practical waveform of I_{s1} for topology 1

Simulated waveform

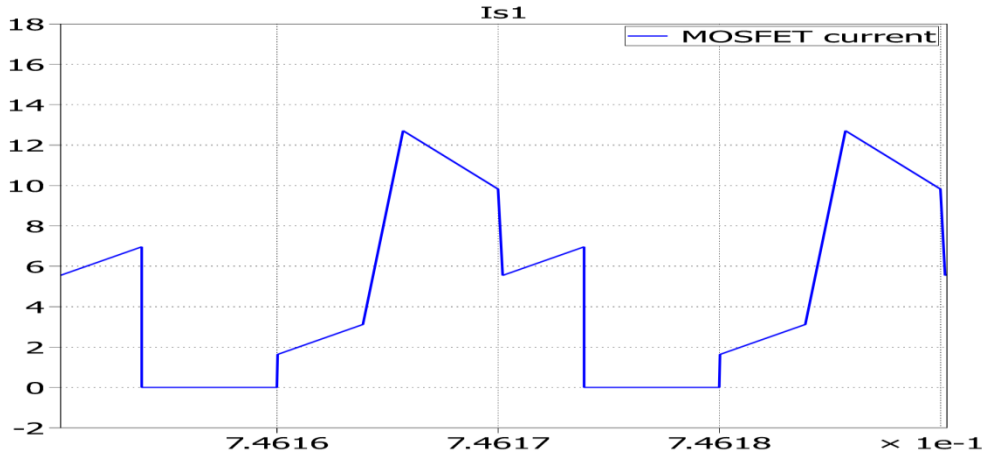

Figure 2.31. Simulated waveform of I_{s1} for topology 1

The ringing in the circuit is mainly because of parasitics. In Figure 2.32, each voltage division is 2A and peak of above current is 5.6 divisions. So, S_2 peak current is $5.6\times 2 = 11.2A$. Figure 2.32 and Figure 2.33 shows the practical and simulated waveforms for switch current I_{S2} of topology 1.

Practical

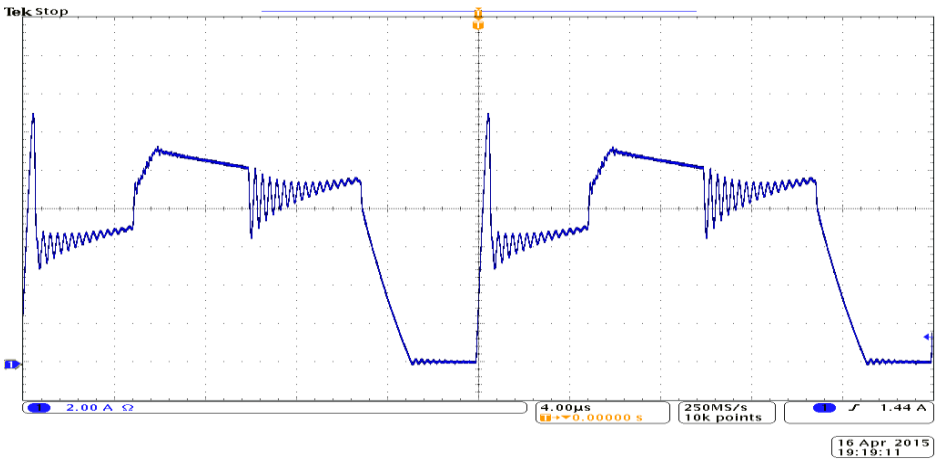

Figure 2.32. Practical waveform of I_{S2} for topology 1

Simulated waveform

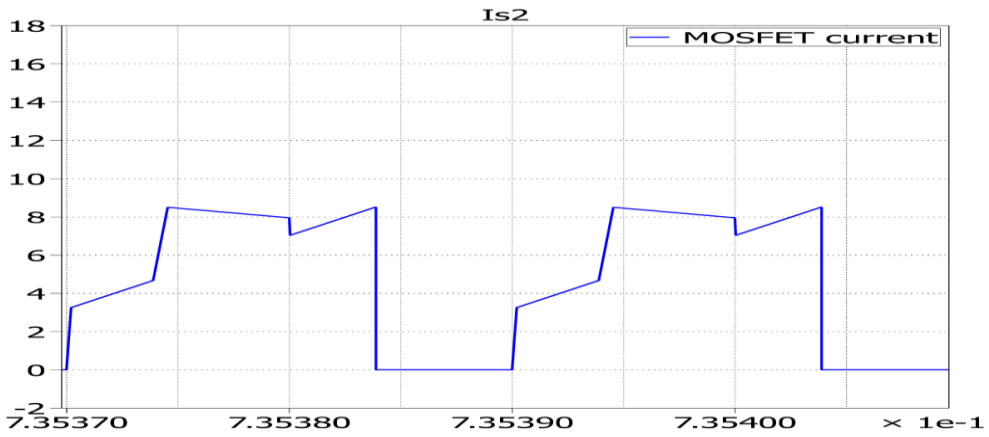

Figure 2.33. Simulated waveform of I_{S2} for topology 1

In Figure 2.34, each voltage division is 1A and peak of above current is 2.8 divisions. So, C_1 peak current is $2.8 \times 1 = 2.8A$. Figure 2.34 and Figure 2.35 shows the practical and simulated waveforms of capacitor C_1 current for topology 1.

Practical

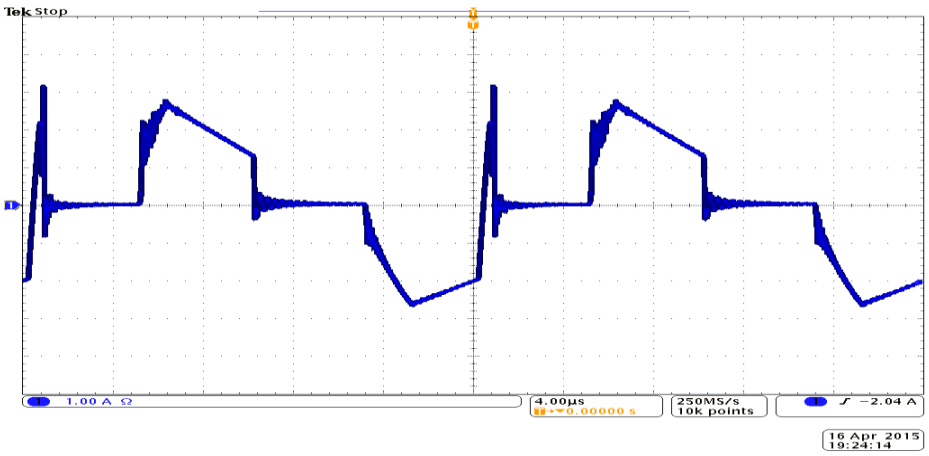

Figure 2.34. Practical waveform of I_{c1} for topology 1

Simulated waveform

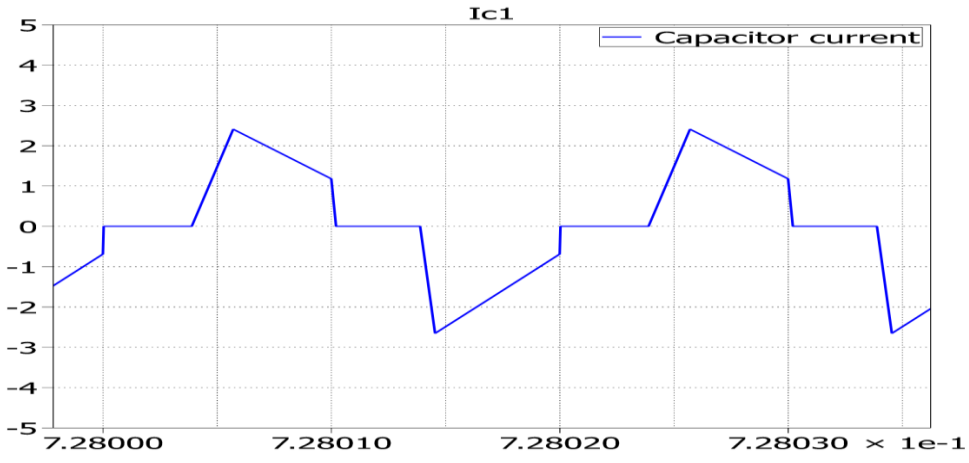

Figure 2.35. Simulated waveform of I_{c1} for topology 1

In Figure 2.36, each voltage division is 0.5A and peak of above current is 5.4 divisions. So, D_1 peak current is $5.4 \times 0.5 = 2.7A$. Figure 2.36 and Figure 2.37 shows the practical and simulated waveforms of diode D_1 current for topology 1.

Practical

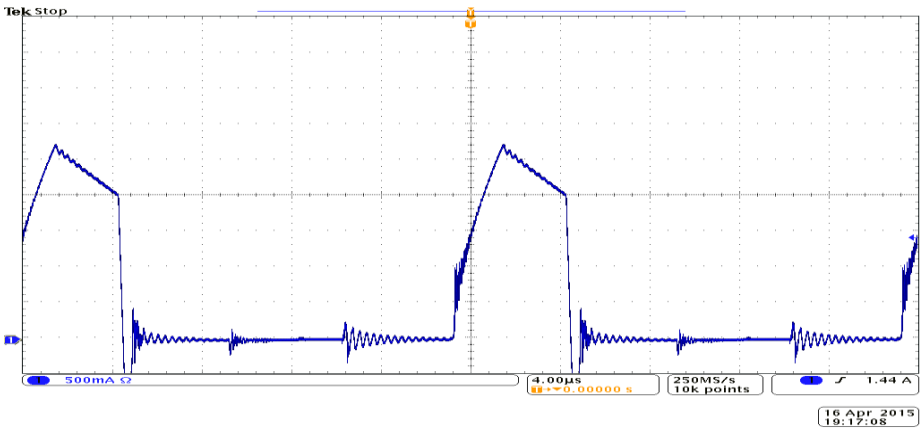

Figure 2.36. Practical waveform of I_{d1} for topology 1

Simulation waveform

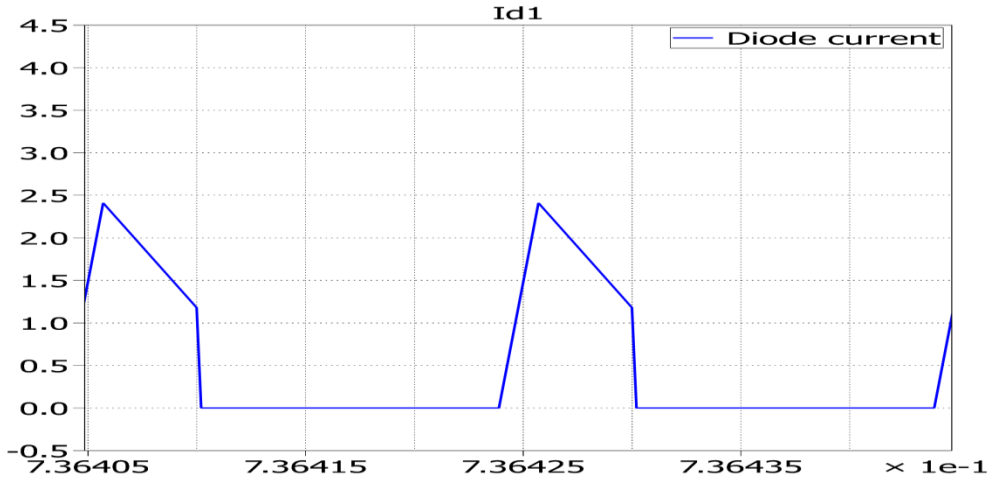

Figure 2.37. Simulated waveform of I_{d1} for topology 1

2.9.2. Topology 2. This section shows practical and simulated waveforms for topology 2. The parameters of the hardware prototype to capture practical waveforms are as shown in Table 2.9.2.

Table 2.9.2 Hardware parameters for topology 2

V_{in} (V)	I_{in} (A)	V_o (V)	R_o (Ω)	I_o (A)	P_{in} (W)	P_o (W)	N	f_{sw} (kHz)
20	11.52	400	795	0.503	230.4	201.2	1.4	50

In Figure 2.38, each voltage division is 50V and total number of divisions is 8. So, the output voltage is $8 \times 50 = 400V$. Figure 2.38 and Figure 2.39 shows the practical and simulated waveforms of output voltage for topology 2.

Practical

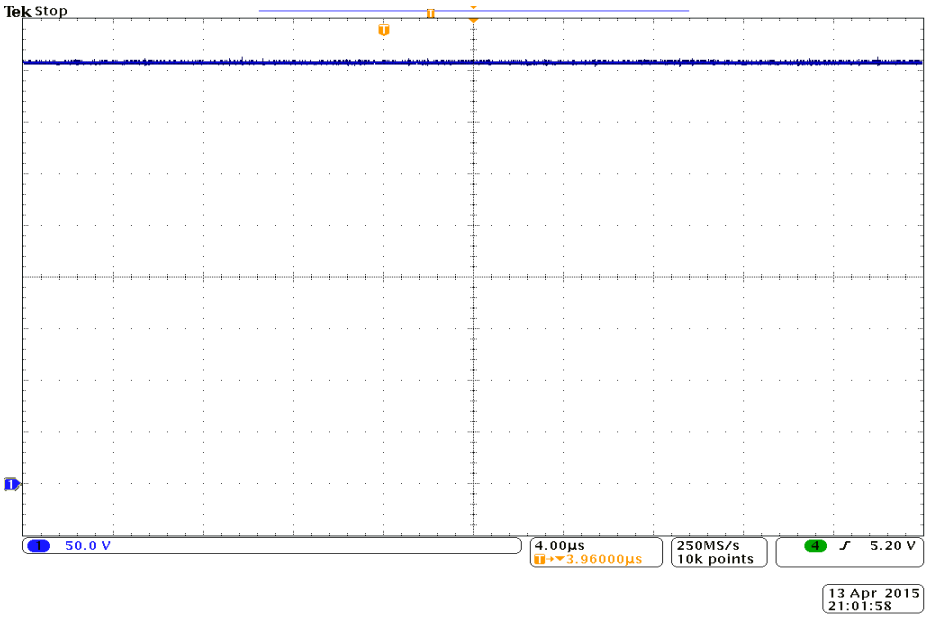

Figure 2.38. Practical waveform of V_{out} for topology 2

Simulated waveform

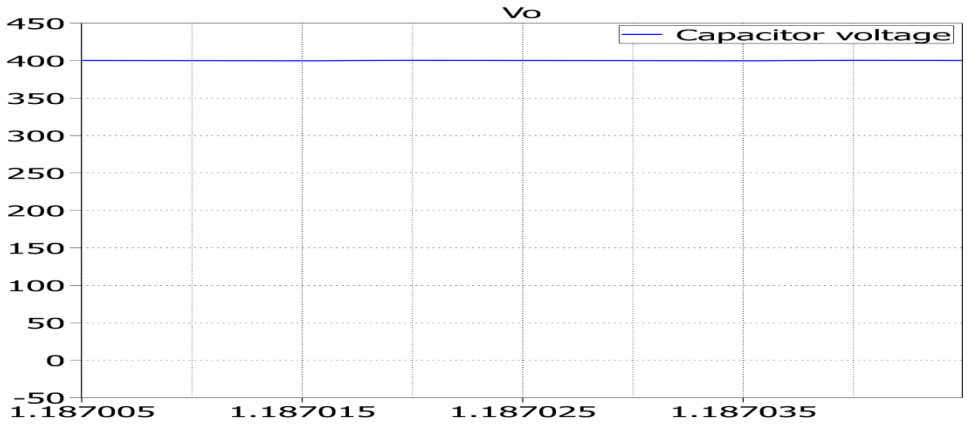

Figure 2.39. Simulated waveform of V_{out} for topology 2

In Figure 2.40, each voltage division is 50V and total number of divisions is around 4. So, capacitor C_1 voltage is $4 \times 50 = 200V$. Figure 2.40 and Figure 2.41 shows the practical and simulated waveforms of capacitor C_1 voltage for topology 2.

Practical

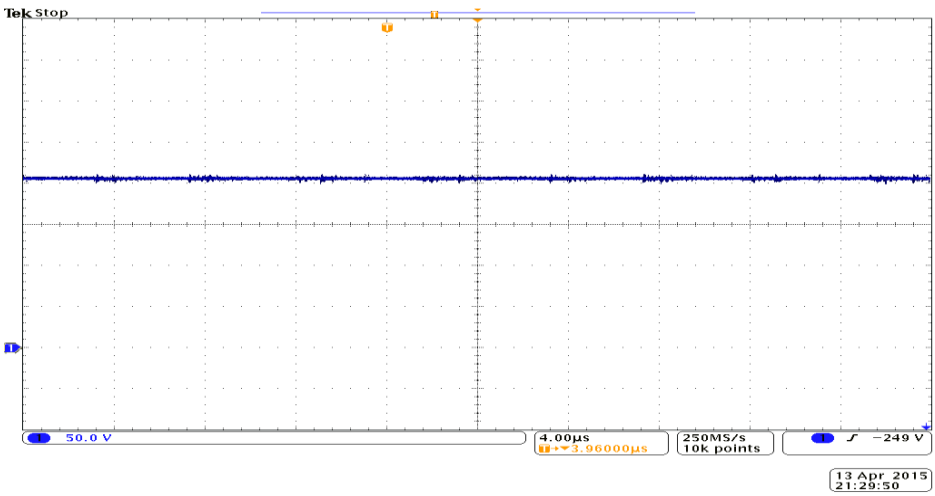

Figure 2.40. Practical waveform of V_{c1} for topology 2

Simulated waveform

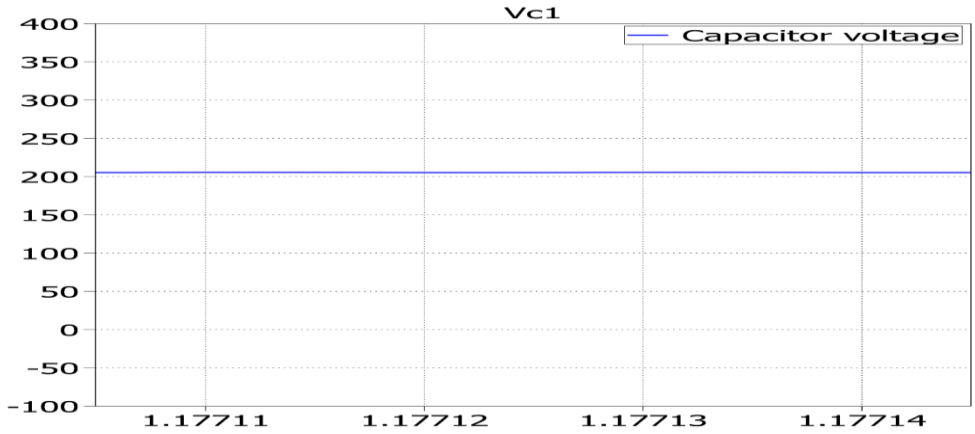

Figure 2.41. Simulated waveform of V_{c1} for topology 2

In Figure 2.42, each voltage division is 25V and total number of divisions is 3.6. So, capacitor C_c voltage is $3.6 \times 25 = 90V$. Figure 2.42 and Figure 2.43 shows the practical and simulated waveforms of capacitor C_c voltage for topology 2.

Practical

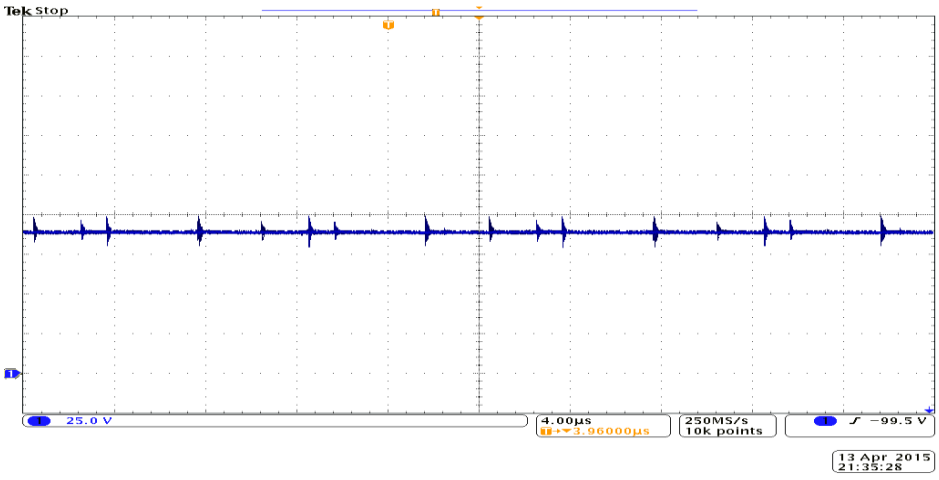

Figure 2.42. Practical waveform of V_{cc} for topology 2

Simulated waveform

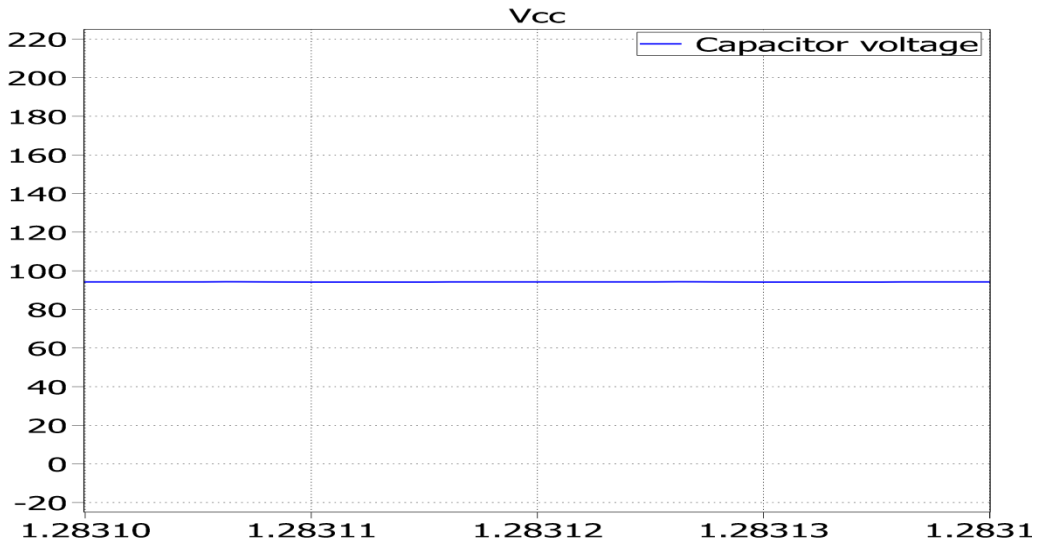

Figure 2.43. Simulated waveform of V_{cc} for topology 2

The below waveform across diode D_2 was measured with negative terminal of the probe connected to cathode and positive to anode, hence the waveform above is negative. The ringing in the waveform is because of leakage inductance and parasitics and may also be because of loop inductance while measuring the waveform. In Figure 2.44, each voltage division is 50V and total number of divisions is 6.2. So, diode D_2 peak voltage is $6.2 \times 50 = 310V$. Figure 2.44 and Figure 2.45 shows the practical and simulated waveforms of diode D_2 voltage for topology 2.

The below waveform across diode D_1 was measured with negative terminal of the probe connected to cathode and positive to anode, hence the waveform above is negative. The ringing in the waveform is because of leakage inductance and parasitics and may also be because of loop inductance while measuring the waveform. In Figure 2.46, each voltage division is 50V and total number of divisions is 6.2. So, diode D_1 peak voltage is $6.2 \times 50 = 310V$. Figure 2.46 and Figure 2.47 shows the practical and simulated waveforms of diode D_1 voltage for topology 2.

Practical

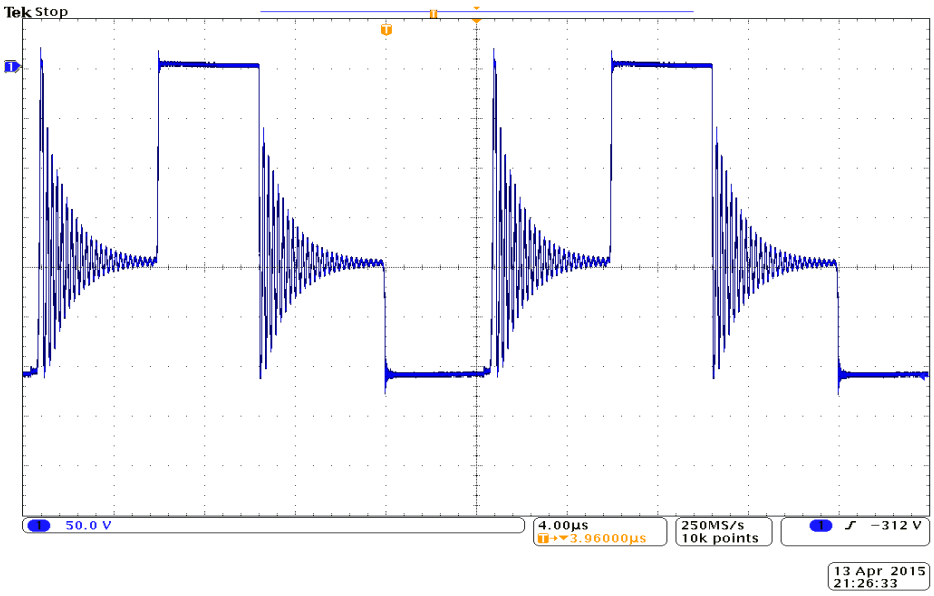

Figure 2.44. Practical waveform of V_{d2} for topology 2

Simulated waveform

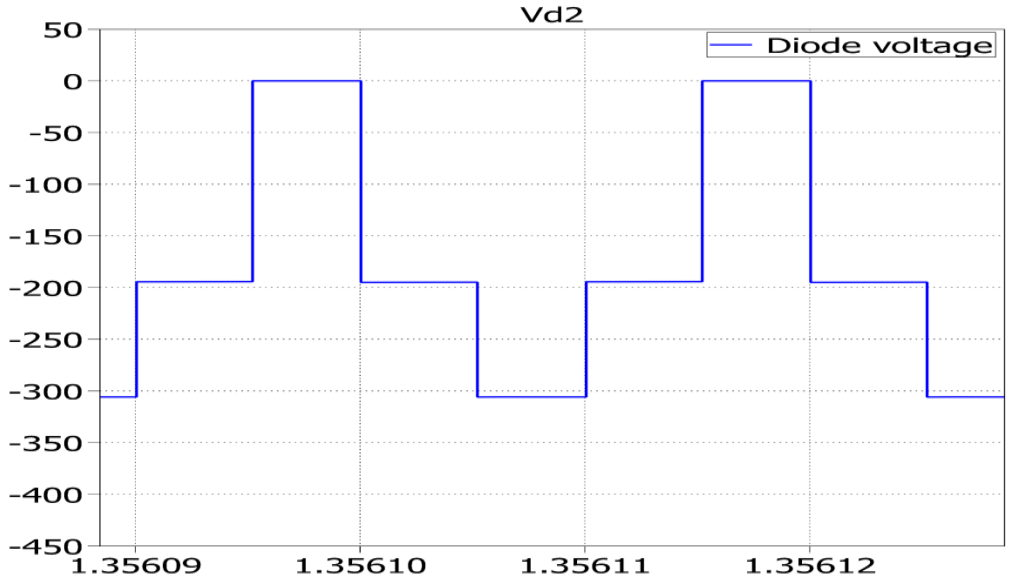

Figure 2.45. Simulated waveform of V_{d2} for topology 2

Practical

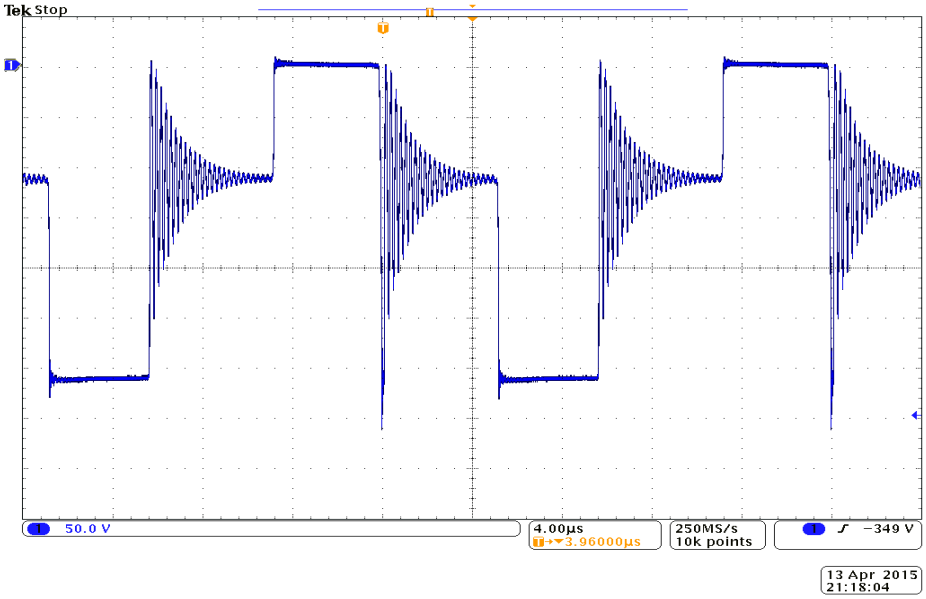

Figure 2.46. Practical waveform of V_{d1} for topology 2

Simulated waveform

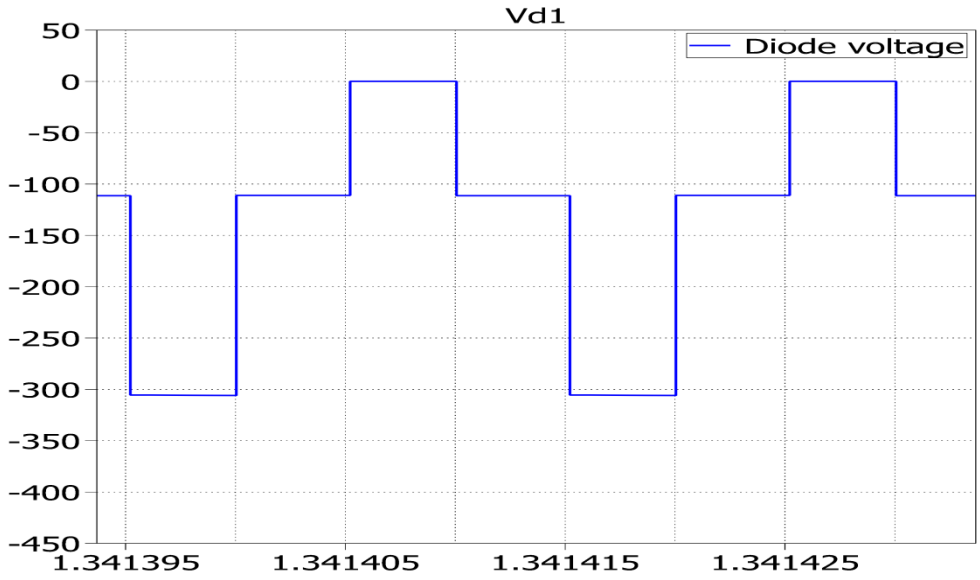

Figure 2.47. Simulated waveform of V_{d1} for topology 2

In Figure 2.48, each voltage division is 20V and total number of divisions is 4.2. So, peak switch voltage is $4.2 \times 20 = 84V$. The voltage spike is because of leakage inductance in the circuit during turn-off of switch. Figure 2.48 and Figure 2.49 shows the practical and simulated waveforms of switch V_{ds1} voltage for topology 2.

Practical

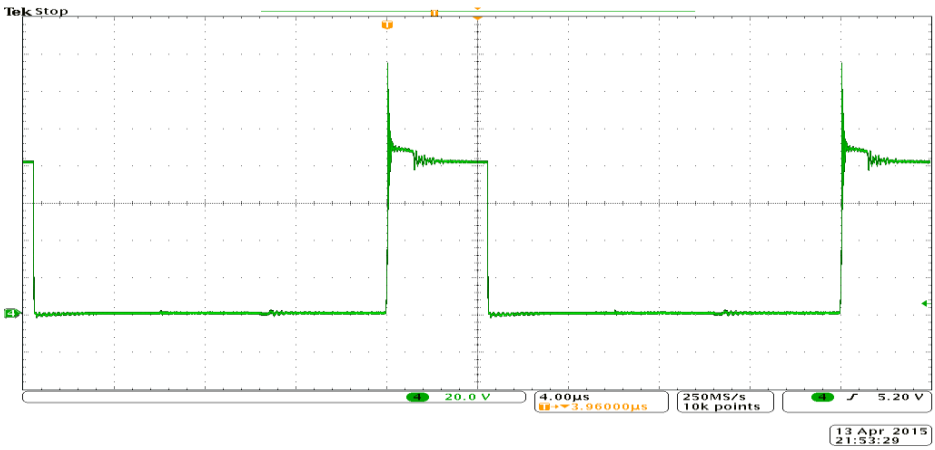

Figure 2.48. Practical waveform of V_{ds1} for topology 2

Simulated waveform

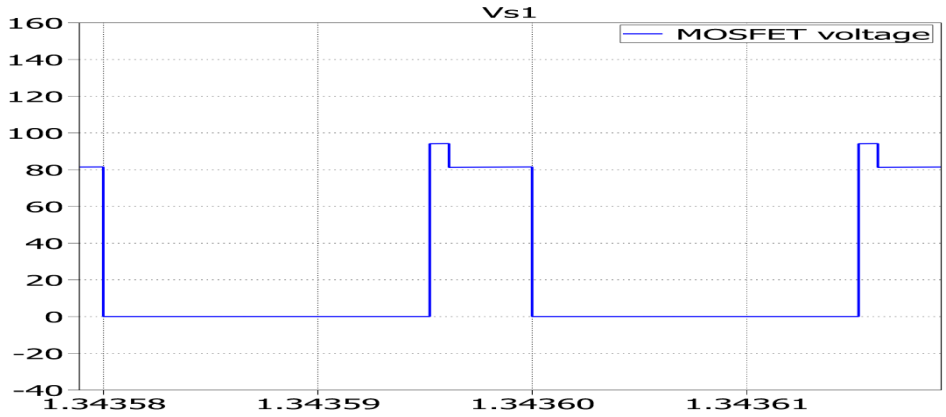

Figure 2.49. Simulated waveform of V_{ds1} for topology 2

In Figure 2.50, each voltage division is 20V and total number of divisions is 4.2. So, peak switch voltage is $4.2 \times 20 = 84V$. The voltage spike is because of leakage inductance in the circuit during turn-off of switch. Figure 2.50 and Figure 2.51 shows the practical and simulated waveforms of switch V_{ds2} voltage for topology 2.

Practical

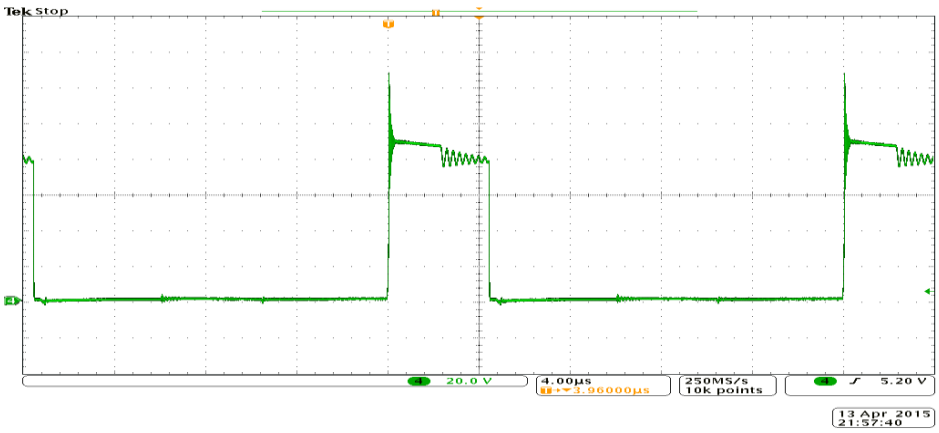

Figure 2.50. Practical waveform of V_{ds2} for topology 2

Simulated waveform

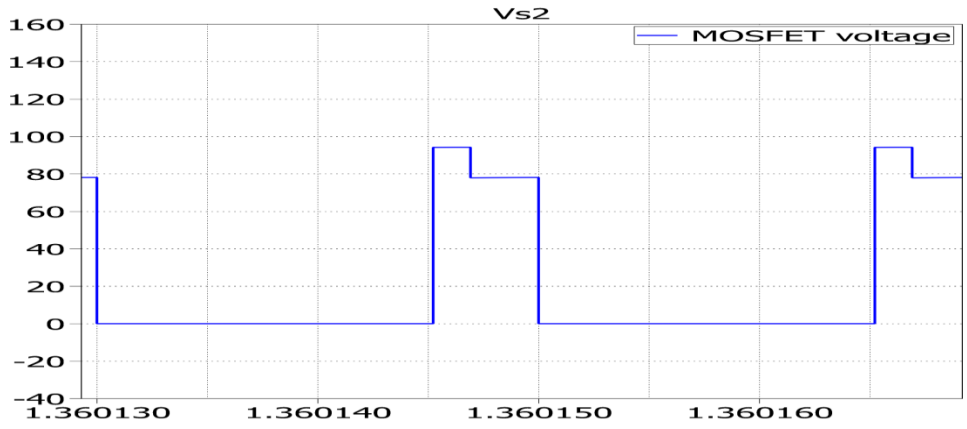

Figure 2.51. Simulated waveform of V_{ds2} for topology 2

In Figure 2.52, each voltage division is 2A and total number of divisions is 7.6. So, peak input current is $7 \times 2 = 14A$. Figure 2.52 and Figure 2.53 shows the practical and simulated waveforms of input current I_{in} for topology 2.

Practical

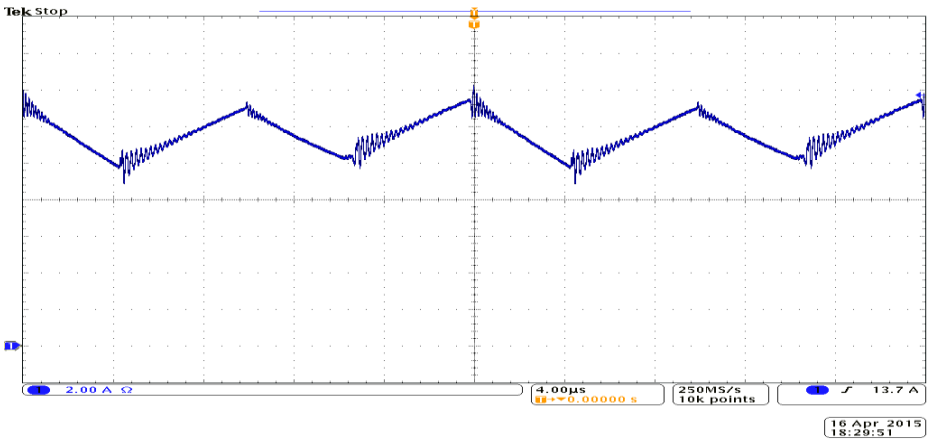

Figure 2.52. Practical waveform of I_{in} for topology 2

Simulated waveform

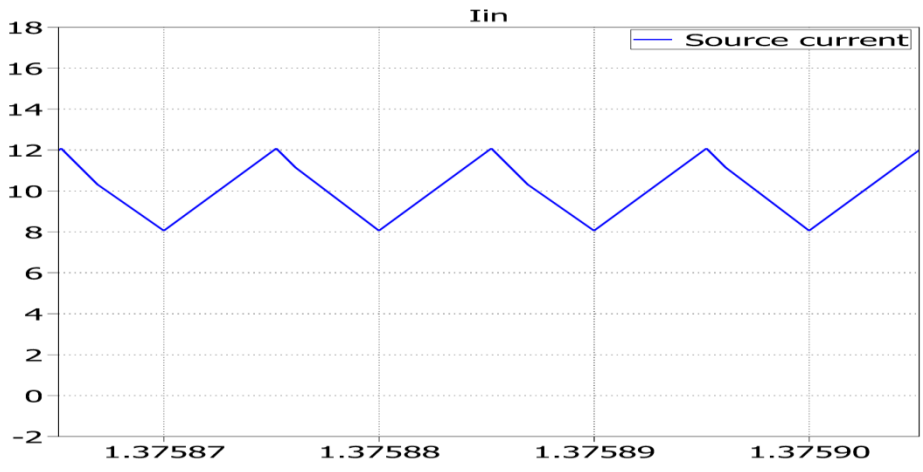

Figure 2.53. Simulated waveform of I_{in} for topology 2

The ringing in the circuit is mainly because of parasitics. In Figure 2.52, each voltage division is 2A and peak of above current is 4.8 divisions. So, L_2 peak primary inductor current is $4.8\times 2 = 9.6A$. Figure 2.54 and Figure 2.55 shows the practical and simulated waveforms of inductor current I_{L2} for topology 2.

Practical

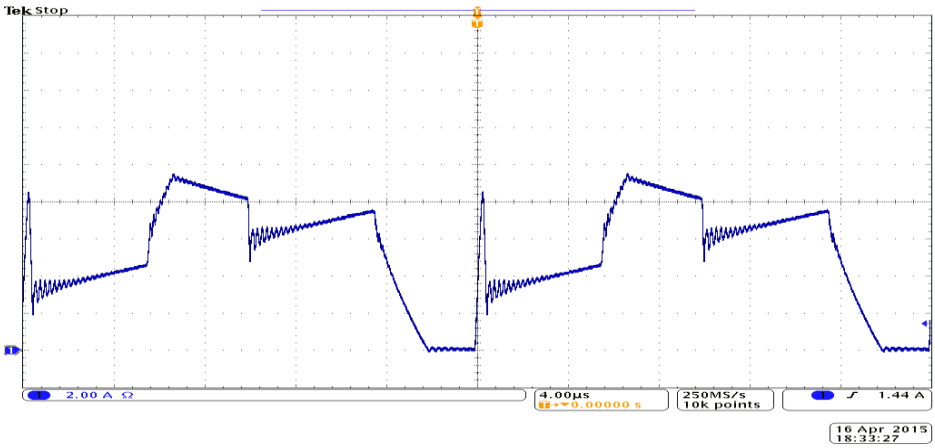

Figure 2.54. Practical waveform of I_{L2} for topology 2

Simulated waveform

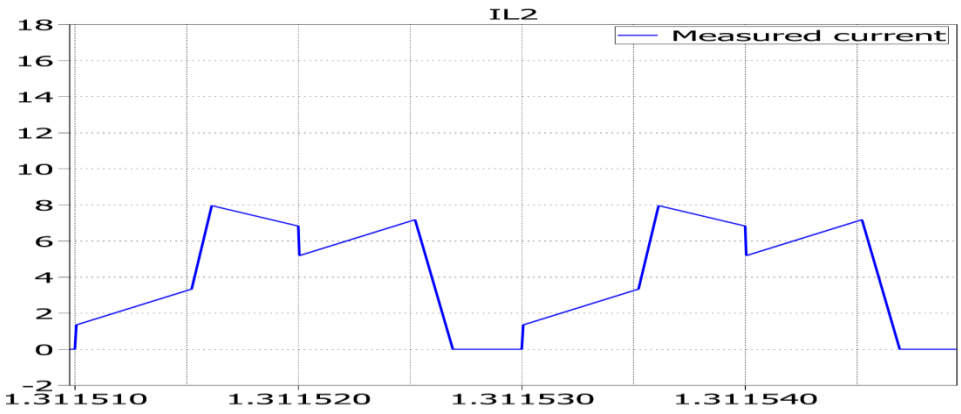

Figure 2.55. Simulated waveform of I_{L2} for topology 2

The ringing in the circuit is mainly because of parasitics. In Figure 2.56, each voltage division is 2A and peak of above current is 5.8 divisions. So, peak L_1 primary inductor current is $5.8\times2=11.6A$. Figure 2.56 and Figure 2.57 shows the practical and simulated waveforms of inductor current I_{L1} for topology 2.

Practical

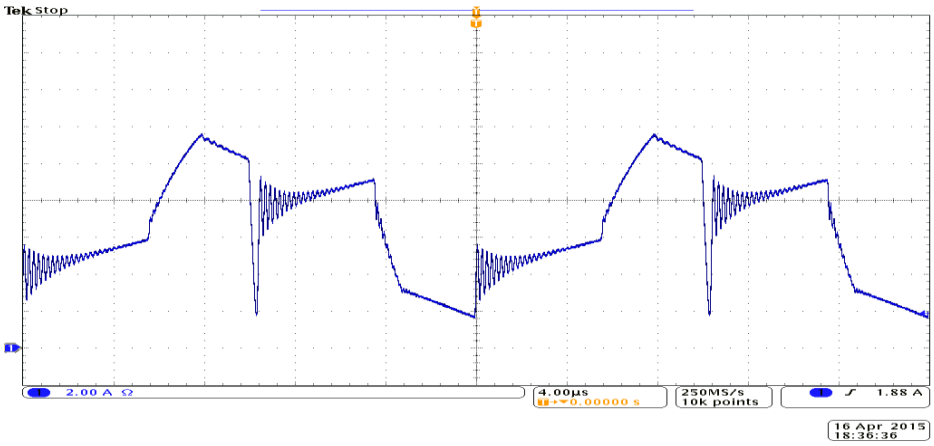

Figure 2.56. Practical waveform of I_{L1} for topology 2

Simulated waveform

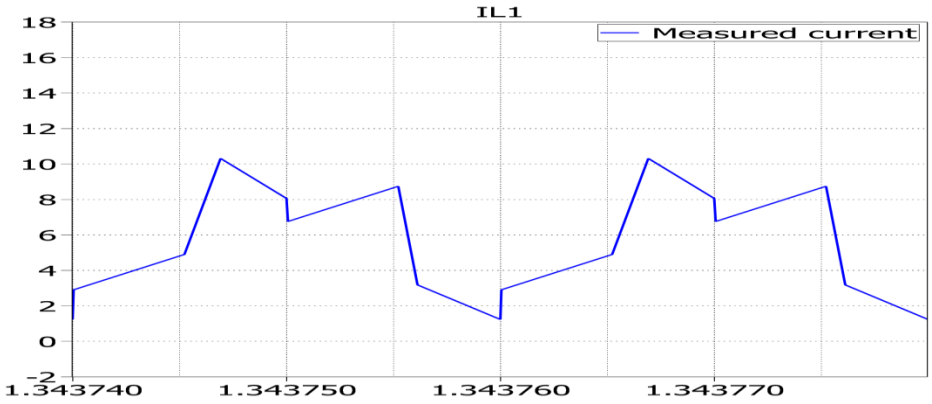

Figure 2.57. Simulated waveform of I_{L1} for topology 2

The ringing in the circuit is mainly because of parasitics. In Figure 2.58, each voltage division is 2A and peak of above current is 7.6 divisions. So, peak S_1 current is $7.6 \times 2 = 15.2A$. Figure 2.58 and Figure 2.59 shows the practical and simulated waveforms of switch current I_{s1} for topology 2.

Practical

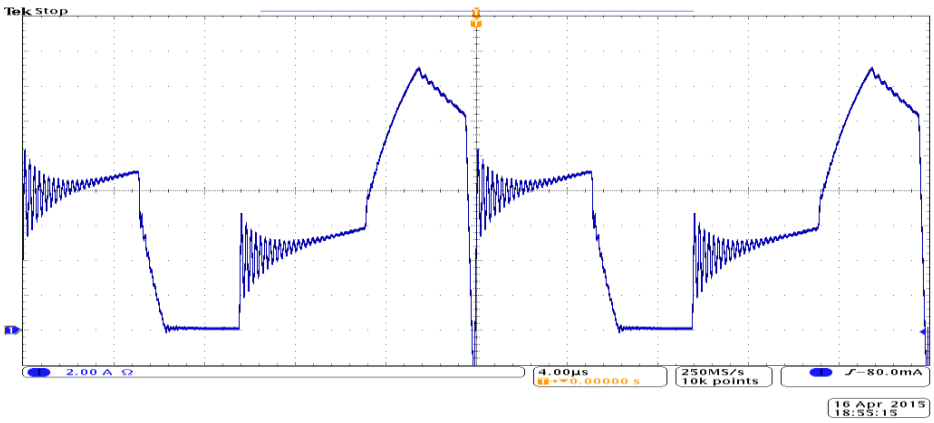

Figure 2.58. Practical waveform of I_{s1} for topology 2

Simulated waveform

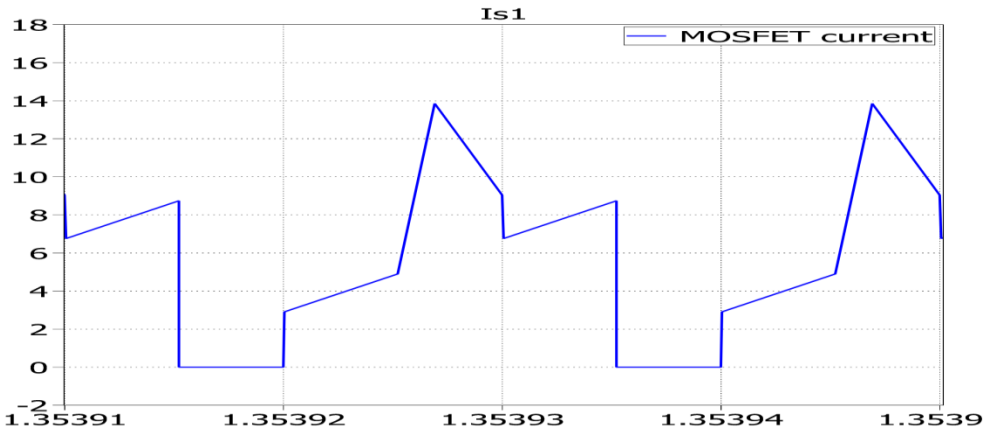

Figure 2.59. Simulated waveform of I_{s1} for topology 2

The ringing in the circuit is mainly because of parasitics. In Figure 2.60, each voltage division is 2A and peak of above current is 4.6 divisions. So, peak S_2 current is $4.6 \times 2 = 9.2A$. Figure 2.60 and Figure 2.61 shows the practical and simulated waveforms of switch current I_{s2} for topology 2.

Practical

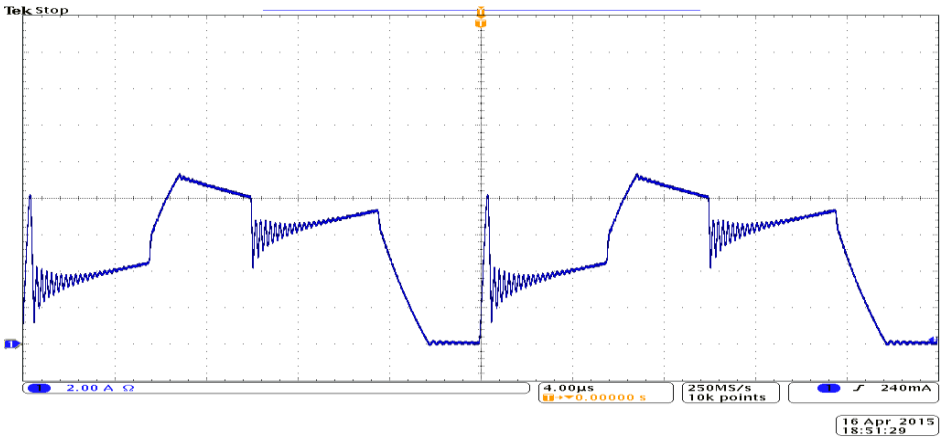

Figure 2.60. Practical waveform of I_{s2} for topology 2

Simulated waveform

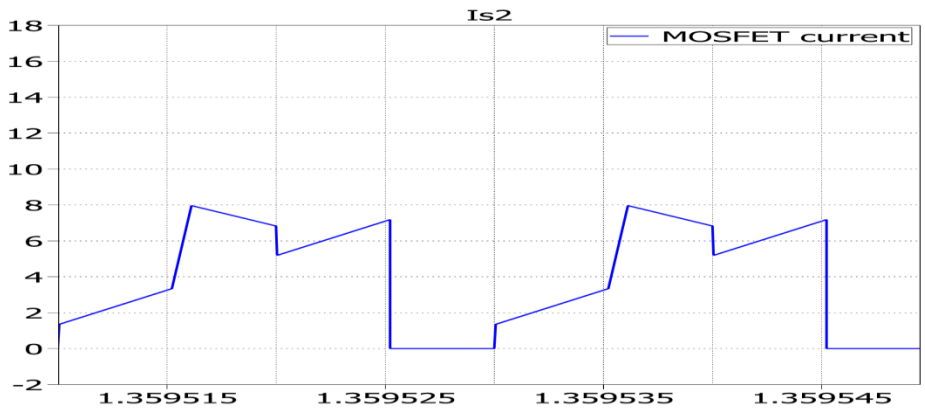

Figure 2.61. Simulated waveform of I_{s2} for topology 2

In Figure 2.62, each voltage division is 1A and peak of above current is 3.2 divisions. So, C_1 peak current is $3.2 \times 1 = 3.2A$. Figure 2.62 and Figure 2.63 shows the practical and simulated waveforms of capacitor current I_{c1} for topology 2.

Practical

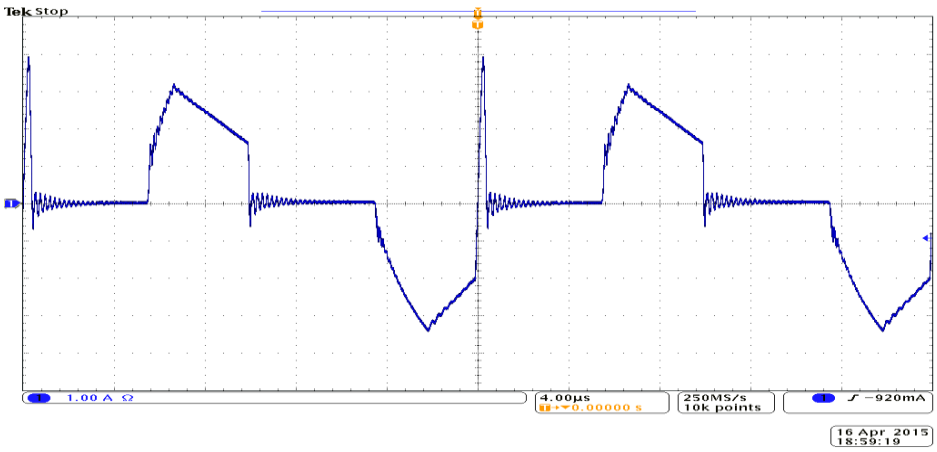

Figure 2.62. Practical waveform of I_{c1} for topology 2

Simulated waveform

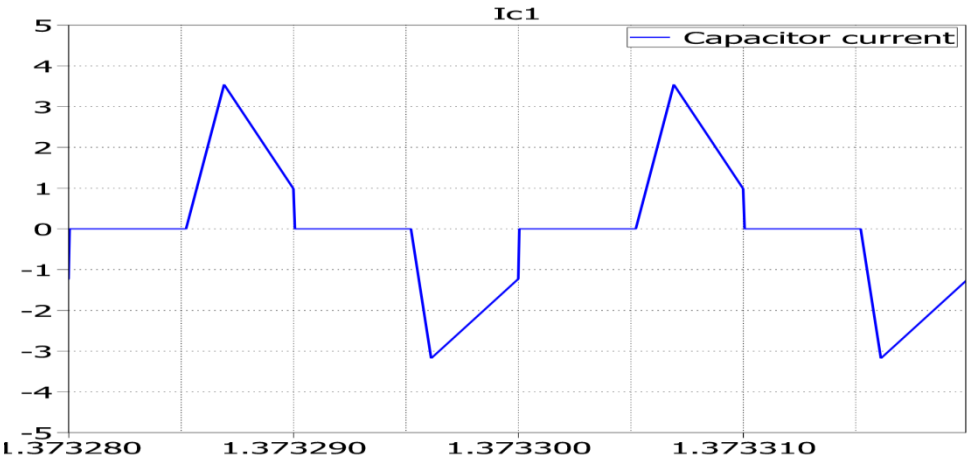

Figure 2.63. Simulated waveform of I_{c1} for topology 2

In Figure 2.64, each voltage division is 0.5A and peak of above current is 6.8 divisions. So, D_1 peak current is $6.8 \times 0.5 = 3.4A$. Figure 2.64 and Figure 2.65 shows the practical and simulated waveforms of capacitor current I_{d1} for topology 2.

Practical

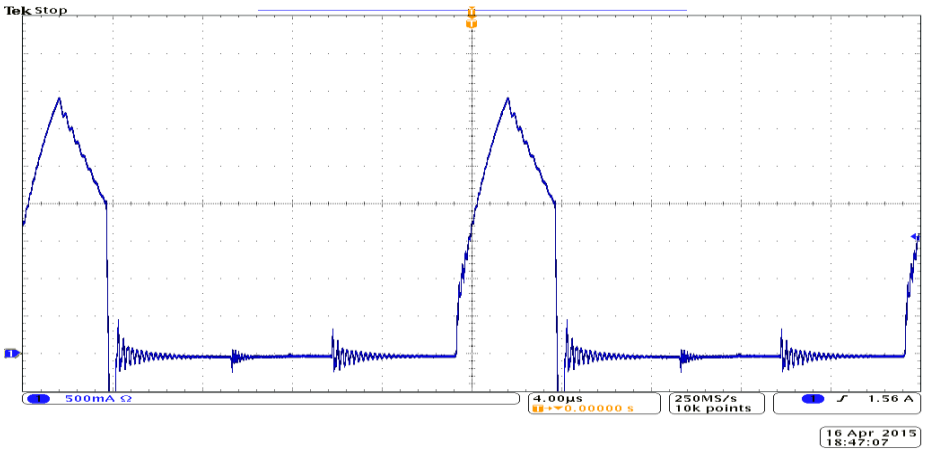

Figure 2.64. Practical waveform of I_{d1} for topology 2

Simulated waveform

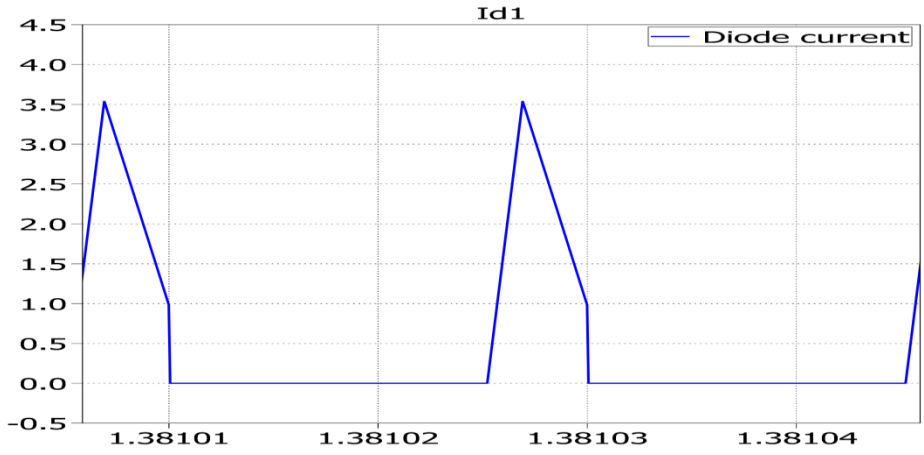

Figure 2.65. Simulated waveform of I_{d1} for topology 2

3. POWER LOSS ANALYSIS IN TOPOLOGIES 1 AND 2 AND VARIATION OF EFFICIENCY WITH COUPLED INDUCTOR TURNS RATIO

3.1. POWER LOSS ANALYSIS IN TOPOLOGIES 1 & 2

Based on the average and RMS current equations for all the components, a power loss analysis is carried out for both the topologies and the results are discussed in this section. The analysis is carried out with the below mentioned parameters for the converter in topology 1. The percentage and breakdown of losses in topology 1 are as mentioned in Figure 3.1 and Table 3.2 respectively. The parameters used for power loss analysis in topology 1 are as shown in Table 3.1.

Table 3.1 Parameters for power loss analysis for topology 1

V_{in} (V)	V_o (V)	R_o (Ω)	D	I_o (A)	P_o (W)	f_{sw} (kHz)	N	I_{in} (A)	L (µH)
20	400	400	0.75	1	400	100	1	20	50

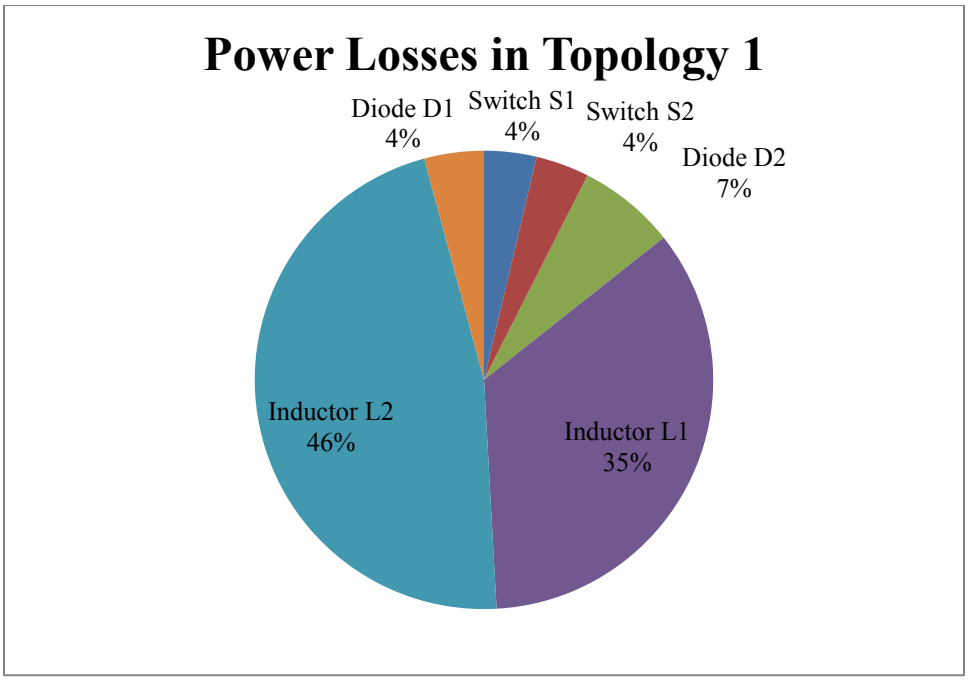

Figure 3.1.Power Loss Analysis in Topology 1

Table 3.2.Breakdown of losses in Topology 1

Component	Power Loss (W)
MOSFET (S_1)	Conduction losses – 0.99 Switching losses – 0.204 Total losses – 1.20
MOSFET (S_2)	Conduction losses – 1.023 Switching losses – 0.204 Total losses – 1.23
Output diode (D_2)	Conduction losses – 2.23
Diode (D_1)	Conduction losses – 1.37
Inductor (L_1)	Conduction losses – 11.3
Inductor (L_2)	Conduction losses – 15.17
	Total losses in topology 1 are 32.49

The equation used for switching losses of MOSFET is

$P_{sw} = (\frac{1}{2} \times I_{Lavg} \times V_s \times (t_{off} + t_{on})) + (\frac{1}{2} \times f_{sw} \times C_{oss} \times V_s^2)$, where I_{Lavg} is the new average current through switch, t_{off} and t_{on} are switch turn-on and turn-off times, and V_s is switch voltage. Similar to the analysis shown above for topology 1, based on the theoretical equations of currents, the power losses are as shown in topology 2. The parameters used for power analysis are as tabulated in Table 3.3. The percentage and breakdown of losses in topology 2 are as mentioned in Figure 3.2 and Table 3.4 respectively.

Table 3.3. Parameters for power loss analysis for topology 2

V_{in} (V)	V_o (V)	R_o (Ω)	D	I_o (A)	P_o (W)	f_{sw} (kHz)	N	I_{in} (A)	L (μH)
20	400	400	0.75	1	400	100	1.5	20	50

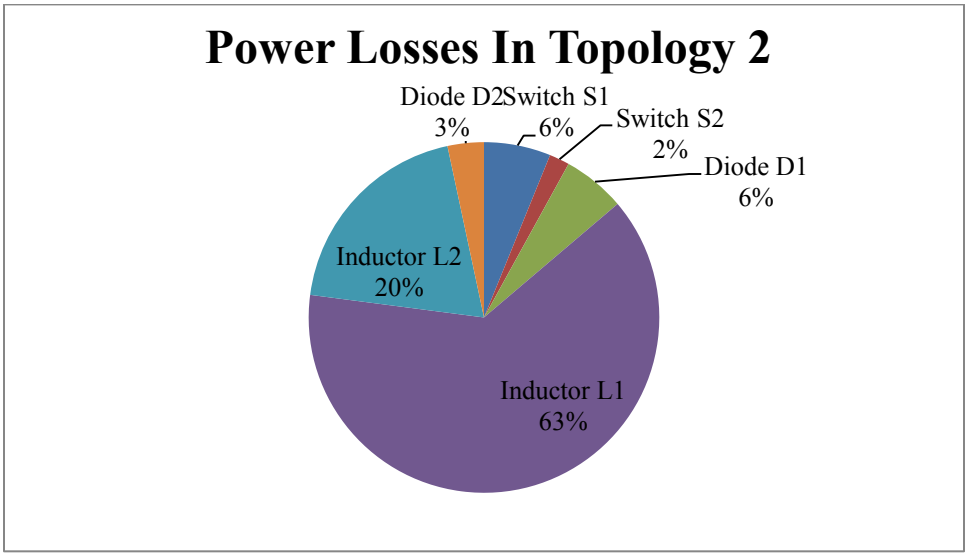

Figure 3.2.Power Loss Analysis in Topology 2

The breakdown of the losses in topology 2 is as shown below

Table 3.4. Breakdown of losses in Topology 2

Component	Power Loss (W)
MOSFET (S_1)	Conduction losses – 1.82 Switching losses – 0.204 Total losses – 2.02
MOSFET (S_2)	Conduction losses – 0.41 Switching losses – 0.204 Total losses – 0.613
Output diode (D_2)	Conduction losses – 1.1
Diode (D_1)	Conduction losses – 1.9
Inductor (L_1)	Conduction losses – 20.8
Inductor (L_2)	Conduction losses – 6.44
	Total losses in topology 2 is 32.88

3.2. EFFECT OF N RATIO ON EFFICIENCY

In order to study the variation of efficiency with coupled inductors turns ratio N, a practical testing has been carried out and the results of the respective tests are discussed in this section of the thesis. To carry out these tests with different turns ratio of coupled inductor, we have designed coupled inductors by varying the turns on the secondary side. All this analysis was carried out for topology 1.

Measurements from LCR meter ("Design#1")

L_2

Primary: 0.15 Ω, 57µH

Secondary1: 0.12 Ω, 59.3µH

Secondary2:0.14 Ω, 60.1µH

L_1

Primary: 0.14 Ω, 61.1H

Secondary1: 0.15 Ω, 58.4µH

Secondary2: 0.12 Ω, 57.6µH

No of turns on primary - 20

No of turns on each secondary – 20

Type of winding – Simultaneously wound primary and two secondary's

Wire gauge used – 22AWG for both primary & secondary, with two 22AWG in parallel for primary and single 22AWG for two secondary windings. ($N_p = N_s$)

Measurements from LCR meter ("Design#2")

L_2

Primary: 0.12 Ω, 62.3µH

Secondary1: 0.3Ω, 89.02µH

Secondary2:0.32Ω, 89.5µH

L_1

Primary: 0.13Ω, 66.4H

Secondary1: 0.48Ω, 96µH

Secondary2: 0.5Ω, 97µH

No of turns on primary - 20

No of turns on each secondary – 24

Type of winding – Simultaneously wound primary and two secondary's

Wire gauge used – 22AWG for both primary & secondary, with two 22AWG in parallel for primary and single 22AWG for two secondary windings. ($N_p = 1.2* N_s$)

Measurements from LCR meter ("Design#3")

L_2

Primary: 0.14Ω, 68.51μH

Secondary1: 0.89Ω, 139.8μH

Secondary2:0.82Ω, 138.6μH

L_1

Primary: 0.12Ω, 62.16μH

Secondary1: 0.8Ω, 128.5μH

Secondary2: 0.77Ω, 127.28μH

No of turns on primary - 20

No of turns on each secondary – 28

Type of winding – Simultaneously wound primary and two secondary's

Wire gauge used – 22AWG for both primary & secondary, with two 22AWG in parallel for primary and single 22AWG for two secondary windings. ($N_p = 1.4* N_s$)

Measurements from LCR meter ("Design#4")

L_2

Primary: 0.14Ω, 71.8μH

Secondary1: 0.95Ω, 149.35μH

Secondary2: 0.93Ω, 148.42μH

L_1

Primary: 0.2Ω, 69.32μH

Secondary1: 1.13Ω, 147.96μH

Secondary2: 1.08Ω, 146.88μH

No of turns on primary - 20

No of turns on each secondary – 32

Type of winding – Simultaneously wound primary and two secondary's

Wire gauge used – 22AWG for both primary & secondary, with two 22AWG in parallel for primary and single 22AWG for two secondary windings. ($N_p = 1.6* N_s$)

Measurements from LCR meter ("Design#5")

L_2

Primary: 0.13Ω, 64µH

Secondary1: 1.72Ω, 207µH

Secondary2:1.77Ω, 209.8µH

L_1

Primary: 0.12Ω, 63.9µH

Secondary1: 1.72Ω, 198µH

Secondary2: 1.78Ω, 199µH

No of turns on primary - 20

No of turns on each secondary – 36

Type of winding – Simultaneously wound primary and two secondary's

Wire gauge used – 22AWG for both primary & secondary, with two 22AWG in parallel for primary and single 22AWG for two secondary windings. ($N_p = 1.8* N_s$)

Measurements from LCR meter ("Design#6")

L_2

Primary: 0.15Ω, 65.3µH

Secondary1: 2Ω, 246.4µH

Secondary2:2.1Ω, 248.3µH

L_1

Primary: 0.14Ω, 63.9H

Secondary1: 2.1Ω, 250.1µH

Secondary2: 2.04Ω, 246.8µH

No of turns on primary - 20

No of turns on each secondary – 40

Type of winding – Simultaneously wound primary and two secondary's
Wire gauge used – 22AWG for both primary & secondary, with two 22AWG in parallel for primary and single 22AWG for two secondary windings. ($N_p = 2* N_s$)

From the results shown in Table 3.5, it can be observed that the efficiency of the converter by varying the turns ratio of coupled inductor was almost found to be same and the slight difference in efficiencies may be because of measurement error.

Table 3.5.N vs efficiency for topology 1

Design #	V_{in} (V)	I_{in} (A)	V_o (V)	I_o (A)	P_{in} (W)	P_o (W)	Eff (%)	N_p : N_s	Duty (%)
1	19.87	11.52	401.4	0.502	228.78	201.65	88.14	**1:1**	75.15
2	19.87	11.23	401.1	0.502	223.14	201.35	90.23	**1:1.2**	72.6
3	19.87	11.37	401.7	0.503	225.92	201.95	89.39	**1:1.4**	70.1
4	19.87	11.33	401.3	0.502	225.12	201.55	89.53	**1:1.6**	69.5
5	19.87	11.39	401.3	0.502	226.31	201.55	89.06	**1:1.8**	66.8
6	19.87	11.39	401.3	0.502	226.32	201.55	89.05	**1:2**	63.8

4. EFFICIENCY ANALYSIS OF THE CONVERTER BY USING SILICON TO GALLIUM NITRIDE MOSFETs

4.1. GaN TECHNOLOGY

GaN stands for Gallium Nitride. It is a binary III /V direct binary band gap semi-conductor. Its wide band gap of 3.4eV makes it possible to be used in applications involving high frequencies. The device structure of the GaN device is shown in Figure 4.1.

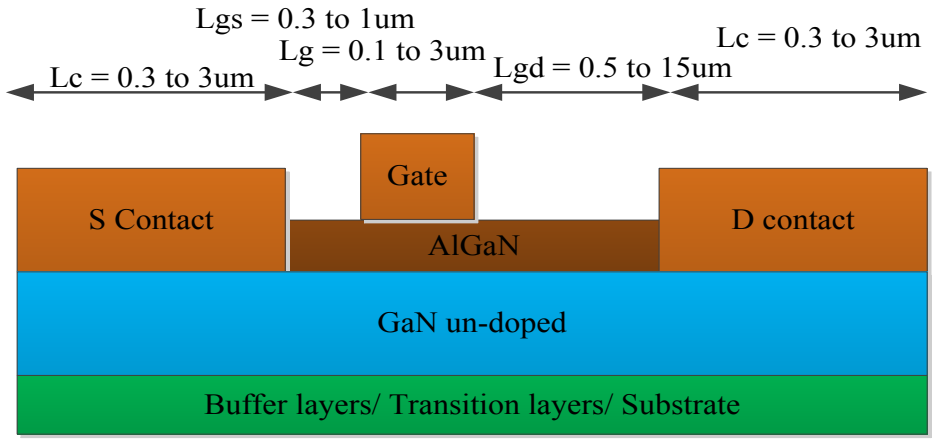

Figure 4.1.Device structure of GaN [21-22]

The high conductivity of the GaN device is because of the strain differences between two materials GaN and AlGaN. This strain differences at the interface between GaN and AlGaN gives rise to piezo effect which creates a high concentration of electrons in a confined space [23-24]. The comparison of Si, SiC and GaN materials are as shown below in the Table 4.1.

Table 4.1.Material properties comparison (www.microsemi.com) [25]

Materials property	Si	SiC-4H	GaN
Band gap (eV)	1.1	3.2	3.4
Critical field 10^6V/cm	0.3	3	3.5

Table 4.1.Material properties comparison (www.microsemi.com) (Contd.)

Electron mobility (cm^2 / V-sec)	1450	900	2000
Electron saturation velocity (10^6 cm/sec)	10	22	25
Thermal conductivity (Watt/cm^2 K)	1.5	5	1.3

The parameters used by the researchers while comparing various materials so called the types of Figure of Merits (FOMs) [26] are as mentioned below

- Rectifier FOM/conduction FOM

  It is given by the formula, $(R_{dson} \times Q_g)$

- Switching FOM

  It is given by the formula, $(R_{dson} \times Q_{gd})$

In order to study the improvement in efficiency of the converter by using GaN MOSFET compared to Si based device, a practical testing is carried out in a prototype of both the topologies 1 and 2 by changing only the MOSFET in the test set-up. For a common comparison platform, a 600V GaN based MOSFETs and a 600V Si based MOSFETs are selected.

Comparison of FOM based on datasheets is as under

- EPC2010 (200V, 12A) - $R_{dson} = 25m\Omega$, $Q_g = 7.5nC$, $Q_{gd} = 2.6nC$

  FOM conduction = 1.875×10^{-10}, FOM switching = 6.5×10^{-11}

- TPH3006PS (600V, 17A) - $R_{dson} = 150m\Omega$, $Q_g = 9.3nC$, $Q_{gd} = 2.2nC$

  FOM conduction = 1.395×10^{-9}, FOM switching = 3.3×10^{-10}

- IPA075N15N3G (150V, 43A) - $R_{dson} = 7.5m\Omega$, $Q_g = 93nC$, $Q_{gd} = 11nC$

  FOM conduction = 6.975×10^{-10}, FOM switching = 8.25×10^{-11}

- IPA075N15N3G (150V, 50A) - $R_{dson} = 20m\Omega$, $Q_g = 31nC$, $Q_{gd} = 6nC$

  FOM conduction = 6.2×10^{-10}, FOM switching = 1.2×10^{-10}

Usually the GaN HEMT devices are normally ON devices. As a circuit designer this not a desired feature so in order to make this normally OFF a cascade connection is being used to manufacture normally-off GaN device. In this cascade connection a low voltage Si based normally OFF NMOS device is connected in series so that the GaN HEMT is normally off [27]. But the performance characteristics by adding this feature degrade the actual performance of the GaN device. The devices used in the hardware prototype are a normally-off device. Figure of the Normally Off type switch is as shown Figure 4.2 [28].

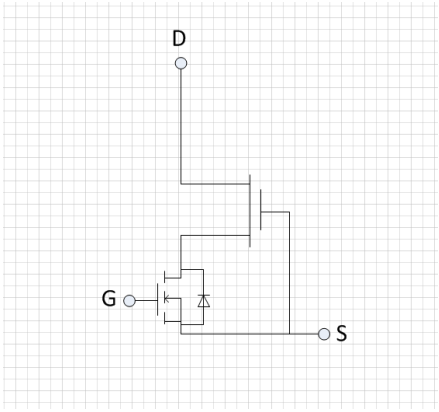

Figure 4.2. Normally OFF GaN used in the prototype [28]

4.2. CHALLENGES WITH GaN [24]

Some of the challenges while dealing with GaN devices could be high switching speed capability, so parasitic is one other serious problem to be dealt about and as the thermal conductivity of GaN is less when compared to SiC so heat management is other critical issue to be kept in mind while using GaN.

4.3. HARDWARE COMPARISON

Conducted a practical testing in topology 1 and measured efficiency of the prototype by only changing MOSFET's in the set-up. One iteration with a Si based

device and other with a GaN device. Tables 4.2 and 4.3 shows the results of efficiency with Si and a GaN device respectively.

MOSFET used – **(Si based) IPA50R140CP – (550V, 23A, 0.140Ω) (Topology 1)**

R_o = 1600Ω, d = 64.1%, f_{sw} = 50kHz, V_{gs} = 12V, N=2.1

Table 4.2.Efficiency with Si based MOSFET

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_o (V)	I_o (A)	P_o (W)	η (%)
20.27	**5.71**	**115.72**	**400.7**	**0.25**	**100.175**	**86.55**

The Figure 4.3 mentioned below shows the drain to source voltage of the Si based switches. Each division is 50V, so the maximum spike level observed for one of the switches was $1.95 \times 50 = 97.5V$.

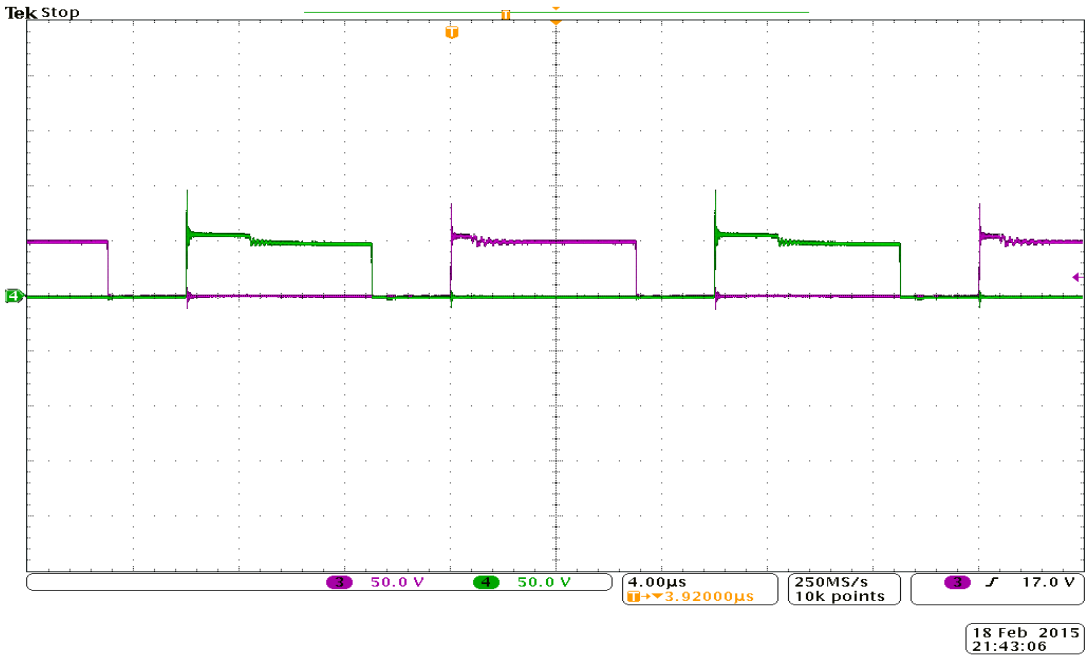

Figure 4.3.Voltage of drain to source with Si based MOSFET

MOSFET used - **(GaN based)** TPH3006PS – **(600V, 17A, 0.150Ω)**

Ro = 1600Ω, d = 65.4%, fsw = 50kHz, Vgs = 12V, N = 2.1 (Topology 1)

Table 4.3.Efficiency with GaN based MOSFET

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_o (V)	I_o (A)	P_o (W)	η (%)
20.27	**5.82**	**117.97**	**400.2**	**0.25**	**100.05**	**84.81**

The Figure 4.4 mentioned below shows the drain to source voltage of the Si based switches. Each division is 50V, so the maximum spike level observed for one of the switches was $2.05 \times 50 = 102.5V$.

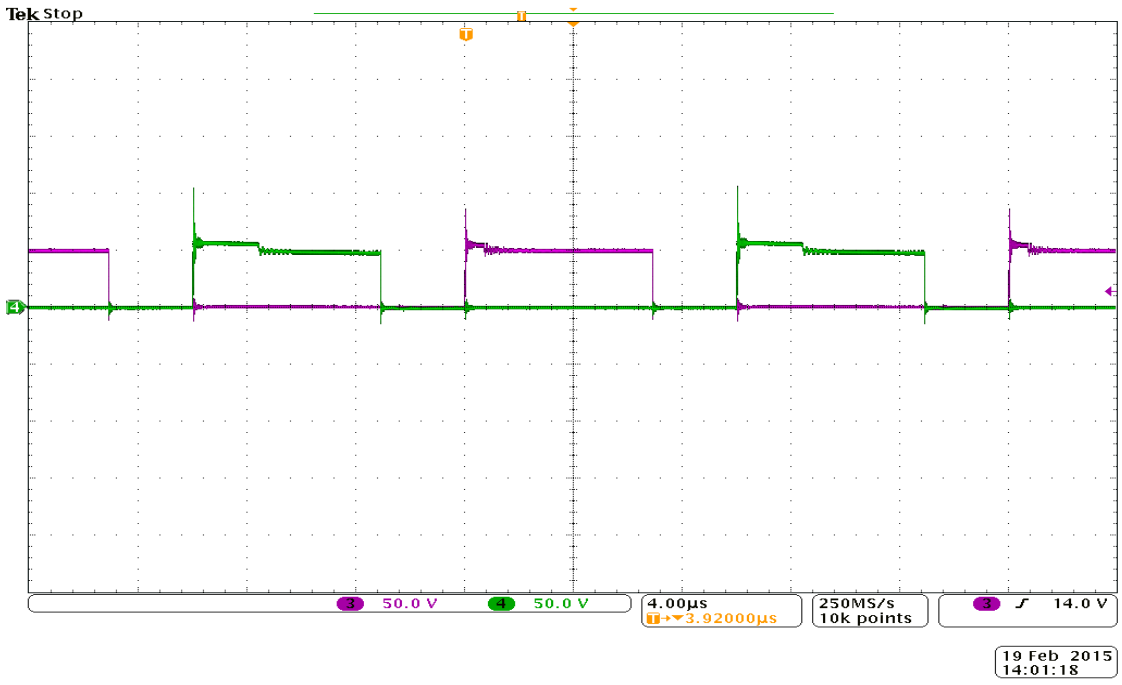

Figure 4.4.Voltage of drain to source with GaN based MOSFET

The efficiency comparison of the Si to GaN device is compared on the same hardware prototype just by changing the MOSFET's in the circuit and respective gate drive circuitry. All other components were exactly same in both the tests for a fair comparison. Also, the MOSFETS are selected about the same drain to source breakdown voltage. The R_{DS_on} of a GaN device was more than the Si counterpart. It is found that the efficiency with GaN device was less than the Si device which is in coherence of the fact that Si device in series with GaN further degrades its performance characteristics.

5. CONCLUSION

In this thesis, two high gain dc-dc converter topologies proposed previously by my colleagues have been analyzed and compared in terms of efficiency, component stresses. Prototypes of the converters were built to carry out the practical analysis. Based on the theoretical analysis and practical measurements it has been observed that both the topologies are almost similar in terms of efficiency. The additional secondary winding in coupled inductors of topology 1 which reduces the duty cycle for a particular input voltage to obtain an output voltage of 400V has not degraded the efficiency seemed a great advantage for topology1. Also, an attempt was made to compare the Si based MOSFETs with GaN (Normally Off) based MOSFETS by replacing only the MOSFETs in the prototype built. The efficiency with Si MOSFET was better in comparison to GaN (Normally Off). This is in coherence of the fact that the silicon NMOS in series with a GaN switch further degrades the performance characteristics of the GaN device.

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