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Hardware integration of ultracapacitor based energy storage to provide grid support and to improve power quality of the distribution grid

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HARDWARE INTEGRATION OF ULTRACAPACITOR BASED ENERGY STORAGE TO PROVIDE GRID SUPPORT AND TO IMPROVE POWER QUALITY OF THE DISTRIBUTION GRID

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ABSTRACT

Grid integration of distributed energy resources (DERs) is increasing rapidly. Integration of various types of energy storage technologies like batteries, ultracapacitors (UCAPs), superconducting magnets and flywheels to support intermittent DERs, such as solar and wind, in order to improve their reliability is becoming necessary. Of all the energy storage technologies UCAPs have low energy density, high power density and fast charge/discharge characteristics. They also have more charge/discharge cycles and higher terminal voltage per module when compared to batteries. All these characteristics make UCAPs ideal choice for providing support to events on the distribution grid which require high power for short spans of time. UCAPs have traditionally been limited to regenerative braking and wind power smoothing applications.

The major contribution of this dissertation is in integrating UCAPs for a broader range of applications like active/reactive power support, renewable intermittency smoothing, voltage sag/swell compensation and power quality conditioning to the distribution grid. Renewable intermittency smoothing is an application which requires bi-directional transfer of power from the grid to the UCAPs and vice-versa by charging and discharging the UCAPs. This application requires high active power support in the *10s-3min* time scale which can be achieved by integrating UCAPs through a shunt active power filter (APF) which can also be used to provide active/reactive power support. Temporary voltage sag/swell compensation is another application which requires high active power support in the *3s-1min* time scale which can be provided integrating UCAPs into the grid through series dynamic voltage restorer (DVR). All the above functionalities can also be provided by integrating the UCAPs into a power conditioner topology.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Page

Paper I

Paper III

LIST OF TABLES

Page

NOMENCLATURE

Symbol	***Description***
DER	Distributed Energy Resource
UCAP	Ultracapacitor
APF	Active power filter
DVR	Dynamic Voltage Restorer
UPQC	Unified Power Quality Conditioner
PC	Power Conditioner
PLL	Phase Locked Loop
P_{DER}	Active power output from DER
P_{UCAP}	Active power output from UCAP
P_{ref}, Q_{ref}	Active and Reactive power commanded references
P_{grid}, P_{load}, P_{inv}	Grid, Load and Inverter Active Powers
Q_{grid}, Q_{load}, Q_{inv}	Grid, Load and Inverter Reactive Powers
E_{cap}	UCAP bank terminal voltage
I_{ucav}	Average current out of the UCAP bank
V_{fdc}, V_{dc}	Dc-link voltage
I_{dclnk}, $I_{dclnkav}$	Dc-link current and average dc-link current
θ	PLL tracking of the system frequency
φ	Phase difference between inverter current and voltage
v_{sd}, v_{sq}	D-q components of the system voltage
i_{dref}, i_{qref}	D-q components of the commanded reference currents
I_{refa}, I_{refb}, I_{refc}	Commanded reference currents of a, b, c phases

I_{apf2a}, I_{apf2b}, I_{apf2c}	Active power filter currents of a, b, c phases
I_{sa}, I_{sb}, I_{sc}	Source or grid currents of a, b, c phases
I_{La}, I_{Lb}, I_{Lc}	Load currents of a, b, c phases
E_{UCAP}	Energy stored in the UCAP in W-min
$V_{uc,ini}$, $V_{uc,fin}$	UCAP initial and final voltages while discharging power
P_{dcin}	Power flowing into the dc-link
V_{sa}, V_{sb}, V_{sc}	Line-neutral source voltages of a, b, c phases
V_{sab}, V_{sbc}, V_{sca}	Line-line source voltages
V_{Lab}, V_{Lbc}, V_{Lca}	Line-line load voltages
V_{inj2a}, V_{inj2b}, V_{inj2c}	Line-neutral injected voltages of a, b, c phase
V_{srms}, V_{Lrms}	RMS values of source and load voltages
$C_1(s)$, $C_2(s)$	Voltage and current compensator transfer functions

1. INTRODUCTION

Most of the appliances today are powered by electricity and electrical power is transmitted over long distances to power the appliances. During the initial days of commercialization and mass-production of electricity, Nikola Tesla proved to the world that electrical power can be transmitted over long distances in a much more efficient way if polyphase alternating current transmission is used instead of direct current transmission. Since then most of the electrical energy is transmitted over long distances using 3-phase alternating current. One of the major drawbacks of electrical energy in an alternating current system is that it cannot be stored electrically. However, it can be converted to electrochemical energy (batteries), electromagnetic energy (super conducting magnets), electrostatic energy (ultracapacitors), kinetic energy (flywheels) and potential energy (pumped hydro). The concept of integrating energy storage at the transmission level for advanced power applications has been explored and in this regard efforts have been made to integrate energy storage into flexible AC transmission (FACTS) power flow controllers. With the integration of energy storage the FACTS power flow controller will have active power capability which enhances its power transfer capability. However, the energy storage integration at the distribution grid level has been rare and the concept of integrating distributed energy storage (DESs) and distributed energy resources (DERs) into the distributed grid is slowly becoming a reality.

Renewable energy generation is growing fast and ideas such as smart grid are trying to change the role of a consumer from being a passive consumer to an active contributor who can supply stored excess power in various DERs, such as solar, wind and

PHEVs back to the distribution grid or the micro-grid. Most of the DERs are intermittent and integrating them with energy storage not only improves the reliability of the DERs but also gives an opportunity to provide additional functionalities such as active and reactive power support and voltage sag/swell compensation to distribution grid. Of all the energy storage technologies UCAPs have low energy density and high power density and fast charge/discharge characteristics. Therefore, they are ideally suited for providing support to events on the distribution grid which require high power and low energy for short spans of time. UCAPs also have higher number of charge-discharge cycles and higher terminal voltage per module when compared to batteries which again make them ideal choice for providing grid support for short time.

The main contribution of this dissertation is in the hardware integration of UCAP-based energy storage into the distribution grid. UCAP based energy storage can be integrated into the distribution grid through a bi-directional dc-dc converter and a dc-ac inverter and this integration can be carried out by connecting the dc-ac inverter in series as a dynamic voltage restorer (DVR) or in shunt as an active power filter (APF) with the grid. The first paper focuses on integrated UCAP and APF design and the integrated system will have active power capability and it will be able to provide *active power support*, *reactive power support* and *renewable intermittency smoothing* to the distribution grid. The integrated APF-UCAP system with active power capability was simulated in PSCAD and hardware integration of the complete system was performed. Designs of major components in the power stage and the control strategy of the bi-directional dc-dc converter are discussed. The simulation of UCAP-APF system which consists of the UCAP, bi-directional dc-dc converter, and the grid-tied inverter is

performed using PSCAD. A hardware experimental setup of the same integrated system is presented and the ability to provide active power support, reactive power support and renewable intermittency smoothing to the distribution grid is dynamically tested. The second paper focuses on integrated UCAP and DVR design and the integrated system will again have active power capability which gives UCAP-DVR system ability to independently compensate voltage sags and voltage swells. The simulation of the UCAP-DVR system which consists of the UCAP, dc-dc converter, and the inverter connected in series with grid is performed using PSCAD. Hardware experimental setup of the integrated system is presented and the ability to provide temporary voltage sag and swell compensation to the distribution grid is dynamically is tested.

Both the APF and the DVR inverters can be integrated at the dc-link of the inverter to form a power quality conditioner and the UCAP bank can be integrated into the dc-link as well through a bi-directional dc-dc converter and the system will have active power capability. With this integration the power conditioner will be able to provide the combined functionalities of APF and DVR systems with energy storage. Therefore, the power conditioner and UCAP based energy storage can improve the power quality of the distribution grid by providing active, reactive power support, intermittency smoothing as well as voltage sag and swell compensation. The power stage and control strategy of the dc-dc converter, the series DVR and the shunt APF are discussed. Hardware integration of the UCAP based energy storage with the power conditioner systems is performed and hardware experimental results are presented. It is observed that experimental results match very well with PSCAD simulations.

PAPER

I. An Integrated Active Power Filter–Ultracapacitor Design to Provide Intermittency Smoothing and Reactive Power Support to the Distribution Grid

D. Somayajula, Student Member, *IEEE*, M. L. Crow, Fellow, *IEEE*

***Abstract*—Grid integration of distributed energy resources (DERs) is increasing rapidly. Furthermore, smart grid technologies are making the grid more bi-directional providing opportunities to consumers to supply power back to the grid. Energy storage technologies like battery and ultracapacitor (UCAP) can be integrated through grid tied-inverters to support variable DERs such as solar and wind. In these cases, the energy storage with active power capability can improve grid performance by providing active and reactive power support. In this paper, the concept of providing active/reactive power support to the distribution grid by UCAPs is presented. UCAPs have higher number of charge-discharge cycles and higher terminal voltage per module when compared to batteries which make them ideal for providing grid support. The UCAP is integrated into the dc-link of the active power filter (APF) through a dc-dc converter. The dc-dc converter provides a stiff dc-link voltage which improves the performance of the grid-tied inverter. Design and control of both the dc-ac inverter and the dc-dc converter are very important in this regard and presented. The simulation model of the overall system is developed and compared to the experimental hardware setup.**

Index Terms-**UCAP, grid-tied inverter, distribution grid, dc-dc converter, APF, d-q control, average current mode control**

I. INTRODUCTION

The integration of distributed energy storage (DES) and distributed energy resources (DER) into the grid is slowly becoming a reality [1]. Renewable energy

generation is growing rapidly and concepts such as the smart grid are changing the role of consumers from passive customer to an active contributor who can supply excess power back to the grid. Most of the DERs are variable and combining them with energy storage technologies like batteries, flywheels, superconducting magnets and ultracapacitors (UCAPs) [2] gives an opportunity to provide active and reactive power support to the distribution grid. Renewable intermittency smoothing of the distribution grid is another application where energy storage integration is needed in the *seconds* to *minutes* time scale [3]. Various rechargeable energy storage technologies like batteries, superconducting magnets, flywheels and UCAPs have active power capability. Among these UCAPs are ideally suited for applications like renewable intermittency smoothing which need active power support in the *seconds* to *minutes* time scale [2], [4]. UCAPs also have higher number of charge/discharge cycles and higher terminal voltage per module when compared to batteries and the cost of UCAPs has been declining rapidly in the last few years [5] making them a better choice when compared to batteries. UCAPs are currently being used mainly in wind power smoothing applications [6] or for regenerative braking applications in hybrid electric vehicles [7]. The concept of providing active and reactive power support to the distribution grid through UCAP energy storage has not been explored. The main contribution of this paper is the development and hardware integration of active power filter (APF) with UCAP energy storage which gives the integrated APF-UCAP system active power capability which aids in providing renewable intermittency smoothing, active and reactive power support to the distribution grid. This cannot be achieved by a conventional APF with dc-link capacitor which does not have active power capability.

In this paper, the UCAP integration with an APF through a bi-directional dc-dc converter is proposed. Similar integration methods for other DERs have been proposed in the literature, but mostly for PV and wind applications [8]-[9]. In [8], the control of a three-phase grid connected inverter is modified such that the PV system can be connected to the inverter directly without the need for a dc-dc converter for maximum power point tracking. In [9], the active and reactive power limits of a grid-connected inverter connected to a wind energy system are calculated. Integrating battery energy storage at the dc-link of a grid-tied inverter to provide real and reactive power support is proposed in [10]. However, the discussion in [10] is centered on the design of the high-power voltage source converter/inverter for the transmission grid and not the distribution grid. Integration of a UCAP through a dc-dc converter into a power conditioning system is proposed in [11], but the focus is again only on the voltage-source inverter and experimental results for the UCAP and dc-dc converter are not provided. A voltage source multilevel converter-based shunt APF with UCAP at the dc-link is explored in [12]. However, the dc-link capacitor is replaced by an UCAP to improve the performance during voltage dips. Integration of a UCAP bank into a unified power quality conditioner (UPQC) system through dc-dc converter is proposed in [13], but providing active and reactive power support for the grid through the shunt APF is not fully explored. In this paper, UCAP energy storage integration into the grid that extends these earlier developments and addresses the following missing application areas is proposed.

- Integration of UCAP with the APF system gives the system active power capability which is necessary for providing active power support and renewable intermittency smoothing

- Experimental validation of the UCAP, dc-dc converter, inverter their interface and control
- Development of inverter and dc-dc converter controls to provide Renewable Intermittency Smoothing as well as Active and Reactive power support to the distribution grid
- Hardware integration and performance validation of the integrated APF-UCAP system

Most DERs are connected to the grid through a three-phase grid-tied inverter which can be controlled to meet various control objectives such as supplying active power, reactive power, harmonic compensation, and frequency regulation etc. A three-phase shunt active power filter (APF) can be controlled in such a way that it meets all the same control objectives. Furthermore, a three-phase grid-tied inverter is similar in topology to a three-phase shunt APF which opens up the possibility of exploring the vast amount of literature available for shunt APFs (see [14]-[17] as representative articles) and modifying the control strategies to suit the present control objectives of the grid-tied inverter.

II. THREE-PHASE GRID CONNECTED INVERTER

A system diagram of the proposed system is shown in Fig. 1. The APF-UCAP system is shunt connected between the system source and the load. The system consists of a UCAP on the input side of the bi-directional dc-dc converter which acts as an interface between the UCAP and the 3-phase grid connected inverter. The major advantage of integrating the UCAP and the APF system is that the system now has the capability to supply and absorb *Active Power* from the grid. And a bi-directional dc-dc

converter interface is necessary since the UCAP voltage profile changes as it charges/discharges energy while the inverter dc-link voltage has to stay constant for accurate control of inverter. Therefore, it acts as a boost converter while the UCAP is discharging energy into the grid and as a buck converter while charging the UCAP from the grid.

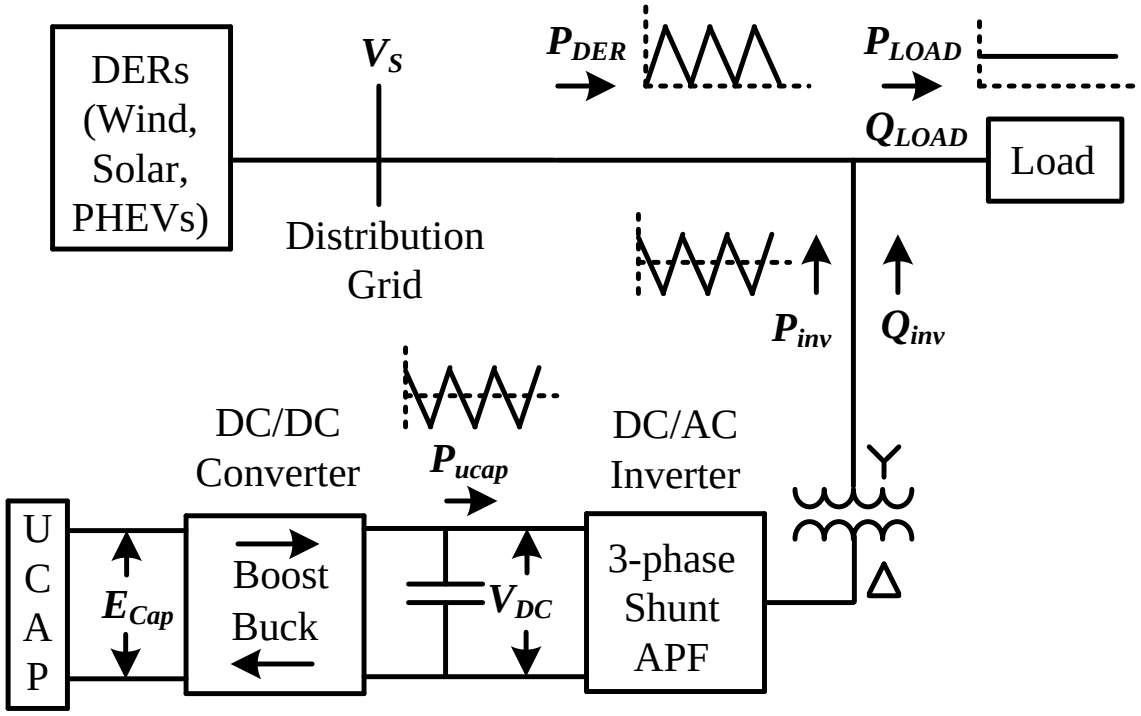

Fig. 1 One line diagram of the APF-UCAP system

A. Power Stage

The power stage which consists of a 3-phase inverter and its controller is shown in Fig. 2. The inverter system consists of an IGBT module, its gate-driver, LC filter and an isolation transformer. The dc-link capacitor voltage has to be regulated for optimum performance of the converter such that:

$$V_{dc} = \frac{2\sqrt{2}}{\sqrt{3}m * n} v_{ab(rms)} \quad (1)$$

where *m* is the modulation index and *n* is the turns ratio of the isolation transformer. In this application for low voltage distribution grids, the line-line rms voltage is 208V, *m* is 0.75, and *n* is $\sqrt{3}$ for the delta-wye transformer which yields the required dc-link voltage V_{dc} of 260V.

B. Controller Implementation

There are various methods to control the 3-phase shunt APF to provide harmonic and reactive power compensation of which the most common approaches are the p-q method [14]-[15] and the i_d-i_q method [16]. In [16], the authors state that the i_d-i_q control performs better in non-sinusoidal and unbalanced conditions when compared to the p-q method, while both methods perform in a similar manner in balanced sinusoidal conditions. In this system, the i_d-i_q method is modified to provide active and reactive power compensation instead of the reactive and harmonic compensation described in [16] such that i_d controls the reactive power and i_q controls the active power [9]. Therefore, based on the references for active and reactive powers P_{ref} and Q_{ref} the reference currents i_{qref} and i_{dref} in d-q domain can be calculated using (2) and (3) where v_{sq} is the system voltage in q-domain. Ideally a higher level integrated controller will be determining the values of P_{ref}, Q_{ref} based on various system inputs like P_{grid}, Q_{grid}, P_{load}, Q_{load}, V_{dc}, V_{ucap}, I_{dclnk} as shown in Fig. 2

$$P_{ref} = -\frac{3}{2}(v_{sq} i_{qref} + v_{sd} i_{dref}) \quad (2)$$

If $v_{sd} = 0$, then $P_{ref} = -\frac{3}{2} v_{sq} i_{qref}$. Similarly,

$$Q_{ref} = \frac{3}{2}(v_{sd} i_{qref} - v_{sq} i_{dref}) \quad (3)$$

and if $v_{sd} = 0$, then $Q_{ref} = -\frac{3}{2} v_{sq} i_{dref}$.

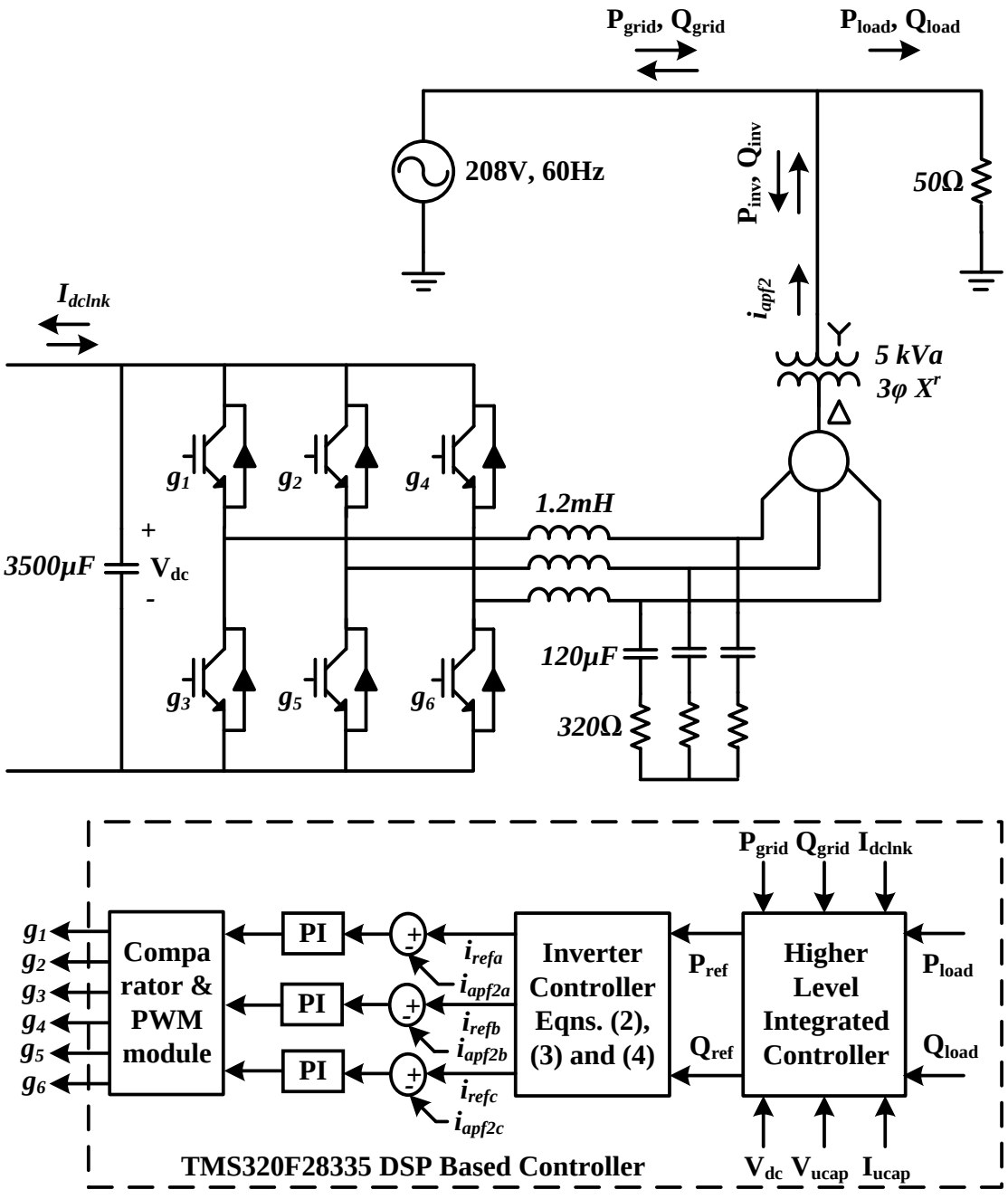

Fig. 2 Three-phase grid-connected inverter and the Inverter Controller

The reference currents in the *d-q* domain can be transformed into the reference currents i_{refa}, i_{refb} and i_{refc} in the *a-b-c* domain using:

$$\begin{bmatrix} i_{refa} \\ i_{refb} \\ i_{refc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{dref} \\ i_{qref} \end{bmatrix} \quad (4)$$

Eqn. (4) requires a PLL to estimate the value of θ and the PLL used in this paper is based on the fictitious power method proposed in [15]. The main advantage of the fictitious power method is it tracks the positive sequence voltage V_{+1} instead of the actual system voltage which is very useful in unbalanced systems. Once the reference currents i_{refa}, i_{refb} and i_{refc} are calculated they are compared with the actual inverter currents i_{apf2a}, i_{apf2b} and i_{apf2c} and the error is passed through a PI controller. There are various methods for current control like hysteresis, sigma-delta and PI control. Among these PI control is the most stable however; it requires the tuning of PI gains based on the system parameters. For the present system the K_p and K_i values were found out to be 0.2 and 50 respectively. Therefore, the transfer function of PI controller is given by:

$$T(s) = 0.2 + \frac{50}{s} \quad (5)$$

Then the PI controller output is passed through a comparator and Pulse width modulator (PWM) which will generate the gate signals for the inverter and this will allow the inverter to supply the commanded active power P_{ref} or reactive power Q_{ref}. In the present scenario for the sake of demonstration and proof of concept validation the system is operated in open loop and P_{ref} and Q_{ref} are commanded directly in the controller instead of these values coming from a higher level integrated controller as proposed in the

control block diagram. Therefore, the actual active power P_{inv} and reactive power Q_{inv} supplied by the inverter may not be the same as the commanded P_{ref} and Q_{ref} . They are estimated as:

$$P_{inv} = 3V_{sa(rms)}I_{apf2a(rms)}\cos\varphi$$
$$Q_{inv} = 3V_{sa(rms)}I_{apf2a(rms)}\sin\varphi \quad (6)$$

In (6), V_{sa} is line-neutral voltage of the grid, I_{apf2a} is the inverter current on the secondary side of the isolation transformer and φ is the phase difference between the V_{sa} and I_{apf2a} waveforms. The complete inverter control algorithm is implemented in a DSP TMS320F28335 which has a clock frequency of 150MHz, an inbuilt A/D module, PWM module and real-time emulation, which are all well-suited for this application. The sampling frequency in the inbuilt A/D module was set at 60 kHz and the switching frequency in the PWM module is set at 12 kHz for the present application.

III. UCAP AND BIDIRECTIONAL DC-DC CONVERTER

A. UCAP Bank Hardware Setup

UCAPs can deliver very high power in a short time span; they have higher power density and lower energy density when compared to Li-ion batteries [18], [19]. The major advantage UCAPs have over batteries is their power density characteristics, high number of charge-discharge cycles over their lifetime and higher terminal voltage per module [5], [18]. These are ideal characteristics for providing active/reactive power support and intermittency smoothing to the distribution grid on a *short term* basis. In [20], it is proposed that UCAPs are currently viable as short term energy storage for bridging power in kW range in the *seconds* to *few minutes* timescale. The choice of the number of

UCAPs necessary for providing grid support depends on the amount of support needed, terminal voltage of the UCAP, dc-link voltage and distribution grid voltages. In the present case the choice was made based on the following parameters. From (1) it is clear that the dc-link voltage needs to be 260V for the 208V distribution grid for optimal performance of the inverter. The terminal voltage of each BMOD0165P048 module is 48V which means connecting three modules in series would bring the initial voltage of the UCAP bank to 144V and connecting four modules in series would bring the initial voltage of the UCAP bank to 192V. For a 260V dc-link voltage these two options are ideal for integrating the UCAP bank through the dc-dc converter since the duty ratio of the converter would be either too low or too high for other cases. It is cost effective as well to use 3 modules in the UCAP bank when compared to 4 modules. In this paper, the experimental setup consists of three 48V, 165F UCAPs (BMOD0165P048) manufactured by Maxwell Technologies which are connected in series. Assuming that the UCAP bank can be discharged to 50% of its initial voltage ($V_{uc,ini}$) to final voltage ($V_{uc,fin}$) from 144V to 72V which translates to depth of discharge of 75%, the energy in the UCAP bank available for discharge is given by:

$$E_{UCAP} = \frac{1}{2} * C * \frac{({V_{uc,ini}}^2 - {V_{uc,fin}}^2)}{60}\ W - min$$

$$E_{UCAP} = {}^1\!/_2 * {}^{165}\!/_3 * {}^{(144^2 - 72^2)}\!/_{60} \quad (7)$$

$$= 7128\ \text{W-min}$$

A bi-directional dc-dc converter is required as an interface between the UCAP and the dc-link since the UCAP voltage varies with the amount of energy discharged while the dc-link voltage has to be stiff. Therefore, bi-directional dc-dc converter is designed to

operate in boost mode when the UCAP bank voltage is between 72V to 144V and the output voltage is regulated at 260V. And when the UCAP bank voltage is below 72V the bi-directional dc-dc converter is operated in Buck mode and draws energy from the grid to charge the UCAPs and the output voltage is again regulated at 260V.

B. Bi-directional Dc-dc Converter Hardware Setup

Various topologies have been proposed for the dc-dc converter for integrating UCAP based energy storage into the grid. A drive system and an auxiliary energy storage system with UCAPs have been proposed in [21]-[22]. In the present paper, a non-isolated bi-directional dc-dc converter which acts as a boost converter while discharging energy from the UCAP and as a buck converter while charging energy from the grid is used. The integrated UCAP and APF system is supposed to respond dynamically to provide *active* and *reactive power support* to the grid as well as provide *renewable intermittency smoothing*. In the case of renewable intermittency smoothing application the bi-directional dc-dc converter should be able to withstand fluctuations in the power outputs of the DERs by absorbing excess power from DERs into UCAP and discharging power from UCAP when the power output from DERs is lower than load requirement.

The model of the bi-directional dc-dc converter and its controller is shown in Fig. 3 (a) where the output of the dc-dc converter is connected to the dc-link of the inverter. The input consists of three 48V 165F UCAPs with a total ESR of 21.3 $m\Omega$. The inductance of 181 μH is chosen for operating the converter in continuous conduction mode (CCM) for heavy load cases and in discontinuous conduction mode (DCM) for light load case. The size of the inductor is an important factor in the dc-dc converter design and as the inductor size increases, the amount of ripple in the inductor current also decreases [17]. Generally it is preferred to operate the converter in CCM with low ripple,

but operating the converter in CCM at light load requires a large inductor. Therefore, in this system the ripple in the inductor current is kept constant at 9A and the converter is allowed to operate in both CCM and DCM for optimum sizing of the inductor over a wide operating range.

Switching frequency also impacts the size of the inductor and is set to 31.25 kHz which also produces a good transient response. The input filter capacitor of 88 µF is used to reduce the high frequency inductor ripple current which if drawn from the UCAP bank may reduce its cycle life. Note that as the size of the inductor decreases, the amount of ripple current increases, which has to be supplied by the input filter capacitor. Thus the size of the inductor and the input filter capacitor are interdependent and their design must be optimized accordingly. An output capacitor of 44µF is used to filter out the high frequency ripple in the output current which is discontinuous and therefore, has higher ripple when compared to the input current. However, the dc-link capacitor provides a portion of the ripple current and the input is more sensitive to high frequency ripple so it has a larger capacitor compared to output. A nominal resistive load of 213.5Ω is used to prevent the converter from operating on no-load.

C. Controller Implementation

Average current mode control is used to regulate the output voltage of the bi-directional dc-dc converter in both *Buck* and *Boost* modes while *Charging* and *Discharging* the UCAP bank. While the UCAP-APF system is *Discharging* power the dc-link voltage V_{out} tends to be less than V_{ref} which causes the reference current I_{ucref} to be positive thereby operating the dc-dc converter in *Boost Mode*. Along similar lines when the UCAP-APF system is absorbing power from the grid the dc-link voltage V_{out} tends to be greater than V_{ref} which causes the reference current I_{ucref} to be negative and thereby

operating the dc-dc converter in *Buck mode*. Average current mode control technique is widely explored in the literature [17] and it was found as the ideal method for UCAP-APF integration as it tends to be more stable when compared to other methods like voltage mode control and peak current mode control. Average current mode controller and the higher level integrated controller are shown in Fig. 3 (a) where the actual output voltage V_{out} is compared with the reference voltage V_{ref} and the error is passed through the voltage compensator $C_1(s)$ which generates the average reference current I_{ucref}. This is then compared to the actual UCAP current (which is also the inductor current) I_{uc} and the error is then passed through the current compensator $C_2(s)$.

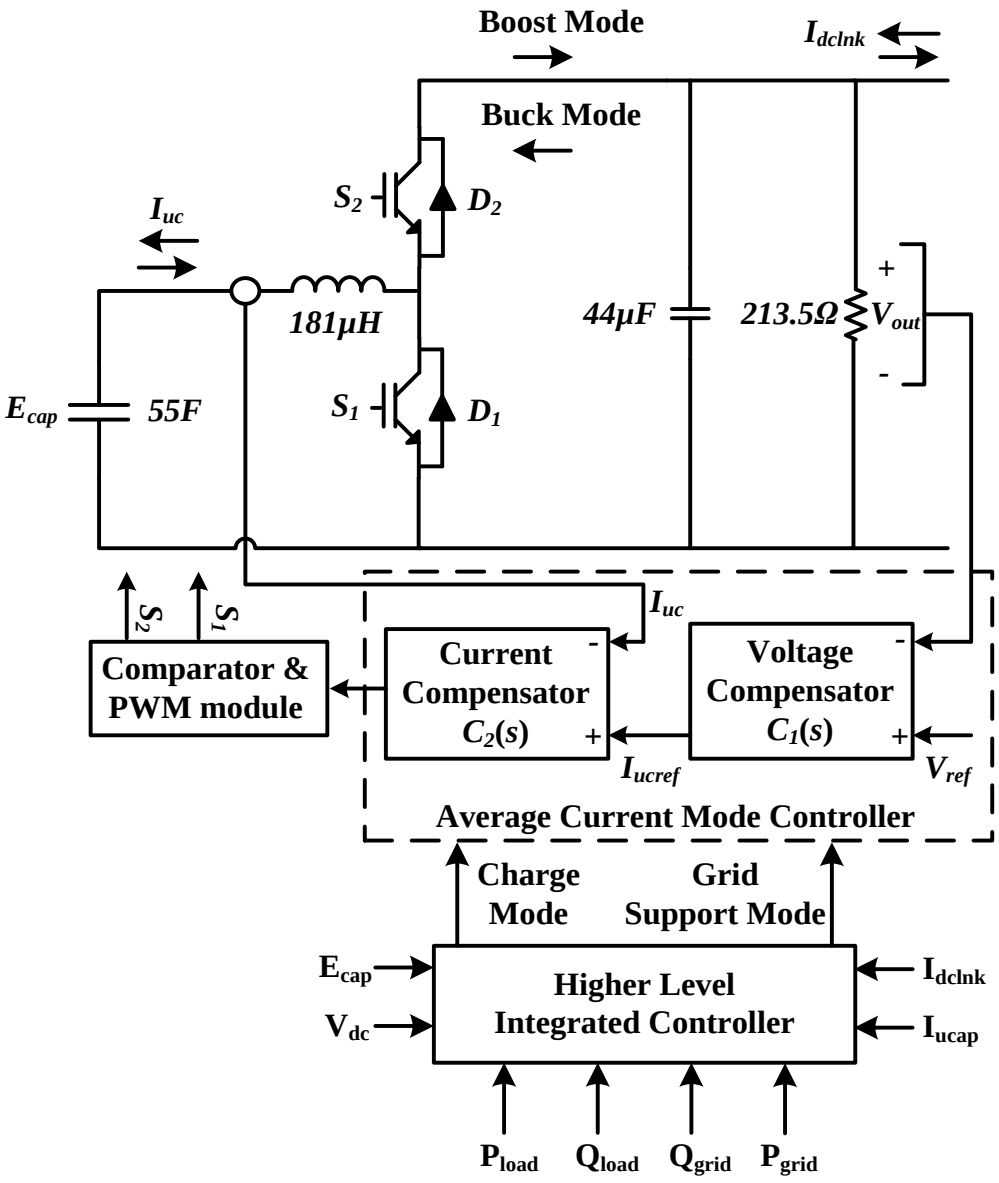

Fig. 3 (a) Model of the bi-directional dc-dc converter and its controller

The converter model for average current mode control is based on the following transfer functions developed in [23]:

$$G_{id}(s) = \frac{V_{out}\left(sC + \frac{2}{R}\right)}{s^2LC + s\frac{L}{R} + (1-D)^2} \tag{8}$$

$$G_{vi}(s) = \frac{(1-D)\left[1 - \frac{sL}{R(1-D)^2}\right]}{\left(sC + \frac{2}{R}\right)} \quad (9)$$

The model of the dc-dc converter in Average current mode control is shown in Fig. 3 (b) which has two loops. The inner current loop $T_i(s)$ which has the current compensator $C_2(s)$, voltage modulator gain V_M and the transfer function $G_{id}(s)$. The outer voltage loop $T_v(s)$ constitutes the voltage compensator $C_1(s)$, current loop $T_i(s)$ and the transfer function $G_{vi}(s)$. The current compensator design $C_2(s)$ must be carried out initially and the voltage compensator $C_1(s)$ design is based on the design of the current compensator due to the dependency of $C_1(s)$ on $C_2(s)$. The current compensator $C_2(s)$ must be designed in such a way that at the cross-over frequency of the current loop there is enough phase-margin to make the current loop $T_i(s)$ stable and it should have a higher bandwidth when compared to the voltage loop $T_v(s)$. Based on these criteria the transfer functions of the current loop $T_i(s)$ and the current compensator $C_2(s)$ are given by:

$$T_i(s) = G_{id}(s).\frac{C_2(s)}{V_M} \quad (10)$$

$$C_2(s) = 1.67 + \frac{231.81}{s} \quad (11)$$

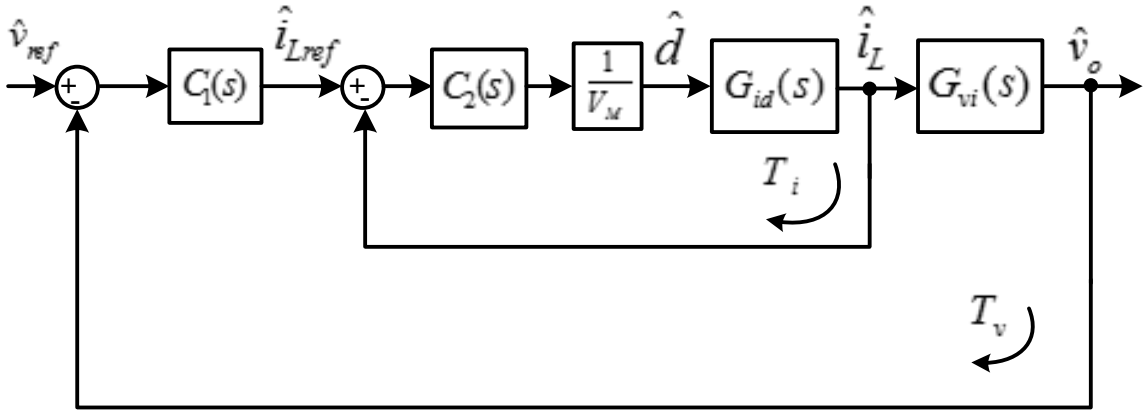

Fig. 3 (b) Block diagram of closed-loop converter in Average Current Mode Control

The closed loop transfer function of the current loop is then given by:

$$T_1(s) = \frac{T_i(s)}{1 + T_i(s)} \tag{12}$$

It can be observed from Fig. 3 (c) that the phase margin is around 90° at the cross-over frequency of the current loop $T_i(s)$ and it has higher bandwidth when compared to the voltage loop $T_v(s)$. The voltage loop compensator $C_1(s)$ design is dependent on the design of $T_1(s)$ and it is a PI compensator whose gain is adjusted to have the desired cross-over frequency. Based on these criterion the transfer functions of the voltage loop $T_v(s)$ and compensator $C_1(s)$ is given by:

$$T_v(s) = G_{vi}(s)C_1(s)T_1(s) \tag{13}$$

$$C_1(s) = 3.15 + \frac{1000}{s} \tag{14}$$

The transfer function of the plant $G_{vi}(s)$ along with the transfer function of $C_1(s)$ of the voltage compensator and the overall voltage loop transfer function $T_v(s)$ are shown in Fig. 3 (c). It can be observed that the voltage loop $T_v(s)$ has a cross-over frequency of around

150 Hz with a phase margin of 73˚ which provides a stable dynamic response. The stability and dynamic performance of the voltage loop $T_v(s)$ determine the stability and dynamic response of the overall system.

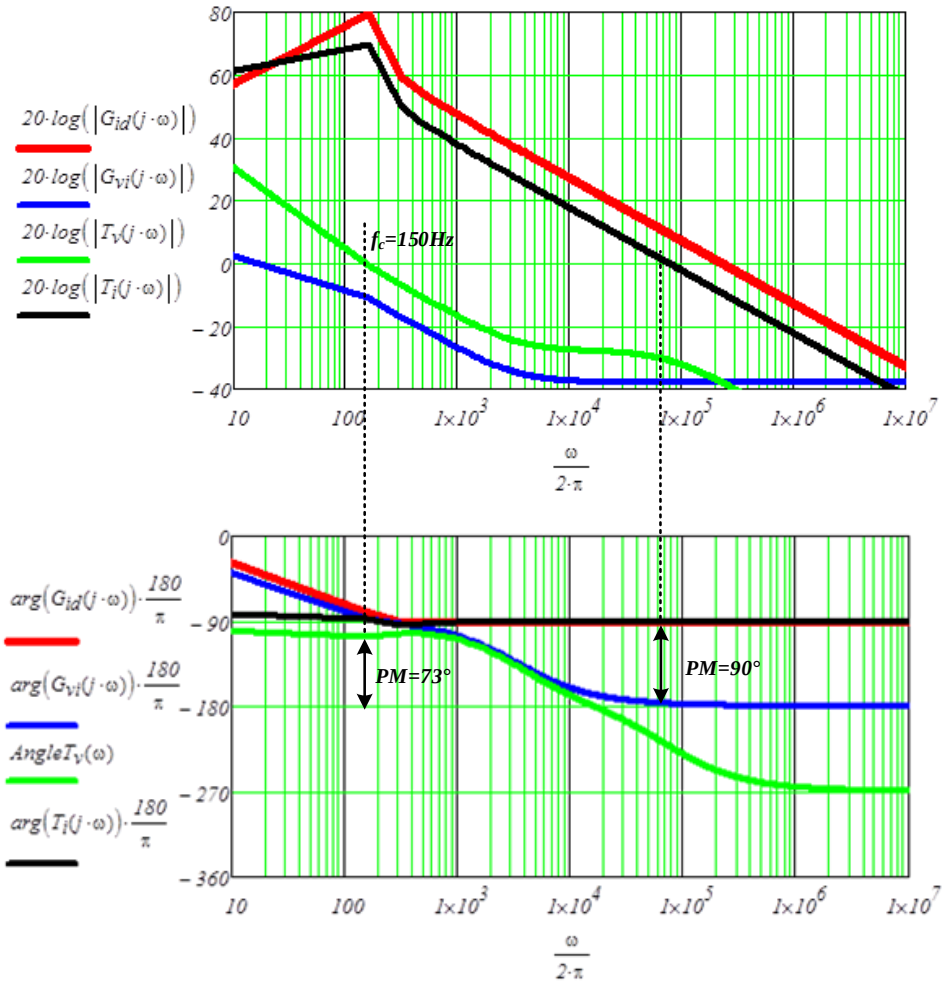

Fig. 3 (c) Model of the bi-directional dc-dc converter and its controller

D. Higher Level Integrated Controller

The higher level integrated controller is designed to make system level decisions on the inverter and dc-dc converter controllers. Based on various system parameters like P_{load}, Q_{load}, P_{grid}, Q_{grid}, V_{ucap}, V_{dc}, I_{dclnk}, I_{ucap} the higher level integrated controller will

decide on operating in one of the following modes *Active Power Support mode*, *Reactive Power Support Mode*, *Renewable Intermittency Smoothing Mode* and *Charge Mode*.

In *Active power support mode* and *Renewable intermittency smoothing mode* the UCAP-APF system must provide active power to the grid. Therefore, the active power capability of the UCAP-APF system must be assessed by the higher level integrated controller. Based on the P_{grid} and P_{load} values the reference P_{ref} is calculated in the higher level integrated controller and it will decide if the UCAP has enough energy to respond to the P_{ref} command based on the UCAP state of charge. If the UCAP has enough capacity to respond to the request then the dc-dc converter controller is operated in *Grid Support Mode* otherwise it is operated in *Charge Mode* where the UCAP is recharged and the power request is met at a later time. In Grid Support Mode the dc-dc converter will operate in a bi-directional fashion in both Buck and Boost modes to respond to the active power requests and regulate the dc-link voltage in a stable fashion while the inverter controller should respond such that the commanded P_{ref} is supplied by the inverter through current control.

In *Reactive power support mode* the UCAP-APF system must provide reactive power to the grid. In this mode the UCAP-APF does not provide any active power to the grid and even the APF losses are supplied by the grid. Based on the Q_{grid} and Q_{load} values the reference Q_{ref} is calculated in the higher level integrated controller. In this mode the dc-dc converter controller can be programmed to operate in *Grid Support Mode* directly since the active power requirement for operating in this mode is minimal. Therefore, the goal of the dc-dc converter controller is to regulate the dc-link voltage in a stable fashion

while the inverter controller should respond such that the commanded Q_{ref} is supplied by the inverter through current control.

In *Charge Mode* the UCAP is recharged by absorbing active power from the grid when the UCAP state of charge falls below 50%. The rate at which the UCAP can be charged is assessed by the higher level integrated controller based on the P_{grid} and P_{load} values and the reference P_{ref} is calculated. Then the dc-dc converter controller is commanded to operate in *Charge Mode* wherein the dc-dc converter will operate in Buck Mode to absorb the power from the grid and the inverter controller must respond to supply commanded P_{ref}.

IV. SIMULATION RESULTS

The simulation of the complete system which includes the 3-phase grid tied inverter and the dc-dc converter is performed using PSCAD. The ability of the system to supply the commanded reactive power is simulated with i_{dref} = -15A which translates to a Q_{ref} of 3819Var from (3). The simulation results are shown in Fig. 4 (a) and (b) where the UCAP is charged until 0.08s, at which point the UCAP voltage E_{cap} reaches a value of 144V. The UCAP is connected to the dc-dc converter at t = 0.10s. At t = 0.12s the inverter is synchronized to the grid. It can be observed from Figs. 4 (a) and 4 (b) that P_{inv}, Q_{inv} and V_{fdc} have converged to the steady state values of -92W, 3570Var and 260V, respectively closely tracking the commanded Q_{ref}.

The inverter current and voltage waveforms when the system provides reactive power support are shown in Fig. 4 (c) where it can be observed that I_{apf2a} tracks the reference current I_{refa} accurately after synchronization with the grid. And I_{refa} and hence I_{apf2a} lags V_{sa} by approximately 90° which is required for reactive power compensation. It

can also be observed from voltage waveforms that the inverter voltage V_{inv1a} is almost sinusoidal after synchronization. The ability of the system to supply commanded active power is then simulated with i_{qref} =-12.0A which translates to P_{ref} of 3054W from (2). The simulation setup is the same as in the previous case and the simulation results are shown in Figs. 5 (a) and 5 (b) where it can be observed that P_{inv}, Q_{inv}, V_{fdc} and $I_{dclnkav}$ have converged to steady state values of 2701W, 466Var, 260V and 10.82A closely tracking the commanded P_{ref}.

Similarly, the simulation results for the renewable intermittency smoothing applications where the UCAP must be capable of both supplying and absorbing active power are shown in Figs. 6 (a) and (b). Since the results for the case where the UCAP and the inverter system supply active power to the grid are already presented in Figs. 5 (a) and (b) so in Figs. 6 (a) and (b) similar results are presented for the case where the UCAP and inverter system absorb active power from the grid which is achieved by commanding a positive i_{qref} of 7A which corresponds to a P_{ref} of -1782W. It can be observed from Figs. 6 (a) and (b) that P_{inv}, V_{fdc} and $I_{dclnkav}$ have converged to steady state values of -1791W, 260V and -6.906A again tracking the commanded P_{ref} closely. The slight difference between the reference values and actual values in all three modes is due to the operation of the system in open loop configuration as explained previously. It should also be noted that simulation results are presented for shorter time span when compared to hardware results due to limitations in PSCAD software. Therefore, it is evident from the simulations that the UCAP and APF system can together respond to changes in i_{qref} and i_{dref} commands and accordingly provide active and reactive power support to the grid. It is also evident that both the dc-dc converter and inverter can operate in a bi-directional

fashion which is necessary when the system is used in renewable intermittency smoothing applications. Active power support, reactive power support and renewable intermittency smoothing are the primary functionalities the UCAP integrated APF system will be providing to the distribution grid. These functionalities of energy storage with user defined or higher level controls will be playing a major role with penetration of distributed energy resources (DERs) on the distribution grid.

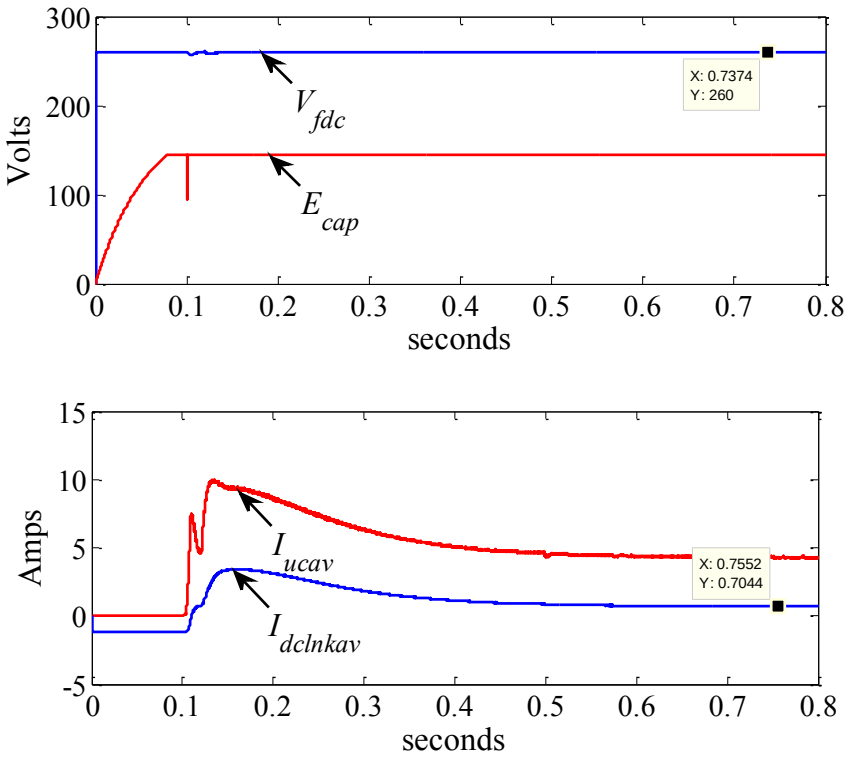

Fig. 4 (a) Currents and voltages of bi-directional dc-dc converter for i_{dref} = -15.0A (reactive power support)

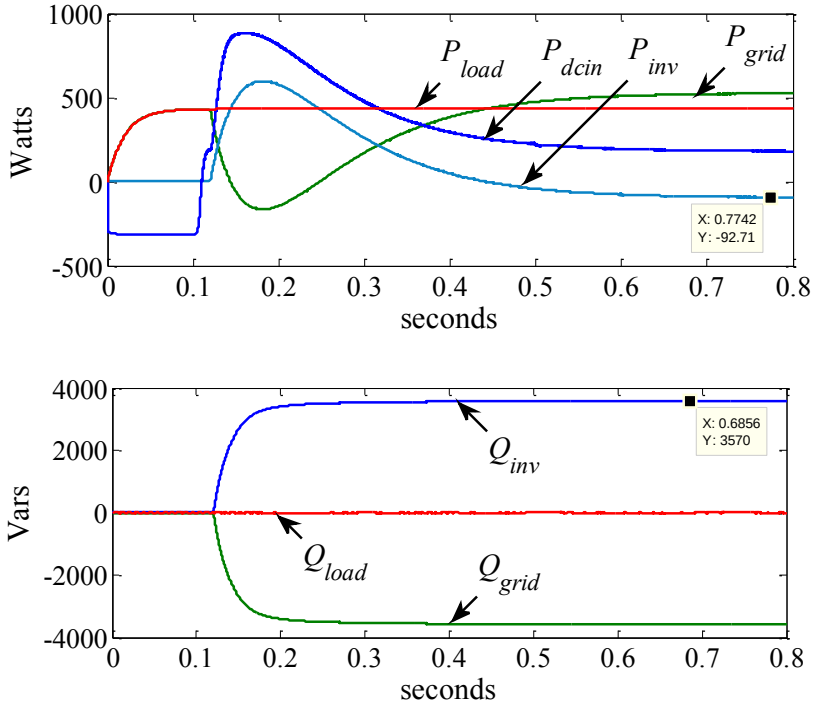

Fig. 4 (b) Grid, load and inverter active and reactive power curves for i_{dref} = -15.0A (reactive power support)

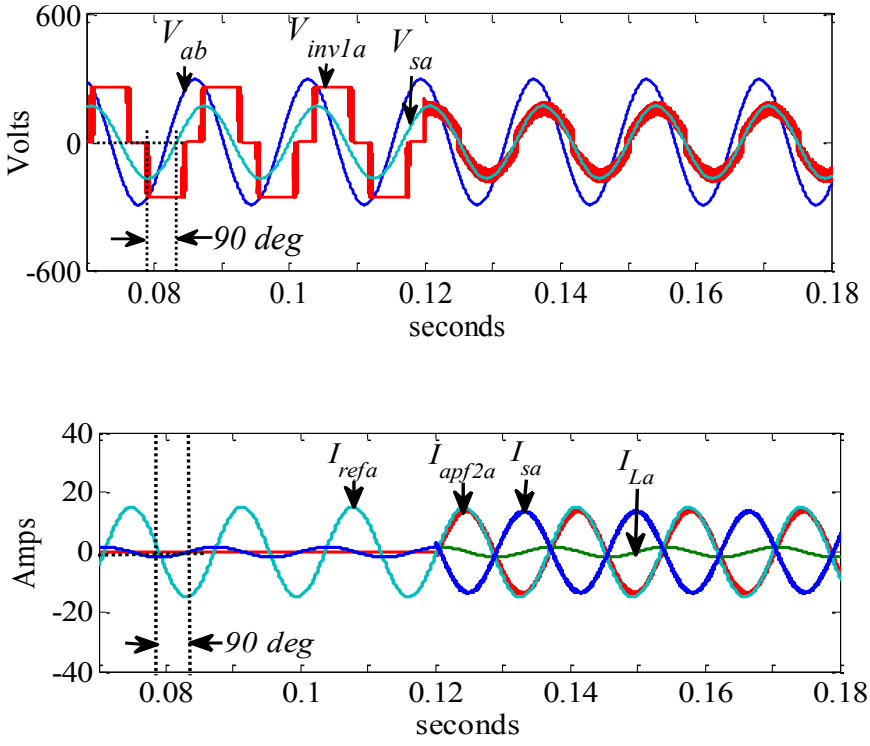

Fig. 4 (c) Currents and voltages of the inverter, grid and load for i_{dref} = -15.0A (reactive power support)

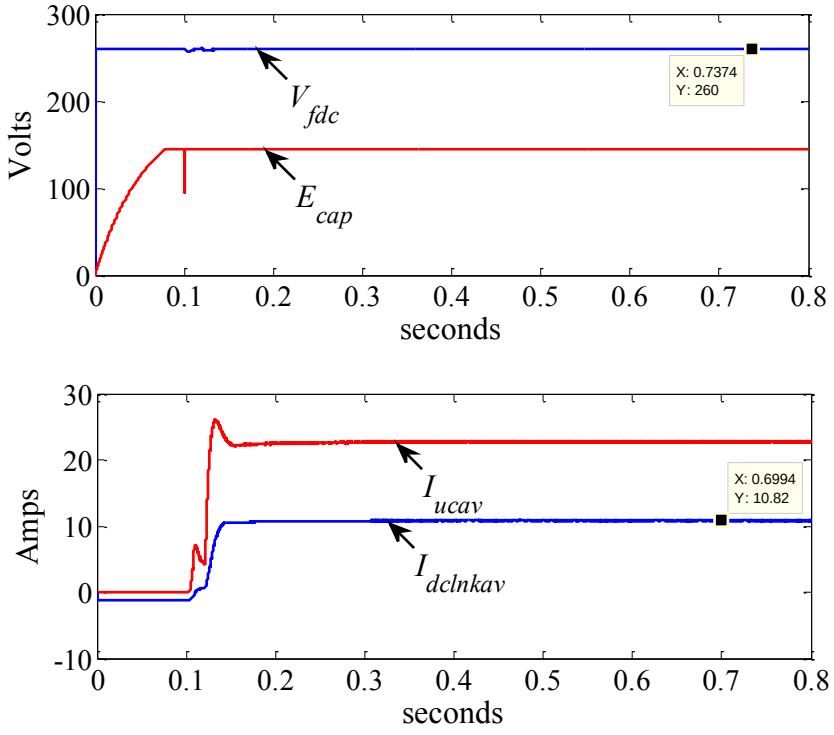

Fig. 5 (a) Currents and voltages of bi-directional dc-dc converter for i_{qref} = -12.0A (active power support)

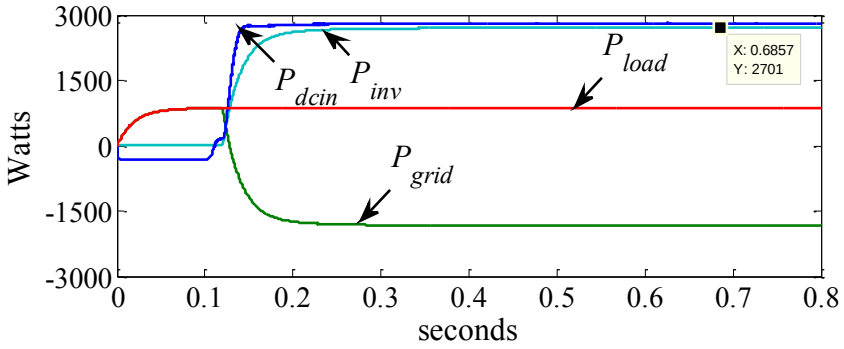

Fig. 5 (b) Grid, load and inverter active and reactive power curves for i_{qref} = -12.0A (active power support)

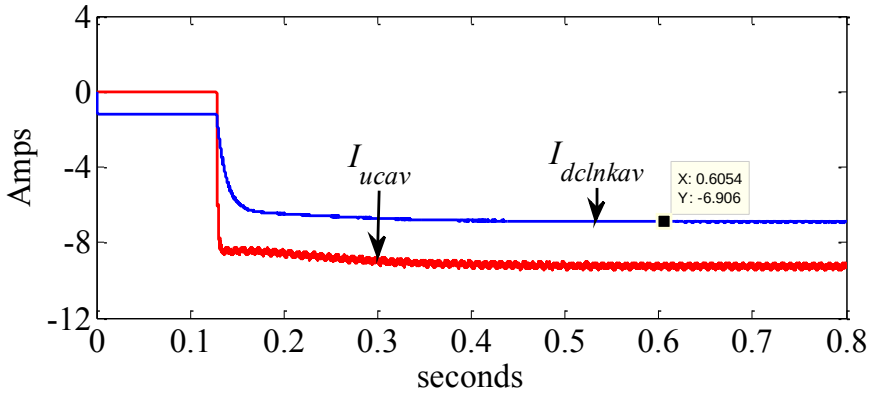

Fig. 6 (a) Currents of bi-directional dc-dc converter for i_{qref} = 7.0A (renewable intermittency smoothing; absorbing active power)

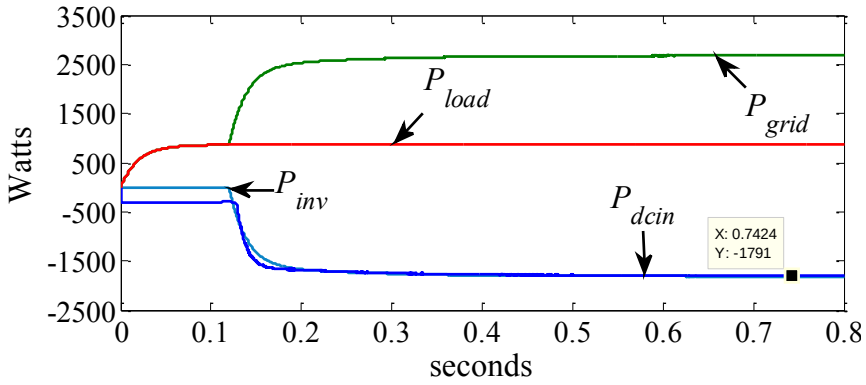

Fig. 6 (b) Grid, load and inverter active power curves for i_{qref} = 7.0A (renewable intermittency smoothing; absorbing active power)

V. EXPERIMENTAL RESULTS

To validate the UCAP-APF performance, a hardware prototype of the system was constructed and is shown in Figs. 7 (a) and 7 (b). In Fig. 7 (a), the complete inverter system is shown. It consists of a sensor board, an interface board, TMS320F28335 DSP controller and their power supply circuit in the top (1st) shelf. The 2nd shelf contains the inverter IGBT module (BSM100GD60DLC) which is a 600V, 100A six-pack module from Infineon, its gate driver SKHI 61R manufactured by SEMIKRON, and the 3500 µF 450Vdc dc-link capacitor; the 3rd shelf has the LC-filter which consists of a 1.2 mH, 45A

3-phase inductor and three 120μF 240Vac capacitors connected in wye configuration through damping resistors of 320 Ω in each phase. The 4th shelf consists of the 5kVA Δ-Y (120V/208V) isolation transformer and a protection circuit breaker before the inverter system is connected to the grid. In Fig. 7 (b) the UCAP and the dc-dc converter system is shown with the dc-dc converter and the oscilloscope (MSO4034B used for recording the data) in the top shelf. The bottom shelf has 3 UCAPs connected in series and nominal load of 213.5Ω.

Fig. 7 (a) Sensor, Interface and DSP boards (1st), Dc-link capacitor and Inverter (2nd), LC filter (3rd), Isolation Transformer (4th)

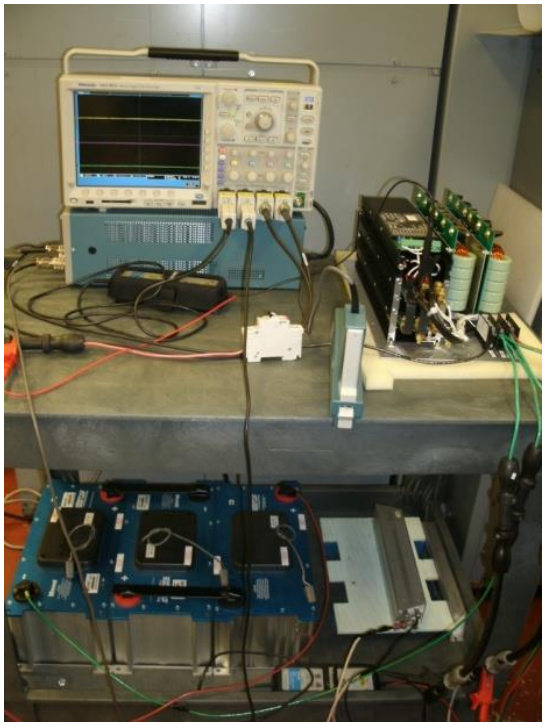

Fig. 7 (b) Bi-directional dc-dc converter and MSO4034B oscilloscope (top shelf), UCAP and 213.5Ω load (bottom shelf)

In Fig. 8 (a) the experimental waveforms of the bi-directional dc-dc converter are shown with the UCAP voltage E_{cap} (CH1), the dc-link voltage V_{fdc} (CH2), the average UCAP current I_{ucav} (CH3) and the dc-link current I_{dclnk} (CH4). Fig. 8 (a) is divided into 7 zones which are labeled from 1 through 7 in the plots. In zone 1 the inverter is supplying

only reactive power and the dc-dc converter is maintaining a stiff dc-link voltage. Zone 2 is a transition mode in which the inverter is changing from supplying reactive power to active power. In Zone 3 the inverter is supplying only active power to the grid which is being discharged from the UCAP. In Zone 4 again the inverter is supplying only active power to the grid however; the amount of active power supplied to the grid in Zone 4 is less than that in Zone 3 which can be observed from I_{dclnk} trace. In Zone 5 inverter is absorbing active power from the grid which is used for charging the UCAP through the bi-directional dc-dc converter. Zone 6 is again a transition mode in which the inverter is changing from supplying active power to supplying reactive power to the grid. In Zone 7 again the inverter is supplying only reactive power to the grid and the dc-dc converter is maintaining a stiff dc-link voltage.

In Fig. 8 (b) the zoomed in view of zone 3 is shown from which it can be observed that the inverter current I_{apf2a} and voltage V_{sa} are almost in phase with little phase difference which clearly shows that the inverter is providing active power support to the grid. The RMS values of V_{sa} and I_{apf2a} are 7.5A and 122V respectively which translates to P_{inv} of 2703.3W and Q_{inv} of 476.6Var from (7) as the phase difference of 10° between V_{sa} and I_{apf2a}; the results are similar for zone 4 where the commanded active power is comparatively less than that in zone 4. It is important to notice zones 3 and 4 of Fig. 8 (a) from which it can be seen that UCAP is discharging power rapidly in these zones therefore, E_{cap} is decreasing rapidly while V_{fdc} remains constant at 260V and I_{ucav} is increasing rapidly while average of $I_{dclnkav}$ remains almost constant. In Fig. 8 (c) the zoomed in view of zone 7 is presented where the inverter is only supplying reactive power to the grid. It can be observed that I_{apf2a} is lagging V_{sa} by nearly 90° and their RMS

values are 10A and 122V respectively which translates to Q_{inv} of 3660Var from (7). Similarly, it can be noticed from zones 1 and 7 in Fig. 8 (a) that E_{cap} is almost constant while I_{ucav} and $I_{dclnkav}$ are almost zero which proves that the active power discharged from the UCAP while providing reactive power support to the grid is minimal.

The bi-directional capability of the dc-dc converter which is necessary for absorbing excess power from DERs in renewable intermittency smoothing applications is shown in Fig. 8 (d) which is the zoomed in view of zone 5. To fully utilize the bi-directional capability of the inverter it must be controlled in such a way that it absorbs active power from the grid. In order to achieve this objective i_{qref} is set to positive 7A and it can be observed that I_{apf2a} and V_{sa} are 180° apart and their RMS values are 5A and 122V respectively which translates to P_{inv} of -1830W. The bi-directional dc-dc converter shifts its operation from Boost mode to Buck mode to absorb the power from the grid. Therefore, in zone 5 of Fig. 8 (a) it can be observed that both I_{ucav} and $I_{dclnkav}$ are negative while the V_{fdc} is still constant at 260V and E_{cap} is increasing slowly while the UCAP is being charged from the power absorbed from the grid.

The differences between the simulation and experimental results for the inverter and the dc-dc converter during active power support (zones 3 and 4), reactive power support (zones 1 and 7) and renewable intermittency smoothing (zone 7) modes are compared in Table I. It can be seen from P_{inv} and Q_{inv} values obtained from simulation and experiment that there is a very close match between the two sets of results in all the four zones. The active power input to the inverter P_{dc} is also listed in Table I which was obtained from the product of the V_{fdc} and $I_{dclnkav}$ which are available from Fig. 8 (a). Based on the experimental values of P_{dc} and P_{inv} the efficiency of the inverter can be

computed and it can be observed that the inverter is around 95% efficient in zone 3 and 93% efficient in zones 4 and 5. In zone 7 while providing reactive power support to the grid; the inverter consumes minimal active power from the grid which is for the dc-link capacitor losses which are not provided by the dc-dc converter therefore, inverter efficiency is not computed for this zone and it is not a performance measurement criterion when the system is in reactive power support mode.

TABLE I Shunt Inverter and Dc-dc converter Results

INVERTER SIMULATION AND EXPERIMENTAL RESULTS						
Zone	P_{inv} (sim)	Q_{inv} (sim)	P_{inv} (exp)	Q_{inv} (exp)	P_{dc} (W)	η (%)
3 (i_{qref}=-12)	2701	466	2703.3	476.66	2885.8	94.66
4 (i_{qref}=-10)	1731.6	277.3	1712.1	301.88	1781.6	92.79
5 (i_{qref}=+6)	-1791	75	-1828	63	-1675.4	92.97
7 (i_{dref}=-15)	-92	3570	-127	3657	-	-
DC-DC CONVERTER EXPERIMENTAL RESULTS						
Zone	E_{cap} (V)	I_{ucav} (A)	I_{dclnk} (A)	P_{in} (W)	P_{out} (W)	η (%)
3	126.0	28.0	10.9	3528	3193	89.92
4	94.0	25.0	6.8	2350	2098	89.28
5	110.0	-10.8	-5.2	-1288	-1358	87.48

The bi-directional dc-dc converter experimental results for zones 3, 4 and 5 where the converter provides active power support to the grid and absorbs active power from the grid are also presented in Table I. The voltage and current values listed in the table are the average for the given zone. It is important to note that the converter is around 90% efficient in zones 3, 4 and around 88% in zone 5 which indicates that the UCAP and bi-directional dc-dc converter operate efficiently while supplying active power to the grid and even while absorbing active power from the grid. It must be noted that the dc-dc converter efficiency can be further improved as these products become more prevalent on the distribution grid by reducing the switching losses using soft-switching schemes or

through the use of resonant topologies where the converter impedance and switching frequency vary to provide zero voltage switching thereby reducing the switching losses.

The bi-directional dc-dc converter experimental results for a mode transition from reactive power support mode to active power support mode (zone 2 to zone 3) are shown in Fig. 8 (e). This mode transition has the maximum amount of active power exchange and therefore, the ripple in the dc-link voltage V_{fdc} will be maximum for this case. It can be observed from Fig. 8 (e) that the overshoot in dc-link voltage V_{fdc} is around 20V which is less than 10% of the output voltage and the settling time is around 340ms. In Figs. 9 (a) and (b) the UCAP-APF system performance when the system experiences unbalanced voltage sag are presented. It can be observed from Fig. 9 (a) that when a 20% voltage sag is generated in phases *a* and *b* the system voltages V_{sa} and V_{sb} experience a voltage sag. However, the inverter current I_{apf2a} remains constant at $7.5A_{rms}$ while providing active power support to the grid even after the system experiences unbalanced voltage sag. This clearly indicates that the PLL tracks the fundamental component even during unbalanced scenarios which allows the UCAP-APF system to provide active and reactive power support to the grid under unbalanced conditions. From the bi-directional dc-dc converter waveforms shown in Fig. 9 (b) it can be observed that during the unbalanced voltage sag which lasts for 1 second the dc-link voltage V_{fdc} has slight fluctuations and settles down to steady state value of 260V very fast.

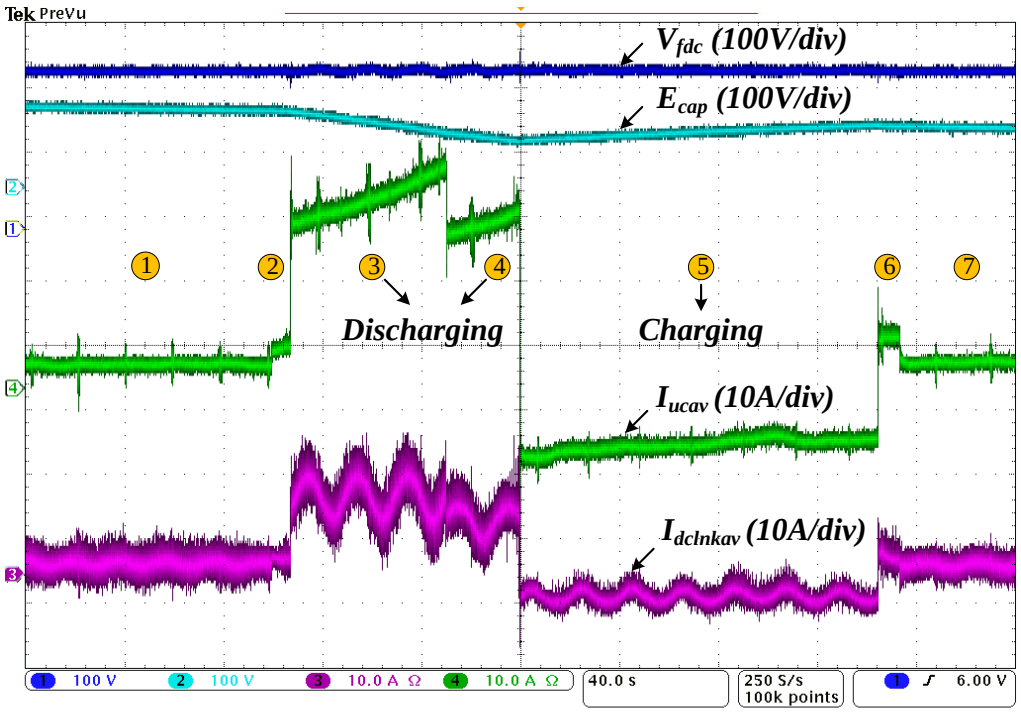

Fig. 8 (a) Bi-directional dc-dc converter waveforms V_{fdc} (CH1), E_{cap} (CH2), $I_{dclnkav}$ (CH3) and I_{ucav} (CH4)

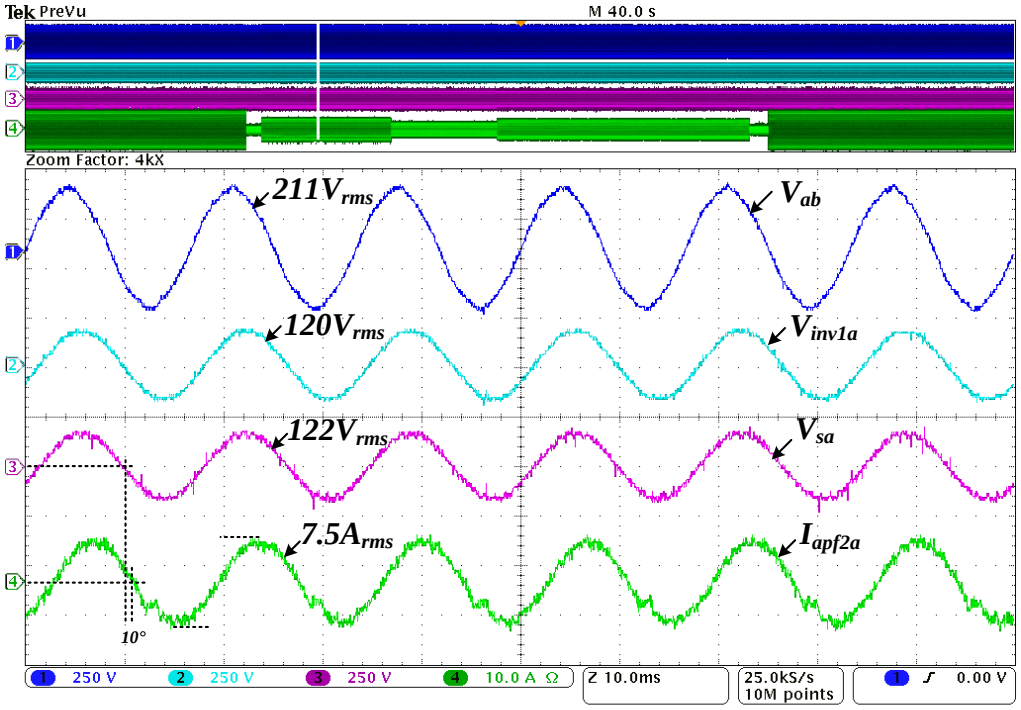

Fig. 8 (b) Inverter experimental waveforms V_{ab} (CH1), V_{inv1a} (CH2), V_{sa} (CH3) and I_{apf2a} (CH4) for zone 3 (active power support i_{qref} =-12.0A)

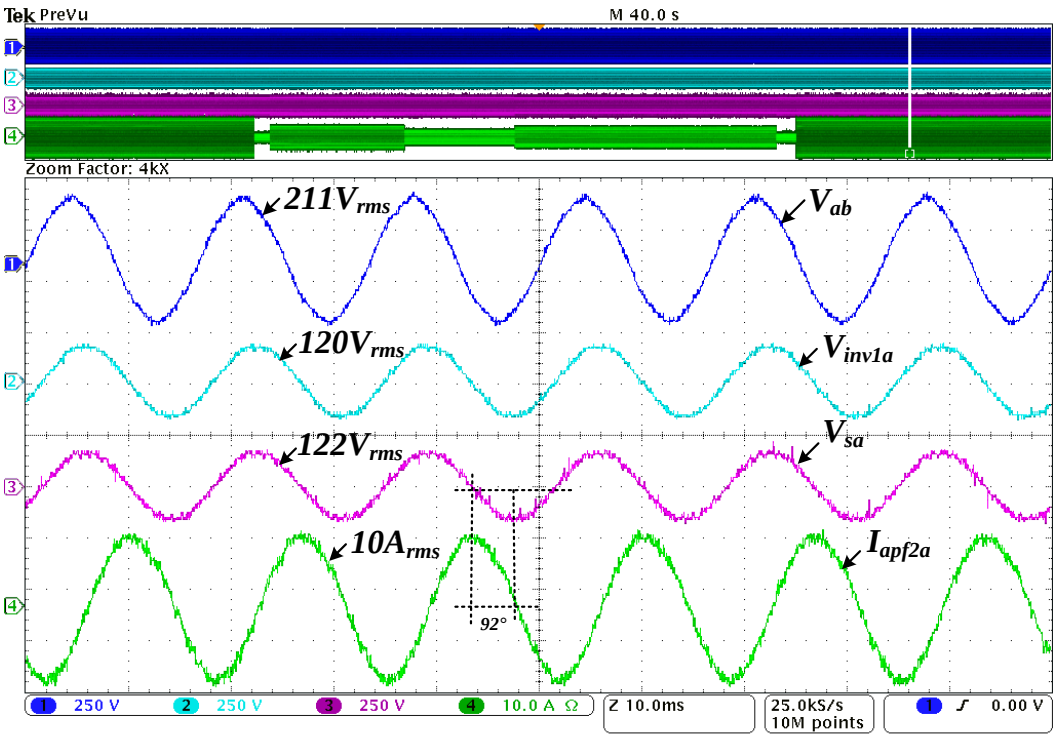

Fig. 8 (c) Inverter experimental waveforms V_{ab} (CH1), V_{inv1a} (CH2), V_{sa} (CH3) and I_{apf2a} (CH4) for zone 7 (reactive power support i_{dref} =-15.0A)

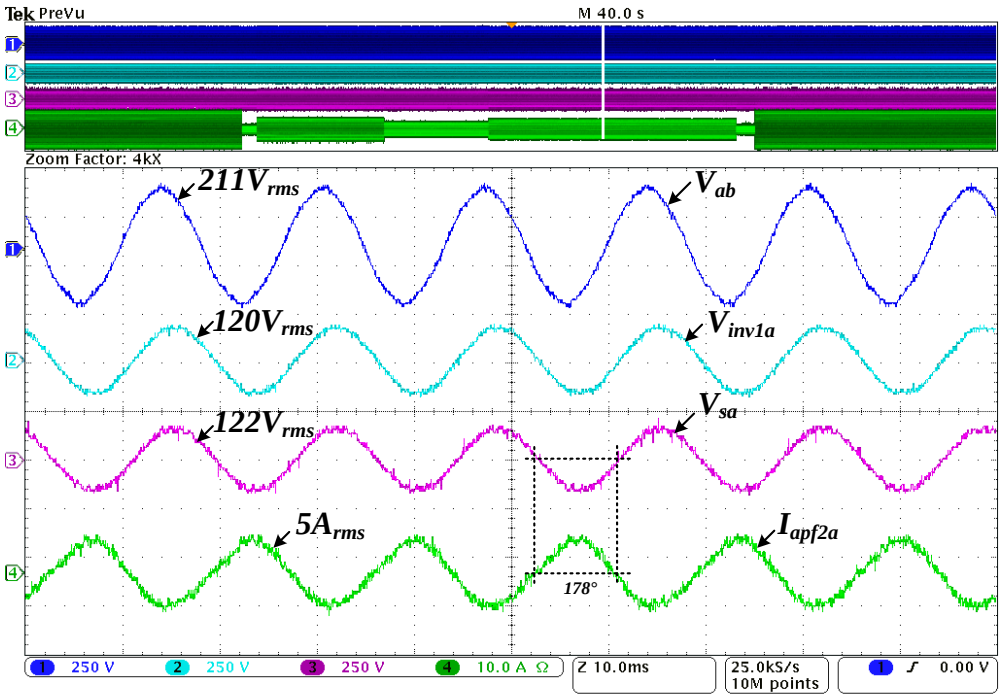

Fig. 8 (d) Inverter experimental waveforms V_{ab} (CH1), V_{inv1a} (CH2), V_{sa} (CH3) and I_{apf2a} (CH4) for zone 5 (absorbing power from grid i_{qref} =7.0A)

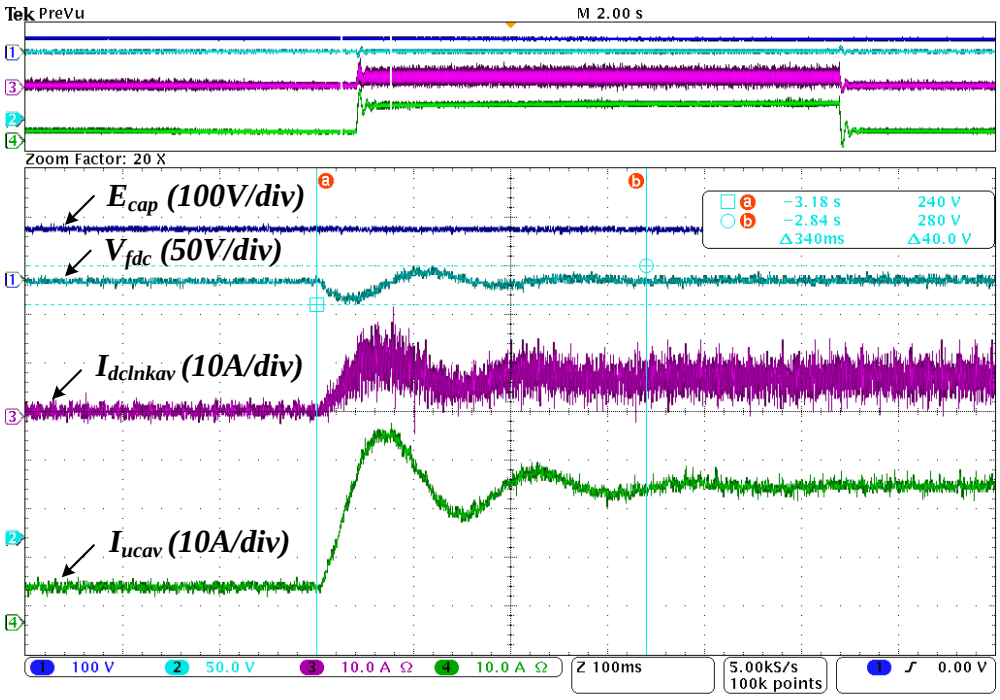

Fig. 8 (e) Bi-directional dc-dc converter waveforms showing transient response during mode transition to active power support mode

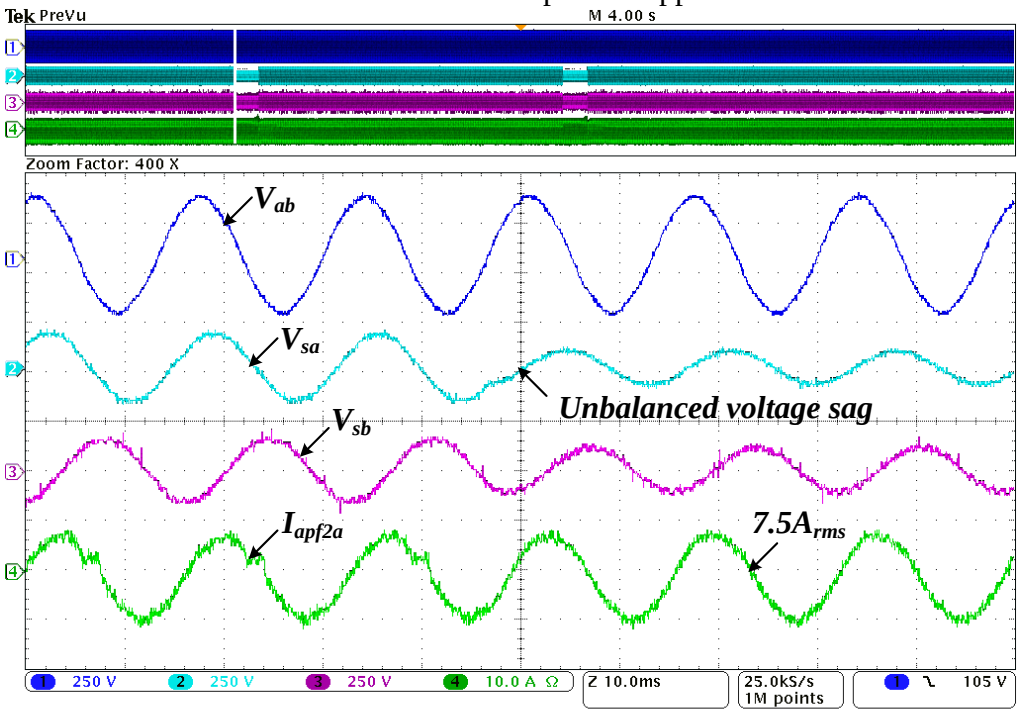

Fig. 9 (a) Inverter experimental waveforms V_{ab} (CH1), V_{sb} (CH2), V_{sa} (CH3) and I_{apf2a} (CH4) for active power support i_{qref} =-12.0A during an unbalanced sag in phases *a* and *b*

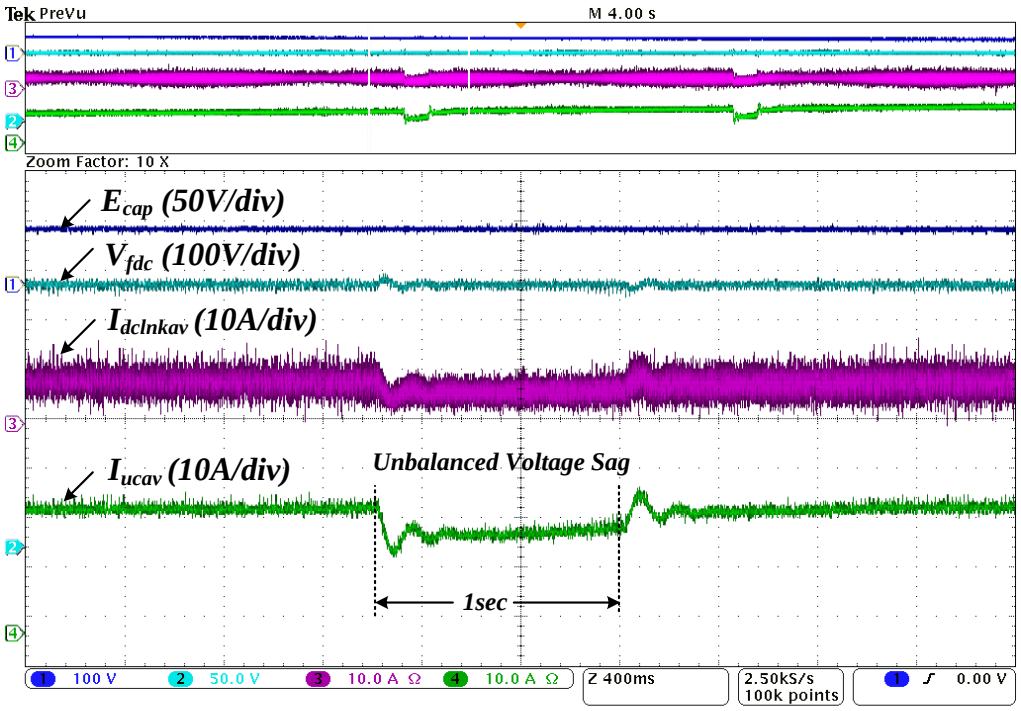

Fig. 9 (b) Bi-directional dc-dc converter waveforms showing transient response in active power support mode during an unbalanced sag in phases *a* and *b*

VI. CONCLUSION

In this paper, the concept of using a UCAP integrated APF design which provides active power support, reactive power support and renewable intermittency smoothing to the low voltage distribution grid is explored. The UCAP integration through a bi-directional dc-dc converter at the dc-link of a grid-tied inverter is proposed. The power stage and control strategy of the grid-tied inverter are discussed. The control strategy of the inverter which is a modified version of the i_d-i_q method is ideal for supplying as well as absorbing the commanded active or reactive power to the grid. Designs of major components in the power stage of the bi-directional dc-dc converter are presented. Average current mode control is used to regulate the output voltage of the dc-dc

converter due to its inherently stable characteristic. A Higher level integrated controller which takes decisions based on the system parameters provides inputs to the inverter and dc-dc converter controllers to carry out their control actions. The simulation of the integrated system which consists of the UCAP, bi-directional dc-dc converter, and the grid-tied inverter is carried out using PSCAD. Hardware experimental setup of the same integrated system is presented and the ability to provide active power support, reactive power support and renewable intermittency smoothing to the distribution grid is dynamically tested. Results from simulation and experiment agree well with each other thereby verifying the concepts introduced in this paper. Similar UCAP based energy storages can be deployed in the future in a micro-grid or a low voltage distribution grid to respond to dynamic requests in active and reactive power and to smooth the intermittencies in the output of various renewable energy sources.

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II. An Integrated Dynamic Voltage Restorer-Ultracapacitor Design for Improving Power Quality of the Distribution Grid

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***Abstract*—Energy storage technologies are increasing their presence in the market and integration of these technologies into the power grid is slowly becoming a reality. Dynamic Voltage Restorer has been used in the past to provide voltage sag and swell compensation to prevent sensitive loads from voltage disturbances on the utility side. In this paper the concept of integrating ultra-capacitor (UCAP) based energy storage into the dynamic voltage restorer topology has been explored. With this integration the DVR will be able to independently compensate voltage sags and swells without relying on the grid to compensate for faults on the grid. UCAPs have low energy density and high power density ideal characteristics for compensation of voltage sags and voltage swells which are both high power low energy events. UCAP is integrated into dc-link of the DVR through a bi-directional dc-dc converter which helps in providing stiff dc-link voltage and the integration helps in compensating deeper voltage sags, voltage swells for longer durations. Design and control of both the dc-ac inverter and the dc-dc converter are discussed. The simulation model of the overall system is developed and compared to the experimental hardware setup.**

Index Terms- **UCAP, DVR, dc-dc converter, DSP, sag/swell, d-q control, PLL, energy storage integration**

I. INTRODUCTION

The concept of using inverter based Dynamic voltage restorers for preventing customers from momentary voltage disturbances on the utility side was demonstrated for the first time by Woodley etal [1]. The concept of using the dynamic voltage restorer

(DVR) as a power quality product has gained significant popularity since its first use. In [1], the authors propose the usage of the DVR with rechargeable energy storage at the dc-terminal to meet the active power requirements of the grid during voltage disturbances. In order to avoid and minimize the active power injection into the grid the authors also mention an alternative solution which is to compensate for the voltage sag by inserting a lagging voltage in quadrature with the line current. Due to the high cost of rechargeable energy storage various other types of control strategies have also been developed in the literature [2-8] to minimize the active power injection from the DVR. The high cost of the rechargeable energy storage prevents the penetration of the dynamic voltage restorer as a power quality product. However, the cost of rechargeable energy storage has been decreasing drastically in the recent past due to various technological developments and due to higher penetration in the market in the form of auxiliary energy storage for distributed energy resources (DERs) like wind, solar, HEVs and PHEVs [9, 10]. Therefore, there has been renewed interest in the literature [10-17] to integrate re-chargeable energy storage again at the dc-terminal of power quality products like STATCOM and DVR.

Various types of rechargeable energy storage technologies based on Superconducting magnets (SMES), flywheels (FESS), batteries (BESS) and Ultra-capacitors (UCAPs) are compared in [10] for integration into advanced power applications like DVR. Efforts have been made to integrate energy storage into the DVR system which will give the system active power capability which makes it independent of the grid during voltage disturbances. In [11] cascaded H-bridge based DVR with a thyristor controlled inductor is proposed in order to minimize the energy storage

requirements. In [12] flywheel energy storage is integrated into the DVR system to improve its steady state series and shunt compensation.

Of all the rechargeable energy storage technologies UCAPs are ideally suited for applications which need active power support in the *milliseconds* to *seconds* timescale [10], [13], [14]. Therefore, UCAP based integration into the DVR system is ideal as the normal duration of momentary voltage sags and swells is in the *milliseconds* to *seconds* range [15]. UCAPs have low energy density and high power density ideal characteristics for compensating voltage sags and voltage swells which are both events which require high amount of power for short spans of time. UCAPs also have higher number of charge/discharge cycles when compared to batteries and for the same module size UCAPs have higher terminal voltage when compared to batteries which makes the integration easier. With the prevalence of renewable energy sources on the distribution grid and the corresponding increase in power quality problems the need for DVRs on the distribution grid is increasing [16]. Super-capacitor based energy storage integration into the DVR for the distribution grid is proposed in [16] and [17]. However, the concept is introduced only through simulation and experimental results are not presented. *In the present paper UCAP based energy storage integration to a DVR into the distribution grid is proposed and the following application areas are addressed,*

- Integration of the UCAP with DVR system gives the system active power capability which is necessary for independently compensating voltage sags and swells
- Experimental validation of the UCAP, dc-dc converter, inverter their interface and control

- Development of inverter and dc-dc converter controls to provide Sag and Swell compensation to the distribution grid
- Hardware integration and performance validation of the integrated DVR-UCAP system

II. THREE-PHASE SERIES INVERTER

A. Power Stage

The one line diagram of the system is shown in Fig. 1. The power stage is a 3-phase voltage source inverter which is connected in series to the grid and is responsible for compensating the voltage sags and swells; the model of the Series DVR and its controller is shown in Fig. 2. The inverter system consists of an IGBT module, its gate-driver, LC filter and an isolation transformer. The dc-link voltage V_{dc} is regulated at 260V for optimum performance of the converter and the line-line voltage V_{ab} is 208V; based on these the modulation index *m* of the inverter is given by:

$$m = \frac{2\sqrt{2}}{\sqrt{3}V_{dc} * n} V_{ab(rms)} \quad (1)$$

where *n* is the turns ratio of the isolation transformer. Substituting *n* as 2.5 in (1) the required modulation index is calculated as 0.52. Therefore, the output of the dc-dc converter should be regulated at 260V for providing accurate voltage compensation. The objective of the integrated UCAP-DVR system with active power capability is to compensate for *temporary voltage sag* (0.1-0.9pu) and *voltage swell* (1.1-1.2pu) which last from 3s-1min [15].

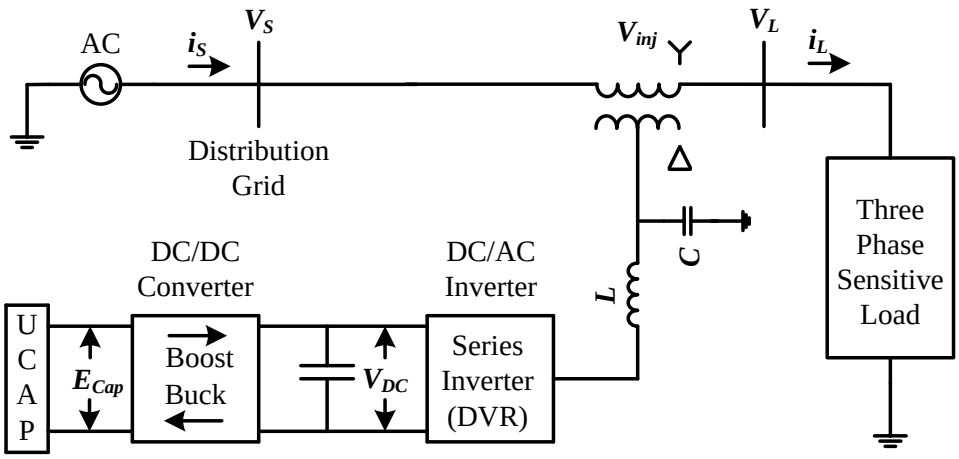

Fig. 1 One line diagram of DVR with UCAP Energy Storage

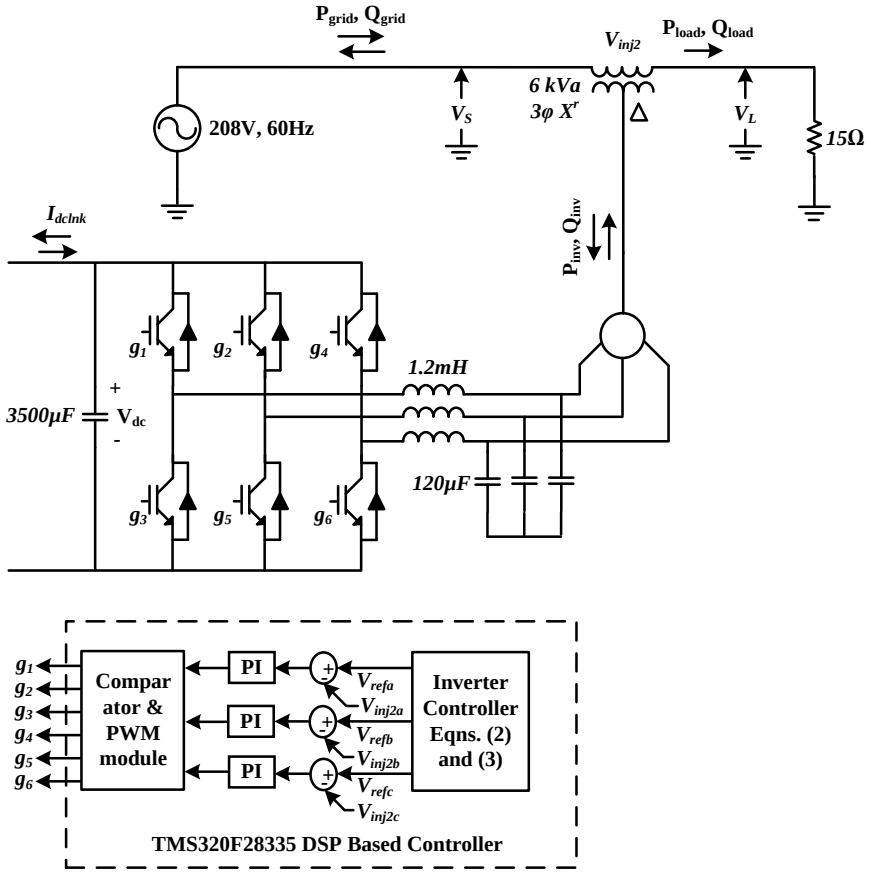

Fig. 2 Model of three-phase Series inverter (DVR) and its controller

B. Controller Implementation

There are various methods to control the series inverter to provide Dynamic Voltage restoration and most of them rely on injecting a voltage in quadrature with advanced phase so that reactive power is utilized in voltage restoration [3]. Phase advanced voltage restorations techniques are complex in implementation but the primary reason for using these techniques is to minimize the active power support and thereby the amount of energy storage requirement at the dc-link in order to minimize the cost of energy storage. However, the cost of energy storage has been declining and with the availability of active power support at the dc-link complicated phase-advanced techniques can be avoided and voltages can be injected in-phase with the system voltage during a voltage sag or a swell event. The control method requires the use of a PLL to find the rotating angle θ. As discussed previously the goal of this project is to use the active power capability of the UCAP-DVR system and compensate temporary voltage sags and swells.

The inverter controller implementation is based on injecting voltages in-phase with the supply side line-neutral voltages. This requires PLL for estimating θ which has been implemented using the fictitious power method described in [18]. Based on the estimated θ and the line-line source voltages V_{ab}, V_{bc}, V_{ca} (which are available for this delta-sourced system) are transformed into the d-q domain and the line-neutral components of the source voltage V_{sa}, V_{sb} and V_{sc} which are not available can then be estimated using:

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\left(\theta - \frac{\pi}{6}\right) & \sin\left(\theta - \frac{\pi}{6}\right) \\ -\sin\left(\theta - \frac{\pi}{6}\right) & \cos\left(\theta - \frac{\pi}{6}\right) \end{bmatrix} \begin{bmatrix} \frac{V_d}{\sqrt{3}} \\ \frac{V_q}{\sqrt{3}} \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} V_{refa} \\ V_{refb} \\ V_{refc} \end{bmatrix} = m * \begin{bmatrix} \left(\sin\theta - \frac{V_{sa}}{169.7}\right) \\ \left(\sin\left(\theta - \frac{2\pi}{3}\right) - \frac{V_{sb}}{169.7}\right) \\ \left(\sin\left(\theta + \frac{2\pi}{3}\right) - \frac{V_{sc}}{169.7}\right) \end{bmatrix} \quad (3)$$

$$P_{inv} = 3V_{inj2a(rms)} I_{La(rms)} \cos\varphi$$
$$Q_{inv} = 3V_{inj2a(rms)} I_{La(rms)} \sin\varphi \quad (4)$$

These voltages are normalized to unit sine waves using line-neutral system voltage of $120V_{rms}$ as reference and compared to unit sine waves *in-phase* with actual system voltages V_s from (3) to find the injected voltage references V_{ref} necessary to maintain a constant voltage at the load terminals where m is 0.52 from (1). Therefore, whenever there is a voltage sag or swell on the source side a corresponding voltage V_{inj2} is injected in-phase by the DVR and UCAP system to negate the effect and retain a constant voltage V_L at the load end. The actual active and reactive power supplied by the series inverter can be computed using (4) from the RMS values of injected voltage V_{inj2a} and load current I_{La} and φ is the phase difference between the two waveforms. The complete inverter control algorithm is implemented in the DSP TMS320F28335 which has a clock frequency of 150MHz, an inbuilt A/D module, PWM module and real-time emulation which are all ideal for this application.

III. UCAP AND BI-DIRECTIONAL DC-DC CONVERTER

A. UCAP Bank Hardware Setup

The choice of the number of UCAPs necessary for providing grid support depends on the amount of support needed, terminal voltage of the UCAP, dc-link voltage and distribution grid voltages. For a 260V dc-link voltage it is practical and cost effective to use 3 modules in the UCAP bank. Therefore, in this paper the experimental setup consists of three 48V, 165F UCAPs (BMOD0165P048) manufactured by Maxwell Technologies which are connected in series. Assuming that the UCAP bank can be discharged to 50% of its initial voltage ($V_{uc,ini}$) to final voltage ($V_{uc,fin}$) from 144V to 72V which translates to depth of discharge of 75%, the energy in the UCAP bank available for discharge is given by:

$$E_{UCAP} = \frac{1}{2} * C * \frac{({V_{uc,ini}}^2 - {V_{uc,fin}}^2)}{60}\ W - min$$

$$E_{UCAP} = {}^1\!/_2 * {}^{165}\!/_3 * {}^{(144^2 - 72^2)}\!/_{60} \quad (5)$$

$$= 7128\ \text{W-min}$$

B. Bi-directional Dc-dc Converter and Controller

A UCAP cannot be directly connected to the dc-link of the inverter like a battery as the voltage profile of the UCAP varies as it discharges energy. Therefore, there is a need to integrate the UCAP system through a bi-directional dc-dc converter which maintains a stiff dc-link voltage as the UCAP voltage decreases while "*Discharging*" and increases while "*Charging*". The model of the bi-directional dc-dc converter and its controller are shown in Fig. 3 where the input consists of 3 UCAPs connected in series and the output consists of a nominal load of 213.5Ω to prevent operation at no-load and

the output is connected to the dc-link of the inverter. The amount of active power support required by the grid during a voltage sag event is dependent on the depth and duration of the voltage sag and the dc-dc converter should be able to withstand this power during "*Discharge*" mode. The dc-dc converter should also be able to operate in bi-directional mode to be able to "*Charge*" or absorb additional power from the grid during voltage swell event. In this paper the bi-directional dc-dc converter acts as a boost converter while "*discharging*" power from the UCAP and acts as a buck converter while "*charging*" the UCAP from the grid.

Average current mode control which is widely explored in literature [19] is used to regulate the output voltage of the bi-directional dc-dc converter in both *Buck* and *Boost* modes while *Charging* and *Discharging* the UCAP bank. This method tends to be more stable when compared to other methods like voltage mode control and peak current mode control. Average current mode controller is shown in Fig. 3 where the dc-link and actual output voltage V_{out} is compared with the reference voltage V_{ref} and the error is passed through the voltage compensator $C_1(s)$ which generates the average reference current I_{ucref}. When the inverter is *discharging* power into the grid during voltage sag event the dc-link voltage V_{out} tends go below the reference V_{ref} and the error is positive I_{ucref} is positive and the dc-dc converter operates in *Boost* Mode. When the inverter is absorbing power from the grid during voltage swell event or *charging* the UCAP, V_{out} tends to increase above the reference V_{ref} and the error is negative, I_{ucref} is negative and the dc-dc converter operates in *Buck* Mode. Therefore, the sign of the error between V_{out} and V_{ref} determines the sign of I_{ucref} and thereby the direction of operation of the bidirectional dc-dc converter. The reference current I_{ucref} is then compared to the actual UCAP current

(which is also the inductor current) I_{uc} and the error is then passed through the current compensator $C_2(s)$. The compensator transfer functions which provide a stable response are given by:

$$C_1(s) = 1.67 + \frac{23.81}{s} \tag{6}$$

$$C_2(s) = 3.15 + \frac{1000}{s} \tag{7}$$

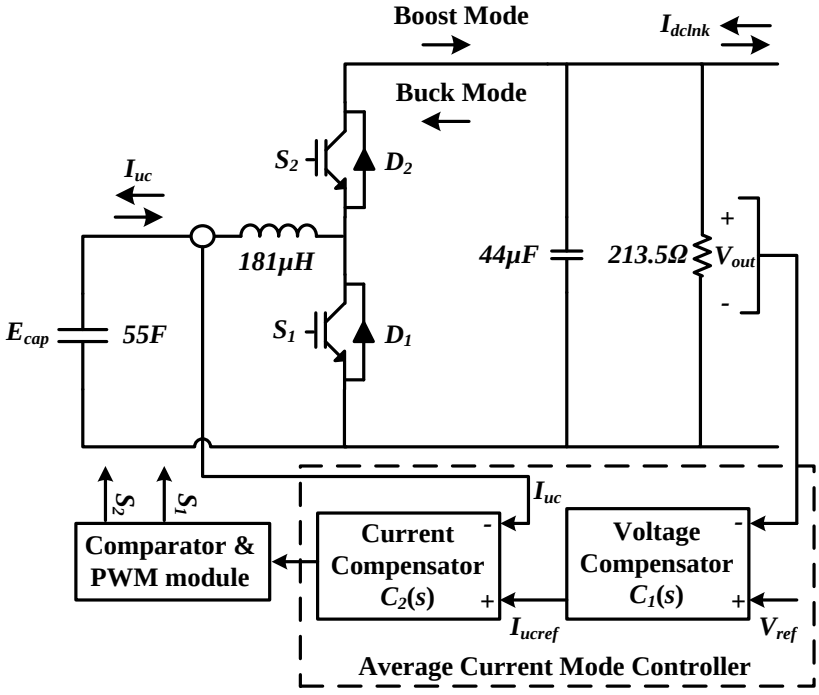

Fig. 3 Model of the bi-directional dc-dc converter and its controller

IV. SIMULATION RESULTS

The simulation of the proposed UCAP integrated DVR system is carried out in PSCAD for a 208V, 60Hz system where 208V is 1pu. The system response for a three-phase voltage sag which lasts for 0.1s and has a depth of 0.84pu is shown in Figs. 4 (a)-(e). It can be observed from Fig. 4 (a) that during voltage sag the source voltage V_{srms} is

reduced to 0.16pu while the load voltage V_{Lrms} is maintained constant at around 0.9pu due to voltages injected *in-phase* by the series inverter. This can also be observed from the plots of the line-line source voltages (V_{sab}, V_{sbc}, V_{sca}) Fig. 4 (b), the line-line load voltages (V_{Lab}, V_{Lbc}, V_{Lca}) Fig. 4 (c) and the line-neutral injected voltages of the series inverter (V_{inj2a}, V_{inj2b}, V_{inj2c}) Fig. 4 (d). Finally, it can be observed from Fig. 4 (e) that V_{inj2a} lags V_{sab} by 30° which indicates that it is *in-phase* with the line-neutral source voltage V_{sa}. In Fig. 5 (a) plots of the bi-directional dc-dc converter are presented and it can be observed that the dc-link voltage V_{fdc} is regulated at 260V, the average dc-link current $I_{dclnkav}$ and the average UCAP current I_{ucav} increase to provide the active power required by the load during the sag. Though the UCAP is discharging the change in the UCAP voltage E_{cap} is not visible in this case due to the short duration of the simulation which is due to limitations in PSCAD software. It can also be observed from the various active power plots shown in Fig. 5 (b) where the power supplied to the load P_{load} remains constant even during the voltage sag when the grid power P_{grid} is decreasing. The active power deficit of the grid is met by the inverter power P_{inv} which is almost equal to the input power to the inverter P_{dc_in} available from the UCAP. Therefore, it can be concluded from the plots that the active power deficit between the grid and load during the voltage sag event is being met by the integrated UCAP-DVR system through the bidirectional dc-dc converter and the inverter. Similar analysis can also be extended for voltage sags which occur in one of the phases (A, B or C) or in two of the phases (AB, BC or CA). However, the active power requirement is greatest for the case where all the three phases ABC experience voltage sag.

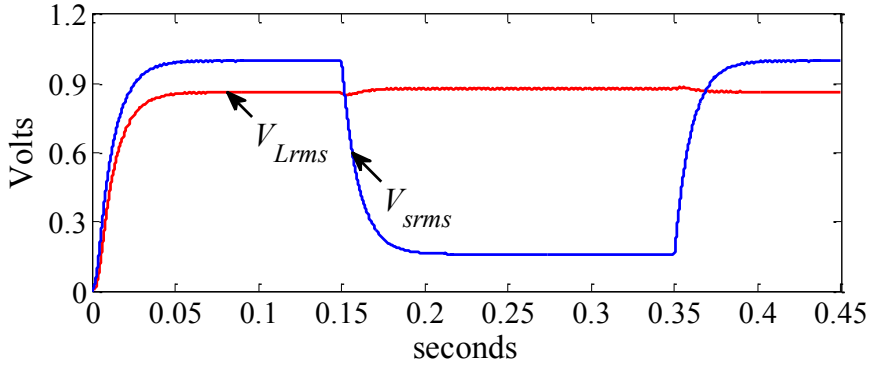

Fig. 4 (a) Source and load RMS voltages V_{srms} and V_{Lrms} during sag

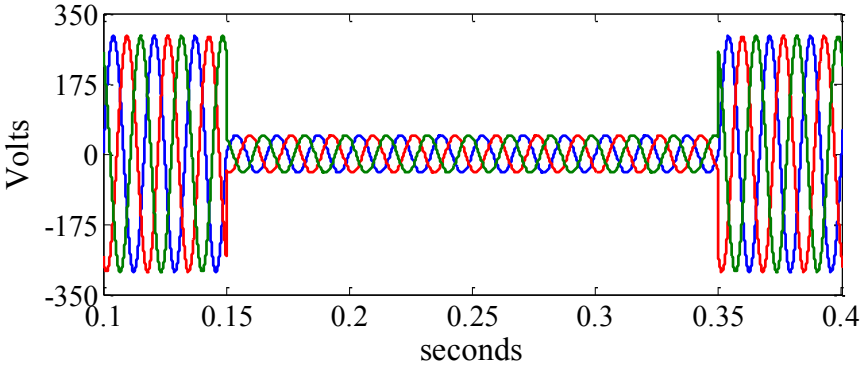

Fig. 4 (b) Source voltages V_{sab} (blue), V_{sbc} (red), V_{sca} (green) during sag

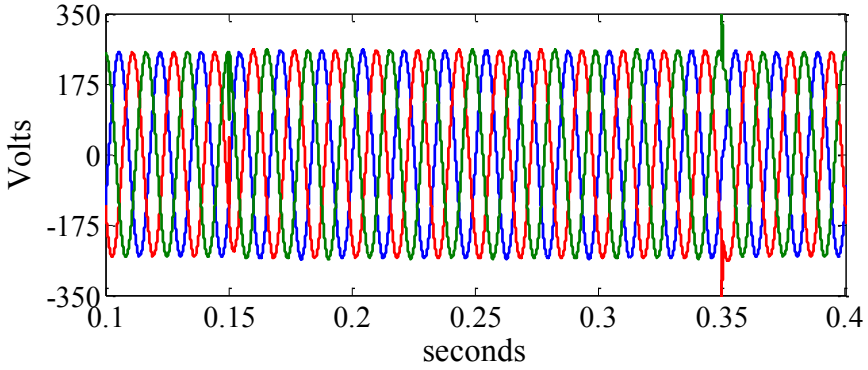

Fig. 4 (c) Load voltages V_{Lab} (blue), V_{Lbc} (red), V_{Lca} (green) during sag

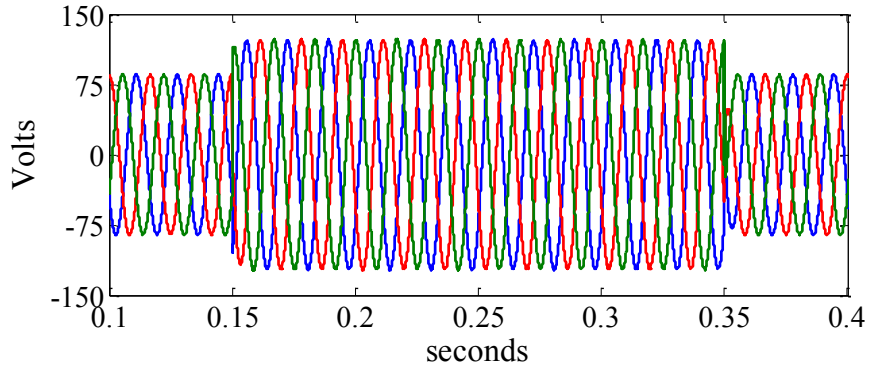

Fig. 4 (d) Injected voltages V_{inj2a} (blue), V_{inj2b} (red), V_{inj2c} (green) during sag

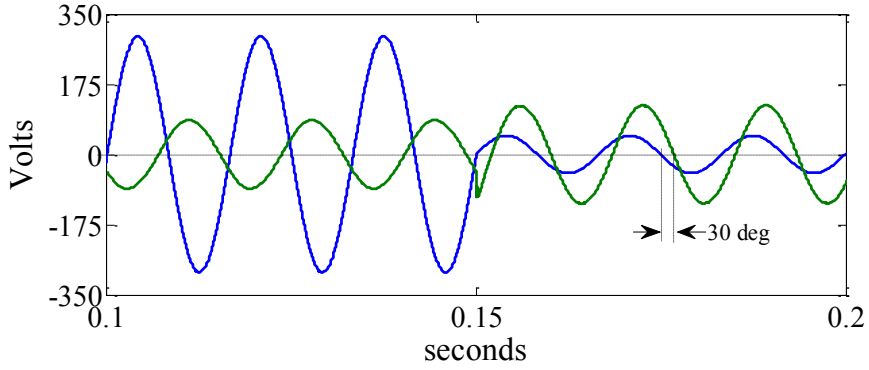

Fig. 4 (e) V_{inj2a} (green) and V_{sab} (blue) waveforms during sag

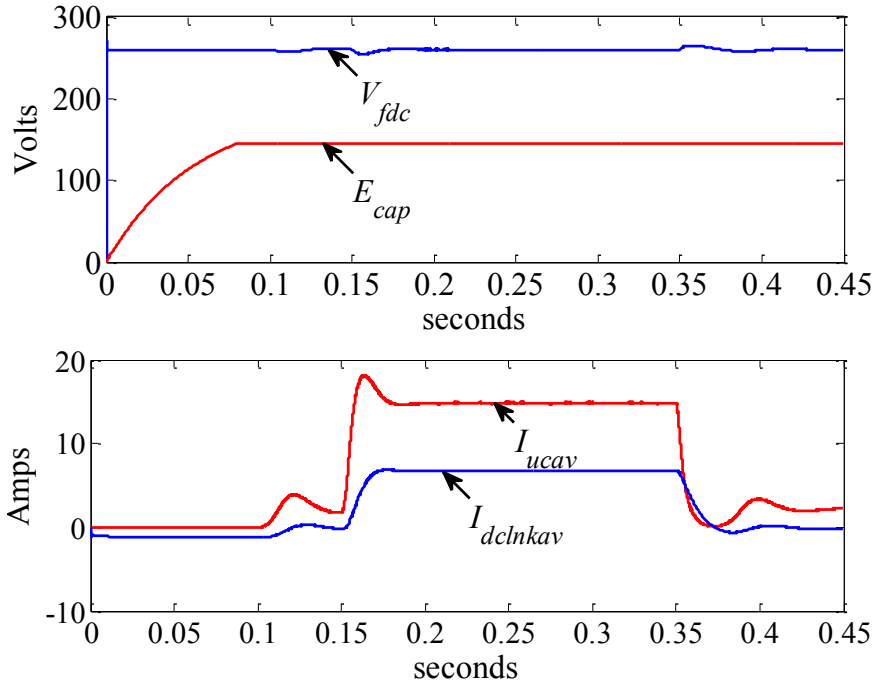

Fig. 5 (a) Currents and voltages of dc-dc converter

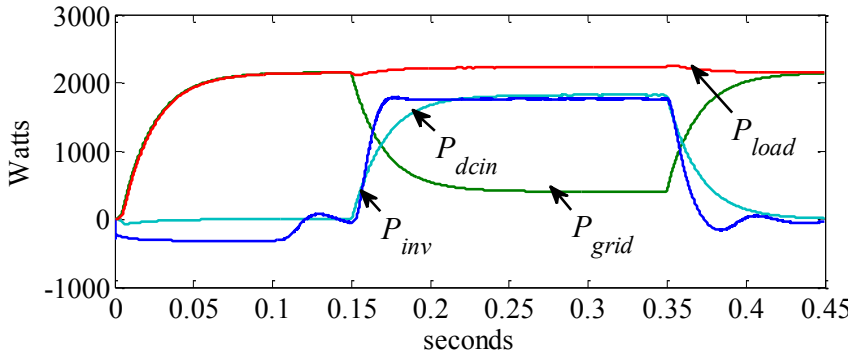

Fig. 5 (b) Active power of grid, load and inverter during voltage sag

The system response for a three-phase voltage swell which lasts for 0.1s and has a magnitude of 1.2pu is shown in Figs. 6 (a)-(e). It can be observed that during voltage swell the source voltage V_{srms} increases to 1.2pu while the load voltage V_{Lrms} is maintained constant at around 1pu due to voltages injected *in-phase* by the series inverter. This can also be observed from the plots of the line-line source voltages (V_{sab}, V_{sbc}, V_{sca}) Fig. 6 (a), the line-line load voltages (V_{Lab}, V_{Lbc}, V_{Lca}) Fig. 6 (b) and the line-neutral injected voltages of the series inverter (V_{inj2a}, V_{inj2b}, V_{inj2c}) Fig. 6 (c). Finally, it can be observed that V_{inj2a} lags V_{sab} by 150° which indicates that it is 180° out of phase with the line-neutral source voltage V_{sa} as required by the in-phase control algorithm. In Fig. 7 (a) plots of the bi-directional dc-dc converter are presented and it can be observed that the dc-link voltage V_{fdc} is regulated at 260V, the average dc-link current $I_{dclnkav}$ and the average UCAP current I_{ucav} change direction to absorb the additional active power from the grid into the UCAP during the voltage swell event. The overshoot in I_{ucav} and $I_{dclnkav}$ during startup at 0.1s and during mode changes at 0.15s and 0.35s is due to the mismatch between the breaker action and the compensator action in PSCAD which is a modeling problem present in the simulation and does not show in the experimental results. Again due to PSCAD limitations which restrict the duration of the simulation the

increase in E_{cap} due to charging of the UCAP during the voltage swell is not visible. This can also be observed from the various active power plots where the power supplied to the load P_{load} remains constant even during the voltage swell when the grid power P_{grid} is increasing. It can be observed from the inverter power P_{inv} and inverter input power P_{dc_in} plots that the additional active power from the grid is absorbed by the inverter and transmitted to the UCAP. Therefore, it can be concluded from the plots that the additional active power from the grid during the voltage swell event is being absorbed by the UCAP-DVR system through the bi-directional dc-dc converter and the inverter.

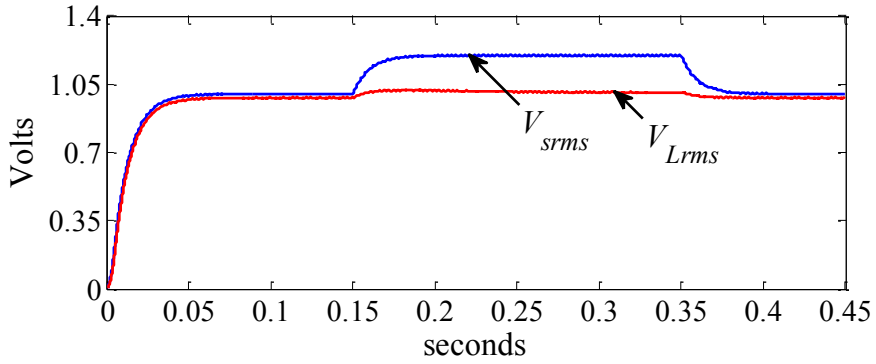

Fig. 6 (a) Source and load RMS voltages V_{srms} and V_{Lrms} during swell

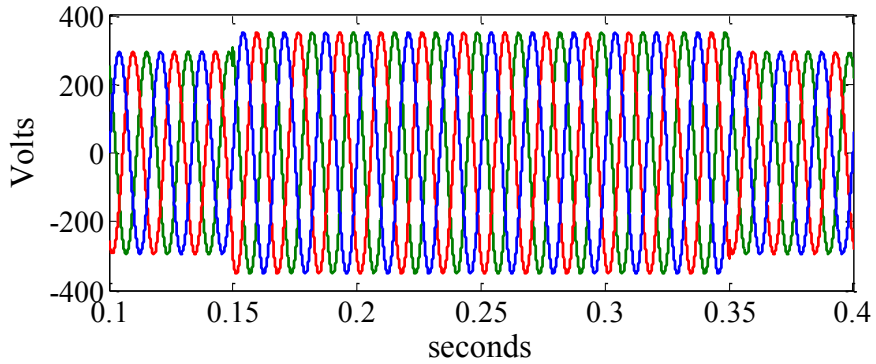

Fig. 6 (b) Source voltages V_{sab} (blue), V_{sbc} (red), V_{sca} (green) during swell

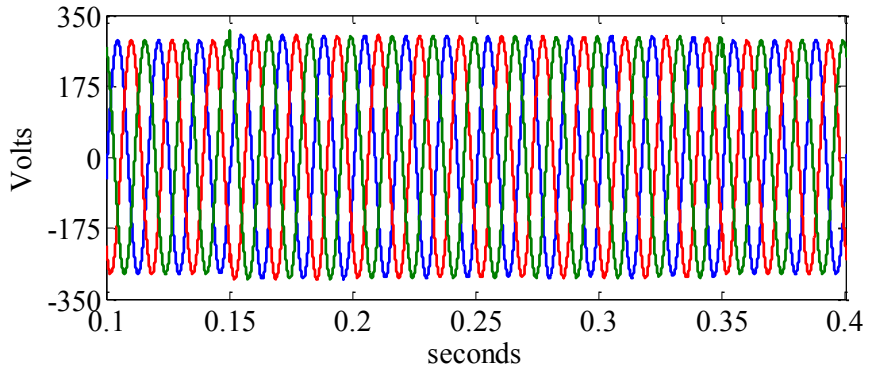

Fig. 6 (c) Load voltages V_{Lab} (blue), V_{Lbc} (red), V_{Lca} (green) during swell

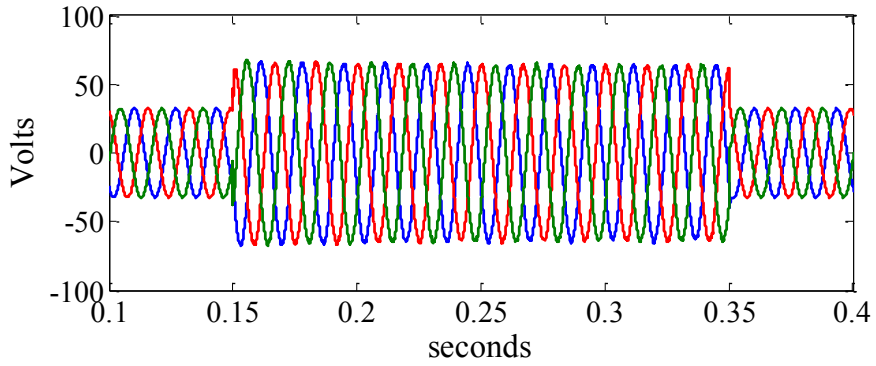

Fig. 6 (d) Injected voltages V_{inj2a} (blue), V_{inj2b} (red), V_{inj2c} (green) during swell

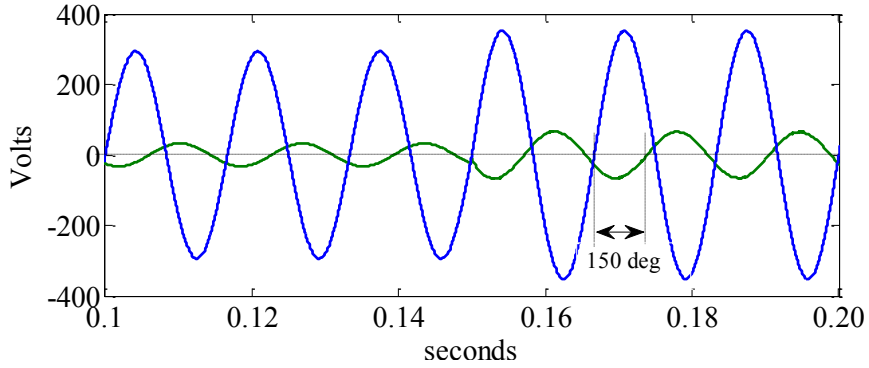

Fig. 6 (e) V_{inj2a} (green) and V_{sab} (blue) waveforms during swell

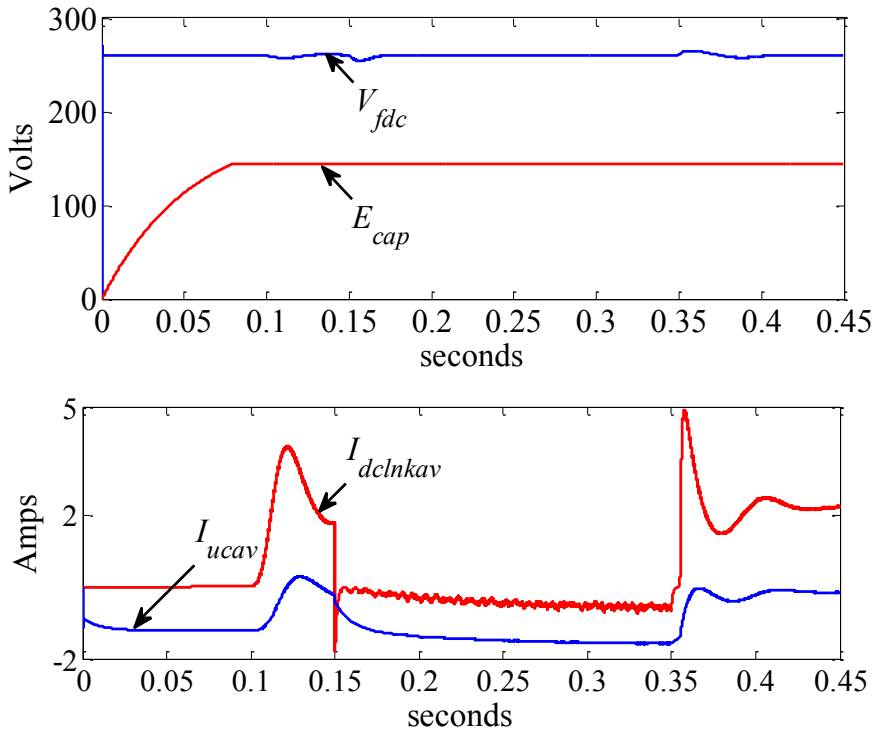

Fig. 7 (a) Currents and voltages of dc-dc converter during swell

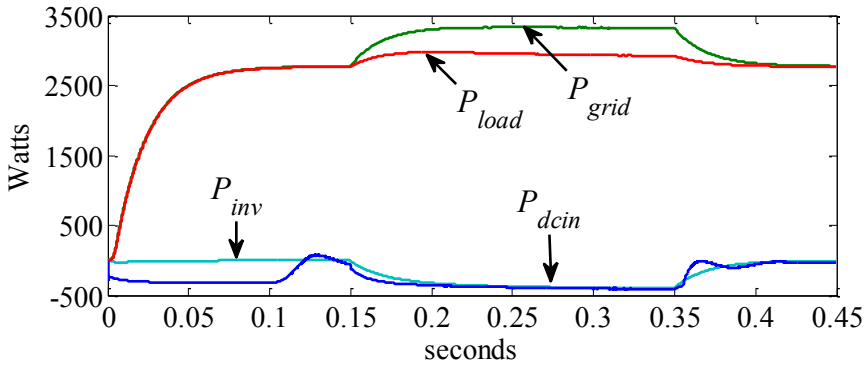

Fig. 7 (b) Active and Reactive power of grid, load and inverter during a voltage swell

V. EXPERIMENTAL RESULTS

In order to verify the concept and simulation results experimentally a hardware prototype of the complete system was constructed and is shown in Figs. 8 (a) and (b). In Fig. 8 (a) the complete inverter system is shown; it consists of a sensor board, an interface board, TMS320F28335 DSP controller and their power supply circuit in the top

(1st) shelf. In the 2nd shelf the Inverter IGBT module (BSM100GD60DLC) which is 600V 100A six-pack module from Infineon, its gate driver SKHI 61R manufactured by SEMIKRON, the 3500µF 450Vdc dc-link capacitor are placed; the 3rd shelf has the LC-filter which consists of 1.2 mH 45A 3-phase inductor and three 120µF 240Vac capacitors connected in wye configuration; the 4th shelf consists of three 2kVa 125V/50V single phase isolation transformers connected in delta configuration on the primary side and the secondary sides are connected in series with the grid through a protection circuit breaker. In Fig. 8 (b) the UCAP, the bi-directional dc-dc converter, the oscilloscope (MSO4034B used for recording the data) and the industrial power corruptor are shown.

Fig. 8 (a) Sensor, Interface and DSP boards (1st), Dc-link capacitor and Inverter (2nd), LC filter (3rd), Isolation Transformer (4th)

Fig. 8 (b) Dc-dc converter and MSO4034B oscilloscope (top shelf), UCAP bank with 3 UCAPs (bottom shelf) and the Industrial Power Corruptor

In Figs. 9 (a) and (b) the experimental waveforms of the inverter and the bi-directional dc-dc converter are shown for the case where the grid experiences voltage sag of 0.84pu magnitude for 1 min duration. In Fig. 9 (a) the dc-link voltage V_{fdc} (CH1), the UCAP voltage E_{cap} (CH2), the dc-link current I_{dclnk} (CH3) and the average UCAP current I_{ucav} (CH4) are shown. It can be observed from Fig. 9 (a) that during the voltage sag E_{cap} is decreasing rapidly and I_{ucav} is increasing rapidly; while V_{fdc} and $I_{dclnkav}$ are constant. Therefore, the dc-dc converter is able to regulate the dc-link voltage to 260V and operate in "*Boost*" mode to discharge active power during a voltage sag event to meet the active power deficit between the grid and the load. In Fig. 9 (b) the zoomed in versions of the line-neutral injected voltage V_{inj2a} (CH1), line-line load voltage V_{Lab} (CH2), the line-line source voltage V_{sab} (CH1) and the load current I_{La} (CH4) during the voltage sag event are shown. It can be observed that during the voltage sag event the magnitude of V_{sab} is reduced while the magnitude of V_{Lab} remains constant due to the injected voltage V_{inj2a} which increases during the voltage sag event to compensate for the voltage sag. It can also be observed that the load current I_{La} is constant and in phase with the injected voltage V_{inj2a} which lags V_{sab} and V_{Lab} by 30°. Therefore, from both inverter and dc-dc converter experimental waveforms it can be concluded that the UCAP integrated DVR system hardware setup is able to respond instantaneously to compensate voltage sags.

Similarly, in Figs. 10 (a) and (b) the dc-dc converter and the inverter experimental waveforms are presented for the case where the grid experiences a voltage swell of 1.2pu magnitude which lasts for 1 min duration. It can be observed from Fig. 10 (a) that during the voltage swell E_{cap} is increasing slowly I_{ucav} and $I_{dclnkav}$ are negative while V_{fdc} stays constant. This indicates that the dc-dc converter is able to regulate the dc-link to 260V

and operate in "*Buck*" mode to Charge the UCAP and absorb the additional power from the grid during the voltage swell into the UCAP which also proves the bidirectional capability of the converter. It can be observed from Fig. 10 (b) that during the voltage swell event the magnitude of V_{sab} has increased while the magnitude of V_{Lab} remains constant due to the injected voltage V_{inj2a} which increases to compensate for the voltage swell. It can also be observed that the load current I_{La} is constant and in phase with the injected voltage V_{inj2a} which lags V_{sab} and V_{Lab} by 180°. Therefore, from the inverter and dc-dc converter experimental waveforms it can be concluded that hardware setup is able to respond instantaneously to compensate voltages swells and operate in bidirectional mode.

TABLE I Series Inverter and Dc-dc converter Experimental Results

SERIES INVERTER EXPERIMENTAL RESULTS						
Zone	Φ	V_{inj2a} (V)	I_{La} (A)	P_{inv} (W)	P_{dc} (W)	η (%)
Sag	0°	102.5	6.8	2091	2206	94.7
Swell	225°	42.43	6.7	-603	-494	83.3
DC-DC CONVERTER EXPERIMENTAL RESULTS						
Zone	E_{cap} (V)	I_{ucav} (A)	I_{dclnk} (A)	P_{in} (W)	P_{out} (W)	η (%)
Sag	126.0	19.0	8.1	2406.6	2206	91.6
Swell	106.0	-4.0	1.9	-494.0	-424.0	85.8

In Table I the inverter and the bi-directional dc-dc converter experimental results are presented for both the sag and swell cases. The values listed in the table for the inverter are the RMS values of the Zoomed in portion of V_{inj2a} and I_{La} waveforms of Figs. 9 (b) and 10 (b). Similarly, the values listed for the dc-dc converter are the values which fall on the Y-bar of Figs. 9 (a) and 10 (a), respectively. Based on these values the inverter output power P_{inv} can be computed using (6) and the inverter input power P_{dc} is the

output power of the dc-dc converter. Based on the values of the input and output powers of the inverter and the dc-dc converter their respective efficiencies can be computed. It can be observed that both the inverter and the dc-dc converter are very efficient for the voltage sag case while their efficiencies drop a little for the voltage swell case where the lower power levels of operation impact the efficiency. Finally, it can be observed that both the dc-dc converter and the inverter have bidirectional capability allowing the DVR integrated with UCAP energy storage to both discharge and absorb active power from the grid instantaneously and compensate Temporary Sags/Swells or Interruptions on the distribution grid which last from 3s-1min. This kind of integration will be necessary to improve the active power capability of the DVR.

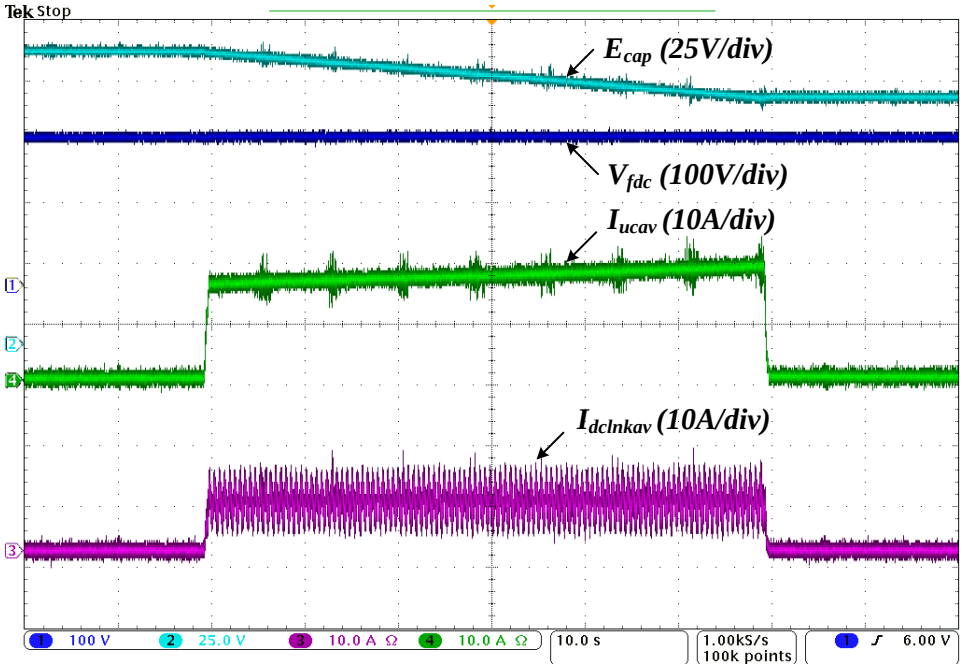

Fig. 9 (a) UCAP and bi-directional dc-dc converter experimental waveforms E_{cap} (CH1), V_{fdc} (CH2), I_{dclnk} (CH3) and I_{ucav} (CH4) during voltage sag

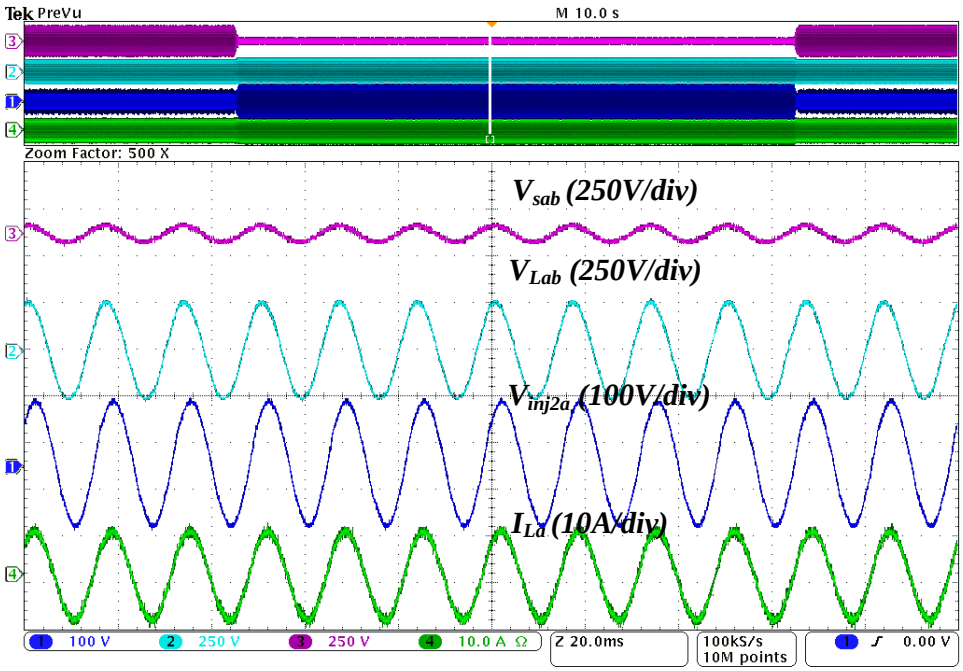

Fig. 9 (b) UCAP and bi-directional dc-dc converter experimental waveforms E_{cap} (CH1), V_{fdc} (CH2), I_{dclnk} (CH3) and I_{ucav} (CH4) during voltage sag

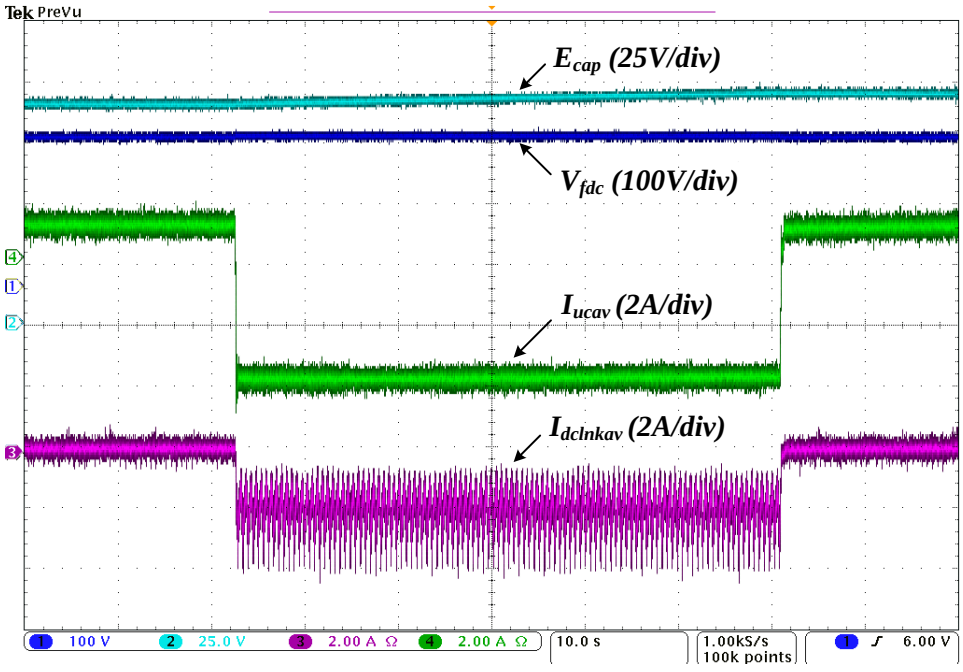

Fig. 10 (a) UCAP and dc-dc converter experimental waveforms E_{cap} (CH1), V_{fdc} (CH2), I_{dclnk} (CH3) and I_{ucav} (CH4) during voltage swell

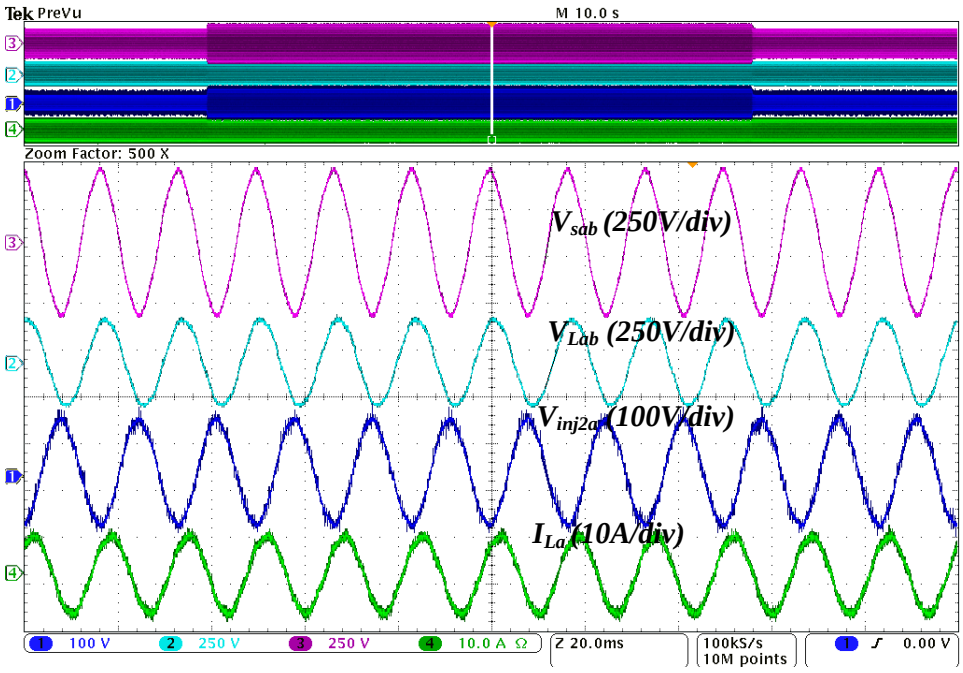

Fig. 10 (b) Inverter experimental waveforms V_{sab} (CH1), V_{Lab} (CH2) and V_{inj2a} (CH3) and I_{La} (CH4) during the voltage swell

VI. CONCLUSION

In this paper, the concept of integrating UCAP based rechargeable energy storage to the DVR system to improve its voltage restoration capabilities is explored. With this integration the DVR will be able to independently compensate voltage sags and swells without relying on the grid to compensate for faults on the grid. The UCAP integration through a bi-directional dc-dc converter at the dc-link of the DVR is proposed. The power stage and control strategy of the series inverter which acts as the DVR are discussed. The control strategy of the inverter is based on in-phase compensation which is simple and easy to implement when the DVR system has the ability to provide active power. Designs of major components in the power stage of the bi-directional dc-dc converter are discussed. Average current mode control is used to regulate the output

voltage of the dc-dc converter due to its inherently stable characteristic. The simulation of the UCAP-DVR system which consists of the UCAP, dc-dc converter, and the grid-tied inverter is carried out using PSCAD. Hardware experimental setup of the integrated system is presented and the ability to provide Temporary Voltage Sag and Swell compensation to the distribution grid dynamically is tested. Results from simulation and experiment agree well with each other thereby verifying the concepts introduced in this paper. Similar UCAP based energy storages can be deployed in the future in a micro-grid or a low voltage distribution grid to respond to dynamic changes in the voltage profiles of the grid and prevent sensitive loads from voltage disturbances.

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III. An UltracapacitorIntegrated Power Conditioner for Reducing Intermittencies and Improving Power Quality of Distribution Grid

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***Abstract*—Penetration of various types of distributed energy resources (DERs) such as solar, wind and PHEVs into the distribution grid is on the rise. There is a corresponding increase in power quality problems and intermittencies on the distribution grid. In order to reduce the intermittencies and improve the power quality of the distribution grid, an ultracapacitor (UCAP) integrated power conditioner is proposed in this paper. UCAP integration provides the power conditioner active power capability which is useful in mitigating the grid intermittencies and in improving the voltage sag and swell compensation. UCAPs have low energy density, high power density and fast charge/discharge rates which are all ideal characteristics for meeting high power, low energy events such as grid intermittencies andsags/swells. In this paper, a UCAP is integrated into the dc-link of the power conditioner through a bi-directional dc-dc converter which helps in providing a stiff dc-link voltage. The integration helps in providing active/reactive power support, intermittency smoothing, and sags/swell compensation. Design and control of both the dc-ac inverters and the dc-dc converter are discussed. The simulation model of the overall system is developed and compared to the experimental hardware setup.**

Index Terms-**UCAP, APF, DVR, dc-dc converter, DSP, sag/swell, d-q control, energy storage integration**

VII. INTRODUCTION

Power quality is a major cause of concern in the industry and it is important to maintain good power quality on the grid. Therefore, there is renewed interest in power

quality products like the dynamic voltage restorer (DVR) and the active power filter (APF). The DVR prevents sensitive loads from experiencing voltage sags/swells [2-3] and the active power filter (APF) prevents the grid from supplying non-sinusoidal currents when the load is non-linear [4]. The concept of integrating the dynamic voltage restorer (DVR) and active power filter (APF) through a back-back inverter topology was first introduced in [1] and the topology was called a unified power quality conditioner (UPQC). The design goal of the UPQC was to improve the power quality of the distribution grid by being able to provide sag, swell and harmonic current compensation. With the increase in penetration of the distributed energy resources (DERs) such as wind, solar and PHEVs, there is a corresponding increase in grid intermittencies and power quality problems on the distribution grid in the *seconds* to *minutes* time scale [17]. Integration of energy storage into the distribution grid is a potential solution which helps in addressing various power quality problems and problems related to grid intermittencies [5-8]. Applications where energy storage integration is needed are being identified and efforts are being made to make energy storage integration commercially viable on a large scale [9-10].

Renewable intermittency smoothing is one application which requires active power support from energy storage in the *seconds* to *minutes* time scale [10]. Different types of optimal controls are being explored to provide smoothing of DERs [12-18]. In [12] a super capacitor and flow battery hybrid energy storage system is integrated into the wind turbine generator to provide wind power smoothing and the system is tested using a real time simulator. In [13] a super capacitor is used as an auxiliary energy storage for PV/fuel cell and a model based controller is developed for providing optimal control. In

[14], a battery energy storage system based control to mitigate wind/PV fluctuations is proposed. In [15] a multi-objective optimization method to integrate battery storage for improving PV integration into the distribution grid is proposed. In [16], a rule based control is proposed to optimize the battery discharge while dispatching intermittent renewable resources. In [17], optimal sizing of a zinc bromine based battery for reducing the intermittencies in wind power is proposed. Voltage sag and swell compensation is another application which needs active power support from the energy storage in the *milliseconds* to *seconds* duration [11].

Active and reactive power support and renewable intermittency smoothing can be provided by modifying the controls of the APF [4] when the APF has active power capability. Voltage sag/swell compensation can be provided by the DVR with active power capability by modifying its controls [3]. A UPQC which has active power capability can meet all the above mentioned control objectives. Energy storage integration is necessary to have active power capability. Various types of rechargeable energy storage technologies based on superconducting magnets (SMES), flywheels (FESS), batteries (BESS) and ultra-capacitors (UCAPs) are compared in [7]. Of all the rechargeable energy storage technologies, UCAPs are ideal for providing active power support for high power, low energy events such as voltage sags/swells and renewable intermittency smoothing which require support in the *seconds* to *minutes* time scale [7]. However, the voltage profile of the UCAP changes as the UCAP discharges and therefore a bi-directional dc-dc converter is necessary for providing a stiff dc-link, voltage which in turn is necessary to provide accurate control.

In this paper, a UCAP-based energy storage integration through a power conditioner into the distribution grid is proposed and the following application areas are addressed,

- Integration of the UCAP with a power conditioner system provides the system *active power capability,*
- *Active power capability* is necessary for independently compensating voltage sags/swells and to provide active and reactive power support and intermittency smoothing to the grid,
- Experimental validation of the UCAP, dc-dc converter, inverter their interface and control,
- Development of inverter and dc-dc converter controls to provide sag/swell compensation and active/reactive support to the distribution grid, and
- Hardware integration and performance validation of the integrated PC-UCAP system.

VIII. THREE-PHASE INVERTERS

A. Power Stage

The one line diagram of the system is shown in Fig. 1. The power stage consists of two back to back 3-phase voltage source inverters connected through a dc-link capacitor. The UCAP energy storage is connected to the dc-link capacitor through a bi-directional dc-dc converter. The series inverter is responsible for compensating the voltage sags and swells and the shunt inverter is responsible for active/reactive power support and renewable intermittency smoothing. The complete circuit diagram of the series DVR, shunt APF and the bi-directional dc-dc converter is shown in Fig. 2. Both the

inverter systems consist of an IGBT module, its gate-driver, LC filter and an isolation transformer. The dc-link voltage V_{dc} is regulated at 260V for optimum voltage and current compensation of the converter and the line-line voltage V_{ab} is 208V. The goal of this project is to provide the integrated power conditioner and UCAP system with active power capability 1) to compensate *temporary voltage sags* (0.1-0.9pu) and *swells* (1.1-1.2pu) which last from 3seconds to 1minute [11], and 2) to provide active and reactive support and renewable intermittency smoothing which is in the *seconds* to *minutes* time scale.

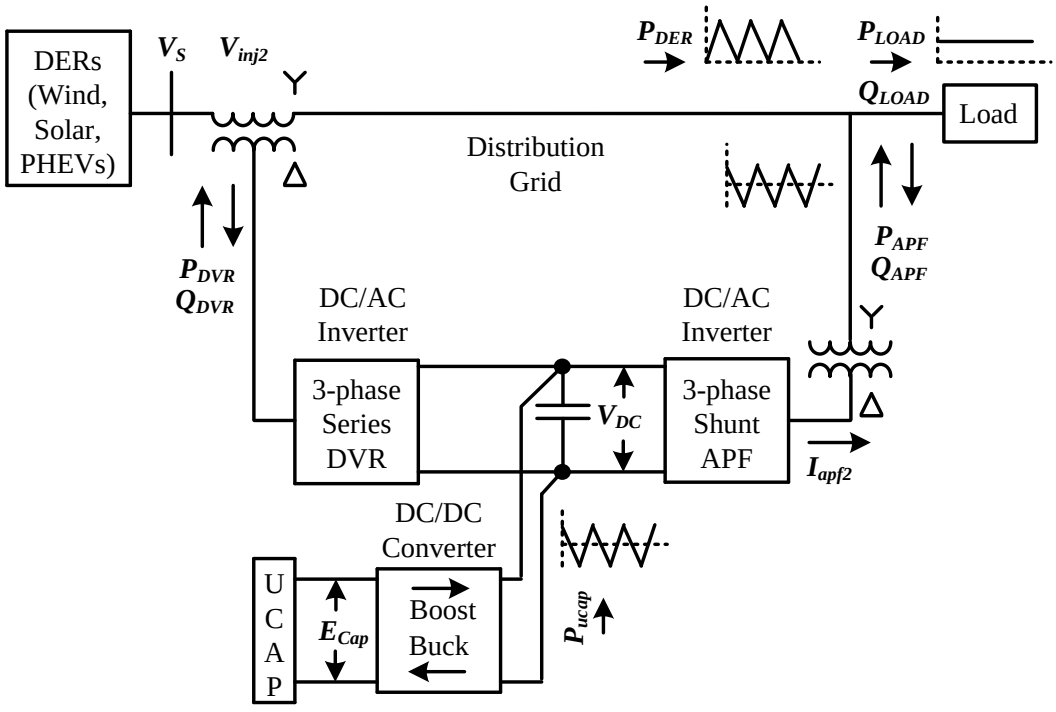

Fig. 1 One line diagram of Power Conditioner with UCAP Energy Storage

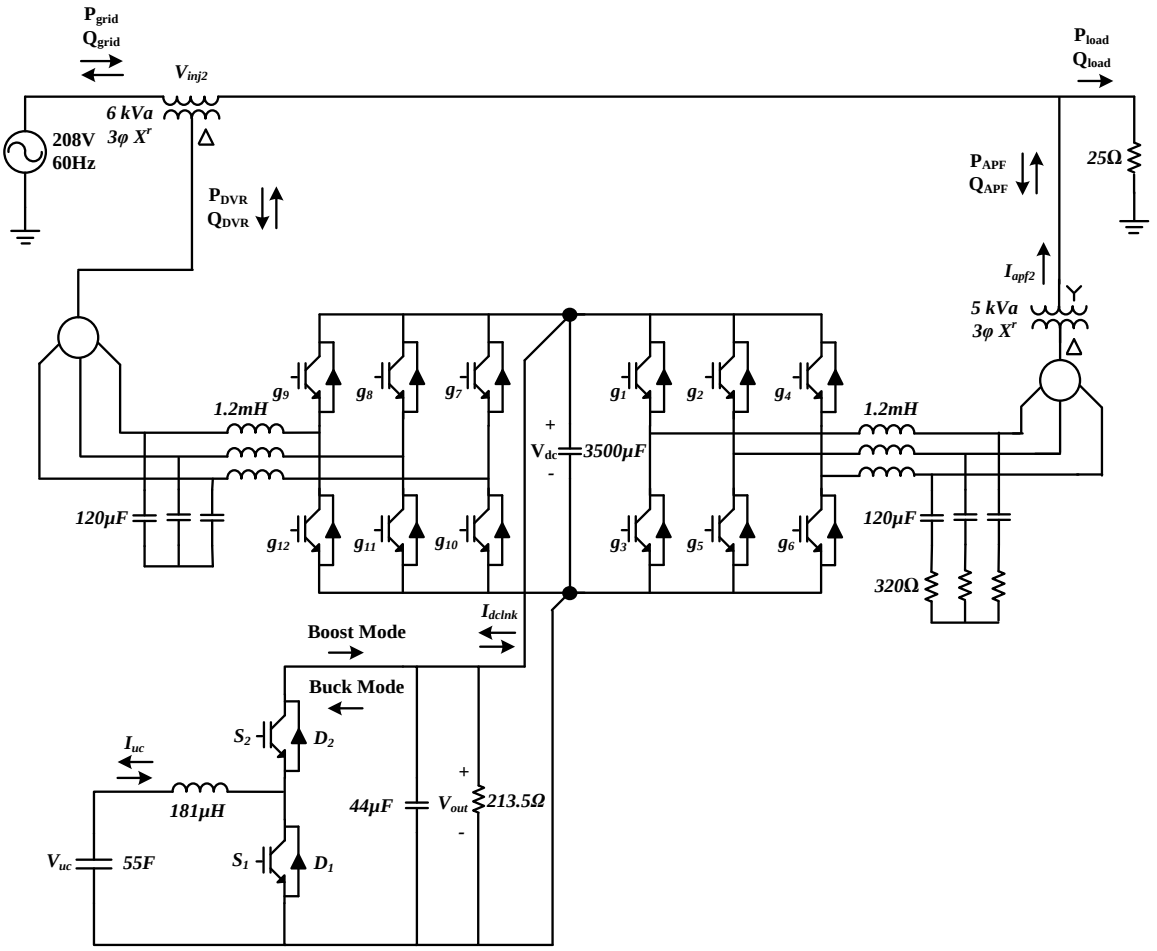

Fig. 2 Model of Power Conditioner with UCAP Energy Storage

B. Controller Implementation

The controller block diagram for the series DVR and the shunt APF is shown in Fig. 3. The series inverter controller implementation is based on the *in-phase compensation* method which requires a PLL for estimating θ. This has been implemented using the *fictitious power method* described in [1]. Based on the estimated θ, the line-line source voltages V_{ab}, V_{bc}, V_{ca} (which are available for this delta-sourced system) are transformed into the d-q domain and the line-neutral components of the source voltage V_{sa}, V_{sb} and V_{sc} (which are not available) can be estimated using:

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\left(\theta - \frac{\pi}{6}\right) & \sin\left(\theta - \frac{\pi}{6}\right) \\ -\sin\left(\theta - \frac{\pi}{6}\right) & \cos\left(\theta - \frac{\pi}{6}\right) \end{bmatrix} \begin{bmatrix} \frac{V_d}{\sqrt{3}} \\ \frac{V_q}{\sqrt{3}} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} V_{refa} \\ V_{refb} \\ V_{refc} \end{bmatrix} = m * \begin{bmatrix} \left(\sin\theta - \frac{V_{sa}}{169.7}\right) \\ \left(\sin\left(\theta - \frac{2\pi}{3}\right) - \frac{V_{sb}}{169.7}\right) \\ \left(\sin\left(\theta + \frac{2\pi}{3}\right) - \frac{V_{sc}}{169.7}\right) \end{bmatrix} \quad (2)$$

$$P_{dvr} = 3V_{inj2a(rms)} I_{La(rms)} \cos\varphi$$
$$Q_{dvr} = 3V_{inj2a(rms)} I_{La(rms)} \sin\varphi \quad (3)$$

These voltages are normalized to unit sine waves using a line-neutral system voltage of $120V_{rms}$ as reference and compared to unit sine waves *in-phase* with actual system voltages V_s from (2) to find the injected voltage references V_{ref} necessary to maintain a constant voltage at the load terminals, where m is the modulation index (0.45 for this case). Therefore, whenever there is a voltage sag or swell on the source side a corresponding voltage V_{inj2} is injected in-phase by the DVR and the UCAP system to negate the effect and retain a constant voltage V_L at the load end. The actual active and reactive power supplied by the series inverter can be computed using (3) from the RMS values of injected voltage V_{inj2a} and load current I_{La} and φ is the phase difference between the two waveforms.

$$P_{ref} = -\frac{3}{2} v_{sq} i_{qref}$$
$$Q_{ref} = -\frac{3}{2} v_{sq} i_{dref} \quad (4)$$

$$\begin{bmatrix} i_{refa} \\ i_{refb} \\ i_{refc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{dref} \\ i_{qref} \end{bmatrix} \quad (5)$$

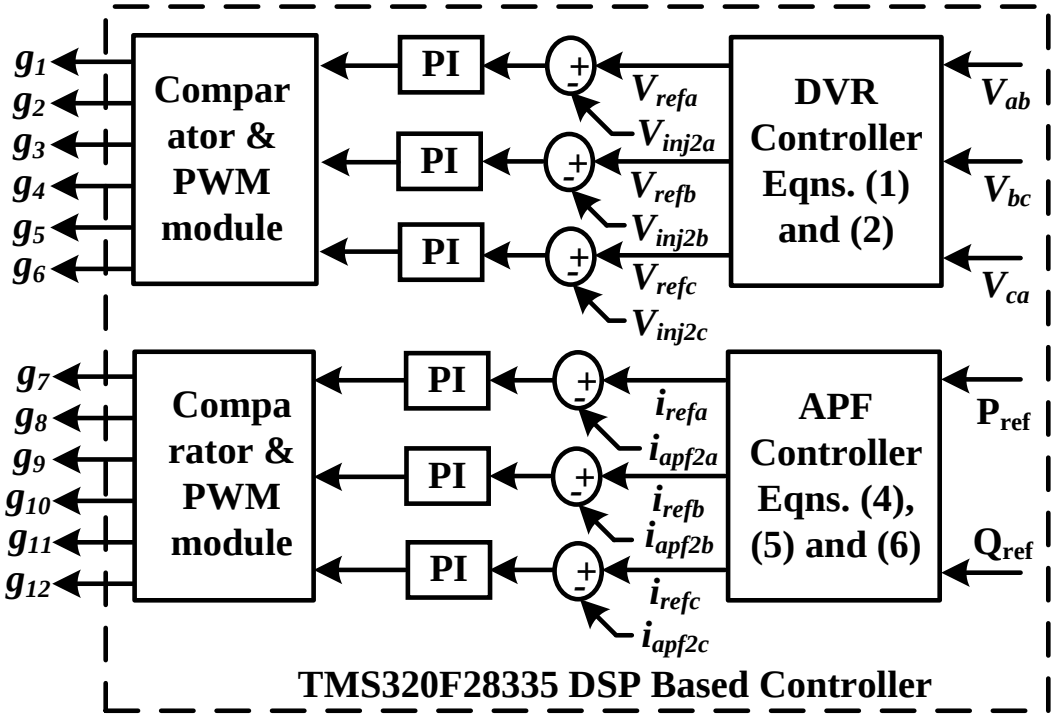

Fig. 3 Controller block diagram for DVR and APF

IX. UCAP AND BI-DIRECTIONAL DC-DC CONVERTER

A. UCAP Bank Hardware Setup

The choice of the number of UCAPs necessary for providing grid support depends on the amount of support needed, terminal voltage of the UCAP, dc-link voltage and distribution grid voltages. For a 260V dc-link voltage, it is practical and cost effective to use three 48V modules in the UCAP bank. Therefore, for this paper the experimental setup consists of three 48V, 165F UCAPs (BMOD0165P048) manufactured by Maxwell

Technologies which are connected in series. Assuming that the UCAP bank can be discharged to 50% of its initial voltage ($V_{uc,ini}$) to final voltage ($V_{uc,fin}$) from 144V to 72V, this translates to depth of discharge of 75% and the energy in the UCAP bank available for discharge is given by:

$$E_{UCAP} = \frac{1}{2} * C * \frac{({V_{uc,ini}}^2 - {V_{uc,fin}}^2)}{60}\ W - min$$

$$E_{UCAP} = {}^{1}/_{2} * {}^{165}/_{3} * {}^{(144^2 - 72^2)}/_{60} \quad (6)$$

$$= 7128\ \text{W-min}$$

B. Bi-directional Dc-dc Converter and Controller

A bi-directional dc-dc converter is required as an interface between the UCAP and the dc-link since the UCAP voltage varies with the amount of energy discharged whereas the dc-link voltage must to be stiff. The model of the bi-directional dc-dc converter and its controller are shown in Fig. 4. The amount of active power support required by the grid during a voltage sag event is dependent on the depth and duration of the voltage sag and the dc-dc converter should be able to withstand this power during "*Discharge*" mode. The dc-dc converter should also be able to operate in bi-directional mode to be able to "*Charge*" or absorb additional power from the grid during voltage swell event. In this paper, the bi-directional dc-dc converter acts as a boost converter while "*discharging*" power from the UCAP and as a buck converter while "*charging*" the UCAP from the grid.

Average current mode control which is widely explored in literature [19] is used to regulate the output voltage of the bi-directional dc-dc converter in both *Buck* and *Boost* modes while *Charging* and *Discharging* the UCAP bank. This method is typically more

stable when compared to other methods such as voltage mode control and peak current mode control. An average current mode controller is shown in Fig. 4 where the actual output voltage V_{out} is compared with the reference voltage V_{ref} and the error is passed through the voltage compensator $C_1(s)$ which generates the average reference current I_{ucref}.

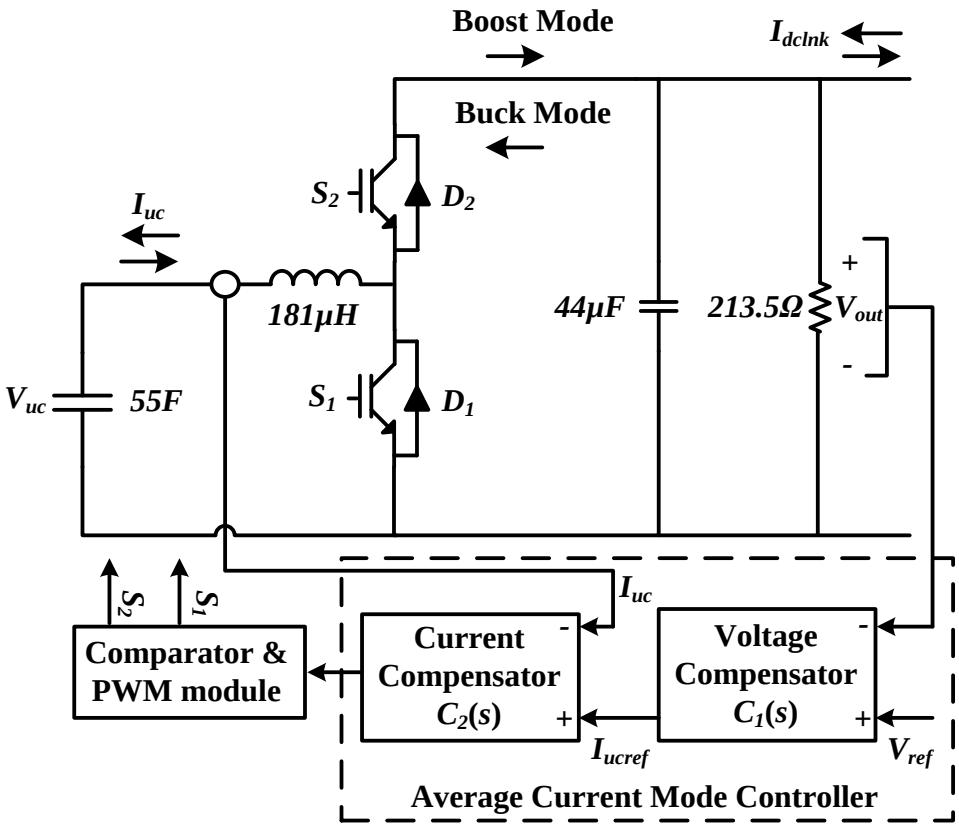

Fig. 4 Model of the bi-directional dc-dc converter and its controller

X. SIMULATION RESULTS

The simulation of the proposed UCAP integrated power conditioner system is carried out in PSCAD for a 208V, 60Hz system where 208V is 1pu. The system response for a three-phase voltage sag which lasts for 0.1s and has a depth of 0.64pu is shown in

Figs. 5 (a)-(e). It can be observed from Fig. 5 (a) that during voltage sag the source voltage V_{srms} is reduced to 0.36pu whereas the load voltage V_{Lrms} is maintained constant at around 1.01pu due to the voltages injected *in-phase* by the series inverter. This can also be observed from the plots of the line-line source voltages (V_{sab}, V_{sbc}, V_{sca}) in Fig. 5 (b), the line-line load voltages (V_{Lab}, V_{Lbc}, V_{Lca}) in Fig. 5 (c), and the line-neutral injected voltages of the series inverter (V_{inj2a}, V_{inj2b}, V_{inj2c}) in Fig. 5 (d). In Fig. 6 (a), the plots of the bi-directional dc-dc converter are presented and it can be observed that the dc-link voltage V_{fdc} is regulated at 260V, the average dc-link current $I_{dclnkav}$ and the average UCAP current I_{ucav} increase to provide the active power required by the load during the sag. This can also be observed from various active power plots shown in Fig. 6 (b) where the power supplied to the load P_{load} remains constant even during the voltage sag when the grid power P_{grid} is decreasing. The active power deficit of the grid is met by the DVR power P_{dvr} which is almost equal to the input power to the inverter P_{dc_in} available from the UCAP. Therefore, it can be concluded from the plots that the active power deficit between the grid and load during the voltage sag event is being met by the UCAP-based energy storage system through the bi-directional dc-dc converter and the inverter. It can also be noticed that the grid reactive power Q_{grid} reduces during the voltage sag while Q_{dvr} increases to compensate for the reactive power loss in the system. Similar analyses can also be carried out for voltage sags which occur in one of the phases (A, B, or C) or in two of the phases (AB, BC, or CA) however, a 3-phase voltage sag case requires the maximum active power support and is therefore presented in these results.

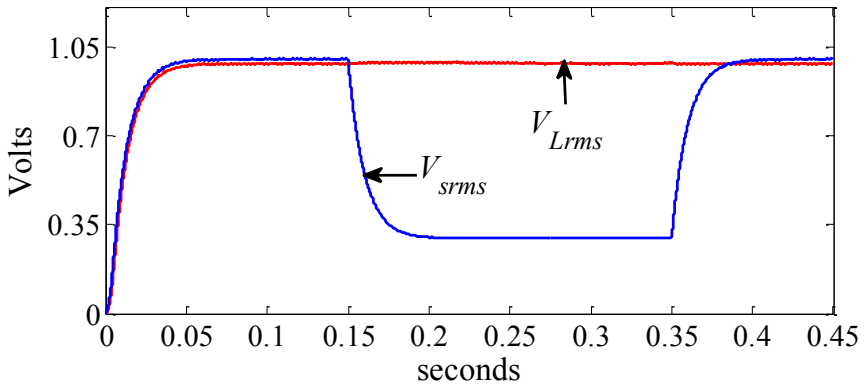

Fig. 5 (a) Source and load RMS voltages V_{srms} and V_{Lrms} during sag

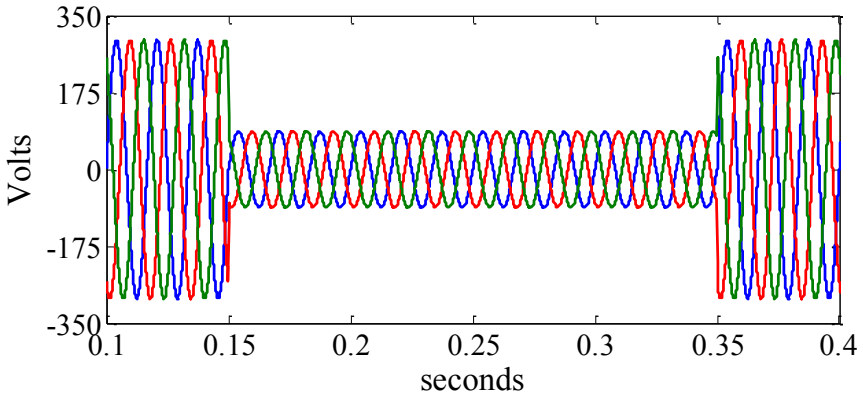

Fig. 5 (b) Source voltages V_{sab} (blue), V_{sbc} (red), V_{sca} (green) during sag

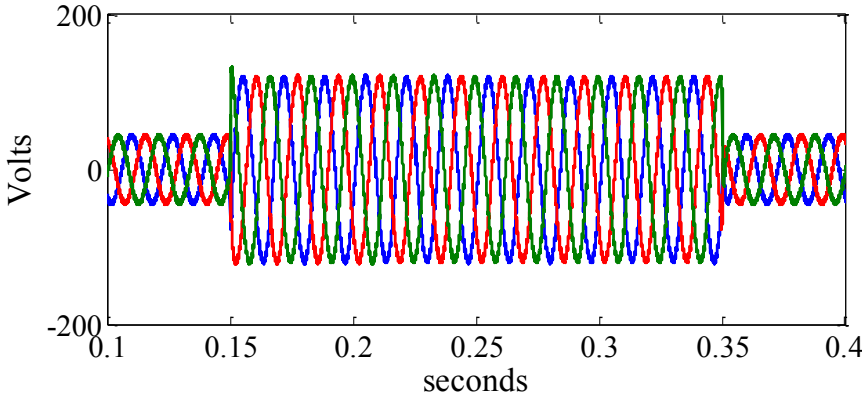

Fig. 5 (c) Injected voltages V_{inj2a} (blue), V_{inj2b} (red), V_{inj2c} (green) during sag

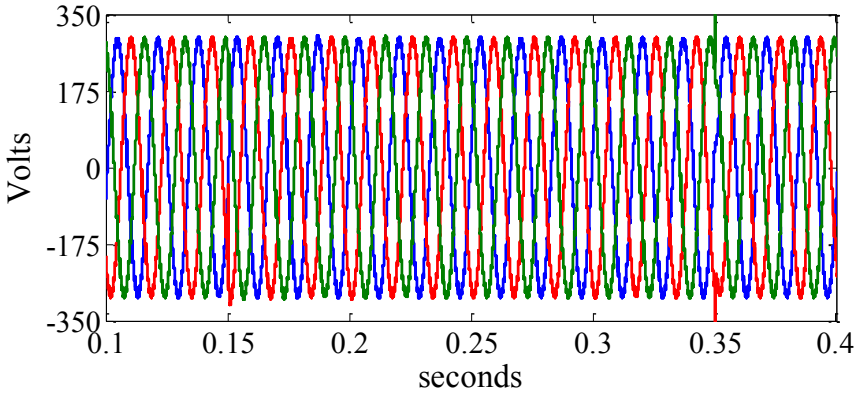

Fig. 5 (d) Load voltages V_{Lab} (blue), V_{Lbc} (red), V_{Lca} (green) during sag

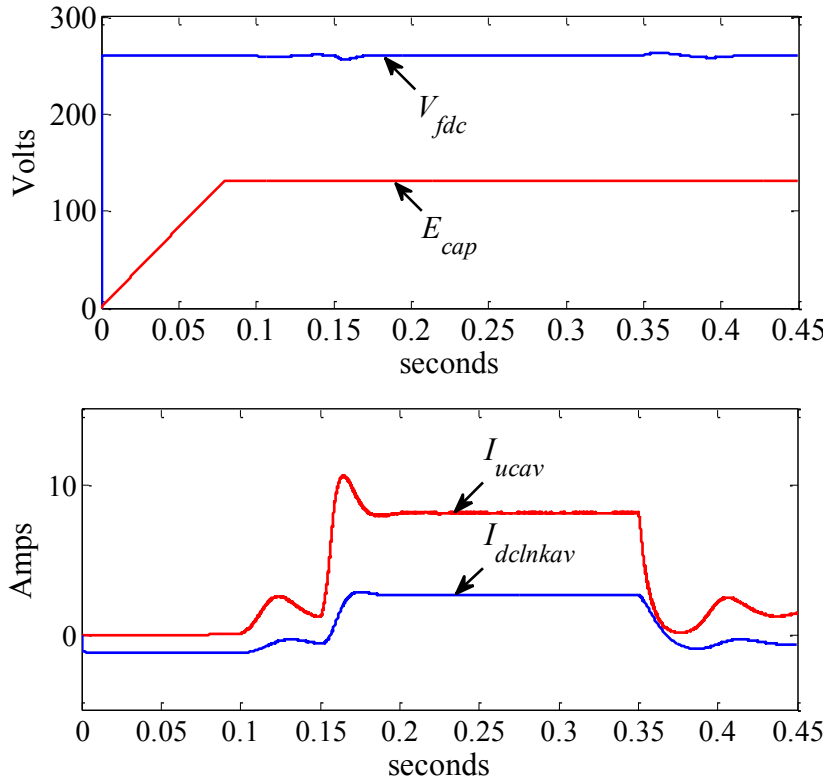

Fig. 6 (a) Currents and voltages of dc-dc converter

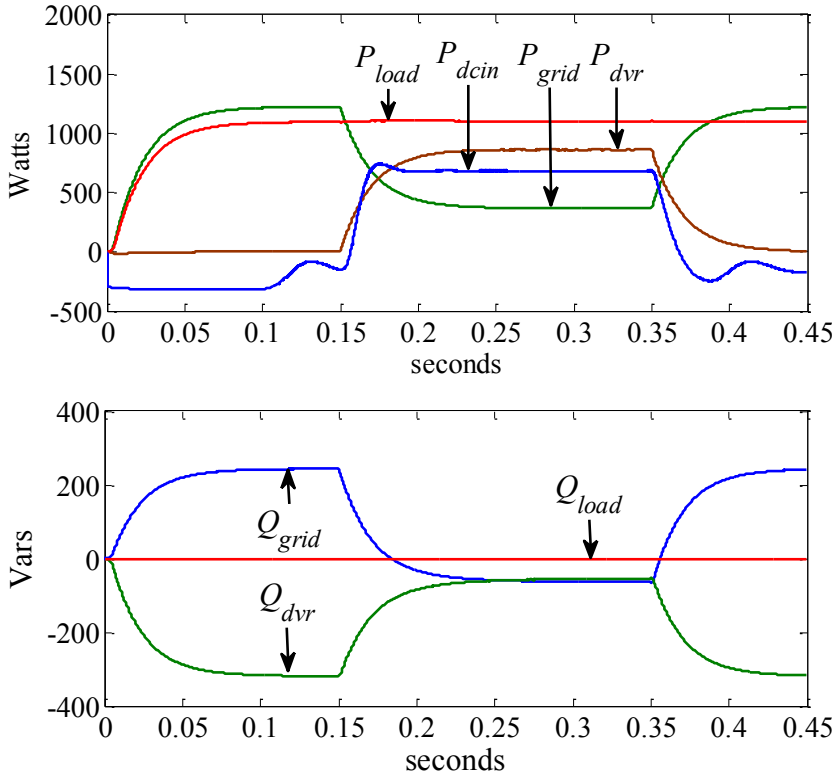

Fig. 6 (b) Active power of grid, load and inverter during voltage sag

The proposed UCAP integrated power conditioner system's performance is also simulated for the active and reactive power support case. The system response is simulated for the reactive power support mode for the initial 0.225s where i_{dref} =-15A for the initial 0.225s which translates to a Q_{ref} of 3819Var from (5). For the remainder of the simulation interval the system response is simulated for active power support mode with i_{qref}=-12A which translates to P_{ref} of 3054W. It can be observed from the currents and voltages of the dc-dc converter waveforms in Fig. 7 (a) that the dc-link voltage V_{fdc} remains constant in both the modes. While the UCAP current I_{ucav} and the corresponding dc-link current $I_{dclnkav}$ are higher for active power support case when compared to the reactive power support case. In Fig. 7 (b) the active and reactive power curves for both the modes are shown and it can be observed from the active and reactive power curves

that the reactive power Q_{apf} reaches the commanded value in the reactive power support mode and the active power P_{dcin} supplied by the UCAP is minimal in this case. In the active power support mode the UCAP and the inverter system supply the required active power and the additional power flows back into the grid. This can be observed from the P_{dcin}, P_{grid}, P_{load} and P_{apf} waveforms.

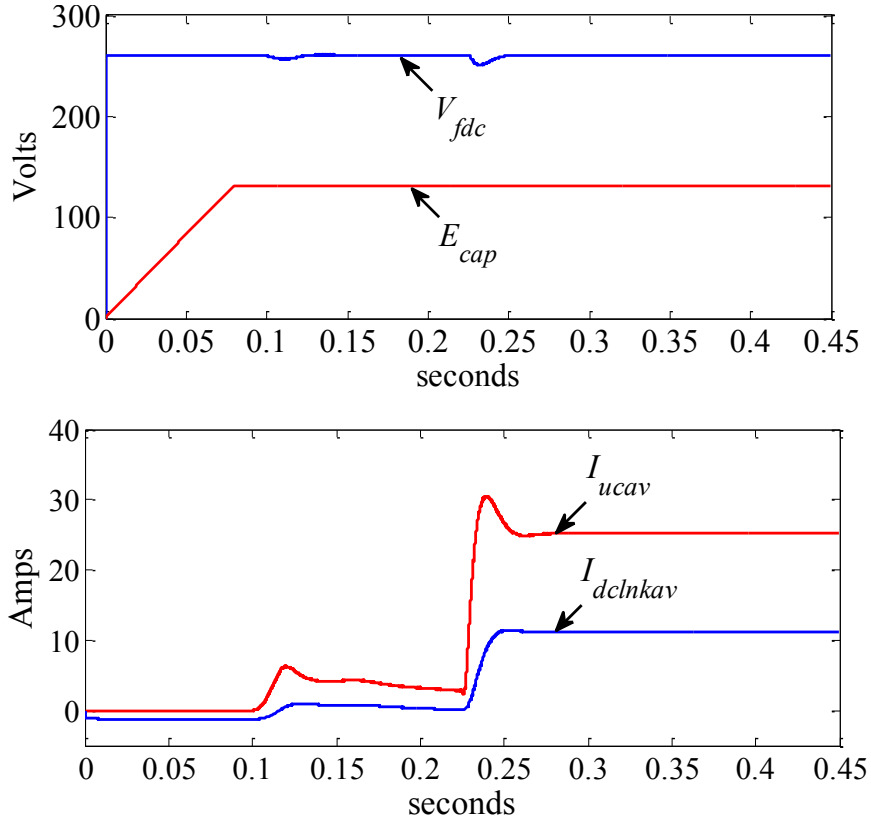

Fig. 7 (a) Currents and voltages of bi-directional dc-dc converter for i_{dref} = -15.0A (reactive power support) and i_{qref} =-12.0A (active power support)

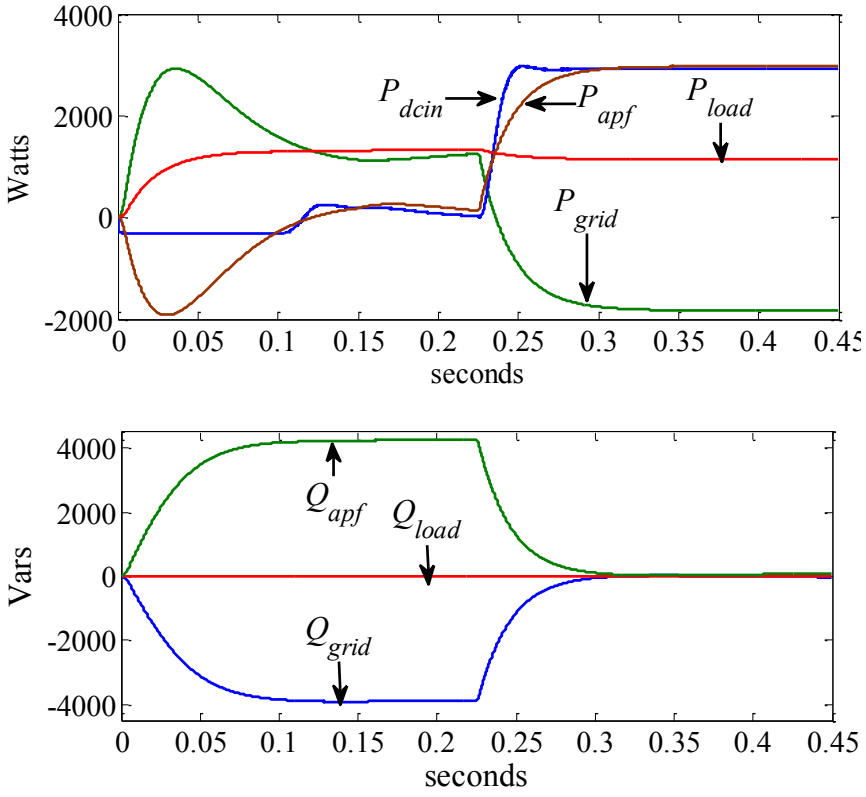

Fig. 7 (b) Grid, load and inverter active and reactive power curves for i_{dref} = -15.0A (reactive power support) and i_{qref} =-12.0A (active power support)

XI. EXPERIMENTAL RESULTS

To verify the concept and simulation results experimentally, a hardware prototype of the complete system was constructed and is shown in Figs. 8 (a) and (b). Fig. 8 (a) shows the complete inverter system which is divided into 4 shelves. The top most shelf consists of a sensor board, an interface board, a TMS320F28335 DSP controller, and the power supply circuit. The 2nd shelf consists of the series and shunt inverters connected back-back through a dc-link capacitor. Each inverter consists of an IGBT module (BSM100GD60DLC) which is a 600V 100A six-pack module from Infineon, and its gate driver SKHI 61R manufactured by SEMIKRON. The inverters are connected back-to-back through a 3500µF 450Vdc dc-link capacitor. The 3rd shelf has the

LC-filters of the series and the shunt inverters. The LC filter of the shunt inverter consists of 1.2 mH 45A 3-phase inductor and three 120μF 240Vac capacitors connected in a wye configuration through 320Ω damping resistors. The series inverter LC filter consists of another 1.2 mH 45A 3-phase inductor and 3-phase 2.5kVar capacitors connected in delta configuration. The 4th shelf consists of three 2kVA 125V/50V single phase isolation transformers for the series inverter connected in delta configuration on the primary side and the secondary sides are connected in series with the grid through a protection circuit breaker. The 4th shelf also has a 5kVA Δ-Y (125V/208V) isolation transformer for the shunt inverter where the secondary side is connected to the grid through a protection circuit breaker. Fig. 8 (b) shows the UCAP, the bi-directional dc-dc converter, the oscilloscope and the industrial power corruptor.

In Figs. 9 (a) and (b), the experimental waveforms of the series inverter and the bi-directional dc-dc converter are shown for the case where the grid experiences a voltage sag of 0.6pu magnitude for a 1 minute duration. In Fig. 9 (a), the dc-link voltage V_{fdc} (CH1), the UCAP voltage E_{cap} (CH2), the dc-link current I_{dclnk} (CH3) and the average UCAP current I_{ucav} (CH4) are shown. It can be observed from Fig. 9 (a) that during the voltage sag, E_{cap} is decreasing rapidly and I_{ucav} is increasing rapidly, whereas V_{fdc} and $I_{dclnkav}$ are constant. Therefore, the dc-dc converter is able to regulate the dc-link voltage to 260V and operate in "*Boost*" mode to discharge active power during a voltage sag event to meet the active power deficit between the grid and the load. In Fig. 9 (b) the zoomed-in versions of the line-neutral injected voltage V_{inj2a} (CH1), line-line source voltage V_{Lab} (CH2), the line-line load voltage V_{Lab} (CH1) and the load current I_{La} (CH4) during the voltage sag event are shown. It can be observed that during the voltage sag

event the magnitude of V_{sab} is reduced while the magnitude of V_{Lab} remains constant due to the injected voltage V_{inj2a} which increases during the voltage sag event to compensate for the voltage sag. Therefore, from both inverter and dc-dc converter experimental waveforms it can be concluded that the UCAP integrated DVR system hardware setup is able to respond instantaneously to compensate voltage sags.

Fig. 8 (a) Sensor, Interface and DSP boards (1st), Dc-link capacitor and Inverter (2nd), LC filter (3rd), Isolation Transformer (4th)

Fig. 8 (b) Dc-dc converter and MSO4034B oscilloscope (top shelf), UCAP bank with 3 UCAPs (bottom shelf) and the Industrial Power Corruptor

In Fig. 10 (a) the experimental waveforms of the bi-directional dc-dc converter are shown with the UCAP voltage E_{cap} (CH1), the dc-link voltage V_{fdc} (CH2), the average UCAP current I_{ucav} (CH3) and the dc-link current I_{dclnk} (CH4). Fig. 10 (a) is divided into 7 zones which are labeled from 1 through 7 in the plots. In zone 1 the inverter is supplying only reactive power and the dc-dc converter is maintaining a stiff dc-link voltage. Zone 2 is a transition mode in which the inverter is changing from supplying reactive power to

active power. In Zones 3, 4, and 5, the inverter is supplying only active power to the grid which is being discharged from the UCAP. In Zones 4 and 5, the inverter is supplying only active power to the grid. However, the amount of active power supplied to the grid in Zone 5 is less than that in Zone 4, which is again less than that in Zone 3. This relationship can be observed from the I_{dclnk} trace. In Zone 6, the inverter is absorbing active power from the grid which is used for charging the UCAP through the bi-directional dc-dc converter. Zone 7 is again a transition mode in which the inverter is changing from supplying active power to supplying reactive power to the grid. In Zone 8 again the inverter is supplying only reactive power to the grid and the dc-dc converter is maintaining a stiff dc-link voltage.

In Fig. 10 (b), the magnified view of Zone 1 is presented where the inverter is only providing reactive power support to the grid by commanding i_{dref}=-10.0A. This can be concluded from the fact that I_{apf2a} is lagging V_{sa} by around 92°. Similarly, it can be noticed from Zones 1 and 7 in Fig. 10 (a) that E_{cap} is nearly constant while I_{ucav} and $I_{dclnkav}$ are nearly zero which proves that the active power discharged from the UCAP while providing reactive power support to the grid is minimal. In Fig. 10 (c) the magnified view of Zone 3 shows where the inverter is only providing active power support to the grid by commanding i_{qref}=-8.0A. This can be concluded from the fact that I_{apf2a} and V_{sa} are almost in phase with little phase difference of around 10°. The results are similar for Zones 4 and 5 where the commanded active power is comparatively less than that in Zone 3. It is important to notice that in Zones 3, 4, and 5, of Fig. 10 (a) that UCAP is discharging power rapidly. Therefore, E_{cap} is decreasing rapidly while V_{fdc} remains constant at 260V and I_{ucav} is increasing rapidly while $I_{dclnkav}$ remains almost constant.

The bi-directional capability of the dc-dc converter and the inverter is necessary for absorbing excess power from any DERs for renewable intermittency smoothing applications. To achieve this objective, i_{qref} is set to 7A and it can be observed from Fig. 10 (d), which is the zoomed in view of Zone 6, that the phase difference between I_{apf2a} and V_{sa} is around 170° which shows that the inverter is absorbing power from the grid. The bi-directional dc-dc converter operates in buck mode to absorb power from the grid. This can be seen from Zone 6 of Fig. 9 (a) where both I_{ucav} and $I_{dclnkav}$ are negative while V_{fdc} is at 260V and E_{cap} is increasing slowly due to the UCAP being charged from the power absorbed from the grid.

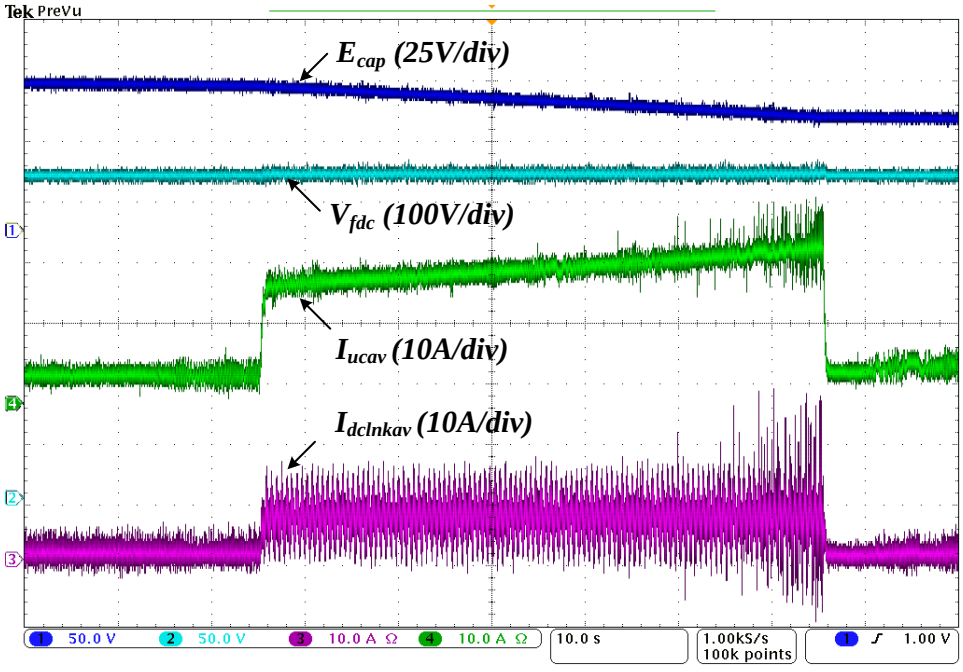

Fig. 9 (a) UCAP and bi-directional dc-dc converter experimental waveforms E_{cap} (CH1), V_{fdc} (CH2), I_{dclnk} (CH3) and I_{ucav} (CH4) during voltage sag

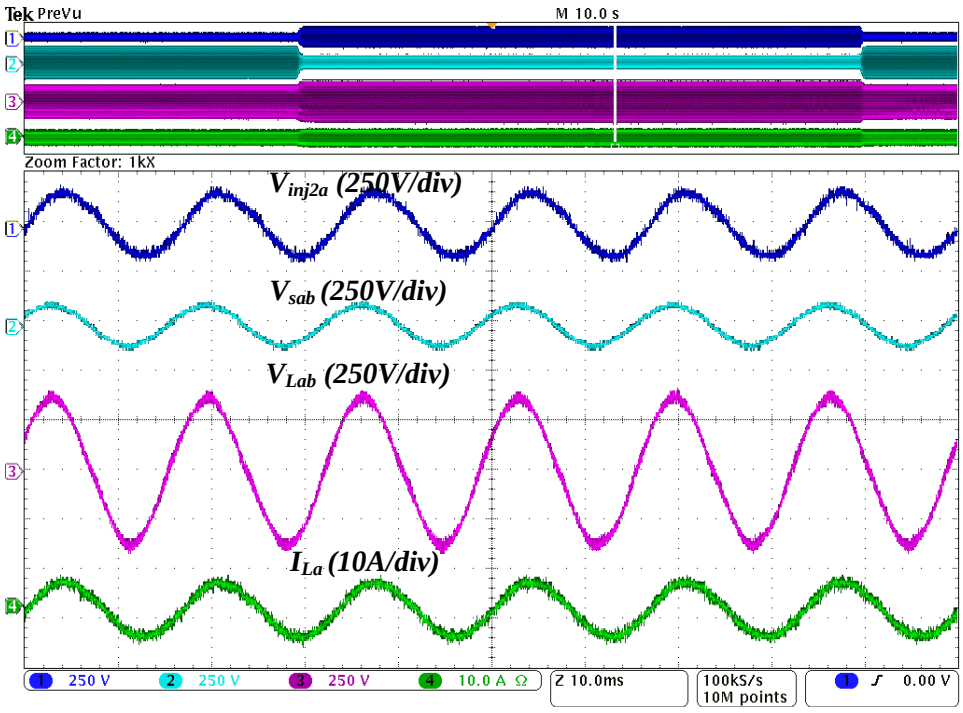

Fig. 9 (b) UCAP and bi-directional dc-dc converter experimental waveforms E_{cap} (CH1), V_{fdc} (CH2), I_{dclnk} (CH3) and I_{ucav} (CH4) during voltage sag

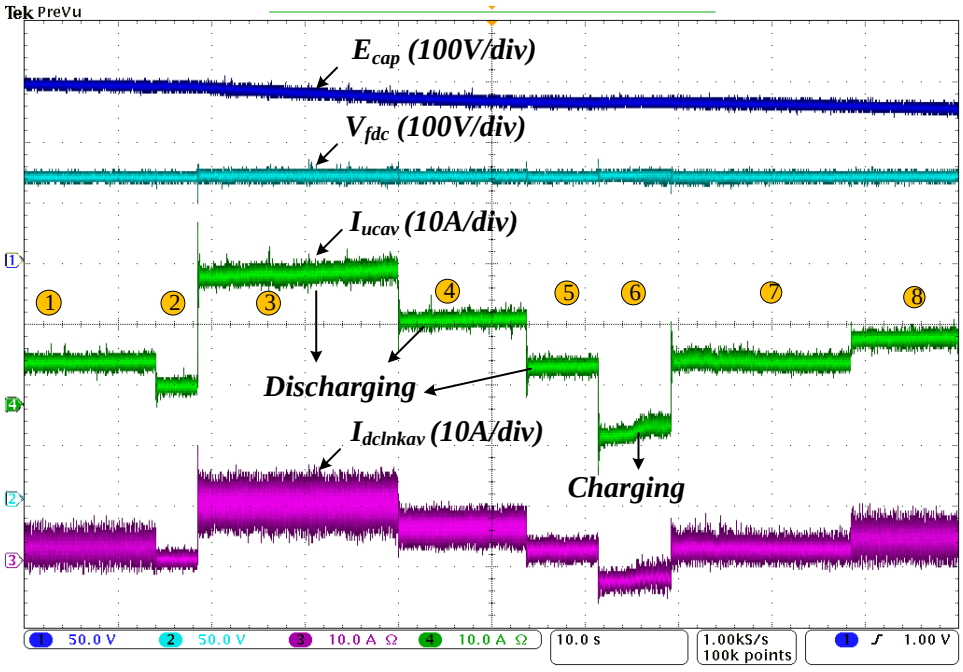

Fig. 10 (a) UCAP and dc-dc converter experimental waveforms E_{cap} (CH1), V_{fdc} (CH2), I_{dclnk} (CH3) and I_{ucav} (CH4) during voltage swell

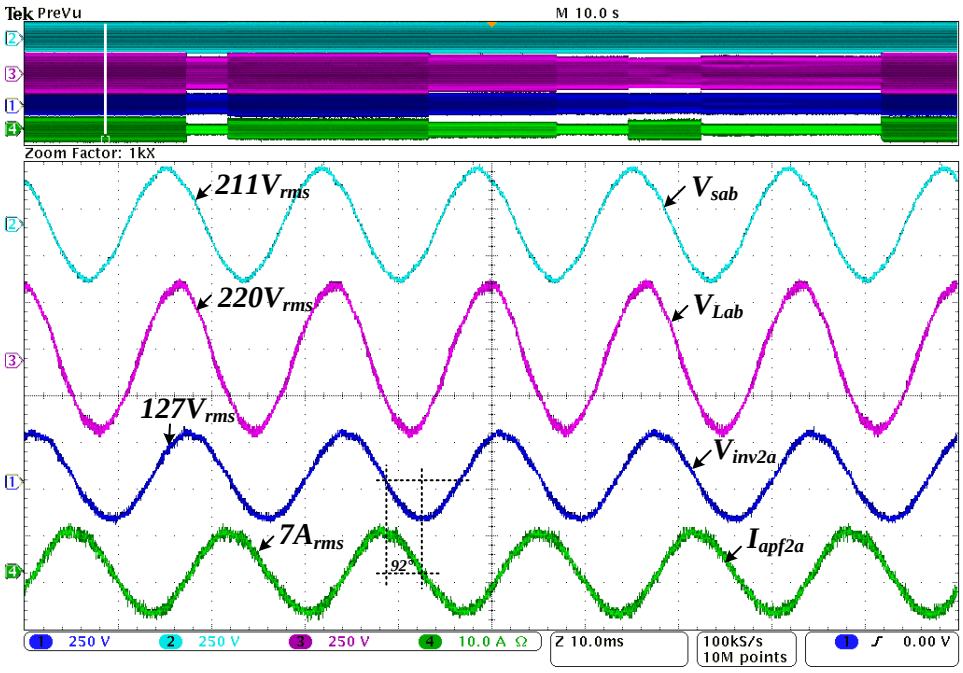

Fig. 10 (b) Inverter experimental waveforms V_{ab} (CH1), V_{inv1a} (CH2), V_{sa} (CH3) and I_{apf2a} (CH4) for zone 1 (reactive power support i_{dref} =-10.0A)

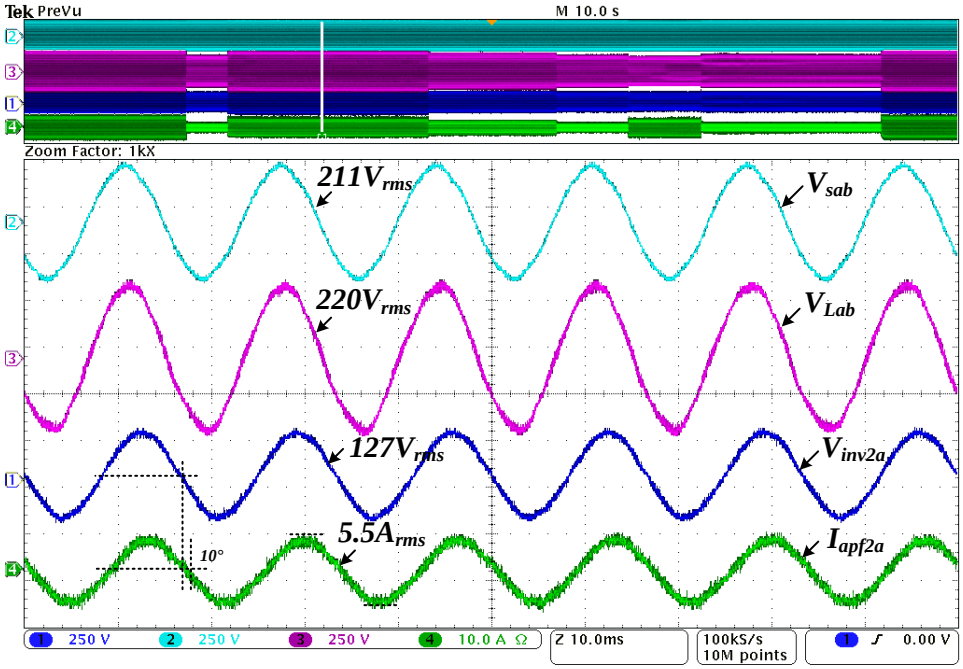

Fig. 10 (c) Inverter experimental waveforms V_{sab} (CH1), V_{Lab} (CH2), V_{sa} (CH3) and I_{apf2a} (CH4) for zone 3 (active power support i_{qref} =-8.0A)

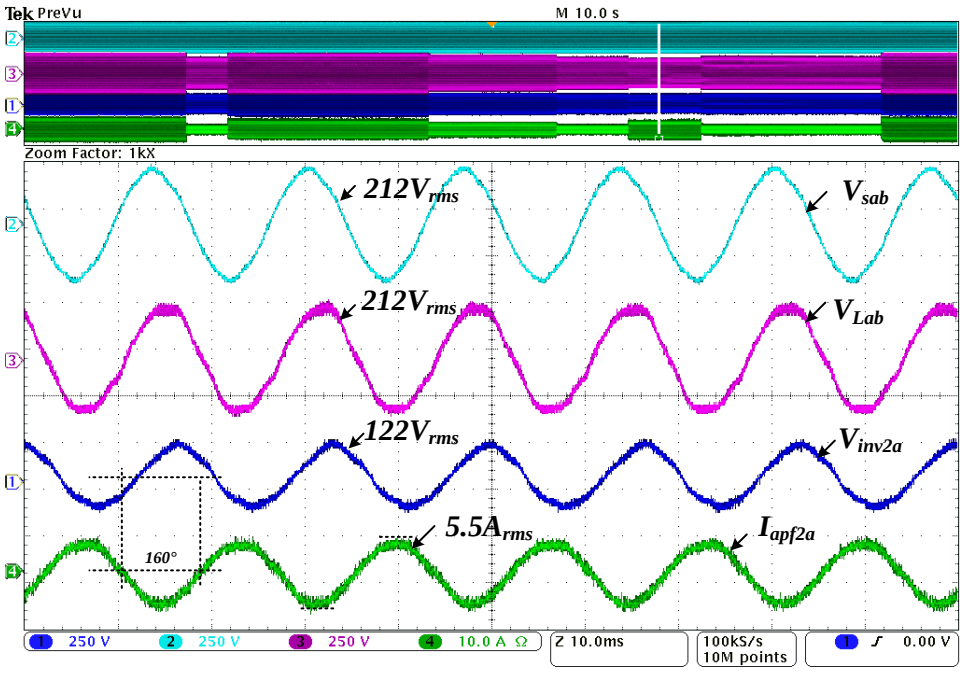

Fig. 10 (d) Inverter experimental waveforms V_{ab} (CH1), V_{inv1a} (CH2), V_{sa} (CH3) and I_{apf2a} (CH4) for zone 6 (UCAP charging i_{qref} =8.0A)

XII. CONCLUSION

In this paper, the concept of integrating UCAP-based rechargeable energy storage to a power conditioner system to improve the power quality of the distribution grid is presented. With this integration the DVR portion of the power conditioner will be able to independently compensate voltage sags and swells and the APF portion of the power conditioner will be able to provide active and reactive power support and renewable intermittency smoothing to the distribution grid. UCAP integration through a bi-directional dc-dc converter at the dc-link of the power conditioner is proposed. The control strategy of the series inverter (DVR) is based on the in-phase compensation and the control strategy of the shunt inverter (APF) is based on the i_d-i_q method. Designs of major components in the power stage of the bi-directional dc-dc converter are discussed.

Average current mode control is used to regulate the output voltage of the dc-dc converter due to its inherently stable characteristic. The simulation of the UCAP-UPQC system is carried out using PSCAD. A hardware experimental setup of the integrated system is presented and the ability to provide temporary voltage sag compensation and active and reactive power support and renewable intermittency smoothing to the distribution grid is tested. Results from simulation and experiment agree well with each other thereby verifying the concepts introduced in this paper. Similar UCAP-based energy storage can be deployed in the future in a micro-grid or a low voltage distribution grid to respond to dynamic changes in the voltage profiles and power profiles on the distribution grid.

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SECTION

2. CONCLUSION

In this dissertation, the concept of integrating UCAP-based rechargeable energy storage to the distribution grid is proposed. UCAP based energy storage is ideal for providing support to high power events on the distribution grid which require support in the *few seconds* to *few minutes* time scale. In this regard, the main contribution of this dissertation is proof of concept validation and hardware integration of UCAP-based energy storage into the distribution grid. The hardware integration is carried out in three parts

- In the first paper, an integrated UCAP-APF is designed to provide the integrated system with active power capability such that it will be able to provide active power support, reactive power support and renewable intermittency smoothing to the distribution grid from few seconds to 10 minutes time scale.
- In the second paper, an integrated UCAP-DVR is designed to allow the integrated system to independently compensate temporary voltage sags and voltage swells on the distribution grid which occur in the 3seconds-1minute time scale without relying on the grid to compensate for faults on the grid.
- In the third paper, the UCAP bank is integrated with a power conditioner (PC) which integrates both the APF and DVR topologies. The new integrated UCAP-PC will be able to provide the combined functionality of both the DVR and the APF. With this integration, the DVR portion of the power conditioner will be able to independently compensate voltage sags and swells and the APF

portion of the power conditioner will be able to provide active/reactive power support and renewable intermittency smoothing to the distribution grid.

The UCAP integration through a bi-directional dc-dc converter at the dc-link of the APF, DVR and power conditioner is proposed. The control strategy of the series inverter (DVR) is based on the in-phase compensation and the control strategy of the shunt inverter (APF) is based on the i_d-i_q method. Designs of major components in the power stage of the bi-directional dc-dc converter are discussed. Average current mode control is used to regulate the output voltage of the dc-dc converter due to its inherently stable characteristic. The simulation of the UCAP-PC system is carried out using PSCAD. A hardware experimental setup of the integrated system is presented and the ability to provide temporary voltage sag compensation and active and reactive power support and renewable intermittency smoothing to the distribution grid is tested. Results from simulation and experiment agree well with each other thereby verifying the concepts introduced. Similar UCAP based energy storages can be deployed in the future in a micro-grid or a low voltage distribution grid to respond to dynamic changes in the voltage profiles and power profiles on the distribution grid in a smart grid scenario.

3. FUTURE WORK

In the future as the concepts of smart grid and the ‘Energy for Internet’ evolve there will be exchange of power between the distribution grid and the consumer. Distributed energy resources (DERs) will be integrated into the distribution grid and energy storage will play a major role in solving problems related to grid intermittencies. As the cost of energy storage decreases and energy storage integration into the grid becomes more viable there will be higher penetration of energy storage into the grid. Power electronics and control will play a major role in the integration of energy storage. New improved topologies, better switching devices, improved efficiencies and reduction in sizing and cost of the power electronic converters will play a major role in integrating energy storage into the grid. In this dissertation, an UCAP integrated through a bi-directional dc-dc converter at the dc-link of the APF, DVR and power conditioner is proposed. Future work would include ways to provide additional functionalities such as frequency regulation through dc-ac inverter. Future work would also include ways to improve the efficiency and reduce the cost of the bi-directional dc-dc converter and the dc-ac inverter. Currently, the bi-directional dc-dc converter is operating in a hard switched fashion with a maximum efficiency of 90%. However, the efficiency can be further improved by reducing the switching losses through the use of soft switching mechanisms. The cost of the system might be reduced through the use of Z-source inverters in which the functionalities of the dc-dc converter and dc-ac inverter are combined into a single topology through passive components. However, lack of in-depth knowledge about the design of the Z-source inverter and their control complexity are major hurdles which will add to the design time.

APPENDIX A

THREE-PHASE PLL IMPLEMENTATION

In this section the discussion on the concept behind the development of the PLL implementation is presented. The PLL used for calculating θ has been implemented using the fictitious power method described in [1] and the circuit is shown in Fig. 1. The circuit is based on the equations (1), (2) and (3) for instantaneous 3-phase power $p'_{3\varphi}$ which is the sum of an average part $\bar{p}'_{3\varphi}$ and an oscillating part $\tilde{p}'_{3\varphi}$. It can be observed from the circuit that the i'_a and i'_c are not exactly measured and hence the name *fictitious power method*. Also, it should be noted that the system converges when $\bar{p}'_{3\varphi}$ given in (3) reaches zero. This happens when $\cos\emptyset = 0$ and $\emptyset = 90°$ i.e. when I_{+1} is orthogonal to the positive sequence voltage V_{+1} and leads V_{+1}; this can be noticed in Fig. 2. The system reaches steady state when the PI controller (K_p=30, K_i=200) filters out the oscillating portion $\tilde{p}'_{3\varphi}$ and the average portion $\bar{p}'_{3\varphi}$ becomes zero. This can be observed in the last plot in Fig. 2 where $p'_{3\varphi}$ has zero average value and the oscillations in $p'_{3\varphi}$ are damped to a great extent. And ω has oscillations which are proportional to the oscillations in $p'_{3\varphi}$. Also, the main advantage of this method is it tracks the positive sequence voltage V_{+1} instead of the actual system voltage which is very useful in unbalanced systems.

$$p'_{3\varphi} = v_a i'_a + v_b i'_b + v_c i'_c \tag{1}$$

$$p'_{3\varphi} = v_{ab} i'_a + v_{cb} i'_c \tag{2}$$

$$p'_{3\varphi} = \bar{p}'_{3\varphi} + \tilde{p}'_{3\varphi} = 3V_{+1} I_{+1} \cos\emptyset \tag{3}$$

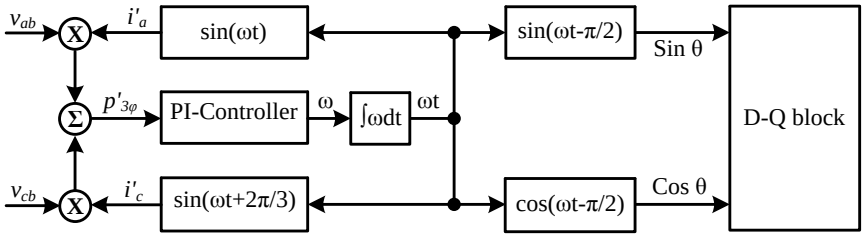


Fig. 1 Three-phase PLL circuit which tracks positive sequence voltage V_{+1}

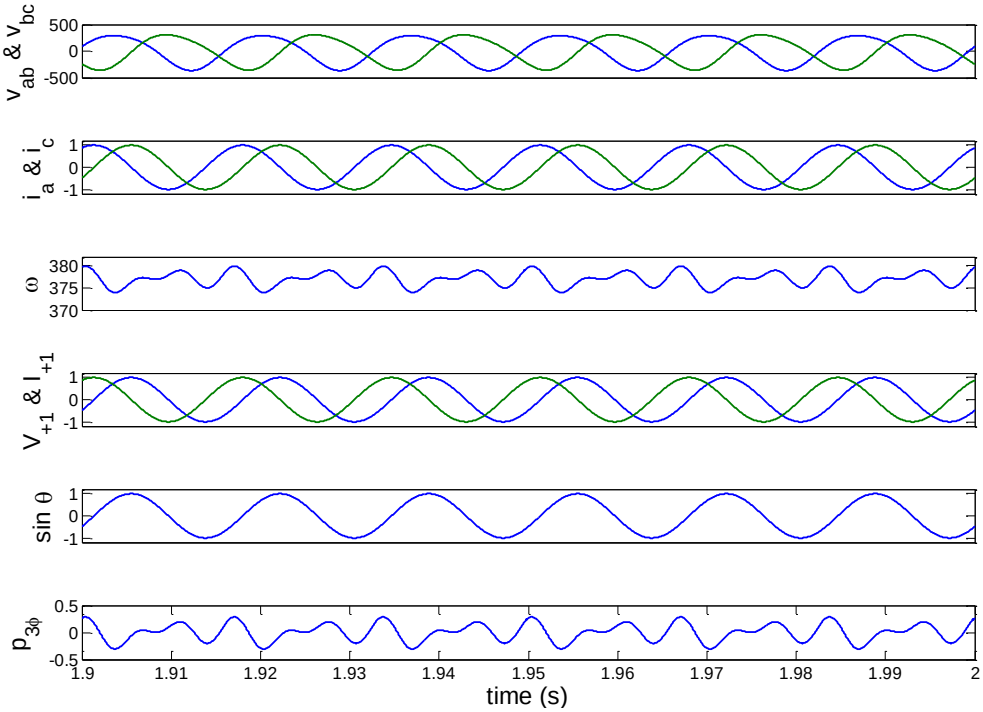


Fig. 2 Results for Three-phase PLL circuit (sin θ tracks the positive sequence voltage V_{+1})

APPENDIX B

EMBEDDED C CONTROLLER CODE FOR DSP

This appendix lists the software programs developed for DSP-based data acquisition and A/D conversion, conversion and PWM switching signal generation of the power conditioner system which includes the controller codes for the series DVR and shunt APF. The complete program LabSeries_Shunt.c with descriptive comments is given below:

```
//
//     LabSeries_Shunt: TMS320F28335
//     (c) Deepak Somayajula
//
//###########################################################################
//
// FILE:   LabSeries_Shunt.c
//
// TITLE: DSP28335ControlCARD; Digital Output
//         4 - bit - counter at 4 LEDs LD1(GPIO9), LD2(GPIO11), LD3(GPIO34)
//         and LD4 (GPIO49)
//         software delay loop; watchdog enabled
//         solution file for LabCurrent_Reference.c
//###########################################################################
//  Ver | dd mmm yyyy | Who  | Description of changes
// =====|=============|======|===============================================
//  3.0 | 5 Mar 2013 | F.B. | LabSeries_Shunt for F28335;
//###########################################################################
#include "DSP2833x_Device.h"
#include <cmath>
#define AdcBufLen 50

//external function prototypes
extern void InitSysCtrl(void);
extern void InitPieCtrl(void);
extern void InitPieVectTable(void);
extern void InitCpuTimers(void);
extern void InitAdc(void);
extern void ConfigCpuTimer(struct CPUTIMER_VARS *, float, float);

// Prototype statements for functions found within this file.
void Gpio_select(void);
void Setup_ePWM(void);
void Setup_ADC(void);
interrupt void cpu_timer0_isr(void);
interrupt void adc_isr(void);

// global variables
float Vab[AdcBufLen+1]={0.0};
float Vbc[AdcBufLen+1]={0.0};
float Vca[AdcBufLen+1]={0.0};

float Vsa[AdcBufLen+1]={0.0};
```

```
float Vsb[AdcBufLen+1]={0.0};
float Vsc[AdcBufLen+1]={0.0};
float vc_alpha[AdcBufLen+1]={0.0};
float vc_beta[AdcBufLen+1]={0.0};

float Irefab[AdcBufLen+1]={0.0};
float Irefbc[AdcBufLen+1]={0.0};
float Irefca[AdcBufLen+1]={0.0};

float Iapfa[AdcBufLen+1]={0.0};
float Iapfb[AdcBufLen+1]={0.0};
float Iapfc[AdcBufLen+1]={0.0};

float z[AdcBufLen+1]={0.0};
float id[AdcBufLen+1]={-5.0};
float vd[AdcBufLen+1]={0.0};

float z1[AdcBufLen+1]={0.0};
float iq[AdcBufLen+1]={0.0};
float vq[AdcBufLen+1]={0.0};
float y2[AdcBufLen+1]={1.5};

float idiffa[AdcBufLen+1]={0.0};
float idiffb[AdcBufLen+1]={0.0};
float idiffc[AdcBufLen+1]={0.0};

float vdiffa[AdcBufLen+1]={0.0};
float vdiffb[AdcBufLen+1]={0.0};
float vdiffc[AdcBufLen+1]={0.0};

float xa[AdcBufLen+1]={0.0};
float xb[AdcBufLen+1]={0.0};
float xc[AdcBufLen+1]={0.0};

float ya[AdcBufLen+1]={0.0};
float yb[AdcBufLen+1]={0.0};
float yc[AdcBufLen+1]={0.0};

//float ILa_mean[5]={0.0};
float P[AdcBufLen+1]={0.0};
float Pdot[AdcBufLen+1]={0.0};
float w[AdcBufLen+1]={377.0};
float wt[AdcBufLen+1]={0.0};
float t[AdcBufLen+1]={0.0};
float sinth[AdcBufLen+1]={0.0};
float sinth1[AdcBufLen+1]={0.0};
float sinth2[AdcBufLen+1]={0.0};
float sinth3[AdcBufLen+1]={0.0};
float costh[AdcBufLen+1]={0.0};
float costh1[AdcBufLen+1]={0.0};

static Uint16 ind=0,indmin1=0,c=0;
float Kp1=0.45,Kp=0.18,Kd=0.0e-5,Ki=50.0,idref=-2.0,iqref=-2.0,cal_I=-45.0,cal_V=226.0,vref=0.00591;
//###########################################################################
//                  main code
//###########################################################################
```

```
void main(void)
{
   int counter=0;     // binary counter for digital output
   InitSysCtrl();     // Basic Core Initialization

   EALLOW;
   SysCtrlRegs.WDCR = 0x00AF;
   EDIS;

   DINT;            // Disable all interrupts

   Gpio_select();     // GPIO58, GPIO60, GPIO34 and GPIO49 as output
                  // to 4 LEDs at Peripheral Explorer)

   Setup_ePWM();      // init of ePWM1A, ePWM2A, ePWM3A

   Setup_ADC();       // ADC setup program

   InitPieCtrl();
   InitPieVectTable();

   EALLOW;
   PieVectTable.TINT0 = &cpu_timer0_isr;
   PieVectTable.ADCINT = &adc_isr;
   EDIS;

   InitCpuTimers();
   ConfigCpuTimer(&CpuTimer0, 150, 16.667);

   PieCtrlRegs.PIEIER1.bit.INTx7 = 1;
   PieCtrlRegs.PIEIER1.bit.INTx6 = 1;

   IER|=1;
   EINT;
   ERTM;
   CpuTimer0Regs.TCR.bit.TSS = 0;
   while(1)
   {
         while(CpuTimer0.InterruptCount == 0);
         CpuTimer0.InterruptCount = 0;

         EALLOW;
         SysCtrlRegs.WDKEY = 0x55;   // service WD #1
         EDIS;
         counter++;
         //GPIO16 and GPIO18 are complements of nPRST and nRST signals for CPLDs on inverter boards
         GpioDataRegs.GPASET.bit.GPIO16 = 0;
         GpioDataRegs.GPASET.bit.GPIO18 = 0;
   }
}
void Gpio_select(void)
{
   EALLOW;
   GpioCtrlRegs.GPAMUX1.all = 0;      // GPIO15 ... GPIO0 = General Purpose I/O
   GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1; // Configure ePWM1A as active
   GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 1; // Configure ePWM1B as active
```

```
    GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1; // Configure ePWM2A as active
    GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 1; // Configure ePWM2B as active
    GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 1; // Configure ePWM3A as active
    GpioCtrlRegs.GPAMUX1.bit.GPIO5 = 1; // Configure ePWM3B as active

    GpioCtrlRegs.GPAMUX1.bit.GPIO6 = 1;  // Configure ePWM4A as active
    GpioCtrlRegs.GPAMUX1.bit.GPIO7 = 1;  // Configure ePWM4B as active
    GpioCtrlRegs.GPAMUX1.bit.GPIO8 = 1;  // Configure ePWM5A as active
    GpioCtrlRegs.GPAMUX1.bit.GPIO9 = 1;  // Configure ePWM5B as active
    GpioCtrlRegs.GPAMUX1.bit.GPIO10 = 1; // Configure ePWM6A as active
    GpioCtrlRegs.GPAMUX1.bit.GPIO11 = 1; // Configure ePWM6B as active

    GpioCtrlRegs.GPAMUX2.all = 0;     // GPIO31 ... GPIO16 = General Purpose I/O
    GpioCtrlRegs.GPBMUX1.all = 0;     // GPIO47 ... GPIO32 = General Purpose I/O
    GpioCtrlRegs.GPBMUX2.all = 0;     // GPIO63 ... GPIO48 = General Purpose I/O
    GpioCtrlRegs.GPCMUX1.all = 0;     // GPIO79 ... GPIO64 = General Purpose I/O
    GpioCtrlRegs.GPCMUX2.all = 0;     // GPIO87 ... GPIO80 = General Purpose I/O

    GpioCtrlRegs.GPADIR.all = 0;     // GPIO31-0 as inputs
    GpioCtrlRegs.GPADIR.bit.GPIO16 = 1;   // peripheral explorer: LED LD1 at GPIO9
    GpioCtrlRegs.GPADIR.bit.GPIO18 = 1;   // peripheral explorer: LED LD2 at GPIO11

    GpioCtrlRegs.GPBDIR.all = 0;     // GPIO63-32 as inputs
    GpioCtrlRegs.GPBDIR.bit.GPIO34 = 1;   // peripheral explorer: LED LD3 at GPIO34
    GpioCtrlRegs.GPBDIR.bit.GPIO49 = 1; // peripheral explorer: LED LD4 at GPIO49
    GpioCtrlRegs.GPCDIR.all = 0;     // GPIO87-64 as inputs
    EDIS;
}
void Setup_ePWM(void)
{
    EPwm1Regs.TBCTL.bit.CLKDIV = 0;     // CLKDIV = 1
    EPwm1Regs.TBCTL.bit.HSPCLKDIV = 0;  // HSPCLKDIV = 1
    EPwm1Regs.TBCTL.bit.CTRMODE = 2; // up - down mode
    EPwm1Regs.TBCTL.bit.PRDLD = 0;       // Shadow Mode
    EPwm1Regs.AQCTLA.all = 0x0060;    // set ePWM1A on CMPA up
                                // clear ePWM1A on CMPA down
    EPwm1Regs.TBPRD = 6250;           // 12KHz - PWM signal
    EPwm1Regs.CMPA.half.CMPA = 3125;  // 50% duty cycle first

    EPwm1Regs.CMPCTL.bit.SHDWAMODE = 0; // Double-Buffer with Shadow register
    EPwm1Regs.CMPCTL.bit.LOADAMODE = 0; // Load on Counter zero
    EPwm1Regs.DBCTL.bit.OUT_MODE = 3;   // DB Module fully enabled 1A
    EPwm1Regs.DBCTL.bit.POLSEL = 2;     // Active HI Complementary
    EPwm1Regs.DBFED = 100;              // FED of 100*TBclk=2.667us
    EPwm1Regs.DBRED = 100;              // RED of 100*TBclk=2.667us

    EPwm2Regs.TBCTL.bit.CLKDIV =  0;// CLKDIV = 1
    EPwm2Regs.TBCTL.bit.HSPCLKDIV = 0;  // HSPCLKDIV = 1
    EPwm2Regs.TBCTL.bit.CTRMODE = 2; // up - down mode
    EPwm2Regs.AQCTLA.all = 0x0060;    // set ePWM2A on CMPA up
                                // clear ePWM2A on CMPA down

    EPwm2Regs.TBPRD = 6250;           // 12kHz - PWM signal
    EPwm2Regs.CMPA.half.CMPA = 3125;  // 50% duty cycle first
    EPwm2Regs.DBCTL.bit.OUT_MODE = 3;   // DB Module fully enabled on 2A
    EPwm2Regs.DBCTL.bit.POLSEL = 2;     // Active HI Complementary
```

```
    EPwm2Regs.DBFED = 100;            // FED of 100*TBclk=2.667us
    EPwm2Regs.DBRED = 100;            // RED of 100*TBclk=2.667us

    EPwm3Regs.TBCTL.bit.CLKDIV = 0;     // CLKDIV = 1
    EPwm3Regs.TBCTL.bit.HSPCLKDIV = 0;  // HSPCLKDIV = 1
    EPwm3Regs.TBCTL.bit.CTRMODE = 2; // up - down mode
    EPwm3Regs.AQCTLA.all = 0x0060;    // set ePWM3A on CMPA up
                              // clear ePWM3A on CMPA down

    EPwm3Regs.TBPRD = 6250;           // 12kHz - PWM signal
    EPwm3Regs.CMPA.half.CMPA  = 3125;  // 50% duty cycle first
    EPwm3Regs.DBCTL.bit.OUT_MODE = 3;   // DB Module fully enabled on 3A
    EPwm3Regs.DBCTL.bit.POLSEL = 2;     // Active HI Complementary
    EPwm3Regs.DBFED = 100;            // FED of 100*TBclk=2.667us
    EPwm3Regs.DBRED = 100;            // RED of 100*TBclk=2.667us

    EPwm4Regs.TBCTL.bit.CLKDIV = 0;     // CLKDIV = 1
    EPwm4Regs.TBCTL.bit.HSPCLKDIV = 0;  // HSPCLKDIV = 1
    EPwm4Regs.TBCTL.bit.CTRMODE = 2; // up - down mode
    EPwm4Regs.AQCTLA.all = 0x0060;    // set ePWM4A on CMPA up
                              // clear ePWM4A on CMPA down

    EPwm4Regs.TBPRD = 12500;          // 12kHz - PWM signal
    EPwm4Regs.CMPA.half.CMPA  = 6250;  // 50% duty cycle first
    EPwm4Regs.DBCTL.bit.OUT_MODE = 3;   // DB Module fully enabled on 3A
    EPwm4Regs.DBCTL.bit.POLSEL = 2;     // Active HI Complementary
    EPwm4Regs.DBFED = 100;            // FED of 100*TBclk=2.667us
    EPwm4Regs.DBRED = 100;            // RED of 100*TBclk=2.667us

    EPwm5Regs.TBCTL.bit.CLKDIV = 0;     // CLKDIV = 1
    EPwm5Regs.TBCTL.bit.HSPCLKDIV = 0;  // HSPCLKDIV = 1
    EPwm5Regs.TBCTL.bit.CTRMODE = 2; // up - down mode
    EPwm5Regs.AQCTLA.all = 0x0060;    // set ePWM5A on CMPA up
                              // clear ePWM5A on CMPA down

    EPwm5Regs.TBPRD = 12500;          // 12kHz - PWM signal
    EPwm5Regs.CMPA.half.CMPA  = 6250;  // 50% duty cycle first
    EPwm5Regs.DBCTL.bit.OUT_MODE = 3;   // DB Module fully enabled on 3A
    EPwm5Regs.DBCTL.bit.POLSEL = 2;     // Active HI Complementary
    EPwm5Regs.DBFED = 100;            // FED of 100*TBclk=2.667us
    EPwm5Regs.DBRED = 100;            // RED of 100*TBclk=2.667us

    EPwm6Regs.TBCTL.bit.CLKDIV = 0;     // CLKDIV = 1
    EPwm6Regs.TBCTL.bit.HSPCLKDIV = 0;  // HSPCLKDIV = 1
    EPwm6Regs.TBCTL.bit.CTRMODE = 2; // up - down mode
    EPwm6Regs.AQCTLA.all = 0x0060;    // set ePWM6A on CMPA up
                                      // clear ePWM6A on CMPA down

    EPwm6Regs.TBPRD = 12500;          // 12kHz - PWM signal
    EPwm6Regs.CMPA.half.CMPA  = 6250;  // 50% duty cycle first
    EPwm6Regs.DBCTL.bit.OUT_MODE = 3;   // DB Module fully enabled on 3A
    EPwm6Regs.DBCTL.bit.POLSEL = 2;     // Active HI Complementary
    EPwm6Regs.DBFED = 100;            // FED of 100*TBclk=2.667us
    EPwm6Regs.DBRED = 100;            // RED of 100*TBclk=2.667us
}
void Setup_ADC(void)
```

```
{
   InitAdc();
   AdcRegs.ADCTRL1.bit.SEQ_CASC = 1;      //Cascaded Mode
   AdcRegs.ADCTRL1.bit.CONT_RUN = 0;      //No Continuous Run
   AdcRegs.ADCTRL1.bit.CPS = 0;           //Set Prescaler to zero
   AdcRegs.ADCTRL1.bit.ACQ_PS = 3;         //Set sample window (ACQ_PS+1)*1/ADCCLK

   AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1 = 0;
   AdcRegs.ADCTRL2.bit.EPWM_SOCB_SEQ = 0;
   AdcRegs.ADCTRL2.bit.EPWM_SOCB_SEQ2 = 0;
   AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 1;
   AdcRegs.ADCTRL2.bit.INT_MOD_SEQ1 = 0;

   AdcRegs.ADCTRL3.bit.ADCCLKPS = 3;     // Divide HSPCLK by 6
   AdcRegs.ADCTRL3.bit.SMODE_SEL = 0;      // Setup the ADC in Sequential Sampling Mode
   AdcRegs.ADCMAXCONV.bit.MAX_CONV1 = 5;   // 6,9 Conversions per start ADCINA0 to
ADCINA7, ADCINB0

   AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0;     // Setup ADCINA0 as input channel.
   AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 1;     // Setup ADCINA1 as input channel.
   AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 2;     // Setup ADCINA2 as input channel.
   AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 3;     // Setup ADCINA3 as input channel.
   AdcRegs.ADCCHSELSEQ2.bit.CONV04 = 4;     // Setup ADCINA4 as input channel.
   AdcRegs.ADCCHSELSEQ2.bit.CONV05 = 5;     // Setup ADCINA5 as input channel.
}
interrupt void cpu_timer0_isr(void)
{
   //static int up_down=1;
   //float sin_theta,sin_beta,sin_gamma; // Angle in radians for sine-triangle PWM
   CpuTimer0.InterruptCount++;
   AdcRegs.ADCTRL2.bit.SOC_SEQ1 = 1;  // start ADC by software
   EALLOW;
   SysCtrlRegs.WDKEY = 0xAA;  // service WD #2
   EDIS;

   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
}
interrupt void adc_isr(void)
{
   //static Uint16 index=0;              // index into ADC buffers
   float x,h,h3,ic_alpha,ic_beta,valpha,vbeta,wc1;
   GpioDataRegs.GPBSET.bit.GPIO49 = 1;
   x = ((AdcRegs.ADCRESULT0>>4))*7.326e-4;
   wc1=1;//wci=3142.85;
   h = 16.6667e-6;
   h3 = 3.3333e-3;//Ki*h=200*20e-6

   //High Pass Filter code using numerical integration (Forward Euler) methods
   if(ind>0)
   {
   indmin1=ind-1;
   }
   else
   {
   indmin1=50;
   c++;
```

```
   if(c==1 && t[0]==0.0)
   {
      z[indmin1]=0.0;
      id[indmin1]=0.0;
      vd[indmin1]=0.0;
      s//id_ac[indmin1]=0.0;
      z1[indmin1]=0.0;
      iq[indmin1]=0.0;
      vq[indmin1]=0.0;
      //iq_ac[indmin1]=0.0;
      y2[indmin1]=1.5;

      idiffa[indmin1]=0.0;
      idiffb[indmin1]=0.0;
      idiffc[indmin1]=0.0;

      vdiffa[indmin1]=0.0;
      vdiffb[indmin1]=0.0;
      vdiffc[indmin1]=0.0;

      xa[indmin1]=0.0;
      xb[indmin1]=0.0;
      xc[indmin1]=0.0;

      ya[indmin1]=0.0;
      yb[indmin1]=0.0;
      yc[indmin1]=0.0;

      P[indmin1]=0.0;
      Pdot[indmin1]=0.0;
      w[indmin1]=377.0;
      wt[indmin1]=0.0;
      t[indmin1]=0.0;
      sinth[indmin1]=0.0;
      sinth1[indmin1]=0.0;
      sinth2[indmin1]=0.0;
      sinth3[indmin1]=0.0;
      costh[indmin1]=0.0;
      costh1[indmin1]=0.0;
   }
}

Iapfa[ind] = cal_I*(((AdcRegs.ADCRESULT0>>4))*7.326e-4-y2[indmin1]);
Iapfb[ind] = cal_I*(((AdcRegs.ADCRESULT1>>4))*7.326e-4-y2[indmin1]);
Iapfc[ind] = cal_I*(((AdcRegs.ADCRESULT2>>4))*7.326e-4-y2[indmin1]);

Vab[ind] = (((AdcRegs.ADCRESULT3>>4))*7.326e-4-y2[indmin1]);
Vbc[ind] = (((AdcRegs.ADCRESULT4>>4))*7.326e-4-y2[indmin1]);
Vca[ind] = (((AdcRegs.ADCRESULT5>>4))*7.326e-4-y2[indmin1]);

id[ind] = idref;
iq[ind] = iqref;

//Filter to filter the 1.5V noise
y2[ind]= y2[indmin1]+h*wc1*(x-y2[indmin1]);
```

```
ic_alpha= ((id[ind])*costh1[indmin1]-(iq[ind])*sinth1[indmin1]);
ic_beta = ((id[ind])*sinth1[indmin1]+(iq[ind])*costh1[indmin1]);

//ic_alpha= ((id[ind]-id_ac[ind])*costh[indmin1]-(iq[ind]-iq_ac[ind])*sinth[indmin1]);
//ic_beta = ((id[ind]-id_ac[ind])*sinth[indmin1]+(iq[ind]-iq_ac[ind])*costh[indmin1]);

Irefab[ind] = 1.0*ic_alpha;
Irefbc[ind] = -0.5*ic_alpha+0.866*ic_beta;
Irefca[ind] = -0.5*ic_alpha-0.866*ic_beta;

//PI controller for 3-phase PLL
if(wt[indmin1] < 6.2831854)
{
   P[ind]=(Vab[ind]*sin(wt[indmin1])-Vbc[ind]*sin(wt[indmin1]+2.0944));
   Pdot[ind]=P[ind]-P[indmin1];
   w[ind]= w[indmin1]+30.0*Pdot[ind]+h3*P[ind];
   wt[ind]= wt[indmin1]+h*w[ind];
   t[ind]= t[indmin1]+h;
   //sinth[ind] = sin(wt[ind]-1.57079633);      //Locks the PLL to Vsa
   sinth[ind] = sin(wt[ind]-1.04719755);    //for tracking Vab th=angle(Vsa)+30;
   sinth1[ind]= sin(wt[ind]-1.57079633);
   sinth2[ind]= sin(wt[ind]-3.66519143);
   sinth3[ind]= sin(wt[ind]+0.52359878);
   costh1[ind]= cos(wt[ind]-1.57079633);
   //costh[ind] = cos(wt[ind]-1.57079633);
   costh[ind] = cos(wt[ind]-1.04719755);
}
else
{
   wt[indmin1]=0.0;
   P[ind]=(Vab[ind]*sin(wt[indmin1])-Vbc[ind]*sin(wt[indmin1]+2.0944));
   Pdot[ind]=P[ind]-P[indmin1];
   w[ind]= w[indmin1]+30.0*Pdot[ind]+h3*P[ind];
   wt[ind]= wt[indmin1]+h*w[ind];
   t[ind]= t[indmin1]+h;
   //sinth[ind] = sin(wt[ind]-1.57079633);    //Locks the PLL to Vsa
   sinth[ind] = sin(wt[ind]-1.04719755);     //for tracking Vab th=angle(Vsa)+30;
   sinth1[ind]= sin(wt[ind]-1.57079633);
   sinth2[ind]= sin(wt[ind]-3.66519143);
   sinth3[ind]= sin(wt[ind]+0.52359878);
   costh1[ind]= cos(wt[ind]-1.57079633);
   //costh[ind] = cos(wt[ind]-1.57079633);
   costh[ind] = cos(wt[ind]-1.04719755);
}

xa[ind]= (Irefab[ind]-Iapfa[ind]);
xb[ind]= (Irefbc[ind]-Iapfb[ind]);
xc[ind]= (Irefca[ind]-Iapfc[ind]);

ya[ind]=60000.0*(xa[ind]-xa[indmin1]);
yb[ind]=60000.0*(xb[ind]-xb[indmin1]);
yc[ind]=60000.0*(xc[ind]-xc[indmin1]);

idiffa[ind]=idiffa[indmin1]+h*(Kp*ya[ind]+Ki*xa[ind])+Kd*(ya[ind]-ya[indmin1]);
idiffb[ind]=idiffb[indmin1]+h*(Kp*yb[ind]+Ki*xb[ind])+Kd*(yb[ind]-yb[indmin1]);
idiffc[ind]=idiffc[indmin1]+h*(Kp*yc[ind]+Ki*xc[ind])+Kd*(yc[ind]-yc[indmin1]);
```

```
    if(idiffa[ind]>1.0)  { idiffa[ind]=1.0;      }
    if(idiffa[ind]<-1.0) { idiffa[ind]=-1.0;    }
    if(idiffb[ind]>1.0)  { idiffb[ind]=1.0;      }
    if(idiffb[ind]<-1.0) { idiffb[ind]=-1.0;    }
    if(idiffc[ind]>1.0)  { idiffc[ind]=1.0;      }
    if(idiffc[ind]<-1.0) { idiffc[ind]=-1.0;}

    //Update the PWM registers
    EPwm1Regs.CMPA.half.CMPA=3125.0*(1.0-idiffa[ind]);
    EPwm2Regs.CMPA.half.CMPA=3125.0*(1.0-idiffb[ind]);
    EPwm3Regs.CMPA.half.CMPA=3125.0*(1.0-idiffc[ind]);

    //Series DVR Control Code
    valpha = cal_V*(0.8164*Vab[ind]-0.4082*Vbc[ind]-0.4082*Vca[ind]);
    vbeta = cal_V*(0.7071*Vbc[ind]-0.7071*Vca[ind]);

    vd[ind] = valpha*costh[indmin1]+vbeta*sinth[indmin1];
    vq[ind] = vbeta*costh[indmin1]-valpha*sinth[indmin1];

    vc_alpha[ind]= ((vd[ind])*costh1[indmin1]-(vq[ind])*sinth1[indmin1])*0.57736;
    vc_beta[ind] = ((vd[ind])*sinth1[indmin1]+(vq[ind])*costh1[indmin1])*0.57736;
    Vsa[ind] = 0.8164*vc_alpha[ind]*vref;
    Vsb[ind] = (-0.4082*vc_alpha[ind]+0.7071*vc_beta[ind])*vref;
    Vsc[ind] = (-0.4082*vc_alpha[ind]-0.7071*vc_beta[ind])*vref;

    vdiffa[ind]= Kp1*(sinth1[ind]-Vsa[ind]);
    vdiffb[ind]= Kp1*(sinth2[ind]-Vsb[ind]);
    vdiffc[ind]= Kp1*(sinth3[ind]-Vsc[ind]);

    if(vdiffa[ind]>1.0)  { vdiffa[ind]=1.0;    }
    if(vdiffa[ind]<-1.0) { vdiffa[ind]=-1.0;    }
    if(vdiffb[ind]>1.0)  { vdiffb[ind]=1.0;       }
    if(vdiffb[ind]<-1.0) { vdiffb[ind]=-1.0;  }
    if(vdiffc[ind]>1.0)  { vdiffc[ind]=1.0;    }
    if(vdiffc[ind]<-1.0) { vdiffc[ind]=-1.0;   }

    //Update the PWM registers
    EPwm4Regs.CMPA.half.CMPA=6250.0*(1.0-vdiffa[ind]);
    EPwm5Regs.CMPA.half.CMPA=6250.0*(1.0-vdiffb[ind]);
    EPwm6Regs.CMPA.half.CMPA=6250.0*(1.0-vdiffc[ind]);

    if(ind==AdcBufLen)
    {
      ind=0;
    }
    else
    {
      ind++;
    }

    //Rewind the pointer to beginning
    //Reinitialize for next ADC sequence
    AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;  // Reset SEQ1
    AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1; // Clear INT SEQ1 bit
//  AdcRegs.ADCTRL2.bit.RST_SEQ2 = 1;   // Reset SEQ2
//  AdcRegs.ADCST.bit.INT_SEQ2_CLR = 1; // Clear INT SEQ2 bit
```

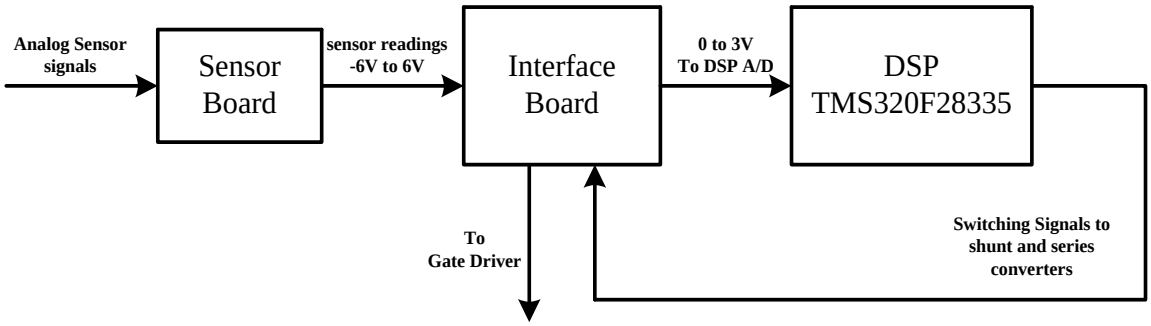
```
    PieCtrlRegs.PIEACK.all = 1;      // Acknowledge interrupt to PIE
    GpioDataRegs.GPBCLEAR.bit.GPIO49 = 1;
}
//===========================================================================
// End of SourceCode.
//===========================================================================
```

APPENDIX C

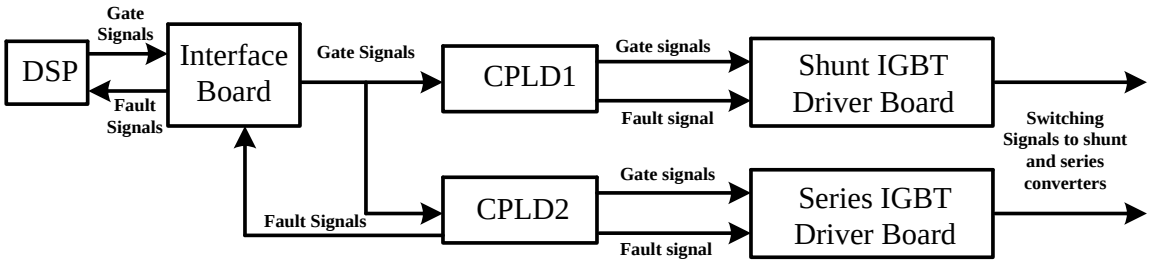
SCHEMATICS FOR PCB BOARD DESIGN

This appendix presents the PCB Design for all circuit boards for DSP-based data acquisition and PWM switching signal generation system. The various PCB schematics is given below:

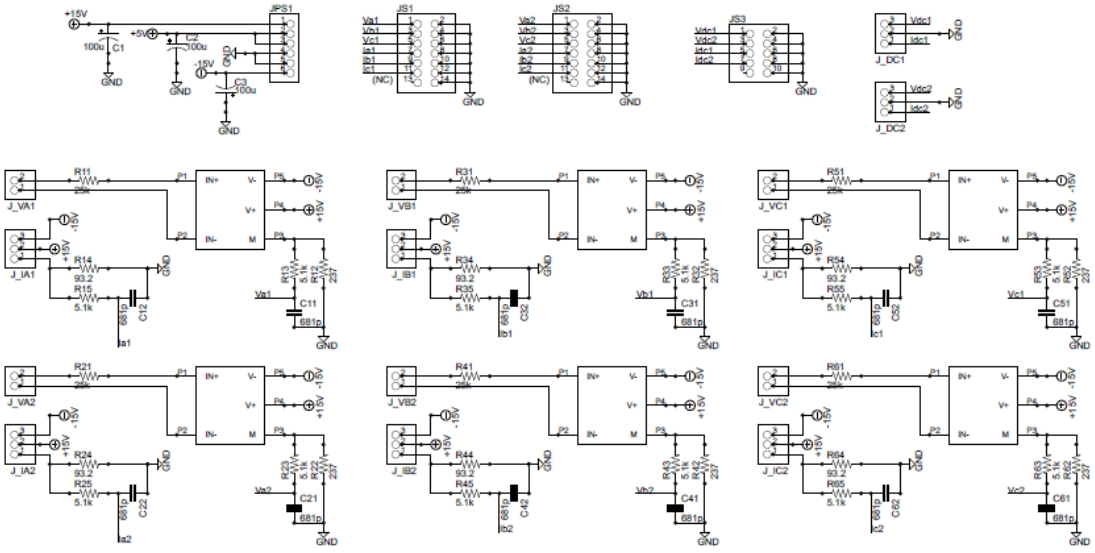
- The sensor board measures the various analog signals and converts them to a -6V to 6V range
- The interface board interfaces the sensed signals and converts them to a 0 to 3V range compatible with the DSP and sends to them DSP,
- Analog to digital (A/D) conversion and control algorithm implementation are carried out in the DSP (TMS320F28335). The control algorithm in the DSP to control the inverter using pulse-width modulation (PWM) technique is programmed using TI's Code Composer Studio (CCS) ver3.3.
- The inverter board has the IGBT module, its driver and the gate drive circuitry.



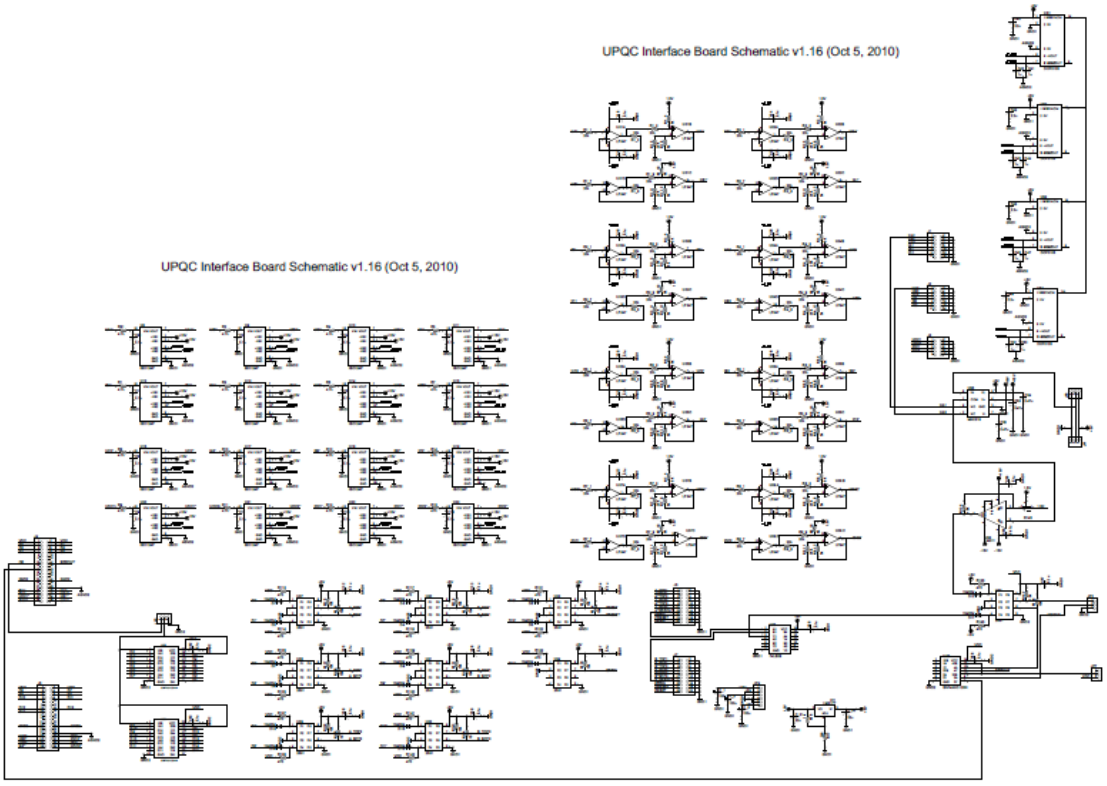
Block Diagram of the interaction between Sensor board, Interface board and DSP Board



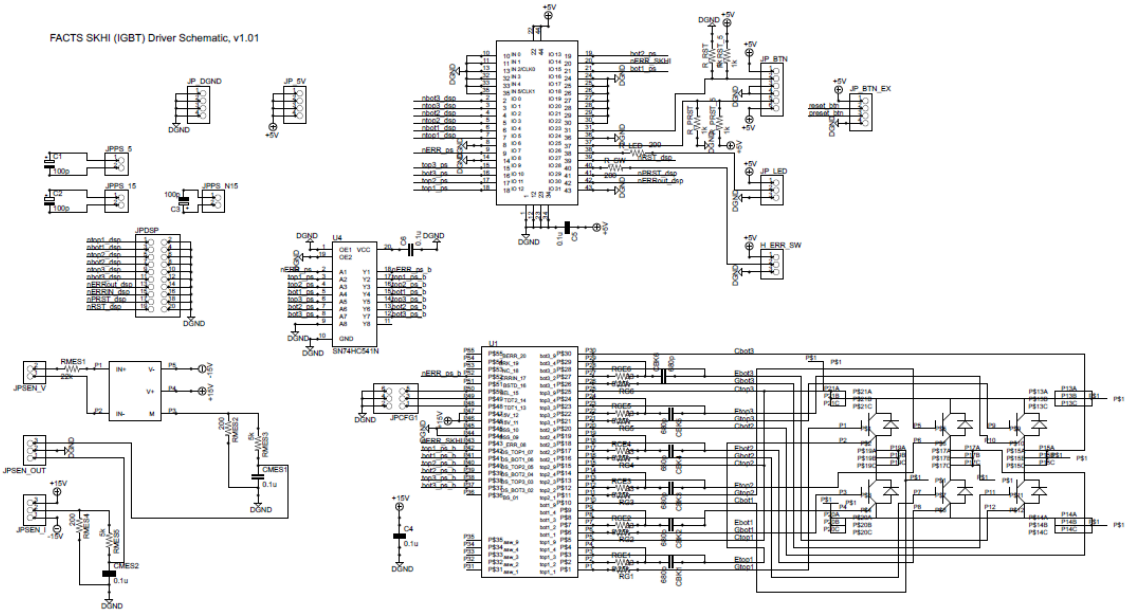
Block Diagram of interaction between Interface boards and the Inverter Boards



PCB Schematic of the Sensor Board



PCB Schematic of the Interface Board



PCB Schematic of the Gate Driver Board with IGBT Module

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VITA

Deepak Balaji Somayajula finished his schooling from his hometown Visakhapatnam, India. He graduated from Pondicherry University (India) with a BSEE degree in 2005. He worked as a Software Engineer at Infosys Technologies, India from 2005 to 2007. He started his MSEE degree at Missouri University of Science and Technology (Rolla) in August 2007 and graduated in December 2009. From September 2009 he worked towards his PhD degree and he graduated in May 2014. He has published papers in various conferences and his dissertation in various journals. He received the best paper award at the 2008 Vehicle Power and Propulsion Conference (VPPC) for the paper titled "Study on the effects of battery capacity on the performance of hybrid electric vehicles". He was a student member of IEEE, a member of IEEE Power Engineering Society and IEEE Industrial Electronics Society. His primary research interest is in modeling, analysis, design, control and hardware integration of various power electronic converters for renewable integration into the power system grid. He is also interested in the design of battery chargers for PHEVs. He worked as a summer intern at Delphi Electronics & Safety during the summer of 2012 where he was involved in the design and digital control of 3.3 kW Level 1 onboard battery chargers for PHEVs.