1972

Design and analysis of a phase-locked loop suitable for synchronization of an optical receiver

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Department:

DESIGN AND ANALYSIS OF A PHASE-LOCKED LOOP SUITABLE FOR SYNCHRONIZATION OF AN OPTICAL RECEIVER

BY

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A THESIS

Presented to the Faculty of the Graduate School of the

UNIVERSITY OF MISSOURI-ROLLA

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

1972

Approved by

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ABSTRACT

The required synchronization of a dynamic crossed-field photomultiplier tube (DCFP) is accomplished by means of a phase-locked loop for which the salient feature is the use of the DCFP as the phase detector. This action is necessitated due to the unique sampling and phase focusing type of operation of the DCFP. The phase-locked loop is implemented by dithering the phase of the synchronizing RF drive signal, bandpass filtering the output pulses of the DCFP and using a synchronous detector at the dither frequency to determine the phase relationship between the incoming mode-locked laser pulses and the RF drive signal. The error signal thus generated is filtered and used to drive the VCO which controls the RF drive phase for the DCFP.

ACKNOWLEDGEMENT

The hardware fabrication and experimental testing of the optical receiver was conducted at McDonnell Douglas Astronautics Company, Eastern Division. The work on this thesis was performed in conjunction with work on Air Force Contract Number F33615-71-C-1472. The author wishes to express his gratitude to the management of department E413 at McDonnell for allowing this thesis in conjunction with the contract work. Also the author wishes to express his thanks to the other members of department E413 who helped in the design, fabrication, and testing of the optical receiver.

The author wishes to express his appreciation and gratitude to his advisor, Dr. John A. Newell for his advice and encouragement throughout this investigation.

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I. INTRODUCTION

In search for a method to transfer a large amount of information at potentially low cost, optical communications have come into importance. The advantages of optical communications over microwave communications are several fold. The carrier frequencies for optical communications are in the neighborhood of 10^{14} Hertz allowing the optical carrier to be modulated at microwave frequencies producing gigahertz bandwidths. The normal transmitter in an optical communication system is a laser. The beamwidth of the typical laser is small when compared to that of a microwave antenna. Consequently the radiated power is more highly concentrated (equivalent to a large antenna gain) allowing for a reduction in the amount of transmitted signal power required. Optical communications are essentially line-of-sight and as such offer additional advantages over microwave communications, two of which are privacy and resistance to jamming. Also optical communications do not suffer a prolonged black out in a nuclear environment.

Another highly important advantage of optical communication which is often overlooked is the potentially small terminal sizes (due to smaller antennas and smaller associated equipment). This facilitates very efficient and

effective satellite to satellite communications.

One form of optical communications uses pulse code modulation (PCM), a simple form of which is binary coding. A variation of this coding technique is to use pulse gated binary modulation (PGBM) which is generated by gating out pulses from a periodic pulse train but still leaving the basic regular repetition rate for the transmitted optical pulses. The transmitted PGBM signal results in a pulse for every "one" in the binary code and no pulse for every "zero" in the code. The binary modulation (PGBM) can be accomplished by using an electro-optic modulator to gate the optical pulses produced by a mode-locked laser. An example depicting the generation of a PGBM signal is shown in Figure 1.

An optical receiver is used to detect the transmitted signal. Because the transmitted binary information has a basic regular repetition rate, the inherent low duty cycle of the laser transmitter allows a gated receiver to be employed to discriminate against background noise. This receiver requires synchronization of the gate with the transmitted pulse repetition rate. Such an optical gated receiver exists and is known as a dynamic crossed-field photomultiplier (DCFP)[1,2]. The purpose of this paper is to develop a method of generating the synchronizing signals required for proper operation of this receiver.

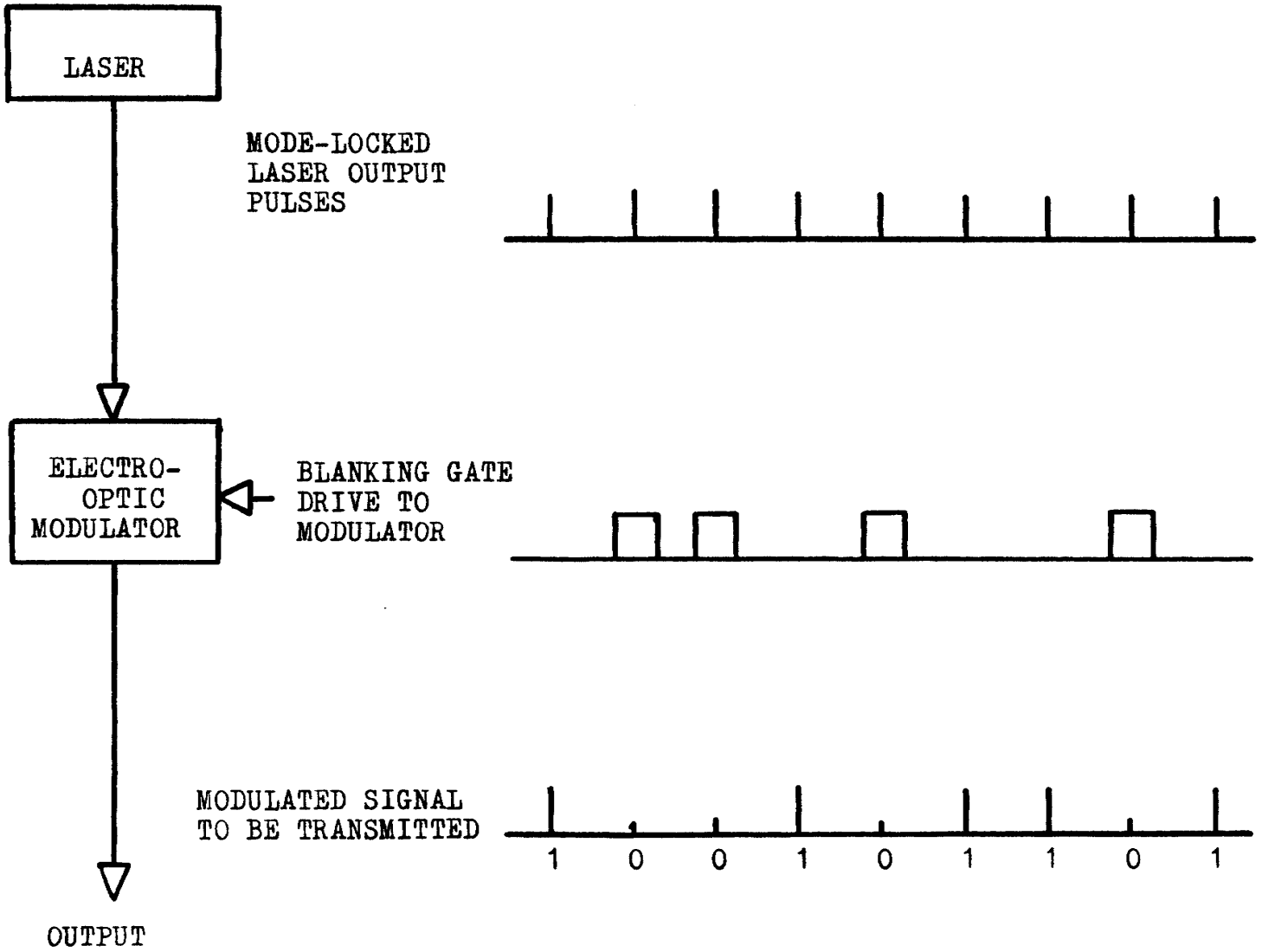


Figure 1. Optical transmitter generating a PGBM signal.

II. LITERATURE SEARCH

The purpose of this section will be to acquaint the reader with the theory of operation of the basic components of an optical communication system. These are the laser and the modulator which comprise the transmitter, and the DCFP along with the synchronization hardware which constitute the receiver. Also a basic theory of operation of phase-locked loops will be presented.

A. The Laser

The optical communication system being considered is a binary one in which the information to be transmitted is encoded and the coded information is then transmitted. The transmitter consists of a laser to generate the signal and a modulator which codes the generated signal. The laser which is used is mode-locked meaning it is essentially forced to oscillate producing a pulse train of light as its output.

The laser is essentially a cavity oscillator. The length of the cavity is determined by the placement of highly reflective end mirrors. A laser rod is inserted into the cavity to provide the source of energy or the gain medium for the oscillator. Optical regenerative gain occurs for light traveling along the cavity axis.

A YAG laser is presently being used in conjunction with the optical receiver. The laser rod is made of Nd^{3+} doped $Y_3Al_5O_{12}$ or Nd : YAlG (neodymium doped yttrium aluminum garnet) and abbreviated YAG. The laser rod is excited or pumped optically by being placed in an elliptical cavity at one focus with a tungsten or krypton pump lamp at the other focus. The laser rod absorbs energy from the pump lamp at specific wavelengths (principally 750 and 810 nanometers). A YAG laser is described by a four energy level system. Electrons are pumped from the lowest to the highest energy level by absorption of energy from the pump lamp. As the electrons pass through the energy levels photons of 1060 nanometer wavelength are emitted and the rod is heated.

The laser can operate in several axial and transverse modes at the same time. Placing an aperature in the optical cavity restricts the operation to the lowest order or TEM_{oo} mode. The axial modes are harmonically related, the basic frequency being determined by the time required for light to travel a round trip between the end mirrors of the optical cavity. The basic frequency for the laser used with the present optical receiver is 300 MHz with the other axial modes occurring at 600 MHz, 900 MHz, 1200 MHz etc.

For a single transverse mode these axial modes can be locked together by insertion of an intracavity loss modulator or phase modulator driven at the fundamental axial

mode frequency (300 MHz). This shutter effect or cyclic gain variation couples the axial modes in an AM manner. If a large number of the axial modes are locked together, the laser will output an optical pulse train with a period

$$T = \frac{2d}{c}$$

where

T = the output pulse period

d = the mirror spacing in the optical cavity

c = the speed of light

and with a pulse width

$$\tau = \frac{T}{N}$$

where

τ = the half amplified optical pulse width

N = the number of locked modes.

and a peak power N times the average power. A 300 MHz laser with 10 locked modes would output 333 picosecond pulses. The number of modes may be increased by keeping the cavity losses to a minimum enabling the cavity to have a wider bandwidth.

The optical receiver is presently being designed to operate at either the 1060 nanometer output of the YAG laser or the 530 nanometer doubled frequency output. The doubling process is implemented by incorporating into the

optical cavity a nonlinear crystal which can be phase matched for second-harmonic generation. The two frequency operation of the receiver is obtained by using two DCFP's with different photocathode materials optimized for the respective wavelengths. This approach is being pursued since the photocathode quantum efficiency for 1060 nanometers is very poor.

The output signal is obtained by making one of the highly reflective end mirrors in the optical cavity partially ($\approx$1%) transmitting. This output signal is also treated as one of the cavity losses. A block diagram of the laser is shown in Figure 2.

B. The Modulator

A modulator is used to impress the desired information to be transmitted upon the output of the laser. The modulation is accomplished by using a crystalline substance which exhibits some electrooptic effect (birefringence). One method of achieving modulation is to pass the laser output through a polarizer and then vary the direction of polarization of the modulating crystal as a function of an applied voltage. Typically the crystal is followed by an analyzer (a second polarizer) which transmits in a unipolar fashion as indicated in Figure 3. This form of an electrooptic modulator makes use of a Pockel cell.[3]

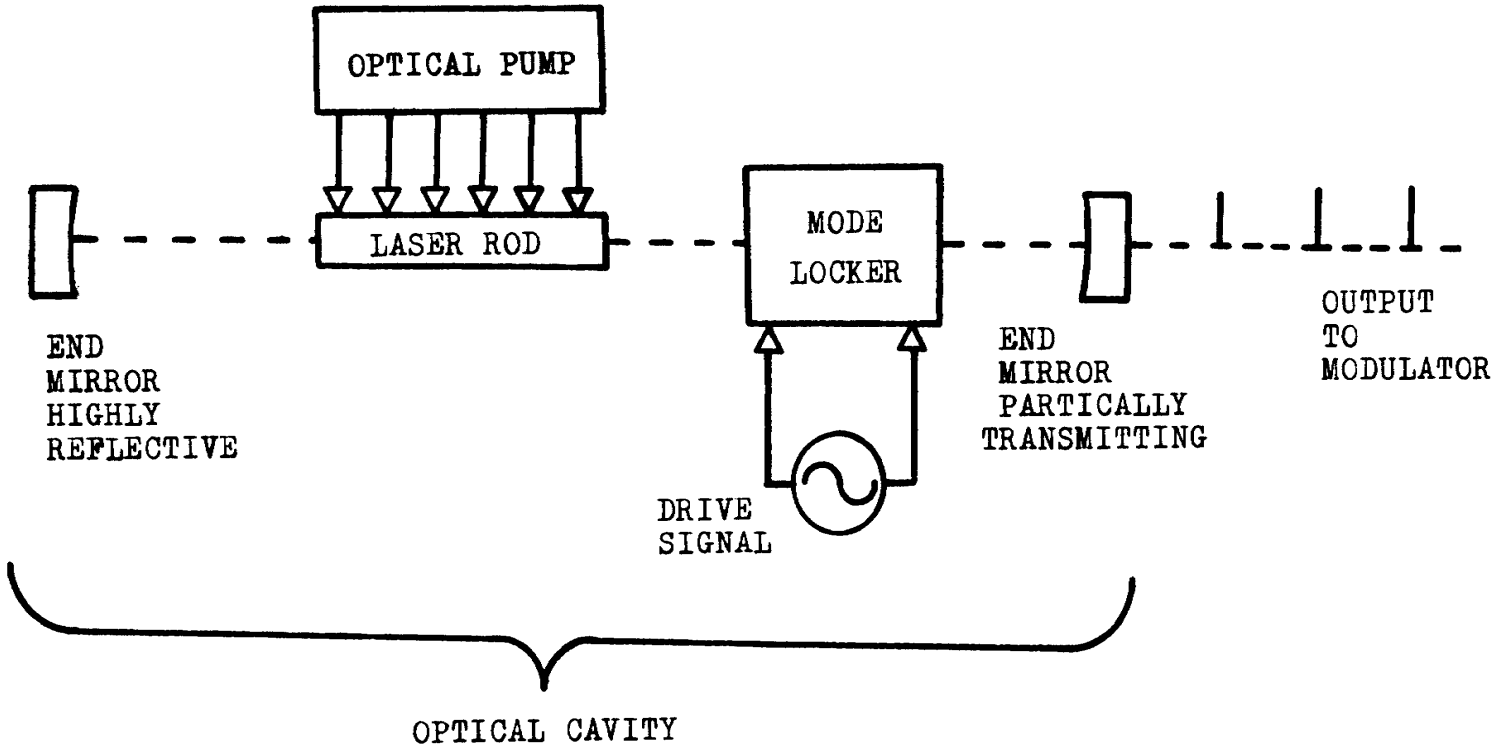


Figure 2. Block diagram of the laser.

C. Theory of Operation of the DCFP

The photodetector which will be used in the optical receiver is a dynamic crossed-field photomultiplier (DCFP). This device operates by the principle of direct photodetection, essentially photon counting. This type of detection responds to the amplitude variations of the incident power and is insensitive to any phase or frequency modulation of the optical carrier.[4]

The DCFP is constructed using two parallel plane electrodes one of which contains a photocathode, a good secondary emitting surface, a collector aperature or anode, and is divided (electrically) into two parts forming a split dynode. A schematic configuration for the DCFP is shown in Figure 4. Crossed magnetic and electric fields exist between the electrodes. The magnetic field is a steady spatially uniform field located between the electrodes and pointing in the negative z direction. The crossed electric field consists of both a static and a dynamic component both parallel to the y axis. The time varying portion of the electric field is spatially uniform between the electrodes while the static component consists of two discrete values being separated where the dynode is split and both directed in the negative y direction.

A stream of photons passing through an aperature in the upper electrode and incident upon the photocathode will cause electrons to be injected into the region between the two electrodes. If the instantaneous value of

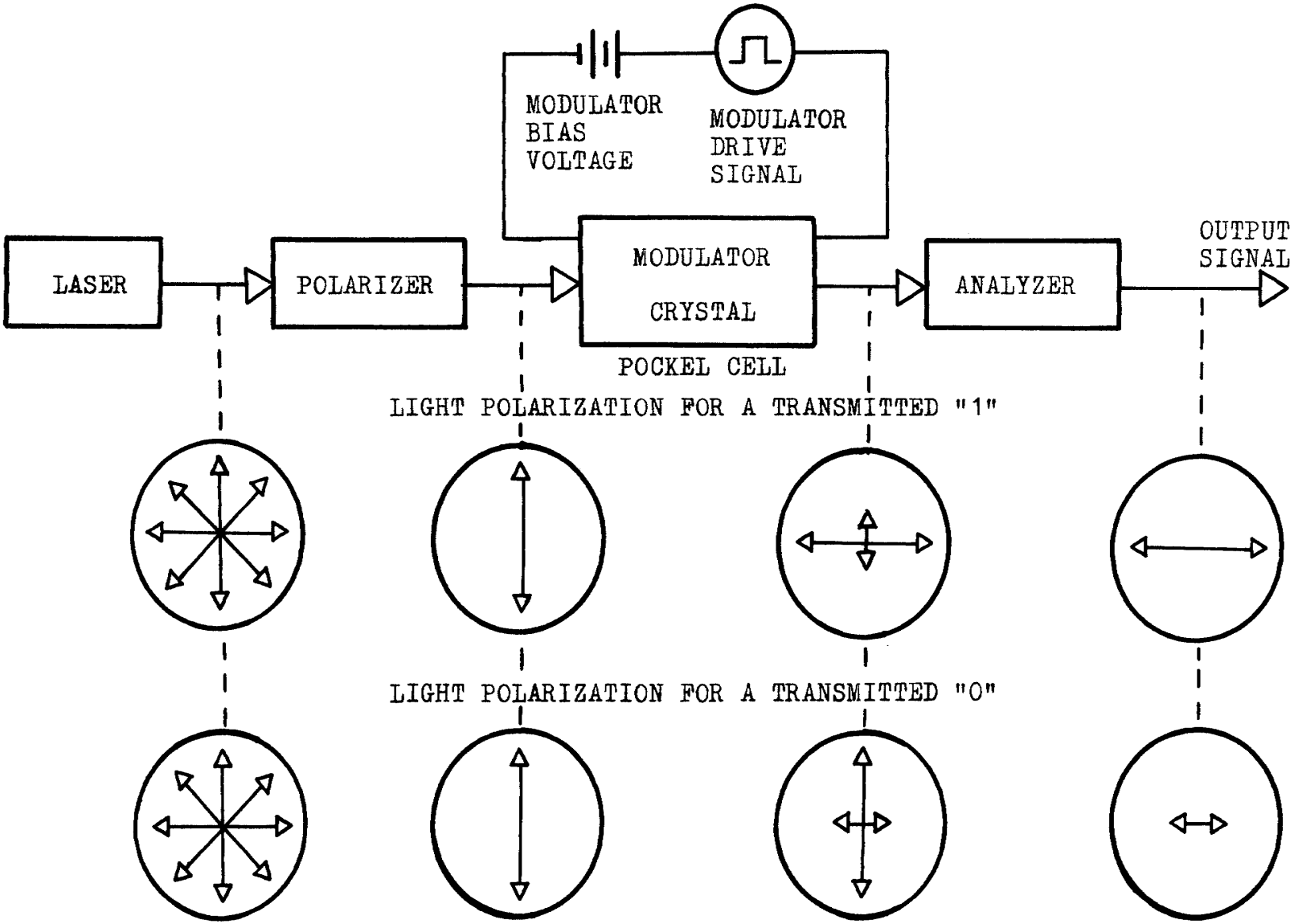


Figure 3. Electrooptic modulator.

the electric field is such that the upper electrode is positive with respect to the photocathode, then the electrons are accelerated towards the upper electrode by the electric field. As the electrons gain velocity the magnetic field will cause their path to curve in a clockwise manner and if the intensity magnitude of the field is sufficient, the direction of the electrons is reversed. The combined influence of the electric and magnetic fields force the electrons to follow a cycloidal path translating some step size along the positive x axis with each cycle of the dynamic electric field. As the electrons return to the dynode, part of their kinetic energy is lost in overcoming the electric field.

The gain in kinetic energy of the electrons during each step is proportional to the differences between the electric field intensities at the times of departure and arrival at the secondary emitting surface. If no dynamic electric field were present, the net gain in kinetic energy would be 0. The initial energy of the photoelectrons and the secondary emission electrons is too low to produce a secondary emission ratio greater than 1, thus without increasing the electron energy the DCFP would not exhibit any gain.[5]

If an electron has gained sufficient kinetic energy from the electric field, it produces δ secondary electrons as it strikes the secondary emitting surface on the lower electrode. These secondary electrons are generated when

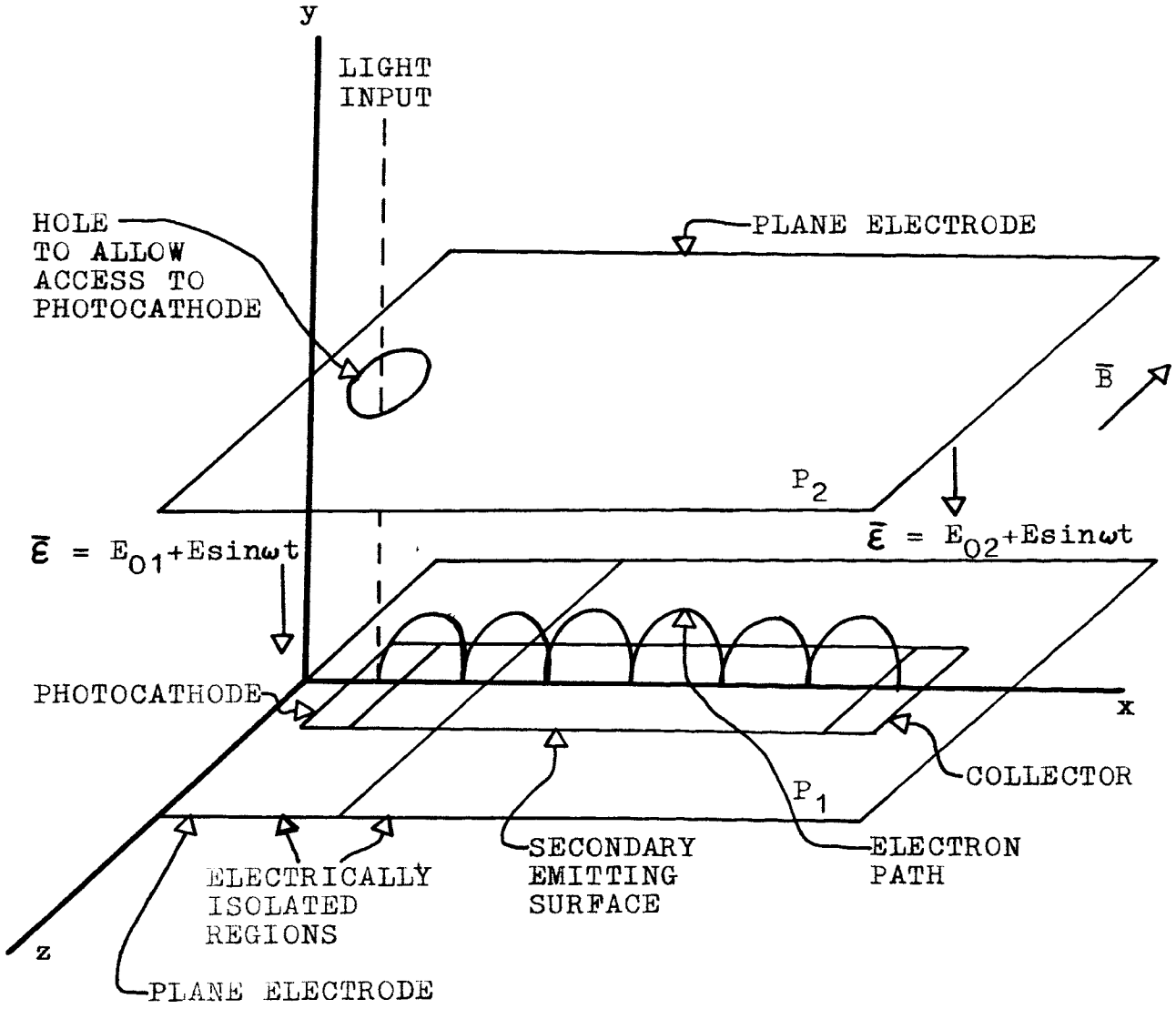


Figure 4. Schematic representation of the DCFP.

the dynamic electric field is reversing direction and are accelerated towards the upper electrode following a path similar to the first electrons, again moving further along the positive x axis. After a number, n, of such steps, the electrons arrive at the collector and produce the output pulse of the DCFP.[5] The gain of the tube, G, is proportional to δ and to the number of steps n being,

$$G = \delta^{(n-1)}$$

the last step at the collector not contributing to the gain because no secondary electrons are produced.

The sampling or gating action of the DCFP arises from the requirement for the electric field intensity to be larger at the time of electron departure than at the time of arrival to enable the tube to exhibit gain. The sampling interval is primarily a function of the ratio of the static to the dynamic electric field intensity with changes of the magnetic field intensity producing only a small variation. This sampling interval is found to vary from 10 percent to 70 percent of the period of the dynamic electric field.[6]

Both the number of multiplication steps n and the secondary emission factor δ are functions of the static and dynamic values of the electric field intensity as well as the magnetic field intensity. As each of these is varied independently, the gain exhibits some peak value. The place of occurrence of this maximum is a function of the values of the two parameters being held constant.

Thus the resultant gain of the DCFP is determined by the value of all three parameters.[5]

The gain mechanism of the DCFP causes phase focusing of the signal being amplified. The influence of the electric field upon the electrons depends upon the phase of the electric field which exists when the electron first enters the region between the electrodes. An electron that enters this region just as the electric field intensity starts increasing in the direction to accelerate the electron away from the lower electrode is overtaken by an electron which leaves at a later phase of the dynamic electric field because this second electron sees a larger initial accelerating potential. This effect causes a bunching of the time of arrival of the electrons. After several steps a definite phase focusing has occurred.[5]

The operation of the DCFP can be summarized as follows. The input signal is sampled over some portion of the dynamic electric field period. This sample is then amplified by means of secondary emission electron multiplication. During this amplification process the signal is phase focused producing an intensely sharp output pulse which occurs synchronously with the dynamic electric field.[2]

Independent optimization of the DCFP sampling function and gain is obtained by means of the split dynode.[7] This allows the static electric field intensity to assume two independent values, one in the region of the first few

steps to control the sampling and the second in the remainder of the amplification region to control the gain.

The DCFP uses a strip dynode and depends on the crossed fields to control the steps size (the number of steps). The dynamic portion of the electric field intensity rigidly controls the electron transit time (one step occurring for each cycle).[5] Present technology electrostatic secondary emission photomultipliers suffer a decrease in gain with increasing frequency due to the spread in transit time of individual electrons from electrode to electrode.[3] The rigid control of this electron transit time from step to step in the DCFP prevents a decreasing gain with increasing frequency. Thus the DCFP is found to be a superior receiver for microwave modulated light.

The optical receiver is designed to operate with an input optical pulse train and at least one gate must be generated for each expected received signal pulse or part of the transmitted information will be gated out by the receiver. The repetition rate of the optical pulse train and the DCFP dynamic electric field or RF drive frequency must be harmonically related, meaning, the RF drive frequency must be equal to, or a harmonic of, the optical pulse train repetition rate. A phase displacement between the dynamic electric field and the incident optical pulse train will cause an amplitude decrease in the DCFP output pulses because part of the received signal will be gated out. In fact a frequency difference between the RF drive

and the optical pulse train will cause the DCFP output pulses to be amplitude modulated at the difference frequency. The percentage modulation is determined by the incident optical pulse width and the DCFP gate width or sampling interval. The average value of the DCFP output pulses is a periodic function, the period of which is equal to the difference frequency of the RF drive and the optical pulse train. This periodic function has been shown to be a result of the convolution of the optical pulse and the DCFP sampling function.[5,6] Using a narrow laser pulse and knowing its shape allows one to infer the nature of the DCFP sampling function by observing the shape of the convolved signals.

D. Theory of Phase-Locked Loops

A feedback automatic-phase-control system is generally referred to as a phase-locked loop. In its simplest form a phase-locked loop consists of three major components, a voltage controlled oscillator (VCO), a phase detector (PD), and a filter (F(s)). The method of interconnection of these devices is shown in Figure 5a. The general use of a phase-locked loop is to synchronize the frequency and phase of two oscillators. This synchronization process fills many needs. A less noisy version of an input signal can be reproduced by synchronization of a local oscillator. The frequency stability of a generator can be improved by phase locking it to a stable source. A phase-locked loop can be

used to demodulate a frequency or phase modulated input signal.

The VCO is essentially a free running oscillator, the frequency of which can be shifted by means of a control voltage. A typical VCO responds as shown in Figure 5b. The free running frequency or the center frequency (f_c) of the VCO is its output frequency for zero control voltage. In the VCO characteristic shown in Figure 5b the VCO is linear, that is, the slope of the VCO output frequency versus the control voltage is a constant.

The phase detector (PD) is a circuit which generates a voltage proportional to the phase difference between two input signals. A linear phase detector characteristic is shown in Figure 5c. Several other types of phase detector characteristics exist, the most common and most analyzed being the sinusoidal characteristic which is shown in Figure 6a. This type of phase detector characteristic can be generated by simply low pass filtering the output of an analog multiplier. Assume the two input signals to the analog multiplier are $\sin(\omega_1 t)$ and $\cos(\omega_2 t-\phi)$.

Then

$$\sin(\omega_1 t)\cos(\omega_2 t-\phi) = \tfrac{1}{2}\sin([\omega_1-\omega_2]t+\phi)+\tfrac{1}{2}\sin([\omega_1+\omega_2]t+\phi)$$

Now if the input frequencies are the same such that

$$\omega_1 = \omega_2$$

then

$$\sin(\omega_1 t)\cos(\omega_1 t-\phi) = \tfrac{1}{2}\sin(2\omega_1 t+\phi)+\tfrac{1}{2}\sin\phi$$

If a low pass filter is added such that the second harmonic

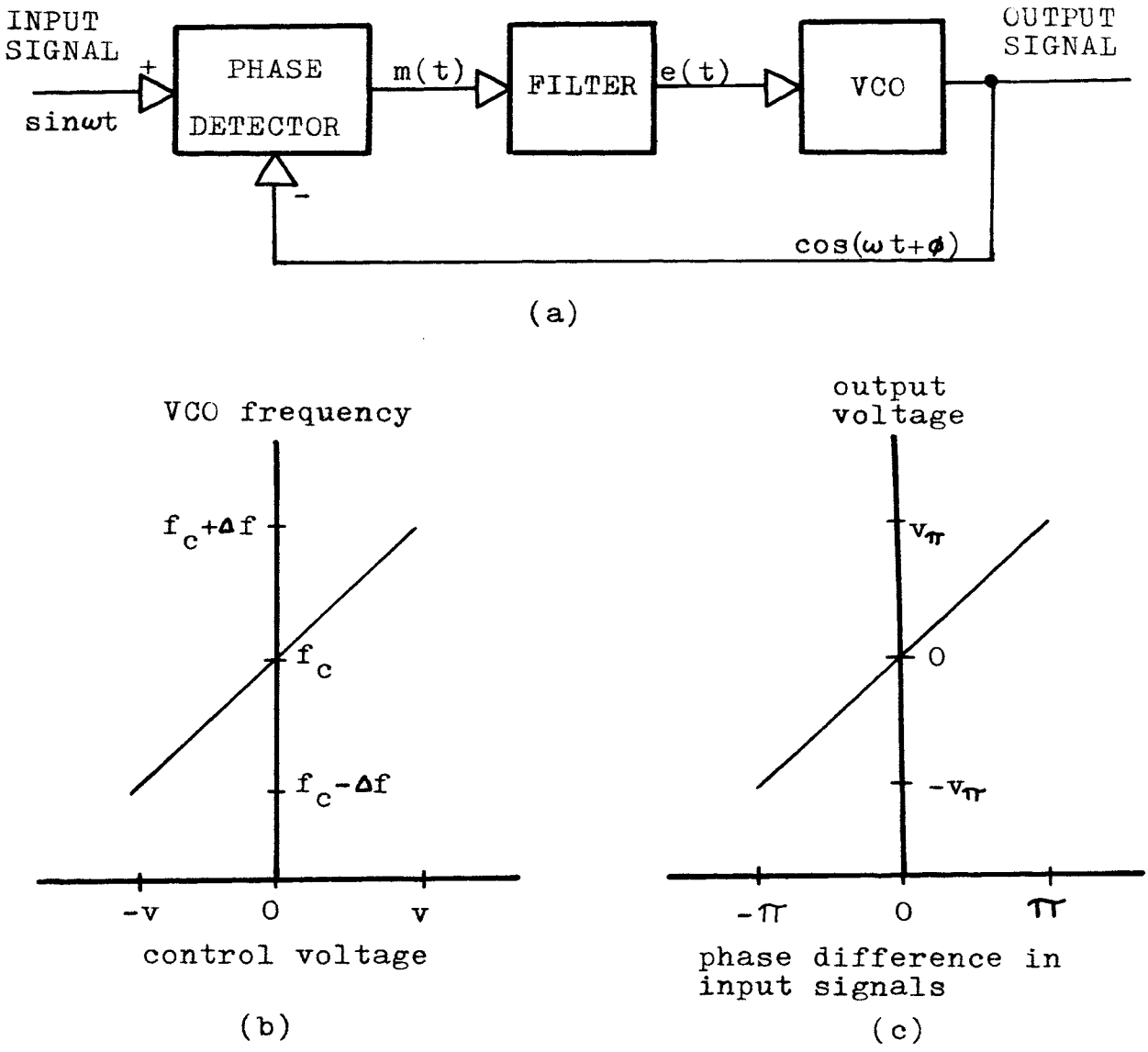


Figure 5. Basic phase-locked loop.(a) Block diagram. (b) VCO characteristic. (c) Phase detector characteristic.

component is filtered out the result is

$$\sin(\omega_1 t)\cos(\omega_1 t - \phi) = \tfrac{1}{2}\sin\phi$$

A sinusoidal phase detector characteristic is thus generated. Other types of phase detectors will generate other characteristics two of which are shown in Figures 6b (triangular) and 6c (sawtooth).

In addition to adding a low pass filter to the phase-locked loop to filter out the second harmonic signal generated in the sinusoidal phase detector, improvements can be made in the loop transient and steady state response by means of a loop filter. Inclusion of a loop filter changes the phase-locked loop from a first order system, to a second order system. A second order phase-locked loop allows improved performance because additional loop parameters may be independently specified thus allowing for a more nearly optimal solution. Specification of three parameters will in general determine the phase-locked loop performance. These parameters are loop bandwidth, ω_n, loop gain, K, and the loop damping ratio, ζ .

1. Linear Model for the Phase-Locked Loop

A linear model for the phase-locked loop may be developed using phase as the control variable. It is assumed that the input and output frequencies are the same, the system is frequency locked, and that the relative input output phases are approximately the same, the system is near phase lock.

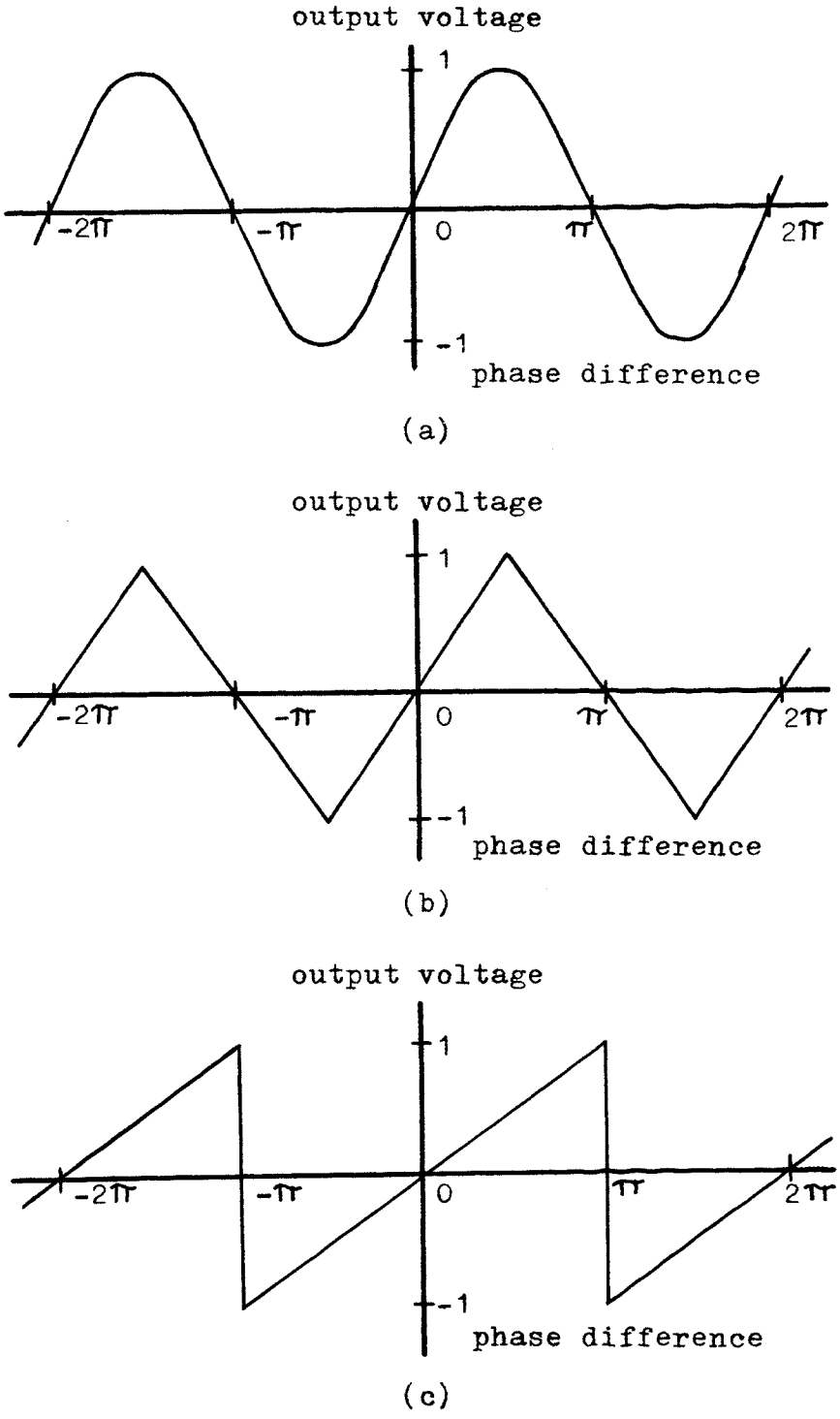


Figure 6. Phase detector characteristics. (a) Sinusoidal. (b) Triangular. (c) Sawtooth.

The phase detector operation may be described as follows

$$V_d = K_d \sin (\theta_i - \theta_o)$$

where

V_d = the phase detector output voltage

K_d = the phase detector gain in volts/radian

θ_i = the loop input phase

θ_o = the VCO output phase

Since the loop is near phase-lock the phase error, $\theta_i - \theta_o$, is small and sin $(\theta_i - \theta_o)$ may be replaced by $\theta_i - \theta_o$. Using this approximation and taking the Laplace transform

$$V_d(s) = K_d(\theta_i(s) - \theta_o(s)).$$

The output signal of the phase detector is filtered by the loop filter before being applied to the VCO. In Laplace notation

$$V_2(s) = F(s)V_d(s)$$

where

$V_2(s)$ = the VCO control voltage

$F(s)$ = the loop filter transfer function

$V_d(s)$ = the output phase detector voltage.

Deviation of the VCO from its center frequency may be expressed as

$$\Delta\omega = K_o V_2$$

where

$\Delta\omega$ = the VCO frequency deviation about its center frequency

K_o = the VCO gain constant in radians per second per volt.

V_2 = the VCO control voltage

Because frequency is the derivative of phase, the operation of the VCO may be further described as follows

$$\Delta\omega = \frac{d\,\theta_o(t)}{dt}$$

$$\Delta\omega = \frac{d\,\theta_o(t)}{dt} = K_o V_2$$

Taking Laplace transforms results in

$$\mathcal{L}\left[\frac{d\,\theta_o(t)}{dt}\right] = s\,\theta_o(s) = K_o V_2(s)$$

or

$$\theta_o(s) = \frac{K_o V_2(s)}{s}$$

Since the factor 1/s represents the transform of an integrator, the phase of the VCO output will be proportional to the integral of the input control voltage.

A block diagram illustrating the linear model of the phase-locked loop is shown in Figure 7a. The closed loop feedback control system shown in Figure 7b is governed by the following equation,

$$\frac{C(s)}{R(s)} = \frac{G(s)}{1+G(s)H(s)}$$

Using the above relationship, the transfer functions which express the operation of the phase-locked loop components may be combined to give the loop equations which predict

the closed loop performance.

$$C(s) = \theta_o(s)$$

$$R(s) = \theta_i(s)$$

$$G(s) = K_d F(s)\frac{K_o}{s}$$

$$H(s) = 1$$

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_d F(s)\frac{K_o}{s}}{1+K_d F(s)\frac{K_o}{s}}$$

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_d K_o F(s)}{s+K_d K_o F(s)}$$

Now specification of the loop filter will determine the closed loop response.

2. Loop Filter

a. First Order Phase-Locked Loop

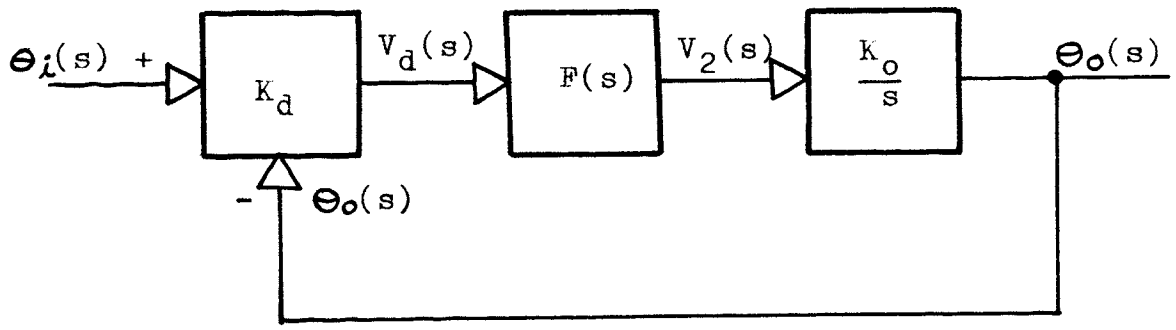
If no loop filter is used, that is,

$$F(s) = 1$$

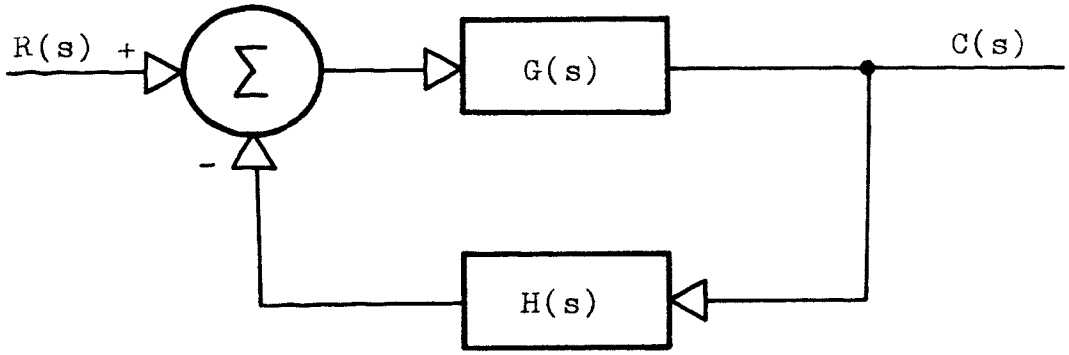
then the closed loop response may be expressed as follows

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d}{s+K_o K_d}$$

The above equation is representative of a first order system.



(a)



(b)

Figure 7. Control system block diagrams. (a) Linear model of the phase-locked loop. (b) General model of a feedback control system.

b. Second Order Phase-Locked Loop

For the second order system the characteristic equation of the closed loop response can be written as follows

$$s^2+2\zeta\omega_n s+\omega_n^2$$

where

ω_n = the loop natural frequency

ζ = the damping ratio

The parameters ω_n and ζ are used in control system design and analysis to characterize performance.

i. Low Pass Filter

If the loop filter is a low pass filter where

$$F(s) = \frac{1}{s\tau+1}$$

then

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d/\tau}{s^2+s/\tau+K_o K_d/\tau}$$

and

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{K_o K_d \tau}}$$

ii. Passive Lead-Lag Filter

If a passive lead-lag type of filter is used where

$$F(s) = \frac{s\tau_2+1}{s(\tau_1+\tau_2)+1}$$

then

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{K_oK_d}{\tau_1+\tau_2}\left(s\tau_2+1\right)}{s^2+\frac{1+K_oK_d\tau_2}{\tau_1+\tau_2}s+\frac{K_oK_d}{\tau_1+\tau_2}}$$

and

$$\omega_n = \sqrt{\frac{K_oK_d}{\tau_1+\tau_2}}$$

$$\zeta = \tfrac{1}{2}\left(\tau_2+\frac{1}{K_oK_d}\right)\sqrt{\frac{K_oK_d}{\tau_1+\tau_2}}$$

iii. Active Lead-Lag Filter

If a high gain operational amplifier is used to synthesize the loop filter the transfer function is

$$F(s) = F(0)\frac{s\tau_2+1}{s\tau_1+1}$$

where

F(0) = the open loop amplifier gain

then

$$\frac{\Theta_o(s)}{\Theta_i(s)} = \frac{\frac{K_o K_d F(0)}{\tau_1}\left(s\tau_2+1\right)}{s^2+\left[(1+K_o K_d F(0)\tau_2)/\tau_1\right]s+K_o K_d F(0)/\tau_1}$$

or for $1 \ll K_o K_d$

$$\frac{\Theta_o(s)}{\Theta_i(s)} = \frac{\frac{K_o K_d F(0)}{\tau_1}\ s\tau_2+1}{s^2+(K_o K_d F(0)\tau_2/\tau_1)s+K_o K_d F(0)/\tau_1}$$

and

$$\omega_n = \sqrt{K_o K_d F(0)/\tau_1}$$

$$\zeta = \tfrac{1}{2}\tau_2\sqrt{K_o K_d F(0)/\tau_1}$$

Note that for F(0) = 1, the passive and the active lead lag filters and loop responses are equivalent. Also by picking a value for F(0), any value of DC gain for the filter may be obtained.

The preceding material on phase-locked loop theory assumed the loop was locked and that the phase error was small, allowing use of the linear model. This assumption is now discarded as the large signal phase error and acquisition performance of the loop are considered.

3. Static Phase Error

When the phase-locked loop is locked and tracking the input signal, a phase offset generally exists between the input and output signals. This phase offset is a static

phase error and its magnitude is found as follows

$$\sin \theta_e = \frac{\omega_i - \omega_c}{K} = \frac{\Delta\omega}{K}$$

where

θ_e = the static phase error

ω_i = the input frequency

ω_c = the VCO center frequency

K = the open loop DC gain

$K = K_o K_d F(0)$

$\Delta\omega = \omega_i - \omega_c$

If θ_e is small then the static phase error is approximated as follows

$$\theta_e \simeq \sin \theta_e \qquad \theta_e \ll 1$$

then

$$\theta_e = \frac{\Delta\omega}{K}$$

4. Dynamic Tracking Error

A second order phase-locked loop can track a frequency ramp input only if the DC loop gain is infinite. For the high but finite gain case the loop can track the frequency ramp for a while but the magnitude of the dynamic error keeps increasing until the loop loses lock. The input signal to the loop could contain a frequency ramp due to the change of the Doppler frequency caused by the overhead pass of a satellite.

The dynamic phase error for the infinite gain second order loop is

$$\sin \theta_e = \frac{\Delta \dot{\omega}}{\omega_n^2}$$

where

$$\Delta \dot{\omega} = \frac{d\Delta\omega}{dt} = \frac{d(\omega_i - \omega_c)}{dt}$$

Assume the phase detector limits the loop dynamic range and no other loop components saturate. The maximum value of sin θ_e is 1 thus the maximum permissible input signal sweep rate is

$$\Delta \dot{\omega} = \omega_n^2$$

Therefore for the high gain second order loop to track the input signal

$$\Delta \dot{\omega} < \omega_n^2$$

and the loop will eventually lose lock as the phase error accumulates (at a rate dictated by $\Delta \dot{\omega}$ and ω_n^2).

5. Hold in Range

Once a phase-locked loop has achieved phase lock, the input frequency may be slowly varied and the loop will track the variation. The permissible range over which the input frequency may be varied and still not lose phase lock is called the hold-in range. The magnitude of the hold-in range is determined by the maximum error signal which can be generated with one of two items determining this maximum. Either some element in the phase-locked loop saturates, or

the permissible value of the static phase error is exceeded. In the first case lock is lost and the loop proceeds to slip cycles generating a beat note (the input and VCO difference frequency) for the error signal. In the second case lock is not lost, but the loop no longer performs satisfactorily and the design specifications may not be met.

Thus

$$\omega_H = K \sin(\theta_e)$$

where

ω_H = the hold in range (about the VCO center frequency)

K = the loop DC gain

θ_e = the permissible value of the static error.

If the phase detector is allowed to saturate, that is, $\sin \theta_e = 1$ then the hold in range is

$$\omega_H = \pm K$$

and the maximum hold in range is equal to the DC loop gain. Thus the phase-locked loop hold-in range can be made arbitrarily large simply by increasing the loop gain.

6. Lock in Range

The lock in range of a phase-locked loop is defined as the input frequency range over which phase-lock is achieved without cycle slipping (the phase error does not exceed 2π).

The lock in range is a function of the loop filter but in all cases is proportional to the loop bandwidth. It can be shown that for the first order loop where F(s) = 1, the lock in range is found to be

$$\omega_L = K$$

or the lock in range (ω_L) is equal to the DC loop gain (K).

For the second order phase-locked loop where the loop filter is a low pass giving

$$F(s) = \frac{1}{s\tau+1}$$

the lock in range is

$$\omega_L = \omega_n$$

or the lock in range is equal to the loop bandwidth.

When a lead-lag filter is used with

$$F(s) = \frac{s\tau_2+1}{s(\tau_1+\tau_2)+1} \quad \text{passive filter}$$

or

$$F(s) = F(0)\frac{s\tau_2+1}{s\tau_1+1} \quad \text{active filter}$$

the lock in frequency is

$$\omega_L = \frac{K_o K_d}{\tau_1+\tau_2} \quad \text{passive filter}$$

or

$$\omega_L = \frac{K_o K_d \tau_2}{\tau_1} \quad \text{active filter}$$

which is equal to the high frequency loop gain giving

$$\omega_L = 2\zeta\omega_n \quad (1 \ll K_o K_d \tau_2)$$

7. Pull in Range

The pull in range of a phase-locked loop is defined as the input frequency range over which phase lock will be eventually achieved although the loop may slip cycles before lock is acquired.

For the phase-locked loop without a loop filter, that is, a first order loop where,

$$F(s) = 1$$

the pull in range is equal to the lock in range.

$$\omega_P = K$$

The pull in range (ω_P) is equal to the DC loop gain (K).

For the second order phase-locked loop the pull in process is highly non linear. When the frequency difference is equal to the lock in range, then lock up will occur without further cycle slipping.

Suppose the phase-locked loop is broken at the input to the VCO so that the open loop characteristics can be observed. The error signal will be a beat note which is the difference frequency between the free running VCO and the input signal. The shape of this beat note will be the same as that of the phase detector characteristic, but it will be filtered and attenuated somewhat by the loop filter. If the loop is closed this error signal or beat note will frequency modulate the VCO with the result that the error signal becomes highly non linear. This non linear error signal or beat note is found to contain a DC value which tends to drive the VCO towards the input signal frequency.

The filter in the second order loop tends to integrate this DC value until sufficient magnitude is reached to drive the VCO close enough to the input frequency to enable lock up to occur.

A general solution for the pull in range of a second order phase-locked loop has not yet been found, but approximations to this solution exist.[8,9] For the loop with an active lead lag filter

$$\omega_p = 2\sqrt{\zeta\omega_n K} \qquad \frac{\omega_n}{K} < .4$$

III. THEORY

A. Basic Theory of Operation of Proposed Receiver

Optical receiver implementation can be accomplished by either of two basic methods of detection known as Heterodyne detection (photomixing) or direct photodetection. In the system under discussion direct photodetection is employed due to several advantages. It is basically simpler than photomixing because of the lack of requirement for a laser local oscillator. Direct photodetection is less sensitive to the input signal frequency (light wavelength) than the heterodyne technique. An application where the received signal would suffer a Doppler shift could be disastrous in a heterodyne system. The magnitude of the Doppler shift could easily be a signal in the microwave frequency range and thus exceed the signal bandwidth. The device used to implement the direct photodetection is the dynamic crossed field photomultiplier (DCFP).

The basic receiver works as follows. The transmitted light pulses are collected in a large aperture, filtered and focused on to the photocathode of the DCFP. The photons in the incident light pulse cause electrons to be ejected from the photocathode surface and these electrons are then multiplied in number by means of secondary emission. The

average number of electrons emitted from the photocathode per incident photon is a measure of the quantum efficiency of the photocathode. In general, light pulses are referred to as consisting of so many photoelectrons rather than the number of photons. The relationship between the number of photoelectrons and the number of photons in a light pulse is the quantum efficiency of the photocathode which is used to detect the light pulse.

The output of the DCFP passes into a threshold detector where the decision is made as to whether a "one" or a "zero" has been transmitted. After the original PGBM modulating signal has been reconstructed the remaining signal processing is the same as that in a conventional microwave PCM receiver.

The remainder of the receiver is concerned with the generation of the synchronizing signal required for proper operation of the DCFP. The synchronizing signal is basically a sinusoidal wave, four times the frequency of and phase locked to the incident optical pulse train. This signal is generated as an integral part of a phase-locked loop which utilizes the DCFP as the phase detector.

This phase-locked loop is unique in that it is implemented by means of dithering the phase of the synchronizing signal about the optimum value (the point where the DCFP has the maximum gain). This phase dither is accomplished by phase modulating the RF drive signal at the dither frequency. Both the phase and the amplitude of the DCFP

output pulses are affected by the phase dither of the RF drive signal. The output pulses contain a time jitter (or phase modulation) caused by and synchronous with the RF drive. The RF drive dither also causes the DCFP gates to jitter with respect to the input optical pulse train resulting in the gate-pulse convolution being amplitude modulated at the dither frequency. The amplitude and phase modulated pulse train is synchronously detected by means of a reference signal from the dither oscillator which was used to originally dither the RF drive. The detected signal is amplified and filtered and becomes the control signal for a voltage controlled crystal oscillator (VCXO). The VCXO output is the required synchronizing signal for the DCFP. A block diagram for the synchronizing of the DCFP via a phase-locked loop is shown in Figure 8.

B. Theory of the DCFP Phase-Locked Loop

In a phase-locked loop the phase detector is used to measure the phase error between the VCO and the input signal. In a microwave receiver some signal processing is normally done prior to the input of the phase detector. As a minimum an antenna and a RF amplifier generally precede the phase detector. For proper operation of a synchronization loop it is required that the signal processing preceeding the phase detector not distort the input phase. For the optical receiver, the DCFP serves as the first RF amplifier receiving its signal directly from the antenna.

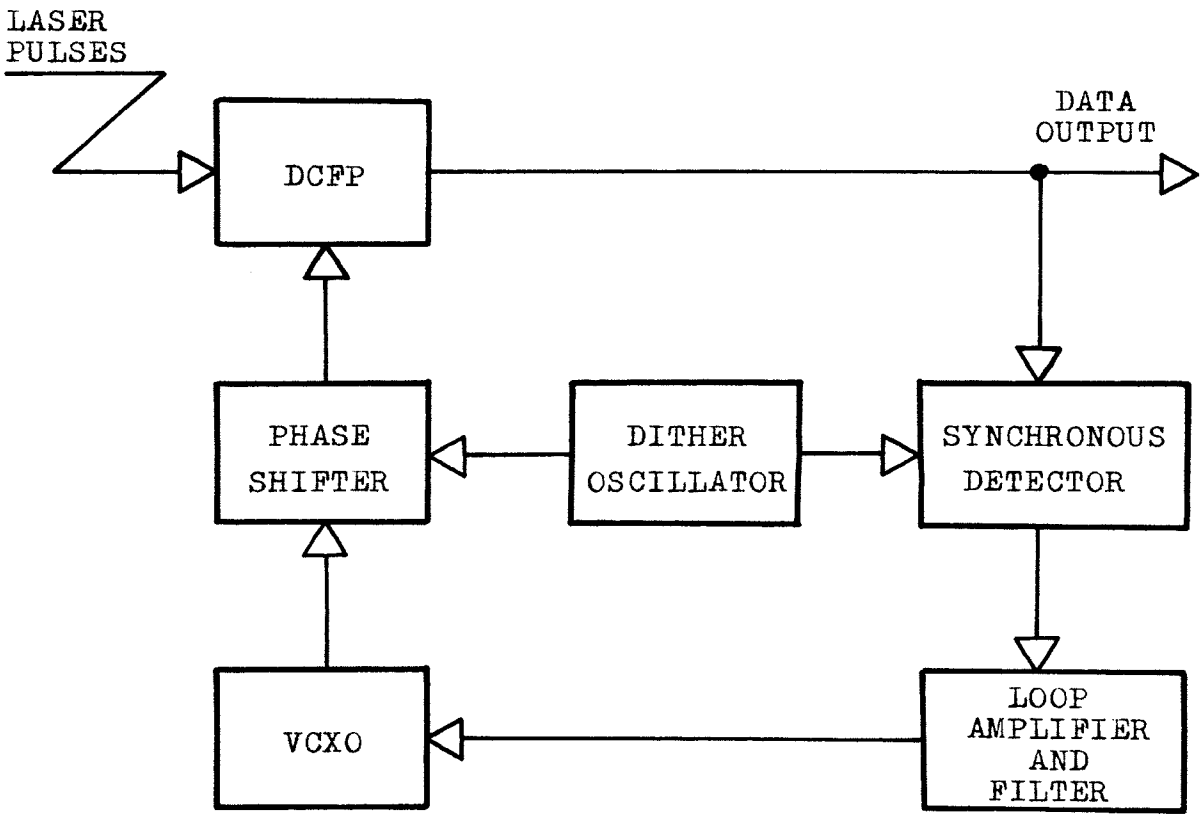


Figure 8. Block diagram of synchronizing phase-locked loop for the DCFP.

The output signal of the DCFP is a pulse which is the phase focused amplification of the sampled incident optical pulse train. This phase focusing action of the DCFP causes the output pulse to occur synchronously with the RF drive signal. Unfortunately this causes the pulse output of the DCFP to be void of normal phase information about the relative phase error between the DCFP RF drive and the incident optical pulse train. This lack of output phase information generates the requirement to use the DCFP itself as the phase detector.

The internal DCFP gate can be swept past the received optical pulse by frequency locking the RF drive to the input optical pulse train and then varying the relative phase displacement between them. The DCFP output pulse amplitude is proportional to the amount of the received optical pulse contained in the gate. This causes the pulse amplitude to vary cyclically modulo 2π with the phase difference between the gate and optical pulse. A typical example of the pulse amplitude variation versus phase displacement is shown in Figure 9. The convolution curve of the received pulse and the DCFP gate is identical to the pulse amplitude versus phase displacement curve.

The optimum operating point for the synchronization process is where the receiver gate is centered on the incident optical pulse allowing maximum receiver sensitivity. Since the DCFP gain following the initial gating process is constant with varying RF drive phase, the phase displacement

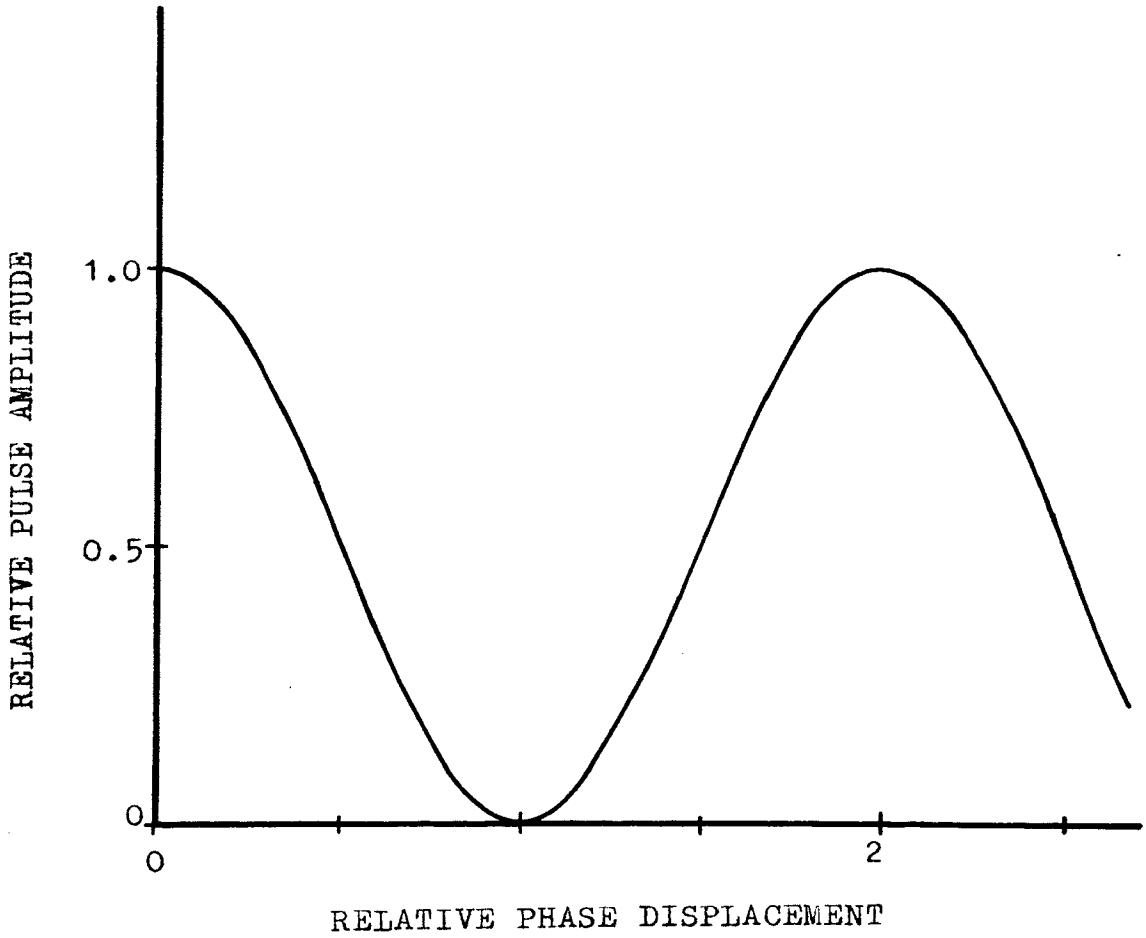


Figure 9. Pulse amplitude variation versus phase displacement between the optical pulse train and the RF drive.

corresponding to the maximum output pulse amplitude indicates where the gate is centered on the received pulse and therefore is the optimal operating phase displacement.

The output pulse amplitude versus phase displacement curve (convolution curve shown in Figure 9) can be used to generate a discriminator or phase detector curve which indicates error signal versus phase displacement. If the convolution curve is offset or displaced by a DC voltage a phase detector curve results. A phase-locked loop tracks about the null or zero voltage point on a phase detector curve. The null point on the generated phase detector curve does not occur at the optimal tracking point for a symmetrical curve. (Non symmetrical phase detector curves tend to case erratic behavior of the phase-locked loop during the acquisition process.) This sub optimal tracking results in a loss of receiver sensitivity caused by gating out or throwing away half of the received signal.

Implementation of this procedure for generating a usable phase detector curve could turn out to be somewhat of a problem. Some method must be found for measuring the peak output pulse amplitude and subtracting half of said peak value from the output pulse amplitudes of the DCFP. The average value of the resulting pulses would be the error signal for the phase-locked loop. Measuring the peak output pulse amplitude would be very difficult since the DCFP would be phase synchronized at a point not corresponding to the peak output pulse amplitude. Also

variations of transmitter power and atmospheric dispersion would cause the value of the peak output pulse to continually change thus requiring continuous monitoring. Due to this severe implementation handicap, and the sensitivity loss, other methods of generating a usable phase detector characteristic for the DCFP will be considered at this time. The problem of generating a phase detector characteristic for the DCFP is somewhat analogous to generating a radar range gate tracker in a radar system. Several implementations are possible to solve this problem. The most common solution used in radar range gate tracking is a split gate or early gate, late gate tracker.[10]

1. Using the DCFP as a Split Gate Tracker

A split gate tracker is useful as a time discriminator. The device functions by generating a discriminator characteristic with respect to time about some reference time value. For a fixed frequency of operation this type of tracker may also be used as a phase discriminator where the input signal is non sinusoidal such as a pulse train.

Essentially the tracker generates a gate which is to be positioned symmetrically about the received pulse. This gate is split into two equal parts sometimes called an "early gate" and a "late gate." The function of the split gate tracker is to center the received pulse inside of the gate such that a symmetrical received pulse will contain equal areas within both the early and late gates. A time

discriminator curve, which directs gate movement so as to center the pulse, is generated by noting the fractional area of the received pulse which is contained in the early and late gates. The differential area between the early and late gates is found by integrating the received pulse over the time of the gate with the early and late gates being used to determine a weighting factor to be applied to the pulse amplitude. Generally the early gate carries a weight of +1 and the late gate a weight of -1. The result of the integration process determines how well the received pulse is in the gate. A positive result from the integration process indicates too much of the pulse occurred in the early gate thus the next generated gate (assuming a periodic pulse) should occur earlier. A negative result from the integration process indicates too much of the pulse occurred in the late gate and thus the next generated gate should occur later. If the integration yields zero the pulse is properly centered in the gate and the next gate should occur at the same relative time. A graphical representation of the split-gate tracker operation is shown in Figure 10.

A split gate tracker can be implemented as follows. The incident signal is divided equally by using an optical beam splitter. Half of the signal power is thus applied to each of two separate matched DCFP's. One DCFP acts as the early gate and the other as the late gate. The late gate DCFP's dynamic electric field is delayed a small

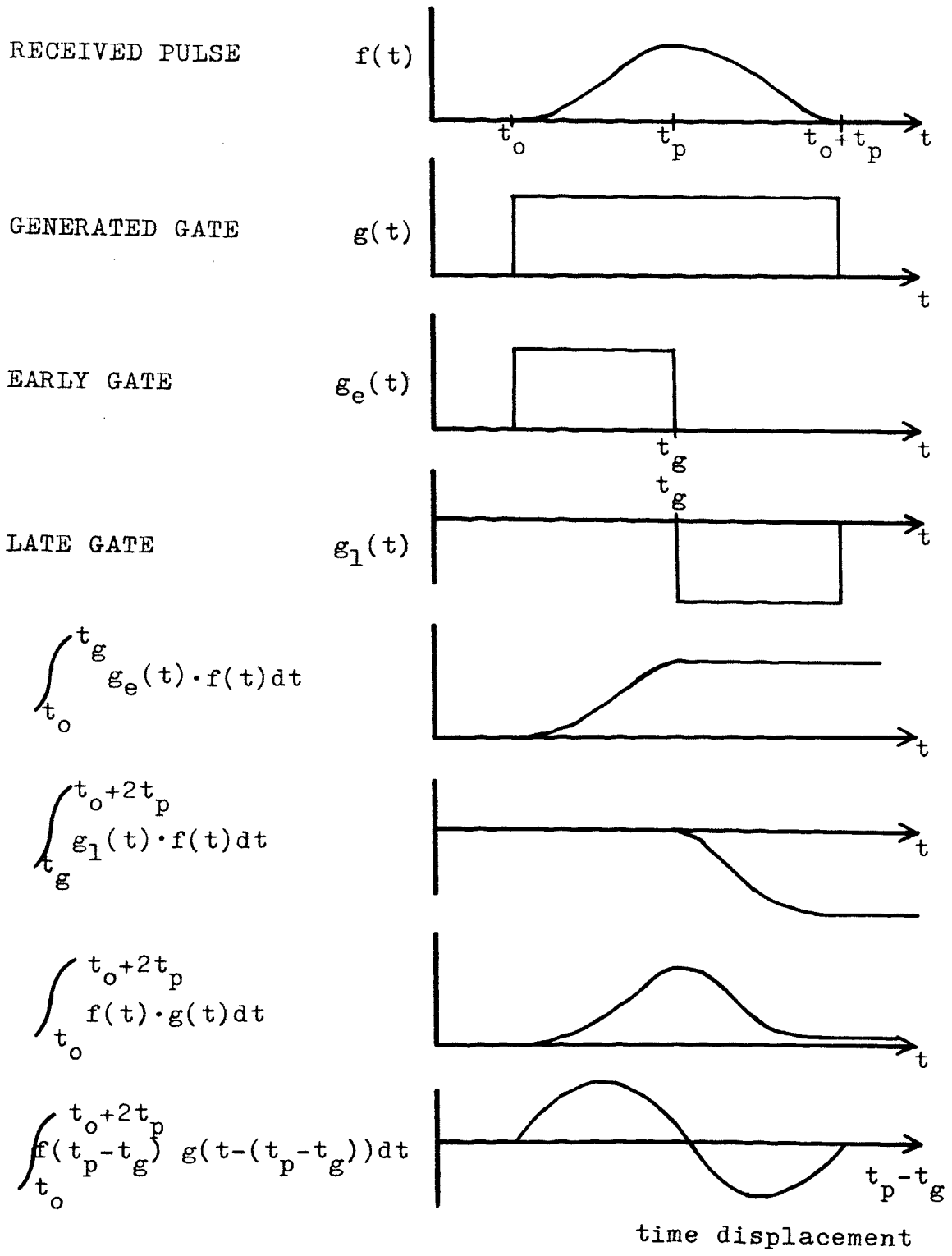


Figure 10. Generation of split gate tracker discriminator curve.

fraction of the gate width. The synchronization is achieved when the signal outputs of the DCFP's are equal.

This split gate synchronization system suffers a loss of sensitivity due to the beam splitter. The biggest disadvantage of the split gate synchronization system is the requirement for two matched DCFP's. Matched channel receivers always work better in theory than in practice. Also some of the signal processing must be accomplished at the input optical pulse repetition rate frequency. Due to these disadvantages a split gate tracker will not be used.

2. Using the DCFP as a Dithered Gate Tracker

Another means of generating a phase detector curve is by dithering (or jittering) the gate position a small fraction of the pulse width in a deterministic manner. If the phase of the dynamic electric field is periodically varied at some rate (the dither frequency) the result is a position modulation or dither of the DCFP gate. The gate dither causes the DCFP output pulses to be amplitude modulated at the dither frequency. The index of modulation can be determined by noting the magnitude of change in the DCFP output pulse (amplitude modulation) and comparing this to the pulse amplitude versus phase displacement which is depicted by the convolution curve for the DCFP. The degree or index of modulation is directly related to the slope or rate of change of the convolution curve, thus the derivative of the convolution curve with respect to phase displacement

determines the magnitude of the pulse amplitude modulation as a function of the phase dither. A typical DCFP convolution curve along with its derivative is shown in Figure 11.

Suppose the DCFP is operating such that the average phase displacement is $\pi/2$ radians and the instantaneous value of the phase displacement is dithered about this average value. As the instantaneous value of the phase displacement decreases the DCFP output pulse amplitude increases. This relationship reverses if the average value of the phase displacement is moved to $3\pi/2$ radians. The relationship between the value of the phase displacement and the output pulse amplitude is indicated by the sign of the derivative of the DCFP convolution curve. The magnitude of this derivative curve indicates the amount of pulse amplitude change per unit phase displacement. The synchronization loop will track at either 0 or π radians phase displacement since these points represent a null on the phase detector curve. Which of the two nulls the loop tracks about depends upon which slope is stable, that is, represents negative feedback.

Demodulation of the gated output pulse using synchronous detection, in which the dither oscillator is used as a reference, yields an error signal whose amplitude is proportional to the magnitude of the DCFP gate error relative to the center of the optical pulse. The polarity of this signal determines the direction of the gate error. If the

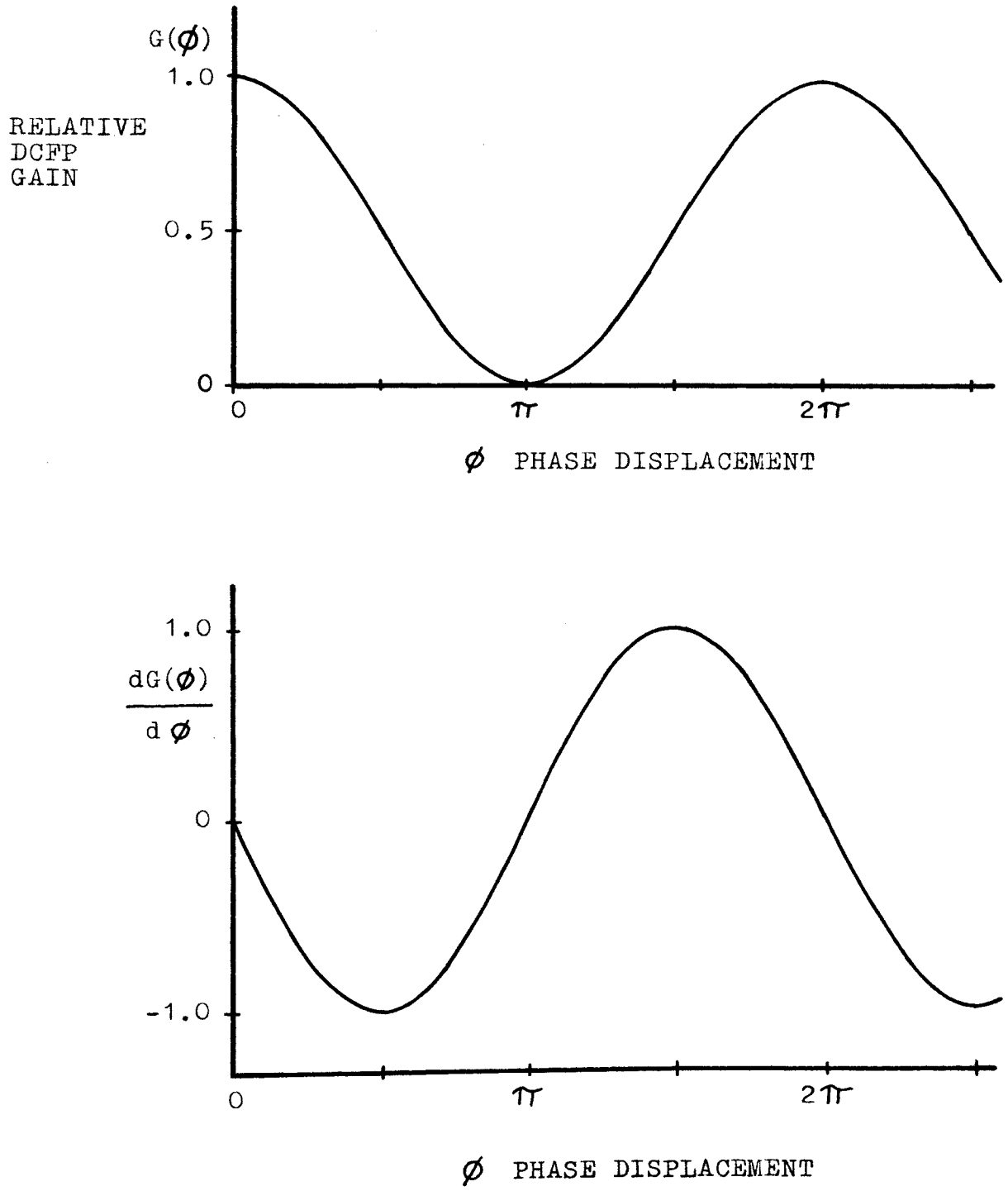


Figure 11. Typical DCFP sampling function and its derivative with respect to phase displacement.

phase displacement between the DCFP gate and the optical pulse is varied 2π radians the synchronously detected signal will trace out a phase detector curve showing how the DCFP functions as a phase detector.

Since the output signal of the DCFP is a pulse the amplitude modulated information is contained directly in the average value of these pulses, causing the amplitude modulated signal to appear directly at base band. Thus amplitude demodulation of the output pulses of the DCFP is not required. Additionally this baseband modulating signal is found to occur as a component of the current from the bias supply which is used to establish the static component of the electric field. The output dither signal of the DCFP can be obtained from a measurement of the bias current which requires none of the output signal power of the DCFP, thus maximizing the available receiver output.

This dithered phase method of synchronization has several advantages. The basic phase-locked loop circuits are implemented at and below the dither frequency, thus simplifying the design somewhat. The only degradation in the receiver sensitivity is that due to the amplitude modulation on the pulse output caused by gating out a small fraction of the received signal.

A phase dither synchronization loop should work adequately and therefore the actual design will be considered in greater detail.

C. The Synchronization Loop Design Goal

The end item usage of an optical receiver is as varied as that of any typical Radio Frequency or microwave receiver. Four projected applications for an optical receiver which in general cover the spectrum of uses and enable establishment of a comprehensive world wide optical communication network are:

1. Receiver for a synchronous earth satellite
2. Receiver for a low earth orbital satellite
3. Airplane receiver
4. Ground station receiver

Transmission between vehicles which are moving with respect to each other will cause the received signal to suffer a Doppler frequency shift. The system employed to generate the synchronizing signals required by the DCFP should be capable of handling these frequency changes.

If the optical signal is to be transmitted through the atmosphere it will suffer some degradation due to the turbulances in the signal path. These degradations will appear as amplitude modulation and time dispersion in the received pulses. Again the optical receiver must be capable of handling the perturbed signal.

Various transmitters will probably be used with the optical receiver and the characteristics of these different laser transmitters will vary somewhat. The wavelength of the transmitter is constrained to be in a region for which the DCFP photocathode has a reasonable quantum efficiency.

Presently work is being carried out in the visible part of the spectrum in the green region. The present optical wavelength is approximately 530 nanometers. The half amplitude pulse width of the laser presently being used is 300 picoseconds. This pulse width might be larger or smaller if a different laser were used. A mode locked laser is essentially a cavity oscillator the stability of which is of the order of 1 part in ten to the sixth at best and typically 1 part in ten to the fifth. The amplitude of the transmitted pulses will vary slightly, (perhaps by 10 percent), due to the instabilities in the gain of the mode locked laser transmitter. The phase-locked loop which is used to synchronize the DCFP must be capable of handling these frequency and amplitude variations.

Besides the laser transmitter and the signal transmission channel causing the received pulse amplitude to vary, the data format (the relative number of "ones" and "zeroes") causes the average value of the received signal strength to vary. The receiver should be able to handle a minimum of a two to one change in the received power level.

The receiver presently being designed is a prototype unit which will be used for a laboratory demonstration of system feasibility. Thus, there is no requirement for the synchronization loop to track a Doppler shift. The tracking loop must track a one kilohertz frequency variation at a one kilohertz rate. This minimum condition should be met even with a two to one change in the receiver input

signal amplitude.

The following is a list of the phase-locked loop design constraints.

1. The bandwidth shall be 2 KHz nominal with 1 KHz minimum.
2. The acquisition range shall be 40 KHz nominal, with 10 KHz minimum.
3. The hold in range shall be greater than 40 KHz nominal with 10 KHz minimum.
4. The static phase error shall be less than five degrees for any input signal in the hold in range.
5. The dynamic phase error shall be such that the loop does not lose lock for an input frequency variation of 1 KHz at a 1 KHz rate or approximately $1X10^6$ Hz/Sec swept frequency.
6. Input signal amplitude variation of two to one shall not cause the phase-lock loop parameters to fall below their minimum values.
7. The acquisition time shall be 1 second nominal with a maximum of 2 seconds.
8. If the pull in range is not adequate to cover the expected input signal frequency variations or if the pull in time is greater than the allowable acquisition time, a sweep acquisition circuit shall be used.
9. The phase-lock loop shall contain a lock detector to indicate when the loop is properly

synchronized.

10. A voltage controlled crystal oscillator (VCXO) shall be used for the voltage controlled oscillator (VCO) due to the inherent high frequency stability and low noise of the VCXO.
11. The phase-lock loop shall be implemented by means of a dithered phase of the RF drive signal to the DCFP. The magnitude of the phase dither shall be such as not to cause more than a five percent amplitude modulation on the output of the DCFP.
12. The dither frequency shall be as low as possible, a nominal value of 250 KHz is acceptable and a maximum value of 1 MHz will be allowed.
13. Provisions shall be made to prevent or to detect and correct false lock which may occur due to the DCFP phase detector characteristics or due to the input data format.
14. The present receiver shall be required to operate in a normal laboratory environment only.
15. The signal frequencies referred to are for the 300 MHz optical pulse train input.
16. The DCFP shall be a 1200 MHz tube and as such will operate at the fourth harmonic of the input signal.

D. Design of the Synchronization Loop

Specification of the loop filter, F(s), for the phase-locked loop determines the loop tracking performance. Before considering the available choices for the loop filter, the loop parameters will be specified which will meet the design goals.

A minimum value for the open loop gain can be determined from the maximum allowable static phase error. If the allowable phase error is five degrees for an initial frequency offset of 40 KHz at 300 MHz or 160 KHz at 1200 MHz then

$$\sin\theta = \frac{\Delta\omega}{K}$$

or

$$K = \frac{\Delta\omega}{\sin\theta}$$

thus

$$K = \frac{2\pi x 40 x 10^3 x 4}{\sin 5^\circ}$$

$$K = 1.15 x 10^7$$

Another design condition specifies that an input signal amplitude variation of two to one should not cause the phase-locked loop parameters to fall below their minimum value. Since the loop gain is directly related to the input signal amplitude, the gain should be doubled to allow for the input amplitude variation, therefore,

$$K \geq 2.3 \times 10^7$$

The bandwidth is specified to be 5 KHz nominal with a 1 KHz minimum. Also the dynamic phase error is specified such that the loop should not lose lock for a 1 KHz input signal variation at a 1 KHz rate at 300 MHz. This is equivalent to sweeping the input frequency 1 KHz in 1/(1 KHz) or 1 millisecond. Thus the input frequency rate of change would be

$$\Delta \dot{f} = 1 \text{ KHz}/1 \text{ millisecond}$$

$$\Delta \dot{f} = 1.0 \times 10^6 \text{ Hz/sec}$$

$$\Delta \dot{f} = 4.0 \times 10^6 \text{ Hz/sec (at 1200 MHz)}$$

Gardner[8] specifies for a second order loop that the maximum rate of change of the input frequency be such that

$$\Delta \dot{\omega} \leq \omega_n^2$$

or the loop will lose lock.

Thus

$$\omega_n \geq \sqrt{\Delta \dot{\omega}}$$

or for the case being considered

$$\omega_n \geq \sqrt{2\pi \times 4 \times 10^6}$$

$$\omega_n \geq 5 \times 10^3 \text{ radians/sec}$$

or

$$f_n \geq .795 \text{ KHz}$$

The loop bandwidth is found to vary directly as the square root of the loop gain. Thus to allow for decreases in the loop gain due to input signal amplitude variations, the loop bandwidth should be somewhat wider than the minimum acceptable value.

If the loop gain is made too high or if the loop bandwidth is too wide the phase-locked loop error signal will become noisy. This situation will exist if the VCXO control signal is sufficiently noisy that the output VCXO phase jitters an amount equivalent to the static phase error. Further increases in the loop gain will decrease the static phase error but increase the output phase jitter. Making the loop bandwidth wider than the amount required to track the input signal variations just increases the noise bandwidth thus lowering the loop signal to noise ratio.

The loop filter is implemented by the use of an active lead-lag filter, since this choice gives the greatest flexability in the design and is adequate to meet the design goals.

The open loop gain is made equal to

$$K = 2.4 \times 10^7$$

and the loop bandwidth is

$$\omega_n = 2\pi \times 10^3 \text{ radians/sec}$$

and for good transient response the loop damping ratio is

$$\zeta = 0.707$$

The loop gain is found as follows

$$K = K_o K_d F(0)$$

where

K = the open loop gain

K_o = the VCXO gain

K_d = the phase detector gain

$F(0)$ = the loop filter gain

The VCXO used in the synchronization loop has an output frequency of 100 MHz and a gain of 10 KHz per volt. This signal is then frequency multiplied by 12 to achieve the desired 1200 MHz drive signal for the DCFP. Thus

$$K_o = (2\pi \times 10\text{KHz/volt}) \times 12$$

$$K_o = 7.55 \times 10^5 \text{radians/volt.}$$

The phase detector gain is found as follows. The RF drive to the DCFP is dithered approximately five degrees, such that the output pulses of the DCFP exhibit five percent amplitude modulation at the dither frequency. This amplitude modulation is detected by measurement of the changing DCFP dynode current. The dither signal is then amplified in an AGC amplifier which removes slowly varying signal level changes due to input power variations. The output signal level of the AGC amplifier is -6.5 dbm or approximately 300 millivolts peak to peak. This signal is applied to a double balanced mixer which is used as the synchronous detector. The gain of the double balanced mixer is approximately -5.5 db or .53 when the local oscillator signal is +7 dbm. The phase detector gain can now be found since a $\pi/2$ radian phase shift represents a peak output signal of the phase detector of

$$K_d = .53 \times \frac{.300/2}{\pi/2}$$

$$K_d = 0.0506 \text{ volts/radian}$$

The required F(O) is found from the following equation

$$K = K_o K_d F(0)$$

$$F(0) = \frac{K}{K_o K_d}$$

$$F(0) = \frac{2.4 \times 10^7}{7.55 \times 10^5 \times 5.06 \times 10^{-2}}$$

$$F(0) = 6.27 \times 10^2$$

For the active lead lag filter

$$\omega_n = 2\pi \times 10^3 \text{ radians}$$

$$\omega_n = \sqrt{K_o K_d F(0)/\tau_1}$$

$$K_o K_d F(0) = K = 2.4 \times 10^7$$

$$\tau_1 = \frac{K}{\omega_n^2}$$

$$\tau_1 = \frac{2.4 \times 10^7}{(2\pi \times 10^3)^2}$$

$$\tau_1 = 6.1 \times 10^{-1}$$

Also

$$\zeta = 0.707$$

$$\zeta = \tfrac{1}{2} \tau_2 \sqrt{K_o K_d F(0)/\tau_1}$$

$$\zeta = \tfrac{1}{2} \tau_2 \omega_n$$

$$\tau_2 = \frac{2\zeta}{\omega_n}$$

$$\tau_2 = \frac{1.414}{2\pi \times 10^3}$$

$$\tau_2 = 2.25 \times 10^{-4}$$

The circuits used to implement this design will be

discussed next.

E. Circuits Used for Design Implementation

1. Bandpass Filter

A bandpass filter is required to precede the AGC amplifier to eliminate undesirable signals. When the loop is unlocked a beatnote, which is more than an order of magnitude larger in amplitude than the desired dither signal, is present at the AGC amplifier input. This large amplitude beatnote signal if not filtered out would set the gain level of the AGC amplifier and the dither signal will not be amplified to the proper level. Also without a bandpass filter a situation exists where false lock can occur. Without a bandpass filter the dominant output signal of the AGC amplifier would be the beatnote. Since the synchronous detector will respond to harmonically related signals at its input, it is entirely possible for the phase-locked loop to lock up at a frequency offset which is harmonically related to the dither frequency. The bandpass filter used is a 5 pole Butterworth filter with a 200 KHz bandwidth. This filter is adequate to prevent false locking on sub harmonics of the dither frequency below 250 KHz (the fifth and greater sub harmonic). To prevent false lock above 250 KHz the range of the VCXO is limited such that the required frequency offset for false lock cannot occur. A schematic diagram of the bandpass filter is contained in Figure 12.

2. Bias Filters

A bias filter is used in conjunction with each of the high voltage power supplies which establish the static component of the electric field for the DCFP. These bias filters are used to reduce the ripple of the high voltage inverter supplies. For the first dynode a single RC low pass filter was adequate to reduce the ripple. Two cascaded RC low pass stages were required for the second dynode filter because the second dynode requires over 100 times the current of the first dynode causing the power supply to produce a larger ripple. Also for the second dynode supply, pickoffs are provided for the bandpass filter and the lock detector (both AC and DC). A schematic diagram of the filters is shown in Figure 12.

3. The AGC Amplifier

The dither signal which is derived from the measurement of the dynode current is amplified by an AGC amplifier which will remove slowly varying signal level changes due to input power variations caused by changing range or laser power. The required gain of the AGC amplifier is found as follows. Assume the DCFP gain is adjusted such that the average dynode current is one milliampere. With a five percent amplitude modulation and a 25 ohm current sensing resistor (50 ohm input impedance for the bandpass filter in parallel with a 50 ohm input impedance to the lock detector)

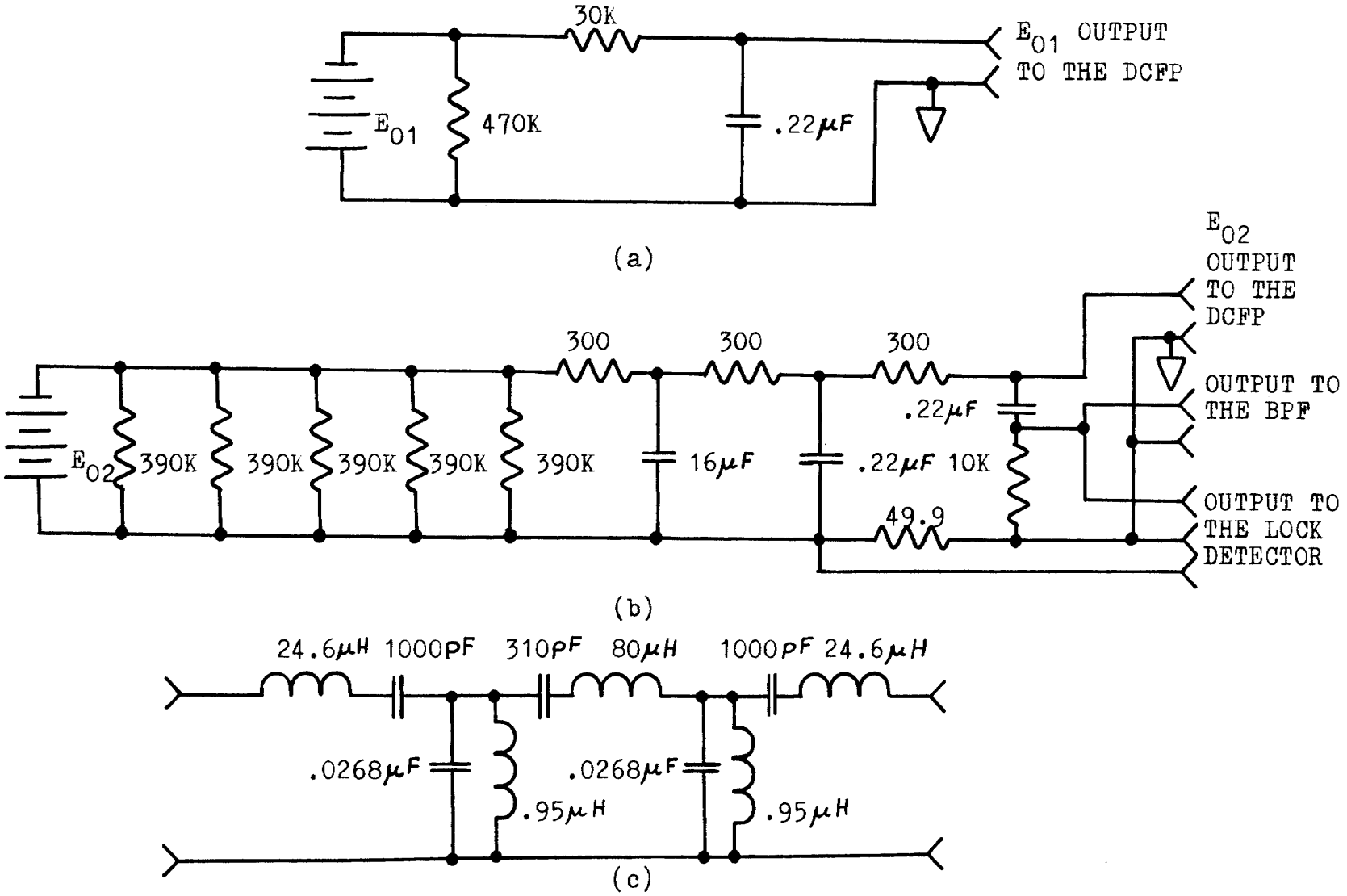


Figure 12. Schematic diagram of a) the E_{01} bias filter, b) the E_{02} bias filter and signal sampler, and c) the bandpass filter.

the magnitude of the dither signal would be

$$V = .05x1x10^{-3}x25$$

$$V = 1.25 \text{ millivolts peak to peak}$$

This signal passes through the bandpass filter which has an insertion loss of 4 db or a voltage gain of .63. The amplified dither signal will be applied to a synchronous detector which requires a .3 volt peak to peak input. Thus the required gain for the AGC amplifier is

$$G = \frac{300x10^{-3}}{1.25x10^{-3}x.63}$$

$$G = 381$$

The hardware implementation of the AGC amplifier uses two cascaded video amplifiers. Each amplifier has a maximum gain of 30 and is composed of two internal common emitter voltage gain stages. The AGC gain variation is obtained by varying the emitter gain degeneration resistors in the common emitter stages. The output signal of the AGC amplifier is peak detected, compared to a reference signal, and amplified to derive an error signal to implement the gain variation. The bandwidth of the error signal is low, approximately 20 Hz, thus the AGC amplifier only responds to slowly varying signal levels. The gain of the first video amplifier is varied while the second amplifier has a fixed gain. A 50 ohm line driver is used at the output of the AGC amplifier to drive the double balanced mixer. A complete schematic of the AGC amplifier is shown in

Figure 13

4. Synchronous Detector

A double balanced mixer serves as the synchronous detector. For this application the mixer functions as a non ideal synchronous switch. The circuitry consists of two transformers and a diode bridge and is shown schematically in Figure 14. The switching action occurs as points a and b are alternately connected to the output through the diode bridge. When the local oscillator input is positive, point a is connected to the output by diodes D_1 and D_2, and point b is connected to the output by diodes D_3 and D_4 when the local oscillator input is negative. The non ideal nature of the switching occurs because the local oscillator signal must develop enough voltage to turn on two of the diodes before the input is connected to the output via the "closed switch".

The recommended drive level for the local oscillator input to the double balanced mixer is +7 dbm, or 5 milliwatts reference to a 50 ohm system. The operating point for the signal input is -6.5 dbm or a 300 millivolt peak to peak signal. If the local oscillator signal is a large amplitude signal (+7 dbm) compared to the input signal (-6.5 dbm), the output signal amplitude will be proportional to the smaller amplitude signal input. The double balanced mixer gain is found by integrating the full wave rectified input signal over that portion of the cycle for

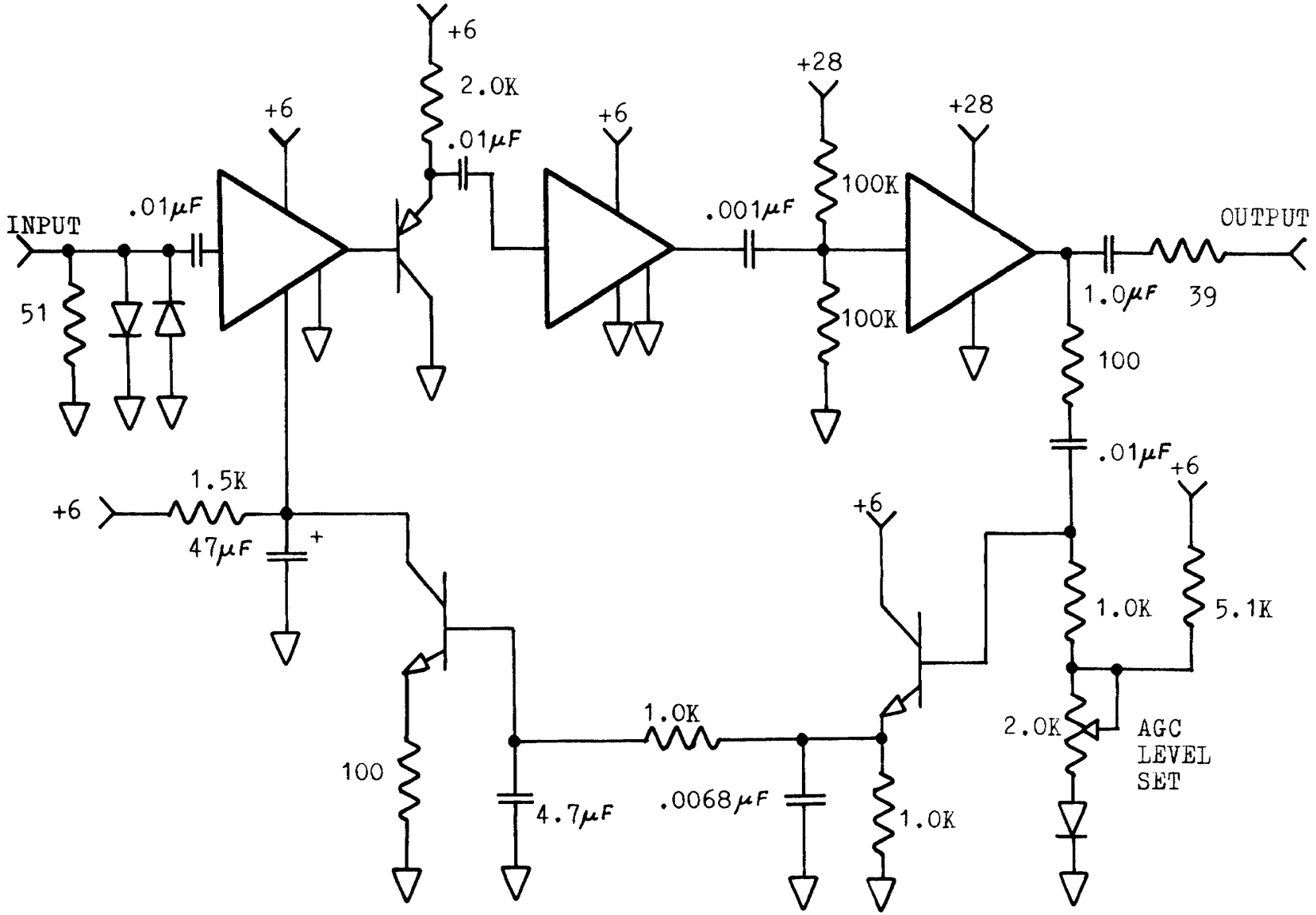


Figure 13. Schematic diagram of the AGC amplifier.

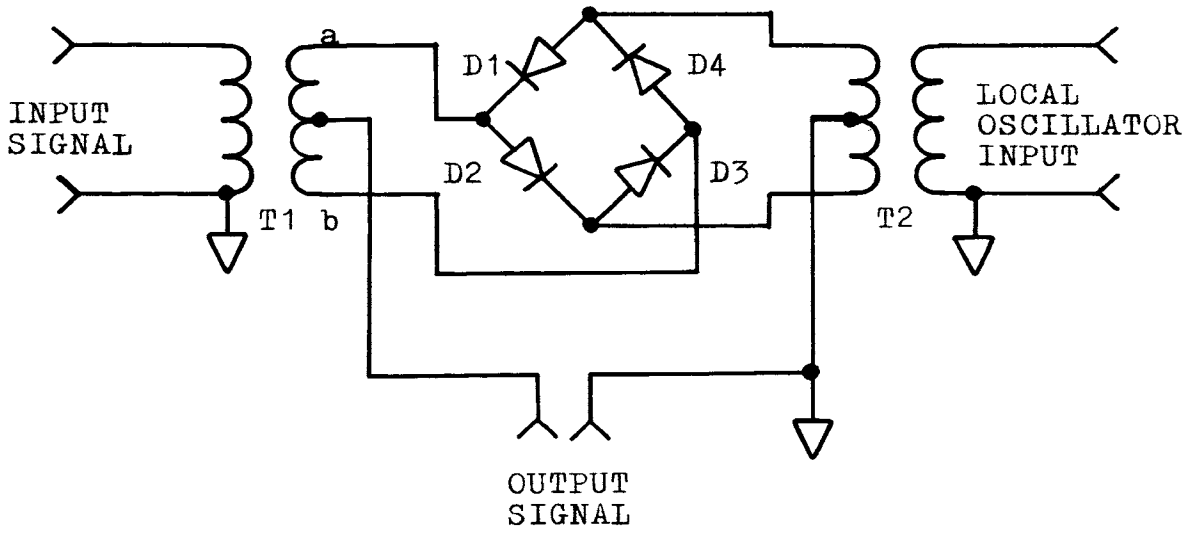


Figure 14. Schematic diagram of a double balanced mixer.

which the diodes in the bridge are conducting. Thus the gain of 0.53 (-5.5 db) is slightly less than $2/\pi$.[11] The output signal is a null when the input and drive signals are $\pi/2$ radians apart, such as with sine and cosine inputs.

5. The Active Filter

The active lead lag filter was synthesized using high gain operational amplifiers. The high DC open loop gain ($F(0) = 627$) was achieved by using three cascaded stages to ensure that the phase-locked loop performance was not affected by the inherent amplifier poles (which occur where the open and closed loop gain curves intersect on the amplifier Bode plot). Also the three cascaded stages were used to implement additional functions. The first stage forms the basic active filter, the second stage is used to sum in the sweep generator signal, and the third stage contains voltage limiting to protect the VCXO and alleviate false lock problems.

The synchronization loop has a high DC gain to produce a small static phase error over the desired input frequency range. When the loop is not phase locked, the high DC loop gain will cause the active filter amplifiers to saturate with a small phase shift of the quadrature inputs to the double balanced mixer. For the proper acquisition sequence to occur, the sweep generator must develop sufficient signal to drive the loop out of saturation and into the linear tracking region to bring the VCXO within the loop lock in

range of the input signal. The maximum rate at which the sweep generator can drive the loop is limited by the loop dynamic tracking capability. The smaller the range over which the loop is swept, the faster the acquisition time can be made. The sweep range is minimized by limiting the magnitude of the error signal prior to the point where the sweep input and error signal are summed together. The loop tracking performance is not affected by the error signal limiting because the limiting occurs at a larger magnitude error signal than the loop can generate and still maintain lock. The basic circuit is shown in Figure 15.

The transfer function for the first stage using Laplace notation is

$$\frac{e_2(s)}{e_1(s)} = \frac{Z_f(s)}{Z_i(s)} = \frac{\dfrac{R_3\left(R_2+\dfrac{1}{sC_1}\right)}{R_3+R_2+\dfrac{1}{sC_1}}}{R_1} = \frac{R_3}{R_1}\,\frac{sR_2C_1+1}{s(R_2+R_3)C_1+1}$$

$e_2(s)$ = the amplifier output signal

$e_1(s)$ = the amplifier input signal

$Z_f(s)$ = the amplifier feedback impedance

$Z_i(s)$ = the amplifier input impedance

The desired transfer function is

$$F(s) = F(0)\frac{s\tau_2+1}{s\tau_1+1}$$

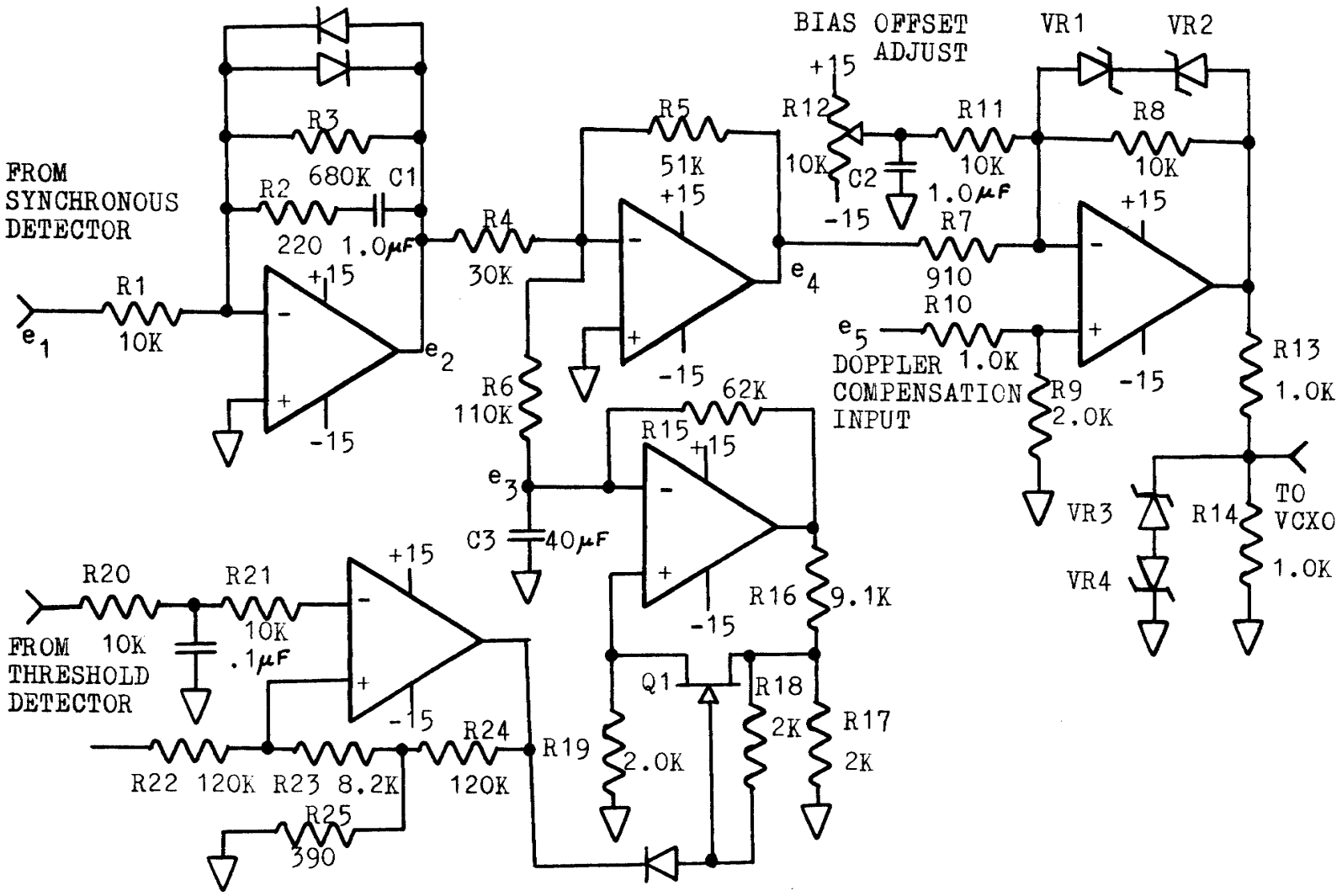


Figure 15. Schematic diagram of the active filter, the summer, the limiter, the sweep generator, and the sweep generator on off switch.

where

$$\tau_2 = R_2C_1 = 2.25\text{x}10^{-4}$$

$$\tau_1 = (R_2+R_3)C_1 = 6.1\text{x}10^{-1}$$

Besides being able to select the desired first stage gain, one additional component can be arbitrarily selected from R_1, R_2, R_3, and C_1 because only three constraints are specified, $F(0)$, τ_1, and τ_2. The magnitude of C_1 was selected to be 1 μF and the value of the first stage gain was calculated to give the desired voltage limiting characteristics.

The value of R_2 can be calculated from

$$\tau_2 = C_1R_2$$

$$R_2 = \frac{\tau_2}{C_1} = \frac{2.25\text{x}10^{-4}}{10^{-6}}$$

$$R_2 = 2.25\text{x}10^{2}$$

or using a standard resistor value

$$R_2 = 220 \text{ ohms}$$

The value of R_3 can be calculated from

$$\tau_1 = (R_2+R_3)C_1$$

$$R_3 = \frac{\tau_1}{C_1} - R_2 = \frac{6.1\text{x}10^{-1}}{10^{-6}} - 220$$

$$R_3 = 6.1\text{x}10^{5}$$

or using an available standard resistor value

$$R_3 = 680\text{K ohms}$$

The value of R_1 now determines the first stage gain and this value was selected to give the desired voltage limiting characteristics.

The voltage limiting was achieved by using the voltage drop across a silicon diode. The voltage current characteristics of a pn diode obey the exponentional equation

$$I = K(e^{\phi V}-1)$$

The two unknown constants, K and ϕ, were found by measuring the voltage and current at two points and solving two equations simultaneously for K and ϕ. Using V = 270 millivolts at I = 1 microamp; and V = 470 millivolts at I = 64 microamps resulted in

$$\phi = 20.8$$

$$K = 3.65x10^{-9}$$

The voltage limiting starts occurring when the diode current is equal to the current in the feedback resistor. Thus

$$I = K(e^{\phi V}-1) = \frac{V}{R_3}$$

or

$$V = R_3K(e^{\phi V}-1)$$

Solving this equation for V by picking a trial value for V and iterating until a solution is found results in V = .214 volts and the corresponding I of .315 microamps.

The output error signal to the VCXO is limited to

approximately ± 1.8 volts to prevent false lock problems. To make this first stage limiting occur at a larger input signal level (equivalent to a 2 volt output), the gain following the first stage should be 2/.214 or 9.35. The gain for the first stage should then be 627/9.35 or 67.2. The value for R_1 can now be calculated

$$\text{Gain} = \frac{R_3}{R_1}$$

$$R_1 = \frac{R_3}{\text{Gain}} = \frac{680K}{67.2}$$

$$R_1 = 9.87K$$

or using a standard resistor value

$$R_1 = 10K$$

The second stage gain is 1.7 with $R_5 = 51K$ and $R_4 = 30K$. The output signal of the sweep generator is summed in at this point. The remaining gain of

$$\frac{627}{68 \times 1.7} = 5.43$$

is achieved in the third stage. The operational amplifier circuit implements twice this gain and the output is then resistively divided by two. This is required to implement the desired voltage limiting. Choosing $R_8 = 10K$ and $R_7 = 910$ with $R_{13} = R_{14} = 1.0K$ gives a composite third stage gain of 5.5.

The zener diodes VR_1 and VR_2 are used to limit the magnitude of the error signal to prevent false lock problems.

The breakdown voltage of the back to back zener diodes is equal to the zener voltage plus the forward voltage drop (one zener diode is forward biased and the other is reverse biased). The zener diodes were chosen such that the sum of these voltage drops was 3.6 volts at the required current (3.6 volts/10K). The amplifier output signal is then divided by two in the resistive voltage divider composed of R_{13} and R_{14}. This limits the error signal applied to the VCXO to 1.8 volts.

A potentiometer is used at the input to the last stage to sum in a DC signal to account for any voltage offsets in the amplifiers and to offset the VCXO frequency from the center value if desired. Also included at this point is an additional summing input, R_{10}, which may be used to sum in a voltage proportional to an expected received Doppler shift as might be available in a satellite data processing computer. VR_3 and VR_4 are included across R_{14} to limit to less than 3 volts the sum of the error signal plus the Doppler input to prevent damage to the VCXO.

6. The Sweep Generator

Improved acquisition range and transient response was obtained by the addition of a sweep generator to drive the VCXO. The sweep signal is generated by using the beginning of an exponential resulting in a triangular waveform. Implementation was obtained by using an operational amplifier utilizing both positive and negative feedback with

a FET switch to turn the sweep generator on and off. The basic circuit is shown in Figure 15.

When the FET switch is opened, the output voltage decays to zero with the same slope as the normal sweep. This is important since a fast transient when the generator is switched off would cause the loop to lose lock.

The peak output voltage of the triangular wave is

$$V_{out} = V_{sat} \frac{1}{1+\frac{R_{16}}{R_{17}}+\frac{R_{16}}{R_{19}}}$$

where V_{sat} is the operational amplifier output saturation voltage. The period of the sweep waveform is

$$T = 2\frac{R_{15}R_6}{R_{15}+R_6}C_3 \, Ln\left(1+\frac{2(R_{15}+R_6)}{R_6\left(\frac{R_{16}}{R_{17}}+\frac{R_{16}}{R_{19}}\right)-R_{15}}\right)$$

The sweep generator must drive the VCXO over the desired acquisition range of $\pm$40 KHz at 300 MHz which requires a VCXO control voltage of

$$V_c = \frac{40 \text{ KHz}}{3\text{x}10\text{KHz/volt}} = \frac{4}{3} \text{ volt.}$$

Thus the magnitude of the sweep voltage should be 4/3 volt. In addition to sweeping the VCXO over the required acquisition range, the sweep generator must develop sufficient magnitude to overcome the magnitude of the voltage limiting which occurs in the first stage when the loop is unlocked. The first stage saturation voltage of 214 millivolts is

multiplied by the remaing gain of 9.35 resulting in a VCXO error signal of 2.00 volts. Adding to this the required sweep range of 4/3 volt yields a required sweep magnitude of 3.33 volts. Dividing by the last stage gain of 5.5 results in a 0.605 volt sweep magnitude required out of the second stage. Allowing a sweep generator magnitude of 4/3 volt and calculating the summing gain required for the second stage yields

$$\frac{R_5}{R_6} = \frac{.605}{4/3} = .452$$

or

$$R_6 = \frac{R_5}{.452} = \frac{51K}{.452} = 113K$$

and choosing a standard resistor value

$$R_6 = 110K \text{ ohms}$$

Now proceeding to calculate the 4/3 volt sweep generator output signal with a ± 15 volt power supply, a V_{sat} of approximately ± 14 volts results, therefore,

$$\frac{4}{3} = 14 \frac{1}{1 + \frac{R_{16}}{R_{17}} + \frac{R_{16}}{R_{19}}}$$

Letting $R_{17} = R_{19}$

$$\frac{4}{3} = 14 \frac{R_{17}}{R_{17} + 2R_{16}}$$

$$R_{16} = \frac{38}{8} R_{17}$$

Choosing $R_{17} = 2.0K$

$$R_{16} = \frac{38}{8} x 2.0K = 9.5K$$

Using a standard resistor value

$$R_{16} = 9.1K$$

The loop will be swept slowly to insure good locking and that some input signal perturbation is possible between acquisition and the time at which the sweep generator is turned off. Thus some time can be spent determining if a good lock has occurred. Let the sweep period be one second. Thus

$$T = 1$$

$$T = 2\frac{R_{15}R_6}{R_{15}+R_6} C_3 Ln\left(1+\frac{2(R_{15}+R_6)}{R_6\left(\frac{R_{16}}{R_{17}}+\frac{R_{16}}{R_{19}}\right)-R_{15}}\right)$$

Let $R_{15} = 62K$ ohms and calculate the required value of C

$$T = 2\frac{(62K)(110K)}{62K+110K} C \; Ln\left(1+\frac{2(62K+110K)}{110K\left(\frac{9.1K}{2K}+\frac{9.1K}{2K}\right)-62K}\right)$$

$$T = 2(39.6K)(C)Ln\left(1+\frac{344K}{110K(9.1-.564)}\right)$$

$$T = (2)(39.6K)C \; Ln\left(1+\frac{3.125}{8.536}\right)$$

$$T = (79.2K)CLn(1.367)$$

$$1 = (79.2)C(.3125)$$

$$C = \frac{1}{24.75K}$$

$$C = 40.4 \times 10^{-6} \text{ farads}$$

Choosing a standard value gives

$$C = 40 \mu F$$

A field effect transistor (FET) is used to implement the on-off switch for the sweep generator and an operational amplifier is used to drive the FET. This amplifier is driven by the output of the lock detector. This circuitry is also shown on the schematic of Figure 15.

7. The Lock Detector

A lock detector was included in the phase-locked loop circuitry to determine when the sweep generator should be turned on and off and also to drive a lock indicator lamp. The lock detector compares the magnitude of the DC to the AC component of the dynode current. When the loop is locked the magnitude of the AC component is small compared to the DC. When the loop is unlocked, the dynode current contains the beatnote frequency between the VCXO and the optical pulse train, and the AC and DC components typically are equal.

The hardware implementation consists of an AC and a DC signal path to a comparator or threshold detector. The DC signal is derived across a sense resistor in series with the dynode power supply. This signal is filtered, amplified, and filtered again, becoming the reference level for

the threshold detector. The AC signal is derived by capacitively coupling the dynode current variations developed across a current sensing resistor. This AC signal is amplified, full wave rectified, amplified again, filtered, and finally becomes the threshold detector input. The schematic diagram of the lock detector is shown in Figure 16.

8. The RF Chain

Between the VCXO output and the DCFP input are many RF components used to add the dither, multiply the frequency, and amplify the power. Following the 100 MHz VCXO is an amplifier which is used to drive a tripler. Provision is made at this point for inserting an external reference signal which is followed by a phase shifter to adjust the external reference phase for proper synchronization. A 300 MHz amplifier is then used to drive a quadrupler which is followed by a 1200 MHz bandpass filter and then an electronic phase shifter to insert the phase dither. A variable attenuator is used at this point to adjust the RF power level which controls the gain of the DCFP. A 1200 MHz power amplifier develops the required drive for the DCFP. A circulator is included between the power amplifier and the DCFP to protect the power amplifier from accidentally disconnecting the DCFP which would cause the power amplifier to burn out.

The majority of the RF hardware was purchased from

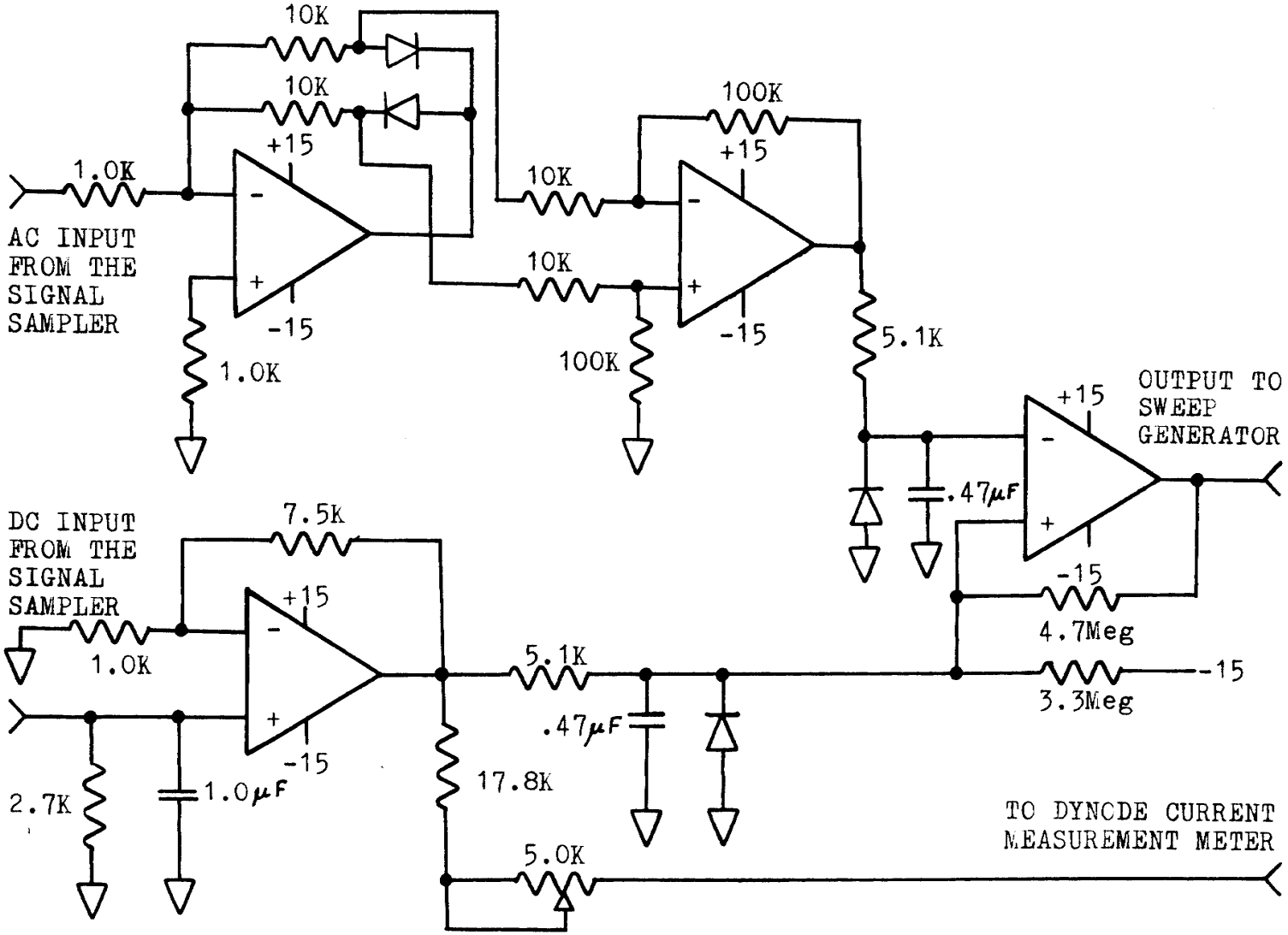


Figure 16. Schematic diagram of the lock detector.

various vendors. Figure 17 shows a block diagram representing the synchronization implementation. Figure 18 is another block diagram showing the details of the RF chain, the acquisition circuit and the tracking circuit.

F. Analysis of the Synchronization Loop Design

The synchronization loop design will now be analyzed to predict the performance and determine if the design goals are being met. The items which will be analyzed are loop gain, loop bandwidth, loop damping ratio, the static phase error, the dynamic phase error, hold in range, lock in range, pull in range, acquisition range with sweep generator, acquisition time, false lock, signal level variations, and other areas such as environment and methods of implementation (dither the phase, the dither frequency, etc.).

1. The Loop Gain

The open loop gain, K, of the phase-locked loop is equal to $K_o K_d F(0)$.

$$K_o = (10\text{KHz/volt}) \times 2\pi \times 12$$

$$K_o = 7.55 \times 10^5 \text{ radians/volt.}$$

where the 10KHz/volt is the VCXO gain constant.

$$K_d = \frac{.300/2}{\pi/2} \times .53$$

$$K_d = 5.06 \times 10^{-2} \text{ volts/radian}$$

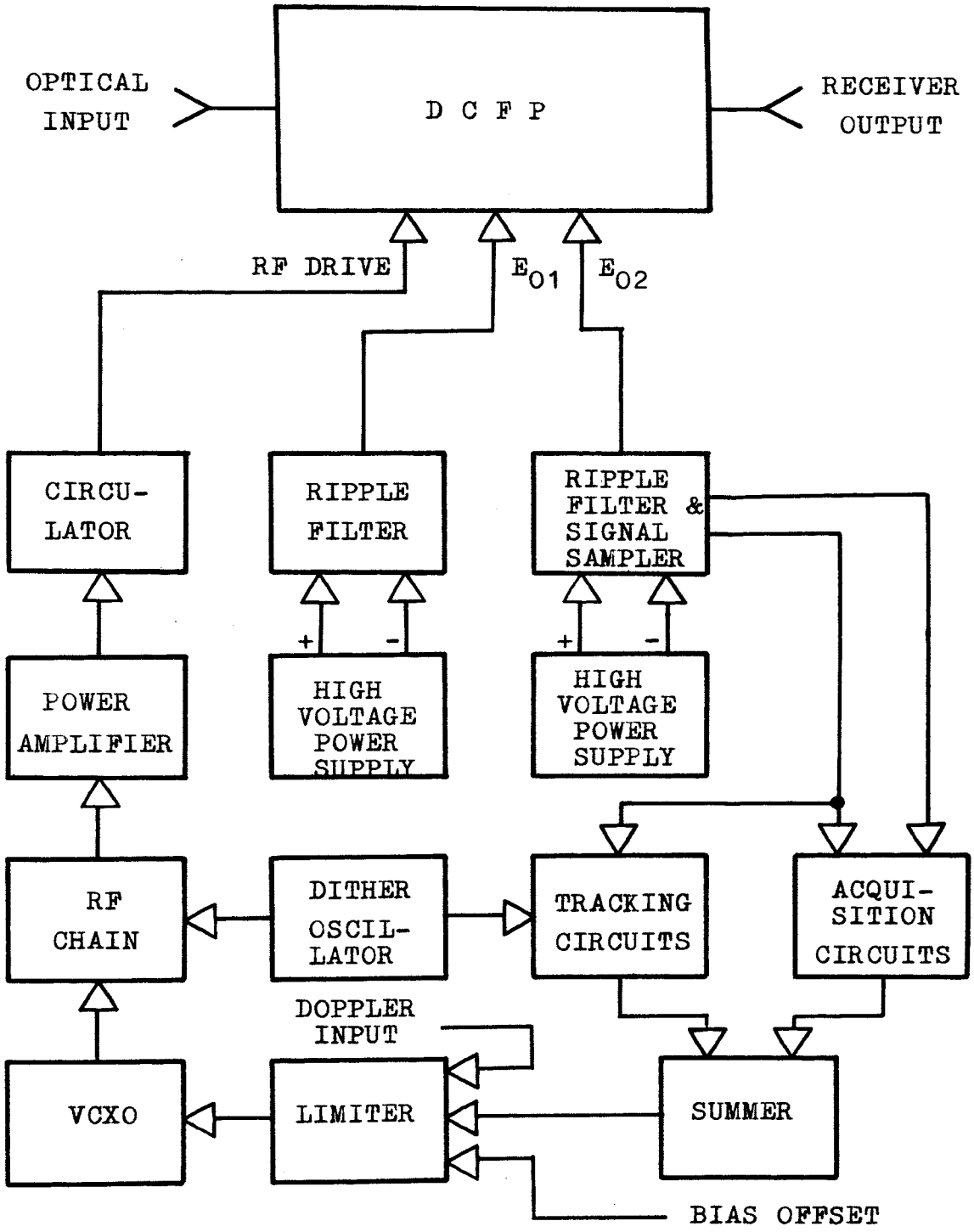


Figure 17. DCFP synchronization loop block diagram.

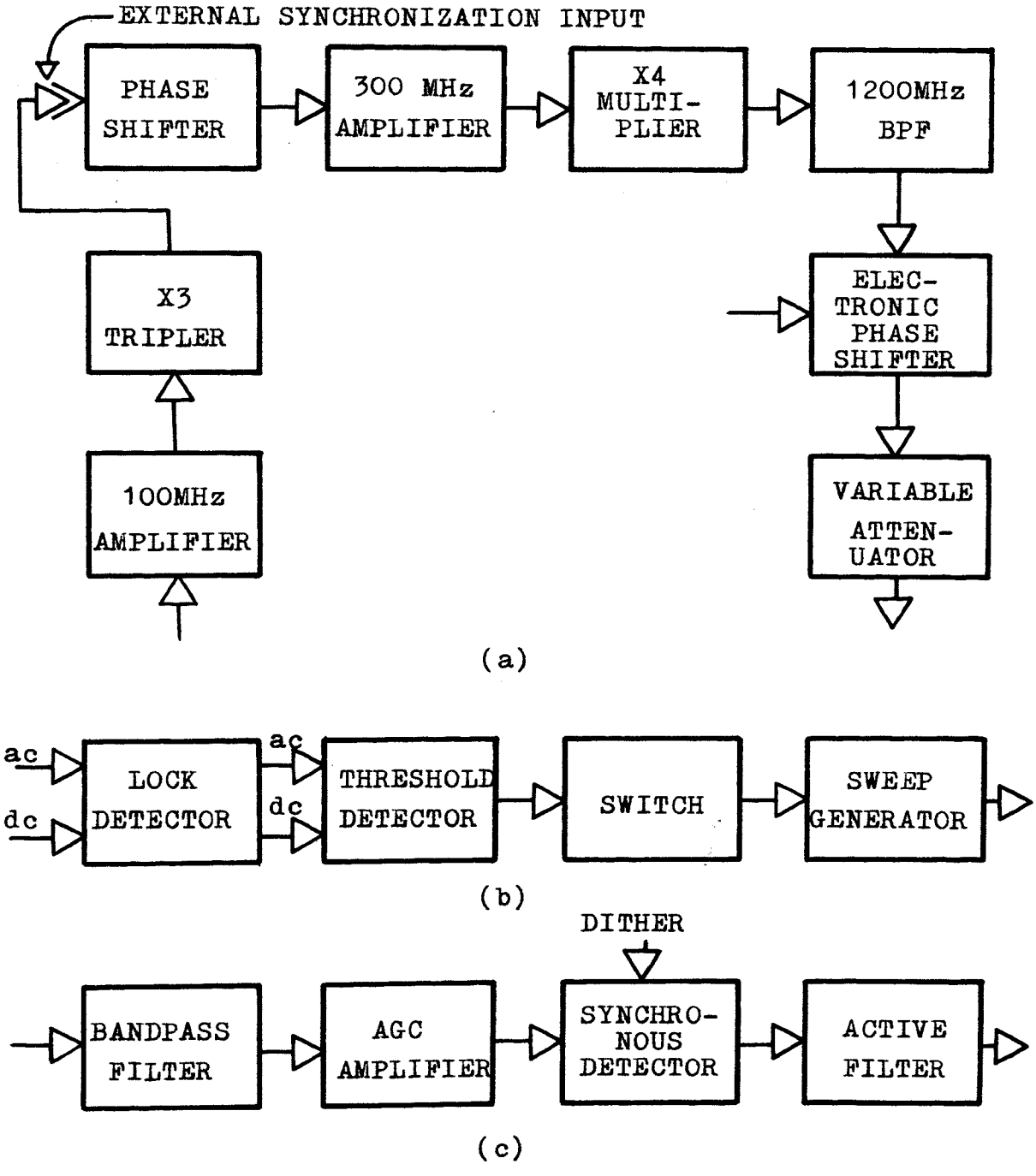


Figure 18. Detailed block diagram a). The RF chain b). The acquisition circuits. c). The tracking circuits.

where .300/2 is the signal peak value set by the AGC amplifier, $\pi/2$ is the maximum phase shift, and .53 is the double balanced mixer gain.

$$F(0) = \frac{R_3}{R_1}\frac{R_5}{R_4}\frac{R_8}{R_7}\frac{R_{14}}{R_{13}+R_{14}}$$

$$F(0) = \frac{680K}{10K}\frac{51K}{30K}\frac{10K}{910}\frac{1K}{1K+1K}$$

$$F(0) = 68x1.7x11x\tfrac{1}{2}$$

$$F(0) = 635$$

where the resistor values referred to are shown on the schematic of Figure 15, and the values were derived in the design section.

$$K = K_o K_d F(0)$$

$$K = 7.55x10^5 x5.06x10^{-2} x6.35x10^2$$

$$K = 2.43x10^7$$

This value for the loop gain compares favorably with the desired design value of $2.4x10^7$.

2. The Loop Bandwidth

The synchronization loop bandwidth may be found from the following relationship

$$\omega_n = \sqrt{K/\tau_1}$$

where τ_1 is the lag break of the lead lag filter. Referring to Figure 15

$$\tau_1 = (R_2+R_3)C_1$$

$$\tau_1 = (2.2\text{x}10^2+6.8\text{x}10^5)(1.0\text{x}10^{-6})$$

$$\tau_1 = 6.8\text{x}10^{-1}$$

$$\omega_n = \sqrt{K/\tau_1} = \sqrt{2.43\text{x}10^7/6.8\text{x}10^{-1}}$$

$$\omega_n = 5.98\text{x}10^3$$

$$f_n = \frac{\omega_n}{2\pi}$$

$$f_n = 0.955\text{KHz}$$

The calculated value of the loop bandwidth, 0.955 KHz, is found to be very close to the original desired value of 1 KHz.

3. The Loop Damping Ratio

The synchronization loop damping ratio is determined by the following equation.

$$\zeta = \tfrac{1}{2}\tau_2\omega_n$$

where τ_2 is the lead break of the lead lag filter. Referring to Figure 15

$$\tau_2 = R_2C_1$$

$$\tau_2 = 2.2\text{x}10^2\text{x}1\text{x}10^{-6}$$

$$\tau_2 = 2.2\text{x}10^{-4}$$

$$\zeta = \tfrac{1}{2}(2.2\text{x}10^{-4})(5.98\text{x}10^3)$$

$$\zeta = .658$$

This calculated value for the loop damping ratio is only about seven percent low.

4. The Static Phase Error

The magnitude of the static phase error may be found from the following relationship

$$\sin \theta_e = \frac{\omega_i - \omega_c}{K}$$

The static phase error was specified for the loop hold in range which was desired to be 40 KHz.

Thus

$$\theta_e = \sin^{-1} \frac{2\pi \times 40 \times 10^3 \times 4}{2.43 \times 10^7}$$

$$\theta_e = \sin^{-1} 4.14 \times 10^{-2}$$

$$\theta_e = 2.4 \text{ degrees}$$

The value of the static phase error is approximately one half of the original specified five degrees. This comes as a result of doubling the DC open loop gain to account for any gain reductions caused by the input power level variations.

5. The Dynamic Phase Error

The dynamic phase error may be found from the following relationship

$$\sin \theta_e = \frac{\Delta \dot{\omega}}{\omega_n^2}$$

The above relationship is really only valid for an infinite gain second order loop. The steady state error due to a swept input frequency is

$$\frac{\Delta\dot{\omega}}{K} \quad \text{radians/sec}$$

as given by Gardner.[8] The accumulated phase error after an elapsed time is

$$\frac{\Delta\dot{\omega}t}{K}$$

The loop will maintain lock as long as this accumulated phase error is less than the maximum allowable phase error of $\pi/2$ radians. The dynamic phase error is

$$\theta_e = \sin^{-1}\frac{\Delta\dot{\omega}}{\omega_n^2}$$

$$\Delta\dot{\omega} = 2\pi \text{x} 1\text{KHz} \text{x} 4/(1/1\text{KHz})$$

$$\Delta\dot{\omega} = 8\pi \text{x} 10^6 \text{ radians/sec/sec}$$

$$\theta_e = \sin^{-1}\frac{8\pi \text{x} 10^6}{(2\pi \text{x}.955\text{x}10^3)^2}$$

$$\theta_e = \sin^{-1}.7$$

$$\theta_e = 44.5 \text{ degrees for } K \rightarrow \infty$$

and the accumulated phase error of $\pi/2$ radians would cause the loop to lose lock after

$$t = \frac{K\pi/2}{\Delta\dot{\omega}} \text{seconds}$$

$$t = \frac{2.43\text{x}10^7 \text{x} \pi/2}{8\pi \text{x} 10^6}$$

$$t = 1.52 \text{ seconds}$$

The present loop can never lose lock due to an accumulated phase error. Even at the maximum dynamic tracking

capability of ω_n^2 or 3.6×10^7 radians/second/second the loop could maintain lock for 1.06 seconds which results in an input frequency change of 3.82×10^7 radians per second or 1.52×10^6 Hz at 300 MHz. This exceeds the loop frequency range of $\pm$40 KHz thus lock would be lost due to saturation of the loop error voltage rather than too large an accumulated phase error.

6. The Hold in Range

The hold in range may be found from the following

$$\omega_H = K \sin \theta_e$$

$$\omega_H = 2.43 \times 10^7 \sin 5^\circ$$

$$\omega_H = 2.12 \times 10^6$$

or for the input signal of 300 MHz

$$f_H = \frac{2.12 \times 10^6}{4 \times 2\pi}$$

$$f_H = 84.3 \text{KHz}$$

This calculated value for the hold in range exceeds the desired value of 40 KHz by more than a factor of 2 and again this was caused by doubling the loop gain to allow for input signal level variations. Before the phase detector could saturate due to a static error, the VCXO error signal would saturate at $\pm$40 KHz (at 300 MHz) corresponding to a phase error of 2.4 degrees.

7. The Lock in Range

The lock in range for the synchronization loop using an active lead lag filter is found to be

$$\omega_l = 2\zeta\omega_n$$

$$\omega_l = 2(0.658)(2\pi x.955x10^3)$$

$$\omega_l = 7.89x10^3$$

or

$$f_l = 1.25KHz$$

or for the 300 MHz input signal frequency

$$f_l = \frac{1.25}{4}KHz$$

$$f_l = 0.314KHz$$

8. The Pull in Range

The synchronization loop pull in range (without any sweep generator) can be found from the following approximation

$$\omega_p = 2\sqrt{\zeta\omega_n K} \quad \text{for} \quad \frac{\omega_n}{K} < 0.4$$

$$\omega_p = 2\sqrt{(0.658)(2\pi)(.955x10^3)(2.43x10^7)}$$

$$\omega_p = 2\sqrt{9.57x10^{10}}$$

$$\omega_p = 6.18x10^5 \text{ radians/sec}$$

or

$$f_p = 98.5KHz$$

or at the 300 MHz input signal frequency

$$f_p = \frac{98.5}{4} \text{KHz}$$

$$f_p = 24.6 \text{ KHz}$$

9. Acquisition Range with a Sweep Generator

The synchronization loop acquisition range with a sweep generator is equal to the frequency range over which the VCXO is swept. The output voltage of the sweep generator is (Referring to Figure 15)

$$V_{out} = V_{sat} \frac{1}{1+\frac{R_{16}}{R_{17}}+\frac{R_{16}}{R_{19}}}$$

$$V_{out} = 14 \frac{1}{1+\frac{9.1K}{2K}+\frac{9.1K}{2K}}$$

$$V_{out} = 1.386 \text{ volts}$$

This voltage is amplified by the following gain before reaching the VCXO

$$V_{out} = 1.386 \frac{R_5}{R_6} \frac{R_8}{R_7} \frac{R_{14}}{R_{13}+R_{14}}$$

$$V_{out} = 1.386 \frac{51K}{110K} \frac{10K}{910} \frac{1K}{1K+1K}$$

$$V_{out} = 3.53 \text{ volts}$$

The magnitude of this sweep voltage is reduced by the magnitude of the voltage limiting of the error signal which

occurs in the first stage of the active filter. The magnitude of this signal was calculated to be 213 millivolts and is multiplied by a gain of 9.35 before reaching the VCXO. Thus the 3.53 volt sweep magnitude should be reduced by 1.99 volts leaving a 1.54 volt sweep magnitude. Thus the acquisition frequency range for the input 300 MHz signal is

$$f_a = (30\text{KHz/volt})(\pm 1.54\text{volt})$$

$$f_a = \pm 46.2\text{KHz}$$

The frequency acquisition range of 46.2 KHz is approximately equal to the desired 40 KHz acquisition range.

10. False Lock

False lock is prevented in the synchronization loop by the combination of three things. First a bandpass filter is used to attenuate the undesirable beatnote signal which caused false lock. Second the range of the VCXO is limited to prevent a beatnote from being generated which is too close to the 1 MHz signal. Third the lock detector will detect false lock (since a beatnote is present during false lock) and the sweep generator will run during false lock. Due to the reduced signal amplitude caused by the bandpass filter as well as the reduced gain of the phase detector the false lock hold in range is reduced over that of true lock and if the sweep generator sweeps sufficiently far, the loop will be swept out of the false lock hold in

range and true lock can then occur.

False lock can only occur at a sub multiple of 1 MHz, that is 1 MHz/N where N is an integer. Theoretically the output of a double balanced mixer is zero for all sub harmonic frequencies of the drive signal. This zero output depends upon the cancellation of large amplitude signals. The extent of this cancellation depends upon the matching of the diodes and the transformer center taps used in the double balanced mixer. Typically the match of the components is adequate to reduce the phase detector gain by an order of magnitude (10x). The bandpass filter attenuates the signals outside the passband by more than 40 db. Also the control signal to the VCXO is amplitude limited to approximately ± 1.8 volts maximum. Thus the highest frequency beatnote which can be generated is 216 KHz allowing false lock to occur at 200 KHz and below. The hold in range, allowing phase detector saturation, is equal to the loop gain. Thus the false lock hold in range is 10^3 less than that for true lock. For false lock

$$\omega_H = K/10^3$$

$$\omega_H = 2.43 \times 10^4 \text{ radians/second}$$

or

$$f_H = 3.87\text{KHz}.$$

As long as the sweep generator sweeps the VCXO further than 3.87 KHz the false lock condition will not be stable.

11. Signal Level Variations

Input optical power level variations will cause the magnitude of the DCFP output dither signal to vary directly as the input power level. The phase detector gain varies directly as the input signal magnitude causing the loop gain to vary with the input optical power level. The AGC amplifier is used to eliminate the low frequency and steady state signal level changes. Thus input signal level change will affect the loop dynamic performance but these signal level changes are limited to two to one changes so the dynamic performance degradation is not severe.

12. Other Design Problems

The acquisition time for the synchronization loop is equivalent to the period of the sweep generator. In addition to the 1 second required for one sweep generator period the lock detector requires some time to determine if lock has occurred and then turn off the sweep generator. This time is approximately one time constant for the filter preceding the threshold detector in the lock detector. This time constant is formed by a .47μF capacitor and a 5.1K resistor or 2.4 milliseconds. Since this filter time constant is short compared to the sweep generator period the acquisition time is determined primarily by the sweep generator period. The maximum acquisition time of 1 sec is equal to the design goal limit of 1 sec nominal.

The sweep generator acquisition was implemented to meet the design goal for both acquisition range and acquisition time. The acquisition range with out a sweep generator (pull in range) was calculated to be 24.6 KHz which is less than the design goal of 40 KHz. The acquisition time without a sweep generator can be found from the approximation for pull in time given by Gardner.[8]

$$t_p \approx \frac{(\Delta\omega)^2}{2\zeta\omega_n^3}$$

where

t_p = the pull in time

$\Delta\omega$ = the initial frequency offset

thus

$$t_p \approx \frac{(40KHzx4x2\pi)^2}{2(0.658)(.955x2\pi x10^3)^3}$$

$$t_p \simeq 3.57 \text{ seconds}$$

This acquisition time of 3.57 seconds is longer that the design goal of 1 second. The design goal for both the acquisition time and range is met with the sweep generator.

A VCXO is used in place of the normal VCO because of the lower noise and inherent higher stability associated with the crystal used in the VCXO. The noise added to the DCFP output by the synchronization loop RF drive signal is a minimum when using a VCXO. Also the stability of the crystal allows the VCXO center frequency to be known accurately. The loop operating frequency range is then a

function of only the input frequency range and is not increased due to the instability of the VCXO.

The synchronization loop is implemented by dithering the phase of the DCFP RF drive at a 1 MHz rate as called out in the design goal. The 1 MHz dither rate was used in lieu of a lower frequency because of the problems associated with false lock. The bandpass filter is easier to implement at a higher dither frequency. Also a very narrow bandwidth for the bandpass filter causes stability problems with the phase-locked loop.

Since the optical receiver is only required to operate in a normal laboratory environment no special design or testing is required to meet environmental specifications such as shock, vibration, acceleration or temperature range.

G. Stability Analysis of the Synchronization Loop

The phase-locked loop used to synchronize the DCFP is a high gain imperfect second order loop. A second order control system is unconditionally stable. This means the loop gain may be increased as much as desired without causing instability. This theoretical performance is not found to be correct for the synchronization loop being considered. Additional poles which were not considered in determining the loop to be unconditionally stable eventually will cause instability as the gain is increased.

A stability analysis of the synchronization phase-locked loop can be performed by evaluation of a log magnitude and phase diagram. This diagram is formed by plotting the magnitude and phase of the open loop gain versus frequency. In addition to the desired open loop transfer function for the second order loop of $G_1(s)$ where

$$G_1(s) = \frac{K_o K_d F(0)}{s} \frac{s\tau_2+1}{s\tau_1+1}$$

the bandpass filter, the AGC amplifier and the three operational amplifier which comprise the loop filter add additional poles to the transfer function.

The bandpass filter is transformed to an equivalent low pass Butterworth response filter by the action of the synchronous detector. The 200 KHz bandpass filter centered at 1 MHz becomes a 100 KHz low pass filter with the following transfer function, $G_2(s)$, where

$$G_2(s) = \frac{(2\pi x10^5)^5}{(s+2\pi x10^5)(s^2+s(1.618)(2\pi x10^5)+(2\pi x10^5)^2)} x \frac{1}{(s^2+s(0.618)(2\pi x10^5)+(2\pi x10^5)^2)}$$

The AGC amplifier consists of a four stage amplifier with each stage having a break frequency at 30 MHz. Since this frequency is so high compared to the frequencies of interest, this response need not be considered in the stability analysis.

The amplifiers which were used in the active filter

have a gain bandwidth product of 3 MHz. The first gain stage has a high frequency closed loop gain of less than unity and as such the bandwidth is in excess of 3 MHz. The second stage with a gain of 1.7 has a pole at 1750 KHz and the third stage with a gain of 11 has a pole at 270 KHz. These three poles have the transfer function, $G_3(s)$, where

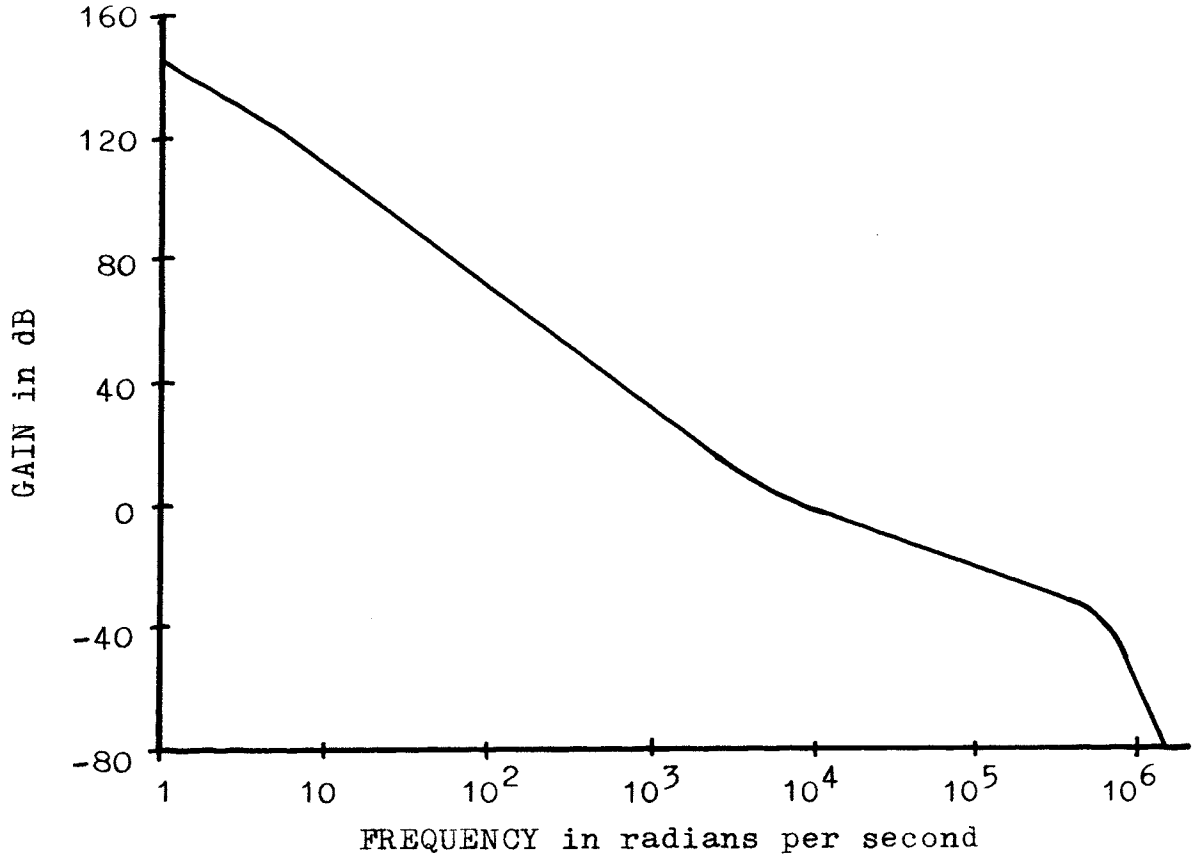
$$G_3(s) = \frac{2\pi x3x10^6}{s+2\pi x3x10^6} \frac{2\pi x17.5x10^5}{s+2\pi x17.5x10^5} \frac{2\pi x2.7x10^5}{s+2\pi x2.7x10^5}$$

The components which comprise the RF chain all have a bandwidth in excess of 5 MHz and thus will not be considered.

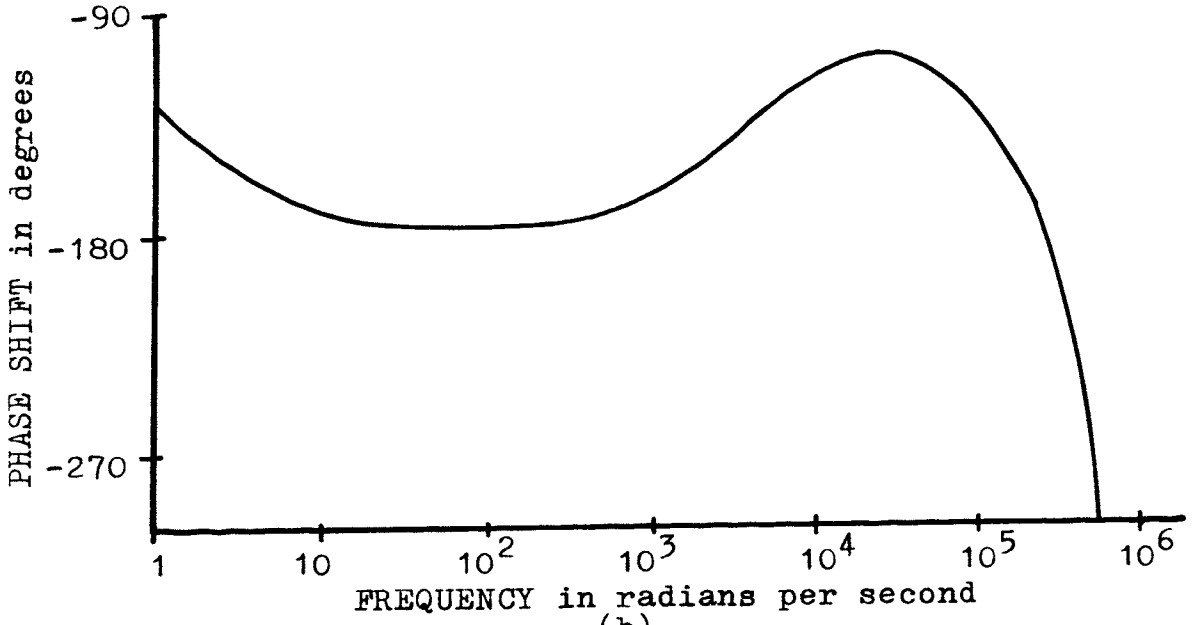
The open loop transfer function can be expressed as G(s), where

$$G(s) = G_1(s)G_2(s)G_3(s)$$

Figure 19 shows the log magnitude and phase diagram for the open loop transfer function. The open loop transfer function has unity gain (Odb) at 10^4 radians per second. The phase shift at this point is -115 degrees giving a phase margin of 180-115 or 65 degrees. 180 degrees of phase shift occurs at $2.7x10^5$ radians per second and at this point the open loop gain is -28 db which gives a loop gain margin of 28 db.



(a)



(b)

Figure 19. Plots for stability analysis. a) Open loop gain versus frequency. b) Open loop phase shift versus frequency.

H. Experimental Results

A receiver was built following the design developed in the design section. The receiver performance was then tested using a frequency doubled (.53 μ meter wavelength) Nd:YAlG laser mode locked at 300 MHz. The following phase-locked loop parameters were measured, static tracking range, static acquisition range, loop bandwidth and damping ratio, transient response to a step input, gain margin, phase margin, and the dynamic tracking capability. In addition the receiver was incorporated into a simulated communication link and bit error rate data was taken as a function of received signal strength.

1. The Static Tracking Range

The static tracking range of the receiver synchronization loop was measured as a function of the received optical power. The VCXO center frequency was adjusted to be within 100 Hz of 100 MHz. Next the mode locked frequency of the laser was varied over the range for which the receiver would maintain lock. The magnitude of the VCXO error signal was observed and the frequency deviation of the mode locked input was calculated using the VCXO gain constant of 10 KHz per volt. These values were then multiplied by 3 to obtain the deviation at 300 MHz. This static tracking range or phase-locked loop hold in range was measured for optical input powers of 20, 60, 200, and 1800

photoelectrons per pulse. (20 photoelectrons per pulse corresponds to approximately 320 photons or about 35 nanowatts.) The experimental results are summarized in Table I.

The minimum hold in range of 48 KHz exceeds the design goal of 40 KHz. The magnitude of the hold in range is determined by the voltage limiting in the output amplifier of the synchronization loop. This voltage limiting was included to eliminate problems associated with false locking of the synchronization loop to a sub harmonic of the dither frequency.

2. The Static Acquisition Range

The static acquisition range of the synchronization loop was measured as a function of the optical input power. The input optical signal level was set to the desired value. The optical beam was interrupted and the mode locked frequency of the laser was then set. The error signal to the VCXO was observed as the obstruction in the optical path was removed. If the synchronization loop acquired in the first sweep (less than one second), the beam was again blocked while the mode locked frequency was incremented. The error signal to the VCXO was again observed as the beam was unblocked to see if the loop acquired during the first sweep. This procedure was repeated until the receiver no longer acquired on the first sweep. The last frequency offset (magnitude of error signal times

Table I.

Synchronization loop measured static tracking frequency range as a function of optical input power.

OPTICAL INPUT photoelectrons per pulse	ERROR SIGNAL MAGNITUDE volts	INPUT FREQUENCY DEVIATION killohertz
20	-1.6	+48
20	+1.6	-48
60	-1.7	+51
60	+1.7	-51
200	-1.8	+54
200	+1.7	-51
1800	-1.8	+54
1800	+1.7	-51

30 KHz per volt) was then recorded as the static acquisition range for that optical power level. This measurement was repeated for frequency deviation both above and below the VCXO center frequency at various input optical powers. The results of these measurements are included in Table II.

The minimum static acquisition range of 33 KHz is 17.5 percent less than the design goal of 40 KHz. As the input signal level increased, the acquisition range decreased and shifted towards frequencies above 300 MHz. The receiver gain was left constant during the testing and at the large input signal levels the DCFP saturated. The large number of electrons in the last secondary emission multiplication steps loaded the internal electric field and caused space charge limiting of the peak dynode current. This changed the DCFP output convolution characteristics with the valley areas being amplified more than the peak areas resulting in an apparent flattening of the curve.

The lock detector functions by comparing the relative magnitude of the AC and DC components of the dynode current. The ratio of these magnitudes is proportional to the flatness of the convolution curve. The flattening of the convolution curve as the DCFP saturated decreased the AC to DC dynode current ratio affecting the proper operation of the lock detector. In addition the circuitry used to full wave rectify the AC dynode current suffers a decrease in gain as the frequency of the beatnote increases

Table II.

Synchronization loop measured static acquisition frequency range as a function of optical input power.

OPTICAL INPUT photoelectrons per pulse	ERROR SIGNAL MAGNITUDE volts	INPUT FREQUENCY DEVIATION killohertz
20	-1.4	+42
20	+1.3	-39
60	-1.7	+51
60	+1.6	-48
200	-1.7	+51
200	+1.5	-45
800	-1.7	+51
800	+1.1	-33
1800	-1.5	+45
1800	+1.1	-33

due to a limited gain bandwidth product of the amplifier used. The combination of the reduced AC component input coupled with the high frequency gain reduction caused the lock detector to indicate lock improperly turning off the sweep generator which prevents acquisition from occurring.

The acquisition range shift towards frequencies above 300 MHz at large input levels was caused by the AGC amplifier. An excess static phase shift of the dither signal occurred in the AGC amplifier as the magnitude of the input dither signal increased due to the DCFP dynode current increase. This static phase shift biased the available error signal in the direction towards higher frequencies. With this additional bias, the sweep generator no longer swept the VCXO frequency with in the loop lock in range for frequencies more than 33 KHz below the 300 MHz VCXO center frequency.

3. The Loop Bandwidth and Damping Ratio

The frequency response of the synchronization loop was measured as a function of received optical power. This test was performed by modulating the laser frequency at a variable rate. The actual laser frequency deviation was kept small, 330 Hz, to ensure that the loop dynamic tracking capability was not exceeded for any frequency rate of interest. The loop response was determined by measuring the error signal to the VCXO and converting this to equivalent frequency deviation by using the gain constant

of the VCXO. Figure 20 shows a graph of the loop frequency response.

The increased amount of peaking in the response as the optical power was reduced is due to a decrease in the loop damping ratio. This was caused by a reduction of the loop gain as a result of a non perfect AGC amplifier. The phase detector gain is directly proportional to the output voltage amplitude of the AGC amplifier. As the input optical power was decreased, the input signal to the AGC amplifier decreased, resulting in a somewhat reduced AGC amplifier output.

Both the loop bandwidth and the loop damping ratio are proportional to the square root of the loop gain. Table III shows how the bandwidth and damping ratio change with the input optical power. These parameters were calculated from Figure 20 using the following equations[12]

$$\omega_m = \omega_n\sqrt{1-2\zeta^2}$$

$$M_m = \frac{1}{2\zeta\sqrt{1-\zeta^2}}$$

where

ω_m = the frequency where the maximum occurs

M_m = the per unit peak value of the response curve

The loop bandwidth varies from 19 percent above to 28 percent below the design value of 1 KHz. The damping ratio varies from 22 to 46 percent below the design value

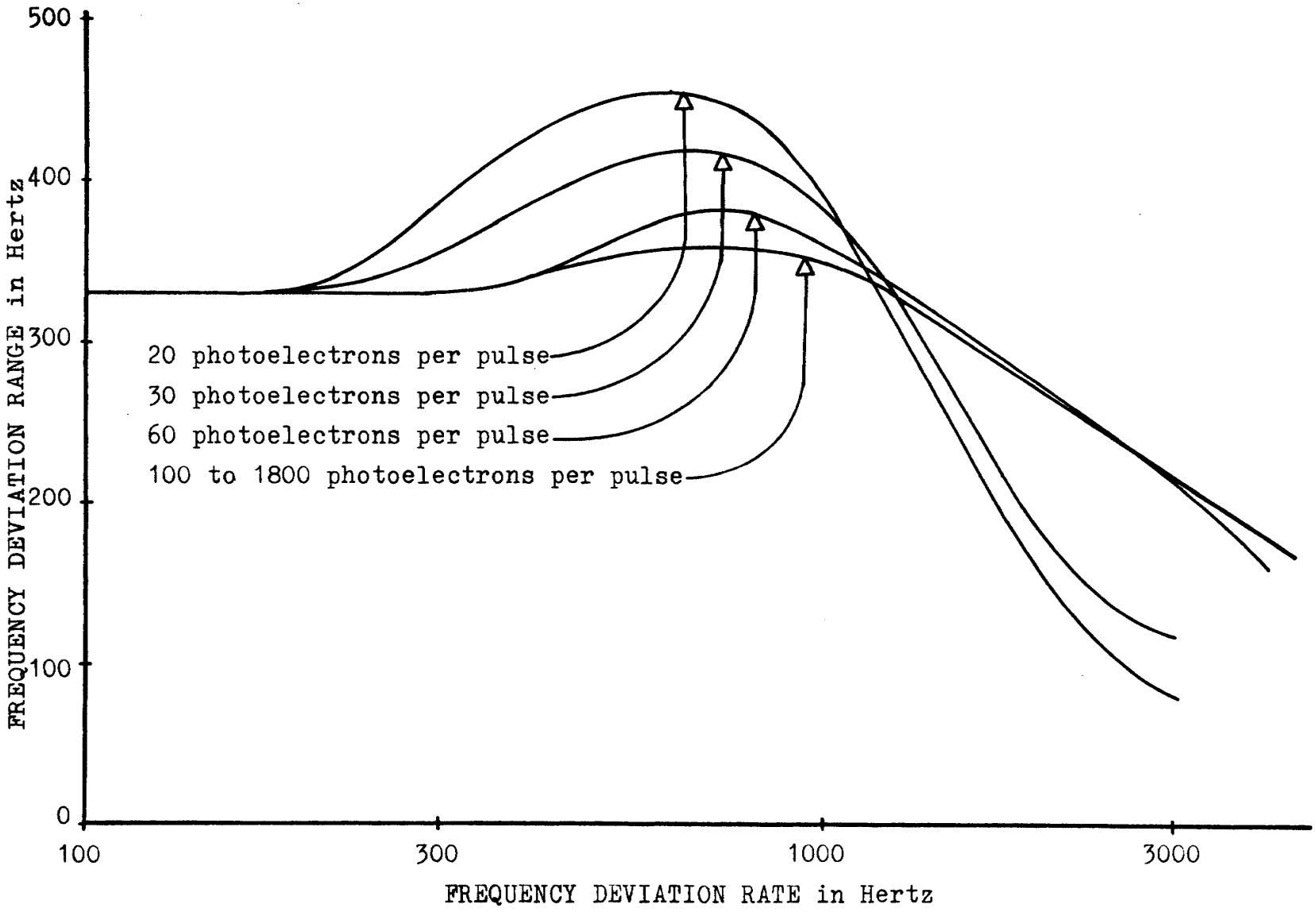


Figure 20. Synchronization loop measured closed loop frequency response as a function of optical power.

Table III.

Synchronization loop calculated bandwidth and damping ratio from the frequency response measurements of Figure 20 at various input optical power levels.

INPUT OPTICAL POWER	M_m	f_m Hertz	ζ	f_n Hertz
photo-electrons per pulse	per unit maximum value	frequency where maximum occurs	damping ratio	loop bandwidth
20	1.38	600	.39	720
30	1.27	670	.44	855
60	1.15	750	.50	1060
100	1.09	750	.55	1190
200	1.09	750	.55	1190
800	1.09	750	.55	1190
1800	1.09	750	.55	1190

of 0.707.

4. The Transient Response to a Step Input

The synchronization loop was subjected to a series of alternating positive and negative frequency steps. This was accomplished by modulating the laser repetition rate with a low frequency square wave. The error signal input to the VCXO was monitored and the peak overshoot was measured as a function of incident optical power. Table IV shows the measured value of the peak overshoot for various optical power inputs.

The loop damping ratio was calculated by using a graphical solution for the following equation[12]

$$M_p = 1+e^{-\zeta\pi/\sqrt{1-\zeta^2}}$$

where

M_p = the peak magnitude of the transient response for a step input

This calculated damping ratio is also shown in Table IV. The decreasing damping ratio with decreasing input power was due to a decreasing loop gain. The amplitude of the dither signal output of the DCFP is directly related to the incident optical power when the DCFP is operating below saturation. The AGC amplifier for the dither signal did not have adequate gain to maintain a constant output signal level. The synchronization loop gain via the phase detector gain is proportional to the square root of the

Table IV.

Calculation of the synchronization loop damping ratio showing the effects of loop gain variation from the loop step response as a function of optical input power.

OPTICAL INPUT POWER photo-electrons per pulse	STEP RESPONSE OVERSHOOT	M_p per unit peak value	ζ calculated damping ratio	ζ^2	ζ^2 x 7.81×10^2	PERCENT DEVIATION
20	1.8/3.0	1.600	0.16	0.0256	20	0
30	1.5/3.0	1.500	0.215	0.0463	36.2	+20.6
40	1.2/3.0	1.400	0.28	0.0785	61.4	+53.5
60	1.1/3.0	1.367	0.305	0.093	72.5	+20.8
100	1.0/3.0	1.333	0.33	0.109	85.3	-14.7
200	0.5/3.0	1.167	0.495	0.245	191	-4.5
800	0.3/3.0	1.100	0.59	0.348	272	-
1800	0.3/3.0	1.100	0.59	0.348	272	-

amplitude of the dither signal out of the AGC amplifier. The equation illustrating this was presented in section III. D. 2. b. iii. and is as follows

$$\zeta = \tfrac{1}{2}\tau_2\sqrt{K_o K_d F(0)/\tau_1}$$

If the calculated value of ζ is squared and normalized this should be directly proportional to the input optical power. This calculation was performed and is presented in Table IV. The magnitude of ζ^2 was normalized to 20 for the optical input of 20 photoelectrons per pulse. The results agree fairly well from 20 to 200 photoelectrons per pulse. The percent deviation was calculated and found to be as high as 53.5 percent at 40 photoelectrons per pulse. This discrepancy is probably due to poor calibration of the laser incident power level. While conducting these tests the laser amplitude exhibited two to one variations at a sub one hertz rate. This amplitude variation explains the discrepancy between the calculated and measured results.

When the magnitude of the loop damping ratio calculated from the overshoot of the step response is compared to that calculated from the peaking in the loop frequency response (preceeding section) the behavior is similar but the magnitudes vary. The calculated damping ratios where the AGC amplifier had adequate gain to function properly agrees fairly well, .59 versus .55, but the damping ratios for minimum input signal vary significantly, .16 versus

.39. One explanation for the different damping ratios is that the magnitude of the dither signal out of the AGC amplifier was different for the two experiments even though the input optical power was the same. At a given optical power level the amount of the DCFP output dither signal is proportional to the magnitude of the amplitude modulation on the output pulses. This amplitude modulation is proportional to the DCFP gain, the magnitude of the RF drive phase dither, and the shape of the laser pulse - DCFP gating convolution curve (the convolution curve slope about the operating point). An attempt was made to hold all of these parameters constant throughout the experimental testing although the parameters were not monitored.

During the testing it was noted that the laser output power was fluctuating considerably. Part of this output power variation could have been caused by a variation in the laser pulse width due to improper adjustments of the end mirror position in the optical cavity. If the laser pulse width increased during the testing, the DCFP convolution curve slope magnitude would decrease (the curve would become flatter). This would result in a decrease in the magnitude of the dither signal thus accounting for the discrepancy in the calculated values of the loop damping ratio.

5. The Gain Margin

An additional amplifier was inserted in the synchronization loop and used to measure the loop gain margin. The amplifier had a bandwidth of 1 MHz, and variable gain (in discrete steps). The amplifier was inserted ahead of the VCXO error signal input and the proper voltage limiting circuitry was added to the amplifier output to prevent false locking problems and damage to the VCXO.

The loop remained stable with a gain increase of 12.5. When the gain was further increased to 25 the synchronization loop broke into oscillation at approximately 50 KHz. The measured gain margin for an additional gain of 25 or 28 db compares very well with the calculated gain margin of 28 db. The synchronization loop was calculated to have 180 degrees of phase shift at 2.7×10^5 radians per second, 43 KHz, and this frequency compares favorably with the 50 KHz measured frequency of oscillation.

6. The Phase Margin

The synchronization loop phase margin was not directly measured but a test was performed giving a relative measure of the accuracy of the calculated phase margin. The amplifier which was used to measure the loop gain margin was again used at the same location in the loop. This time the amplifier gain was set to 1.25, approximately 2 db, (the closest available value to unity gain). The amplifier

bandwidth was decreased from 1 MHz in discrete steps until the synchronization loop started oscillating. With an amplifier bandwidth of 3 KHz the loop was stable and when the bandwidth was decreased to 1 KHz the loop broke into oscillation at a frequency of 1.2 KHz.

The loop was calculated to have a 65 degree phase margin at 10^4 radians per second. Taking into account the 2 db change in gain gives a phase margin of 67 degrees at a frequency of 1.2×10^4 radians per second. The 1 KHz break frequency of the amplifier produces 50.2 degrees of phase shift at 1.2 KHz or 7.55 K radians per second. At 7.55 K radians per second the original loop had a gain of 3 db and a phase margin of 57 degrees. The addition of the 2 db gain and 50 degrees of phase shift caused the loop to oscillate with 5 db of gain and -173 degrees of phase shift which is reasonably close to the criteria for oscillation of 0 db gain and -180 degrees of phase shift (a loop gain of -1). These close results add experimental support to the accuracy of the log magnitude (gain) and phase shift versus frequency curves which were used to calculate the 65 degree phase margin.

7. The Dynamic Tracking Capability

The dynamic tracking capability of the synchronization loop was measured as a function of the received optical power by observing the error signal to the VCXO while frequency modulating the laser. The rate of the modulation

was varied in a 1, 3, 5, 7, 10, etc. sequence and the maximum range of frequency variation over which the loop would maintain lock was measured. This test was performed where the VCXO center frequency x3 was equal to the laser frequency and also where the laser had an initial static offset of 30 KHz both above and below 300 MHz. These results are presented in Tables V., VI., and VII. Figures 21, 22, and 23 show the graphs of this dynamic tracking data.

Above the 100 photoelectron per pulse level the three families of curves are fairly consistent. At the low frequency rates the frequency range is reduced for the cases with the static frequency displacement, but this is to be expected due to the limited dynamic range of the VCXO error signal. As the number of photoelectrons per pulse decrease, the dynamic tracking capability also decreases due to the reduced bandwidth and damping ratio caused by the lower loop gain. The measured dynamic tracking capability is fairly consistent among the three families of curves with the exception of the 30 and 60 photoelectrons per pulse levels for the 300 MHz input frequency (Figure 21). These two curves cross which is not correct. Also for the 300.03 MHz input, the curves for the 60 photoelectron per pulse input falls below the curves for the 20 and 30 photoelectron levels. These discrepancies were probably caused by undetected changes in the input power level due to instability of the laser.

Table V.

Synchronization loop dynamic tracking capability indicating input frequency range versus rate at various input optical power levels for an input frequency of 300.00 MHz.

FREQUENCY RATE in Hertz	MAXIMUM FREQUENCY TRACKING RANGE in killohertz						
	1800 photo-electrons per pulse	800 photo-electrons per pulse	200 photo-electrons per pulse	100 photo-electrons per pulse	60 photo-electrons per pulse	30 photo-electrons per pulse	20 photo-electrons per pulse
1	84	84	76	76	72	84	30
3	84	84	72	66	60	60	30
5	72	72	72	60	42	48	24
7	72	72	66	60	30	42	12
10	72	72	66	54	24	30	6
30	48	48	36	24	12	12	2.4
50	30	30	24	12	6	6	1.8
70	24	24	18	9	4.8	4.8	1.2
100	15	18	12	6	4.2	3.6	0.72
300	6	6	4.5	1.8	1.2	0.36	0.12
500	3.6	3.6	3.0	1.2	0.9	0.12	.096
700	2.4	2.4	2.4	0.9	0.6	0.09	.057
1000	2.4	2.4	2.4	0.9	0.6	.066	.045
2000	2.1	2.1	1.8	0.6	0.3	.015	-
3000	1.8	1.5	1.2	0.45	0.24	.006	-
5000	1.05	1.05	0.9	0.24	0.12	.003	-

Table VI.

Synchronization loop dynamic tracking capability indicating input frequency range versus rate at various input optical power levels for an input frequency of 300.03 MHz.

FREQUENCY RATE in Hertz	MAXIMUM FREQUENCY TRACKING RANGE in killohertz						
	1800 photo-electrons per pulse	800 photo-electrons per pulse	200 photo-electrons per pulse	100 photo-electrons per pulse	60 photo-electrons per pulse	30 photo-electrons per pulse	20 photo-electrons per pulse
1	48	48	45	42	33	33	33
3	48	48	42	33	24	33	33
5	42	42	33	27	21	30	30
7	39	39	30	24	18	24	24
10	33	36	27	21	15	21	18
30	24	24	18	12	6	12	12
50	21	21	12	7.5	3	6.0	6.0
70	18	15	9	5.1	1.5	3.75	3.6
100	12	12	7.5	2.4	1.2	3.0	2.7
300	5.4	6.0	2.7	1.2	0.6	1.2	1.2
500	3.0	3.0	1.8	0.75	0.45	0.60	0.60
700	2.4	2.4	1.2	0.60	0.45	0.60	0.45
1000	2.4	2.4	1.2	0.60	0.36	0.60	0.42
2000	1.8	1.8	0.9	0.30	0.18	0.30	0.18
3000	1.35	1.5	0.6	0.21	0.09	0.15	0.12
5000	0.84	0.84	0.36	0.12	-	-	-

Table VII.

Synchronization loop dynamic tracking capability indicating input frequency range versus rate at various input optical power levels for an input frequency of 299.97 MHz.

FREQUENCY RATE in Hertz	MAXIMUM FREQUENCY TRACKING RANGE in killohertz						
	1800 photo-electrons per pulse	800 photo-electrons per pulse	200 photo-electrons per pulse	100 photo-electrons per pulse	60 photo-electrons per pulse	30 photo-electrons per pulse	20 photo-electrons per pulse
1	42	42	42	39	39	24	21
3	42	42	42	33	24	21	18
5	39	39	39	27	21	18	15
7	36	36	36	24	18	15	12
10	33	33	33	21	15	12	10.5
30	24	24	24	15	10.5	4.8	4.5
50	21	21	21	10.5	6.0	3.6	3.0
70	18	19.5	18	7.5	4.5	2.4	2.4
100	15	15	15	4.5	3.0	1.5	1.5
300	4.5	6	6	2.4	1.5	0.9	0.6
500	3.75	3.75	3.75	1.8	1.2	0.51	0.3
700	3.0	3.0	3.0	1.2	0.6	0.45	0.3
1000	2.4	2.4	2.4	1.2	0.6	0.39	0.24
2000	1.8	1.8	1.8	0.9	0.33	0.21	0.12
3000	1.5	1.5	1.5	0.6	0.21	0.12	0.03
5000	0.9	0.9	0.9	0.3	0.15	-	-

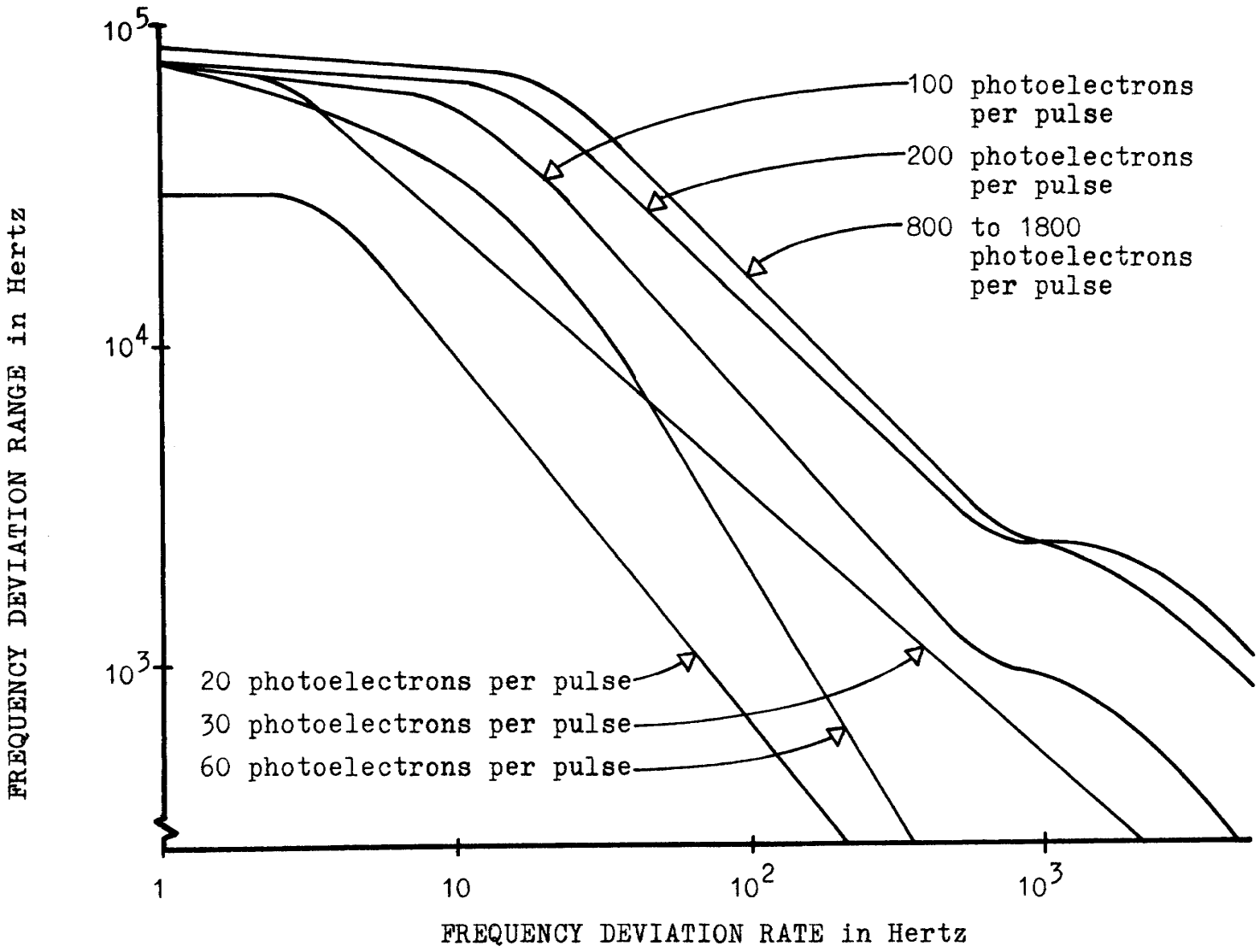


Figure 21. Synchronization loop measured dynamic tracking capability showing the input frequency deviation range versus rate at various optical power levels for an input frequency of 300.00MHz.

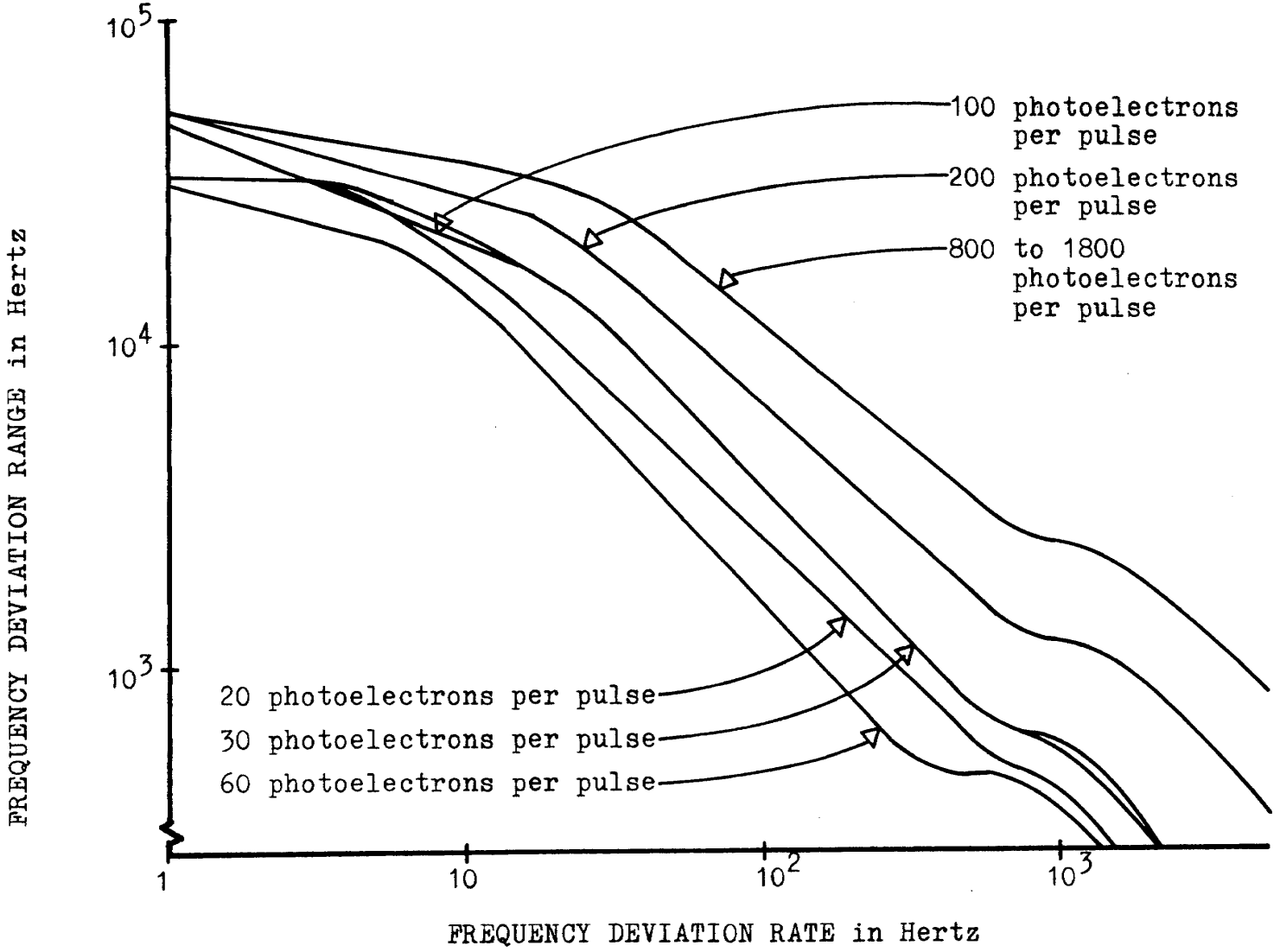


Figure 22. Synchronization loop measured dynamic tracking capability showing the input frequency deviation range versus rate at various optical power levels for an input frequency of 300.03 MHz.

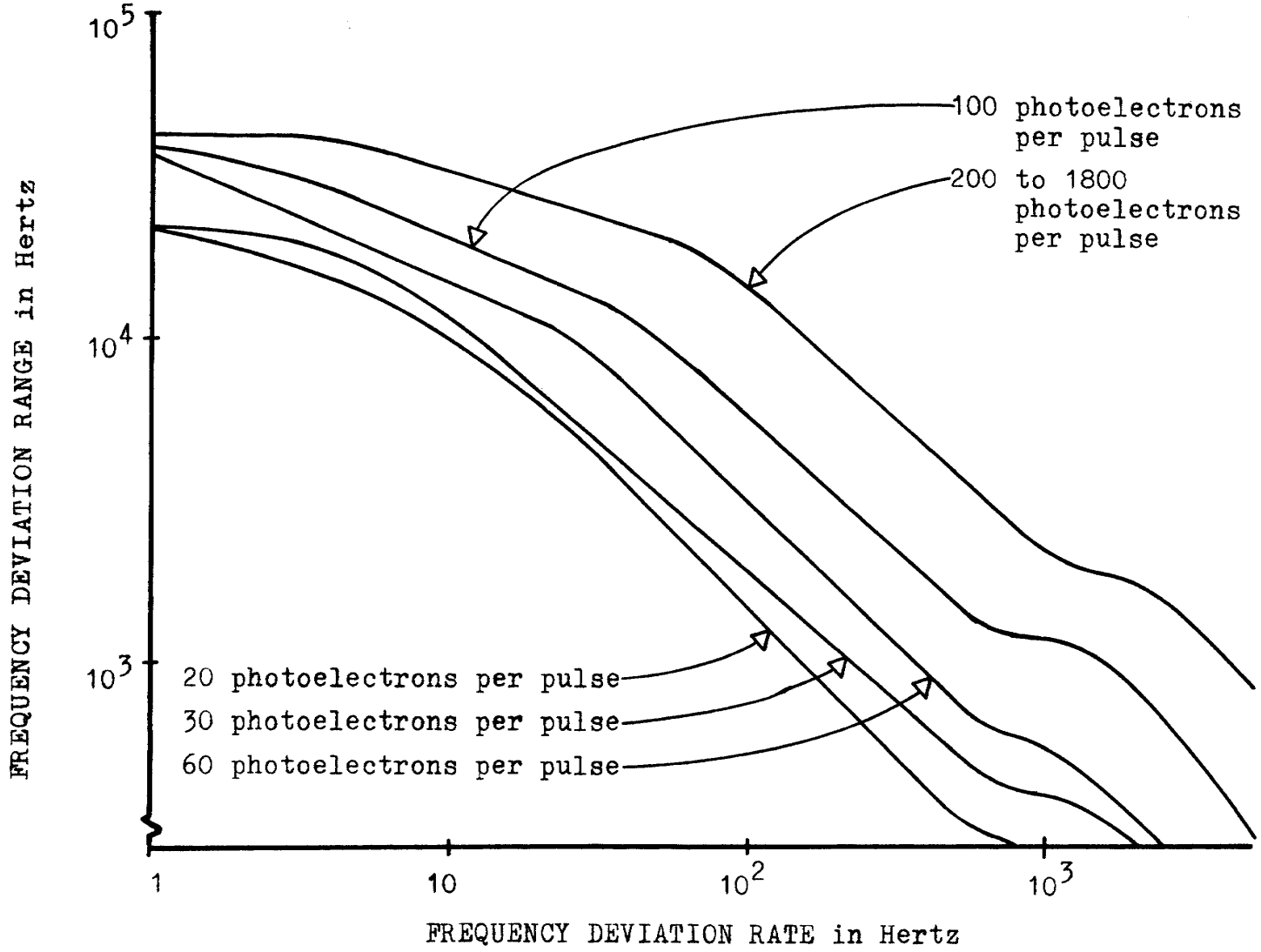


Figure 23. Synchronization loop measured dynamic tracking capability showing the input frequency deviation range versus rate at various optical power levels for an input frequency of 299.97 MHz.

The dynamic tracking frequency range for several frequency rates was derived from the curve for the 300 MHz laser frequency (Figure 21) and used to determine the minimum loop bandwidth required for this performance. This was done for the complete family of curves for the different input optical powers. For the loop to maintain lock

$$\Delta\dot{\omega} \leq \omega_n^2$$

Therefore the loop bandwidth must be greater than the square root of the rate of change of the input frequency ($\Delta\dot{\omega}$). The magnitude of $\Delta\dot{\omega}$ is given by

$$\Delta\dot{\omega} = \frac{\text{input frequency change}}{\text{length of time required for change}}$$

The laser modulating waveform was triangular which results in the length of time required for the frequency change being equal to one half the triangular wave period.

$$\Delta\dot{\omega} = \frac{\text{input frequency change}}{\frac{1}{2} \text{ the triangular wave period}}$$

This is equivalent to

$$\Delta\dot{\omega} = 2\text{x frequency range x}2\pi\text{ x frequency rate}$$

The frequency range is the input frequency change. The frequency rate refers to the laser modulating rate or the triangular waveform frequency. The frequency range in Figure 21 refers to 300 MHz, therefore, these values must be multiplied by 4 to reflect the rate of change of the input signal at 1200 MHz resulting in

$$\Delta\dot{\omega} = 8x \text{ frequency range } x2\pi x \text{ frequency rate}$$

$$\omega_n > \sqrt{16\pi \text{ x frequency range x frequency rate}}$$

The magnitude of the calculated bandwidth is presented in Table VIII.

The calculated equivalent loop bandwidth for the high input optical powers (200 photoelectrons 1190 to 1350 Hz) compares favorably to the bandwidth measured from the frequency response (1190 Hz at 200 photoelectrons, Table III.) and also for the calculated bandwidth of 955 Hz (Section F. 2).

At the low input optical power levels, the inadequate gain in the AGC amplifier caused a decrease in the synchronization loop gain. The loop bandwidth is proportional to the square root of the gain, therefore, the 1300 Hz bandwidth at 200 photoelectrons should reduce to $1300/\sqrt{10}$ or 411 Hz at 20 photoelectrons. The calculated bandwidth at the 20 photoelectron level was 300 Hz. This additional decrease in the loop bandwidth was probably due to poor loop transient response as a result of the decreased damping ratio. This decreased damping ratio occurred because the damping ratio is directly proportional to the square root of the loop gain.

The synchronization loop would acquire at slightly less ($> \frac{1}{2}$) than the maximum dynamic tracking capability. This agrees with the acquisition results summarized by Gardner[8] showing the probability of acquisition as a

Table VIII.

Calculation of the minimum equivalent synchronization loop bandwidth from the measured dynamic tracking capability at 300.00 MHz.

NUMBER of photo-electrons per pulse	SWEEP RATE Hertz	SWEEP RANGE kilo-hertz	16 x RANGE x RATE MHz/sec^2	ω_n Radians/ Second	f_n in Hertz
20	30	2.6	3.92	1980	315
	100	0.54	3.22	1795	286
	300	0.18	2.72	1650	262
30	30	12	18.1	4255	677
	100	1.9	9.55	3090	492
	300	0.35	5.28	2300	366
60	30	9	13.6	3690	587
	100	3.4	17.1	4140	658
	300	1.4	21.1	4595	730
100	30	22	33.2	5760	916
	100	6.4	32.2	5680	905
	300	2.0	30.2	5500	875
200	30	37	55.8	7470	1190
	100	13	65.4	8080	1285
	300	4.8	72.4	8500	1350
800 TO 1800	30	48	72.4	8500	1350
	100	16	80.5	8980	1430
	300	5.6	84.5	9200	1465

function of the sweep rate. As the sweep rate is increased, the probability of acquisition goes from 1 to 0 as the sweep rate goes from $.5\omega_n^2$ to ω_n^2.

The synchronization loop meets the desired dynamic tracking capability of a 1 KHz range at a 1 KHz rate when the input signal is above 150 photoelectron per pulse. Even though the design goal is not met for lower input signals the loop still acquires and tracks the test laser which indicates that possibly the design goal was set higher than that required.

8. Measured Error Rates

A communication link was set up using a 300 MHz mode locked ND:YAlG frequency doubled laser, a 300 Mbps (Mega bits per second) electrooptic modulator, and the optical receiver. The transmitted data consisted of a 63 bit pseudorandom noise or pn code. The transmitted information was reconstructed by using a threshold detector following the DCFP output. This threshold detector, included as part of the receiver, decides whether a "1" or a "0" was transmitted by comparing the received signal to a reference threshold level. This threshold level is adjusted to produce the minimum error rate.

The reconstructed data output of the receiver was digitally compared to the transmitted data in an error rate comparator (essentially an exclusive or gate followed by

a flip flop). The number of errors was then measured by a gated counter.

The error rates were measured for various input power levels and at different background (noise) levels. The results are presented in Table IX. Figures 24, 25, and 26 show the measured error rates plotted along with the theoretical error rate.

The deviation between the theoretical and experimental results at the high input power levels is explained partly by use of a nonideal modulation. The modulator extinction ratio or the ratio of the transmitted one to zero was nonideal and was observed to vary at different points in the pn code.

Part of the deviation can also be attributed to the stability of the laser. At low signal levels the laser output was stabilized by using an AGC circuit which was removed to conduct the test at higher input powers due to the high insertion loss of the AGC circuitry.

A similar error rate test was conducted at much higher power levels using a photodiode in place of the DCFP optical receiver. A similar deviation between theoretical and experimental results occurred. This essentially eliminated the receiver as the cause of the discrepancy.

The experimental testing indicated that almost no degradation in the communication link may be attributed to the receiver or the phase dither synchronization.

Table IX.

Measured error rate data for the optical receiver for various levels of input signal versus background level.

INPUT OPTICAL POWER photoelectrons per pulse	BACKGROUND POWER photoelectrons per pulse	MEASURED ERROR RATE errors/bit
20	0	1.0×10^{-3}
20	.4	1.2×10^{-3}
20	4	3.0×10^{-3}
30	0	8.0×10^{-5}
30	.4	1.2×10^{-4}
30	4	2.7×10^{-4}
40	0	4.1×10^{-5}
40	.4	5.6×10^{-5}
40	4	8.0×10^{-5}
60	0	5.1×10^{-6}
60	.4	5.8×10^{-6}
60	4	1.4×10^{-5}
100	0	5.6×10^{-7}
100	.4	6.2×10^{-7}
100	4	8.5×10^{-7}
200	0	2.2×10^{-8}
200	.4	3.0×10^{-8}
200	4	5.3×10^{-8}

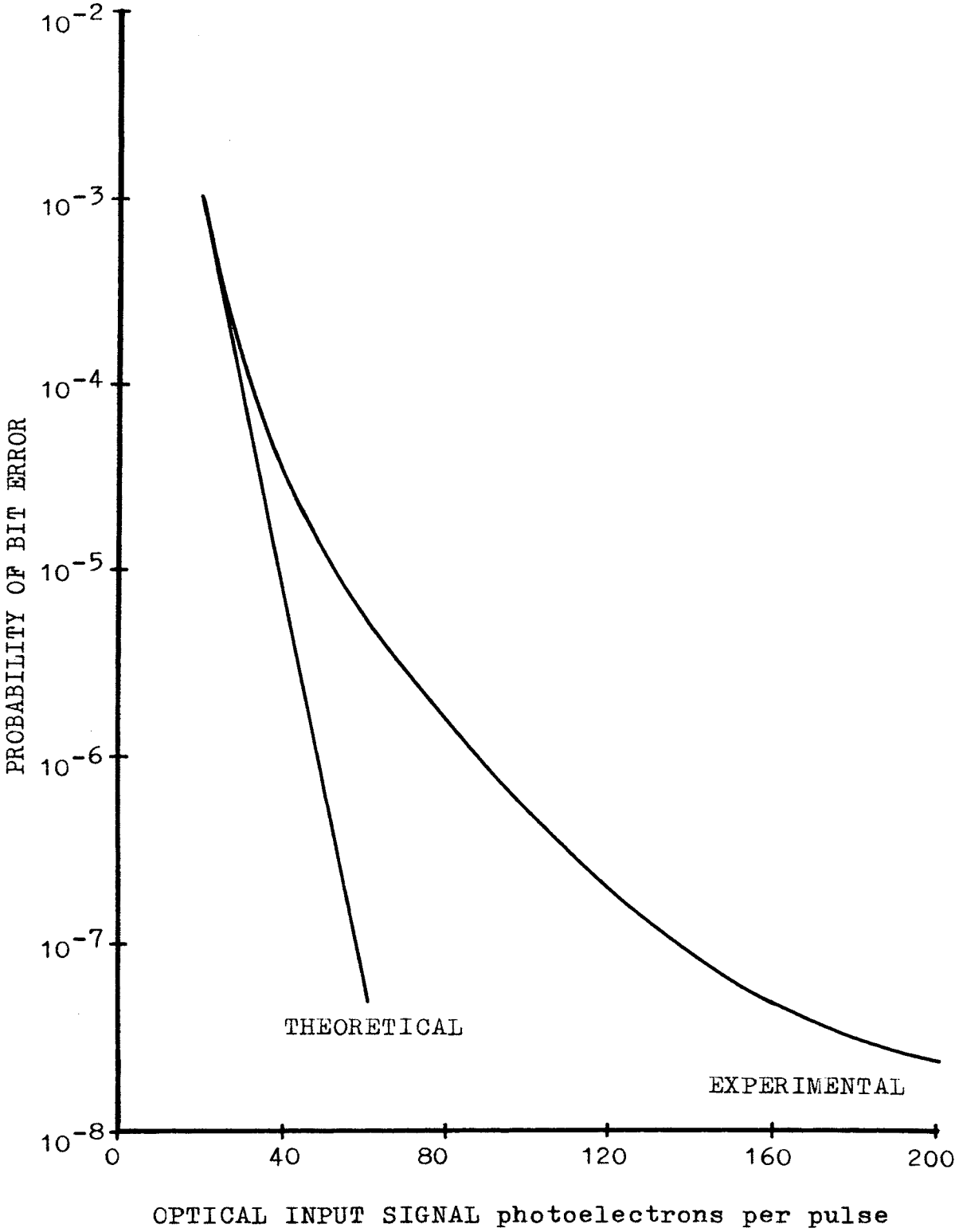


Figure 24. Optical receiver measured bit error rate for an average modulator extinction ratio of 10 to 1 with no background photoelectrons.

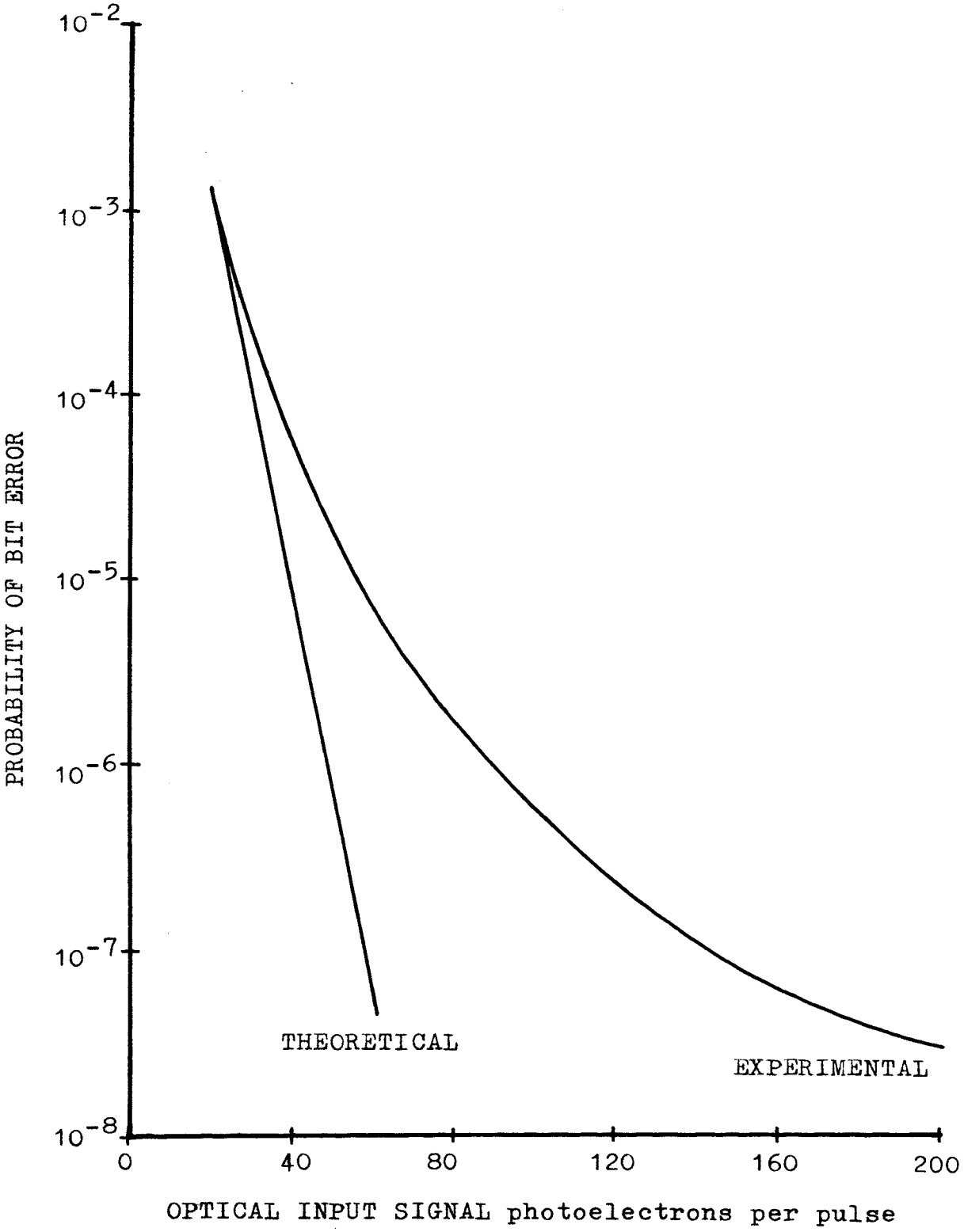


Figure 25. Optical receiver measured bit error rate for an average modulator extinction ratio of 10 to 1 with 0.4 photoelectrons per pulse background.

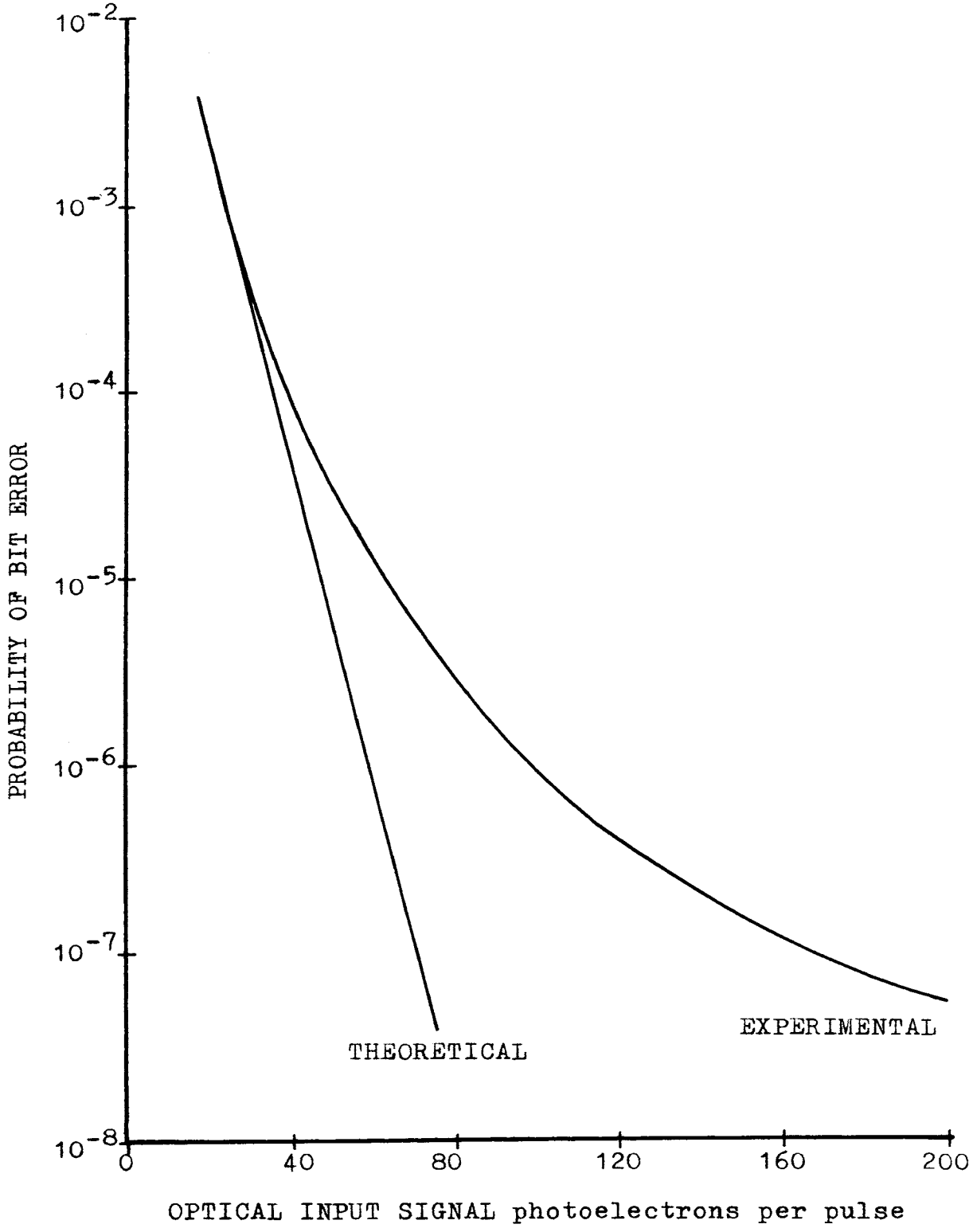


Figure 26. Optical receiver measured bit error rate for an average modulator extinction ratio of 10 to 1 with 4.0 photoelectrons per pulse background.

IV. CONCLUSION

A dynamic crossed field photomultiplier tube makes an ideal receiver for an optical PCM communication link. The DCFP has good high frequency response allowing high data rate communications. In addition high internal gain gives good sensitivity and the inherent internal gating in conjunction with the PCM data format allows discrimination against background radiation. The dynamic electric field drive to the DCFP, which controls the internal gating, requires synchronization to the input optical signal. This required synchronization serves a dual purpose. Beside allowing proper gating operation of the DCFP, the synchronization can be used as the basic bit synchronization for the receiver. Receiver bit synchronization was not required in this first optical receiver, but will be required in future receivers.

A set of goals was specified for the design of the optical receiver synchronization. A unique phase dithered phase-locked loop approach was used to meet the design goals. The dynamic electric field drive of the DCFP was phase dithered. The tube output was synchronously detected, filtered, and amplified to form the error signal input to a VCXO which controls the dynamic electric field drive phase and frequency. An error signal beatnote

detector was used to indicate lock and control the sweep acquisition generator.

The receiver synchronization loop was first designed and then the design was analyzed to see if the design goals were being met. The receiver was then fabricated and tested. The experimental results agreeded fairly well with the analytic results. The largest discrepancy occurred in the loop dynamic tracking capability. At high optical input power levels, the measured dynamic tracking capability was adequate to meet the design goal. At lower input levels the dynamic tracking capability did not meet the design goal. This was due to a reduction in the desired loop bandwidth and damping ratio caused by a decrease in the loop gain. This lower loop gain was attributed to inadequate performance of an AGC amplifier which amplified the DCFP output dither signal. The AGC amplifier had insufficient gain at the low input levels. The DCFP output dither signal magnitude was experimentally found to be less than the value predicted when the AGC amplifier was designed.

The synchronization loop could meet all the design goals with a redesign of the AGC amplifier.

If desired, reduced acquisition time and improved tracking performance could be obtained with a wider loop bandwidth. An optical receiver for use in a satellite terminal in a communication system would require some

ability to track input Doppler frequency shifts. Also the receiver would have to be suitable for working in a space environment. Some reduction in the receiver size and complexity would also be required. The low frequency synchronization electronics could easily be minaturized using techniques available today. The RF circuitry could be reduced by elimination of the intermediate amplifiers and multipliers between the VCXO and the RF power amplifier by phase locking a high power RF amplifier directly to the VCXO. Incorporation of these recommended changes would result in a space qualifiable optical receiver.

BIBLIOGRAPHY

1. Gaddy, Oscar Lee "Microwave Crossed-Field Secondary Emission Photo-Multiplication", Ph.D. Thesis, University of Illinois, Urbana-Champaign, June 1962.

2. Gaddy, Oscar L. and Holshouser, Donald F., "A Microwave Frequency Dynamic Crossed-Field Photomultiplier", Proceedings of the IEEE, Vol.51, No.1, January 1963, 153-162

3. Pratt, William K. Laser Communication Systems, New York: John Wiley and Sons, 1969.

4. Ross, Monte, Laser Receivers, New York: John Wiley and Sons, 1966.

5. Leverenz, Donald James, "A study of the sampling process in the DC biased dynamic crossed-field electron multiplier", Ph.D. Thesis, University of Illinois, Urbana-Champaign, 1969.

6. Leverenz, Donald J. and Gaddy, Oscar L., "Measurement of the Duration of the Sampling Function in the Dynamic Crossed-Field Photomultiplier.", Proceedings of the IEEE, Vol. 57, No.12, December 1969, 2153-2154.

7. Leverenz, Donald J. and Gaddy, Oscar L., "Subnanosecond Gating Properties of the Dynamic Cross-Field Photomultiplier.", Proceedings of the IEEE, Vol.58, No.10, October 1970, 1487-1490.

8. Gardner, Floyd M., Phaselock Techniques, New York: John Wiley and Sons, 1966.

9. Viterbi, Andrew J., Principles of Coherent Communications, New York: McGraw-Hill, 1966.

10. Barton, David K. and Ward, Harold R., Handbook of Radar Measurement, New Jersey: Prentice-Hall, 1969.

11. Relcom RF Components Catalog dated September 15, 1971 Palo Alto California (associated with Watkins-Johnson)

12. D'Azzo, John J. and Houpis, Constantine H., Feedback Control System Analysis And Synthesis, New York: McGraw-Hill, 1960.

Bibliography (continued)

13. Stuhlinger, Ernst, Ion Propulsion For Space Flight, New York: McGraw-Hill, 1964.

14. Geusic, Joseph E. et. al. "Coherent Optical Sources for Communications", Proceedings of the IEEE, Vol.58, No.10, October 1970, 1419-1439.

15. Leinwoll, Stanley, Understanding Lasers and Masers, New York: John F. Rider, 1965.

16. Lindgren, Nilo, "Optical Communications-A Decade of Preparations.", Proceedings of the IEEE, Vol.58, No. 10, October 1970, 1410-1418.

17. Ross, Monte et.al., "Short-Pulse Optical Communications Experiments", Proceedings of the IEEE, Vol.58, No. 10, October 1970, 1719-1726.

18. Schwartz, Mischa, Information Transmission, Modulation and Noise, New York: McGraw-Hill, 1959.

19. Stiffler J.J., Theory of Synchronous Communications, New Jersey: Prentice-Hall, 1971.

VITA

Douglas Wayne Dreisewerd was born September 28, 1943, in St. Louis, Missouri. He received his elementary and secondary education in the Normandy School District in St. Louis County, Missouri. He entered the University of Missouri-Rolla in September 1961. While serving as a cooperative education student, he attended undergraduate night school at both the Washington University university college and at the St. Louis extension division of the University of Missouri-Rolla. In May 1966 he graduated from the University of Missouri-Rolla with a B. S. degree in Electrical Engineering. In the fall of 1966 he entered the Electrical Engineering Department of the University of Missouri-Rolla St. Louis Graduate Engineering Center. He is a member of Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi honorary societies and the Institute of Electrical and Electronic Engineers.

Appendix A

DOPPLER FREQUENCY SHIFT

Several references were made to a Doppler frequency shift and at this time these references will be clarified.

In Section III A it was mentioned that with a heterodyne detector a Doppler frequency shift of the optical carrier could result in a Doppler frequency which exceeds the signal bandwidth. A typical Doppler frequency shift will now be calculated.

Consider a low earth orbital satellite containing a transmitter generating a carrier frequency f, and an earth based receiver. The received signal, at frequency f', is slightly different in frequency due to a Doppler shift. The magnitude of this frequency shift can be found from one of the well known Lorentz transformation formulas, often called the "relativistic Doppler effect" and given as follows,[13]

$$f' = f\frac{\sqrt{1-u^2/c^2}}{1+(u/c)\cos\alpha}$$

where

f = the transmitted frequency

f' = the Doppler shifted received frequency

u = the relative velocity between the

transmitter and the receiver

c = the speed of light

α = the angle between the velocity vector of the transmitter and the radius vector between the transmitter and the receiver.

The magnitude of the velocity vector of the transmitter can be calculated from the following equation,[13]

$$u_{orb} = R_o\sqrt{g_o/r}$$

where

u_{orb} = the orbital velocity

R_o = the earths radius

g_o = the acceleration due to the earths gravitational field

r = the radius of the orbit

Let the satellite be 100 miles above the surface of the earth, thus

$$r = R_o + 100$$

$$r = 6378\times10^3 + 100\times1.609\times10^3$$

$$r = 6.5389\times10^6 \text{ meters}$$

therefore

$$u_{orb} = 6.378\times10^6\sqrt{\frac{9.81}{6.5389\times10^6}}$$

$$u_{orb} = 7.81\times10^3 \text{ meters/second}$$

The relative velocity between the transmitter and the receiver differ slightly from the orbital velocity due to

the surface velocity of the earth, u_s, which is

$$u_s = \frac{2\pi R_o}{24x60x60 \text{ sec}}$$

$$u_s = 0.465x10^3 \text{ meters/second}$$

For the following calculations this "receiver velocity" will be ignored since its magnitude is small and the direction of the satellite's orbit determines if it is aiding or opposing.

The magnitude of the frequency shift due to the Doppler effect (f_d) is given by

$$f_d = f-f'$$

and if $u \ll c$ then

$$\frac{f'}{f} = 1-\frac{u}{c}\cos\alpha$$

or

$$f' = f-\frac{u}{c}f\cos\alpha$$

$$f-f' = f_d = (\frac{u}{c}\cos\alpha)f$$

Now if we let

$$u = 7.81x10^3 \text{ meters/second}$$

$$c = 3x10^8 \text{ meters/second}$$

$$\alpha = \pi/4 \text{ (a typical value)}$$

$$f = 10^{14} \text{ Hz } (3\mu\text{meter wavelength, infrared})$$

then

$$f_d = \left(\frac{7.81\text{x}10^3}{3\text{x}10^8}\cos\pi/4\right)\text{x}\,10^{14}$$

$$f_d = 1.84\text{x}10^9 \text{ Hertz}$$

If the signal bandwidth is 300 MHz then the Doppler frequency shift is more than 6 times the signal bandwidth.

In Section III C concerning the synchronization loop design goal it was mentioned that an operational receiver synchronization loop would have to track the Doppler shift of the data rate. This frequency change will now be calculated.

The Doppler shift on the optical carrier modulating signal, the 300 MHz transmitted information, would be

$$f_d = \left(\frac{7.81\text{x}10^3}{3\text{x}10^8}\cos\pi/4\right) 3\text{x}10^8$$

$$f_d = 5.52\text{x}10^3 \text{ Hz}$$

or if the full 1.2 GHz bandwidth of the DCFP were used, the Doppler frequency shift would be four times the previous number, or approximately 22 KHz. The range of the Doppler shift for an angle variation of $\alpha = 0$ to $\alpha = \pi$ would be $\pm\sqrt{2}$x22 KHz or $\pm$31.2 KHz.