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Design of an intermediate frequency amplifier and variable frequency oscillator

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Department:

DESIGN OF AN INTERMEDIATE FREQUENCY AMPLIFIER AND VARIABLE FREQUENCY OSCILLATOR

BY

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A

THESIS

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LIST OF SYMBOLS

A	---- Amplification
C	---- Capacitance
c	---- Collector
db	---- Decibel
e_i	---- AC input voltage
e_o	---- AC output voltage
f	---- Frequency
f_α^{co}	---- Frequency at which $\lvert\alpha\rvert$ is reduced by 3 db
G	---- Power Gain
g_i	---- Input conductance
g_o	---- Output conductance
h_{ij}	---- Hybrid parameters
I	---- DC current
I_B	---- DC base current
I_C	---- DC collector current
$I_{c\beta o}$	---- Collector current with collector junction reversed biased and base open circuited.
$I_{c\beta o}$	---- Collector junction is reversed biased and emitter is dc open circuited.
I_{co}	---- Same as above
I_E	---- DC emitter current
i	---- AC current
i_b	---- AC base current
i_c	---- AC collector current
i_c	---- AC emitter current

i_o ---- AC output current

i_i ---- Network currents

j ---- $\sqrt{-1}$

K ---- A fraction

L ---- Inductance

M ---- Mutual inductance

N ---- N type semiconductor material

P ---- Power

Q ---- Ratio of reactance to resistance

R ---- Resistance

R_B ---- External base resistance

R_E ---- External emitter resistance

R_g ---- Generator resistance

r_b ---- Equivalent base resistance

r_b' ---- Base spreading resistance

r_c ---- Equivalent collector resistance

r_e' ---- Emitter diffusion resistance

S ---- Stability factor

V_{cc} ---- Collector bias voltage

X_c ---- Capacitive reactance

X_L ---- Inductive reactance

Y ---- Admittance

y_i ---- Short circuit parameters

Z ---- Impedance

z_i ---- Open circuit impedance parameters

GREEK LETTER SYMBOLS

α ---- Short circuit current amplification factor

β ---- Current amplification of feedback network

Δf ---- Bandwidth

η ---- Efficiency

π ---- Number of radians equivalent to 180°

ω ---- Angular frequency

CHAPTER I

THE PROBLEM

A. INTRODUCTION

Since the advent of the transistor in 1948 many technological barriers have been overcome in the field of semiconductors. Unfortunately, however, there is a considerable period of time between the discovery of a scientific phenomena and its widespread use and understanding by practicing engineers. The motivating factor which prompted this investigation was primarily the lack of knowledge which the author possessed concering transistors. The selection of the amplifier and oscillator design confined the study primarily to the transistor. Considerable time, however, had to be spent in the study of basic transistor theory before any phase of the design could be effected.

B. THE PROBLEM

Statement of problem. This study was undertaken to investigate the theoretical and practical application of the transistor in a band pass amplifier and a variable frequency oscillator. The primary objective was to develope a unified

design approach for both circuits. The specifications which the intermediate frequency amplifier was expected to meet were; (1) a power gain of 50 db; (2) a one megacycle flat response using stagger tuning. The oscillator was to be variably tuned and operate at a frequency of ten megacycles.

Importance of the study. Band pass amplifiers are used in many electronic applications. In any communication network where radio frequencies are used as the carrier of information it is necessary to have at the receiving portion of the system ample means for the amplification of the incoming signal. The intermediate frequency amplifiers in radio receivers, for example, provide up to 90% of the required gain, therefore, these amplifiers are a major part of most receiving systems. Oscillators find application in many types of systems including radar, radio, and television as prominent examples.

It might be well to point out, at this time, that many of the concepts used in design of low frequency amplifiers are applicable to high frequency circuit design with some reservation. In general, the design of high frequency circuits are more complex due to the nature of the transistor and circuit components.

C. THE SCOPE OF THE INVESTIGATION

The investigation was divided into two parts, a theoretical analysis of the circuits and an experimental verification of the design.

Theoretical investigation. The design of the amplifier circuit involved an investigation of the neutralization of transistors, coupling networks, bias stability, input impedance measurements, high frequency equivalent circuits, and basic transistor theory. Much of the information obtained in the study of the amplifier proved useful in the design of the oscillator circuit.

Experimental verification. The intermediate amplifier and oscillator were constructed. Experiments were then conducted to enable a comparison with the theoretically expected results and those actually obtained.

D. REVIEW OF LITERATURE

In the interest of preserving the coherence of the investigation a review of literature will not be given at this time. As the need arises, background information will be provided during the developement of the different phases

of the design.

E. ORGANIZATION OF THE REMAINDER OF THE THESIS

In Chapter II the equivalent circuit to be used in the design of the amplifier is presented. Included also is a study of the theory of neutralization, the design of the neutralizing circuit, and the experimental results obtained.

Chapter III is devoted to the theoretical determination and experimental verification of the input impedance of the transistor in the grounded emitter configuration. The bias network and stability of the transistor is treated in Chapter IV. Chapter V is concerned with the determination of the required bandwidth and coupling networks. Chapter VI is devoted to the determination of power gain. The material in Chapter VII is concerned entirely with radio frequency oscillator design and experimental results obtained from tests performed on the circuit.

The conclusions and suggested fields of endeavor which could prove fruitful as far as providing additional information about transistor amplifiers and oscillators are mentioned in Chapter VIII.

CHAPTER II

NEUTRALIZATION OF THE TRANSISTOR AMPLIFIER

A. INTRODUCTION

A two terminal pair network is unilateral if an excitation placed at one terminal pair produces a response at the second terminal pair and an excitation applied to the second terminal pair produces no response at the first terminal pair. Networks capable of transmission in both the forward and reverse direction are considered nonunilateral or bidirectional.

A transistor is inherently a nonunilateral device. This fact presents the design engineer with a formidable problem when attempting to design a tuned radio frequency amplifier. In this respect vacuum tubes have a definite advantage since they are essentially unilateral in nature except at extremely high frequencies.

B. THEORY OF NEUTRALIZATION

Methods of neutralization. The transistor being of a nonunilateral nature is capable of backward transmission or internal feedback. The disadvantage of this is twofold:

1. The input and output immittances respectively are functions of the load and generator impedances.
2. The circuit may become oscillatory without the addition of an external feedback circuit.

The above disadvantages make it necessary to neutralize transistor circuits used in the above mentioned application.

When stages of an amplifier are tuned the dependence of output and input immittances on the load and generator impedances make accurate alignment of the stages virtually impossible. For example, if the reasonant frequency of the second stage of a three stage amplifier is changed by some increment of frequency, the impedance offered to the following stage is subject to a change as well as the input impedance to the second stage. Therefore, a means by which these disadvantages are eliminated is required if transistors are to be used at high frequencies in tuned amplifiers.

Currently there are two means available by which the effects of backward transmission on the input and output impedances of transistors can be eliminated. First, the stages may be purposely mismatched, that is, instead of matching a

1500 ohm output to a 300 ohm input, allow the output to see approximately a 300 ohm load. The loss of power for a mismatch such as this is only approximately 2 db. Second, the amplifier may be made unilateral or neutralized by the addition of an external network. It is the second method which is of primary concern since, its use results in maximum power gain from the transistor. In some cases[1] where complete neutralization is used, the amplifier has a greater gain than that obtained from the unneutralized unit.

Theory of neutralization. A two port device can be defined completely by two voltages and two currents as shown below in Fig. 1.

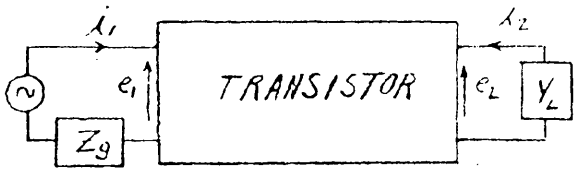

FIG. 1 TRANSISTOR TERMINAL VOLTAGES AND CURRENTS

There are six sets of two linear equations which may be used to describe a two terminal pair network. These equations involve six sets of different parameters, four of which are useful in determining internal feedback. These parameters are:

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[1] All references are in the bibliography

1. h parameters
2. y parameters
3. z parameters
4. g parameters

These equations have this general form in matrix notation:

$$\begin{bmatrix} M_1 \\ M_2 \end{bmatrix} = \begin{bmatrix} K_{11} & K_{12} \\ K_{21} & K_{22} \end{bmatrix} \times \begin{bmatrix} L_1 \\ L_2 \end{bmatrix} \qquad (1)$$

where M_i denotes the dependent variable, L_i the independent variable, and K_i the network parameters. The K parameters have a physical relationship to the network depending on their position in the matrix. They are:

K_{11} is an input immittance
K_{12} is a backward transfer ratio
K_{21} is a forward transfer ratio
K_{22} is an output immittance

K_{12} is the parameter which determines the magnitude of the response at the input terminal for an excitation at the output terminals. K_{12} is responsible for internal feedback.

The network is unilateral if K_{12} is equal to zero. The importance of unilateralization is readily seen by comparing the input and output immittance of a unilateral and a nonunilateral network.

Consider the circuit in Fig. 1. The two linear equations for the nonunilateral configuration are:

$$e_1 = h_{11} i_1 + h_{12} e_2$$
$$i_2 = h_{21} i_1 + h_{22} e_2 \qquad (2)$$

The input impedance is

$$Z_{IN} = h_{11} - \frac{h_{12} h_{21}}{h_{22} + Y_L} \qquad (3)$$

The output admittance is

$$Y_0 = h_{22} - \frac{h_{12} h_{21}}{h_{11} + Z_g} \qquad (4)$$

When the network is made unilateral h_{12} is equal to zero and the input impedance is

$$Z_{IN} = h_{11} - 0 \qquad (5)$$

The output admittance is

$$Y_0 = h_{22} - 0 \qquad (6)$$

Thus, we see that a neutralized network has an input and output immittance which is independent of Z_g or Y_L. The problem of reflected impedances is thereby eliminated by complete neutralization, which in essence, is achieved by making the input terminal's response independent of the ex-

citation at the output terminals.

An equivalent circuit for the common emittor connection is shown in Fig. 2 below[2].

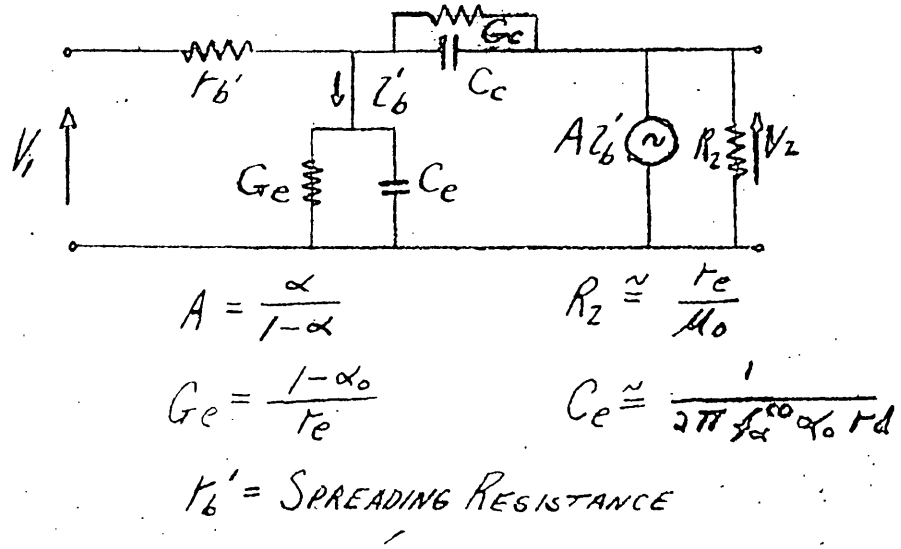


FIG. 2 HIGH FREQUENCY EQUIVALENT CIRCUIT

To determine the external feedback required to cause the backward transmission to be zero a balanced bridge circuit shown in Fig. 3 is utilized in the analysis. R_2 and r_c are neglected because of their large relative magnitudes.

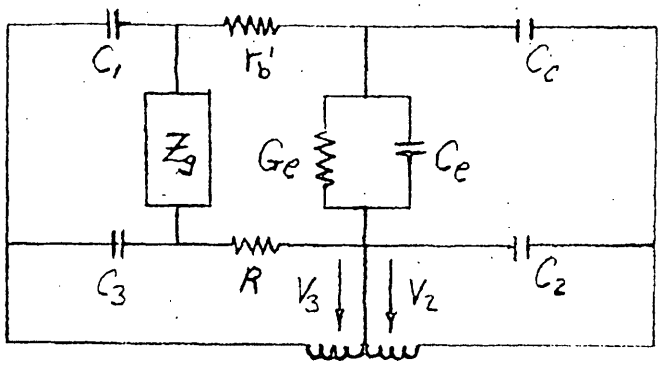


FIG. 3 A BRIDGE NEUTRALIZED CIRCUIT

The required elements to effect complete neutralization are C_1, C_2, C_3, and R. For a balanced bridge

$$\frac{C_1}{C_3} = \frac{R}{r_b'} = \frac{C_c}{C_2} \qquad (7)$$

If $r_b' \ll \frac{1}{\omega C_c}$ then the effects of feedback through C_c are cancelled by inserting only C_1. This does not result in complete neutralization but does considerably reduce the variation of input and output impedance. The partially neutralized output impedance is derived in Appendix 1.

The 2N1271 has an extremely low $r_b'C_c$ product, typically, 300 psec. The symbol used for 10^{-12} is "p". C_c is approximately 3 pfrds and r_b' is very much less than X_c.

C. EXPERIMENTAL DETERMINATION OF THE NEUTRALIZING CAPACITANCE

The neutralizing capacitance was determined experimentally by applying a RF signal at 10 Mc. to the output of the transistor. The magnitude of the signal at the input was tuned to a minimum by varying C_n. The circuit used to accomplish this is shown schematically in Fig. 4. Fig. 5 shows the actual reduction of feedback voltage by neutralization. The actual change was .03v to .002v with a signal of .31v on the collector.

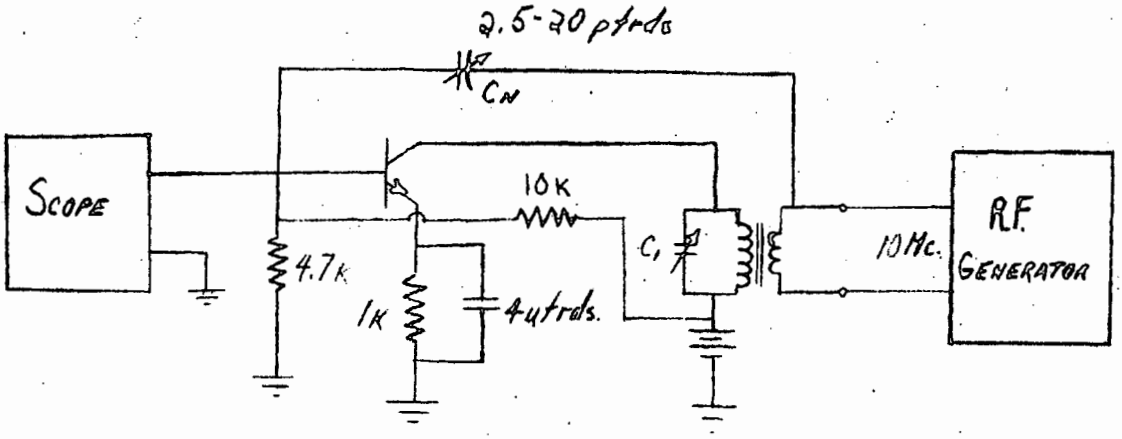


FIG. 4 NEUTRALIZATION OF TRANSISTOR

A.

B.

FIG. 5 THE BASE TO EMITTER VOLTAGE

A. UNNEUTRALIZED

B. NEUTRALIZED

Procedure. The procedure used in the experimental determination of C_n was to apply a signal to the output and vary C_1 until maximum voltage was obtained at the oscilloscope. This indicated when the collector tank circuit was tuned to 10 Mc. C_n was then adjusted until the signal at the base was the smallest value obtainable. The neutralizing capacitor was then measured on the "Q" Meter. The values obtained for C_n are shown in Table 1.

TABLE I NEUTRALIZING CAPACITANCE

Unit	C_n	N_2/N_1 C_n
B	4.0	1.66
C	4.8	1.96
D	7.6	3.15

The quantity N_2/N_1 C_n is the value of C_n used if the output transformer had a turns ratio of one to one. C_n x N_2/N_1 should be approximately equal to C_c where N_1/N_2 = 2.41

Conclusions. The effect of neutralization on the circuit was realized when upon completion of the amplifier stages an attempt was made to accurately tune the coupling

networks. Without neutralization the spurious oscillations were so severe that no tuning could be accomplished until the neutralizing capacitors were adjusted. The values obtained for C_n were within the specified range for C_c and are therefore in agreement with the theoretical expectations.

CHAPTER III

INPUT AND OUTPUT IMPEDANCE DETERMINATION

A. INTRODUCTION

Prior to the design of interstage coupling networks the input and output impedances of the transistor must be known. This enables the designer to meet the circuit requirements for a specified Q and, at the same time, match impedances to effect maximum power transfer from stage to stage.

Statement of the problem. The input and output impedance of a transistor used in high frequency applications must be neutralized unless the transistor has incorporated in it some particular mechanism which causes it to completely or, at least, for all practical purposes to act as a unilateral device. The tetrode transistor is one of this type. A potential is placed across the base region which reduces the effective path for carriers, consequently, a decrease in the high frequency resistance r_b' is realized.

The transistor chosen for this particular application is a surface alloy diffused base transistor manufactured by the Philco Corporation. This transistor is es-

pecially suited for high frequency applications at ten megacycles because it has a low $r_b' C_c$ product. This transistor, however, must be neutralized by some external means. Neutralization and the reason it is required are discussed in Chapter II.

The problem is the determination of the input and output impedance of the transistor with neutralization. The neutralized input and output impedances are, with good approximation, equal to the input and output short circuit impedances of the transistor. This method is suggested by the Philco Corporation.[3]

The chapter is divided into two parts, (1) a theoretical analysis of the experimental measurements to be carried on and (2) experimental results.

B. THEORETICAL ANALYSIS OF INPUT AND OUTPUT IMPEDANCES

The transistor can be described adequately using h parameters.

$$e_1 = h_{11} i_1 + h_{12} e_2$$
$$i_2 = h_{21} i_1 + h_{22} e_2 \qquad (8)$$

Upon addition of a neutralizing network adjusted so that $h_{12} = 0$ a new set of h parameters are obtained.

$$e_1 = h_{11}' i_1 + (0)\, e_2$$
$$i_2 = h_{21}' i_1 + h_{22}' e_2 \qquad (9)$$

If in a transistor $E_2 = 0$ a good approximation to the neutralized input impedance is

$$Z_{IN} = \frac{e_1}{i_1} = h_{11} \qquad (10)$$

The y parameters for the transistor are defined by the following equations:

$$i_1 = y_{11} e_1 + y_{12} e_2$$
$$i_2 = y_{21} e_1 + y_{22} e_2 \qquad (11)$$

In the typical junction transistor today y_{11} is much less than y_{12}. The magnitude of difference between y_{11} and y_{12} being approximately a factor of 10 or greater, the input impedance is not affected appreciably by neutralization, that is,

$$y_{11}' = y_{11} + y_{11}'' \qquad (12)$$
$$y_{11}'' \cong y_{12} \qquad (13)$$
$$y_{11}' \cong y_{11} \qquad (14)$$

The admittance parameters y_i' apply to the neutralized circuit, y_i'' to the neutralizing circuit alone, and y_i to the transistor.

The short circuited input impedance was measured at 9.0, 9.5, 10.0, 10.5, and 11 megacycles. The circuit used to measure this is shown in Fig. 6. The equivalent circuit used to theoretically determine the input impedance was chosen because it is well suited for this particular application. It was developed by J. B. Angell.[4] The equivalent circuit and solution for the input impedance is shown in Appendix 2. The short circuit and partially neutralized output impedances are determined and compared in Appendix 1.

C. EXPERIMENTAL DETERMINATION OF INPUT AND OUTPUT IMPEDANCE

The first method investigated to provide input and output impedances proved too inaccurate and cumbersome to warrant its use. Essentially, the approach was to resonate a tank circuit with the input capacitance of the transistor and then remove the tank circuit from the input. The tank circuit was then connected to the input terminals of a Q meter and the required capacitance to resonate the circuit at the specified frequency was measured. The magnitude of the input impedance was determined by measuring the voltage across the input and the current through it. Once the magnitude of the input impedance and the capacitive reactance was obtained the resistive component of the input was

determined. The result of the measurement was not in agreement with the theoretical expectations due to the variation in stray capacitance caused by moving the tank circuit, and the difficulty in reading input voltages accurately.

The method which was used with a fair degree of success was one incorporating a high frequency bridge circuit used in conjunction with a sensitive receiver. The bridge circuit also provided measurement in far less time than the previous method described.

The equipment used in this measurement was 605A General Radio Frequency Standard Oscillator, A General Radio Type 916A Bridge, and a Hammerlund Super-pro Receiver. This equipment was connected as shown in Fig. 6.

The Type 605B Standard Signal Generator has a frequency Range of 9.5 k.c. to 30 Mc. and the output is continually variable from 0.5 microvolts to .1 volt. The type 916A Radio Frequency Bridge is a null instrument for use in measuring impedance at frequencies from 400 k.c. to 60 Mc. The Hammerlund Super-pro Receiver covers a frequency range of 100 k.c. to 20 Mc. The receiver has two features which are essential to permit its use as a bridge detector, a manual

AVC "on-off" switch, and a beat frequency oscillator.

The oscillator, which provided a constant amplitude signal, was connected to the input of the bridge. The unknown terminals were connected to the input (or output) terminals of the transistor. The output of the bridge was connected to the receiver which was tuned to the frequency of the oscillator. The AVC was turned off to enable accurate selection of the null point, and the beat frequency oscillator in the receiver allowed detection of the constant amplitude RF from the bridge.

The impedances were read from the bridge. Since the bridge was a series impedance measuring device the readings were converted to their effective parallel impedances. This was accomplished and the result shown in Table II.

TABLE II

INPUT AND OUTPUT IMPEDANCE OF THE 2N1271
WITH FREQUENCY AS THE VARIABLE

I_c = 2 ma., V_c = 10

UNIT B.

Frequency	R_{in} (ohms)	C_{in} (pfrds)	R_o (ohms)	C_o (pfrds)
11.0	467	15	2290	5
10.5	504	15	2290	5
10.0	505	15	2000	5
9.5	523	15	2600	5
9.0	467	15	2270	5

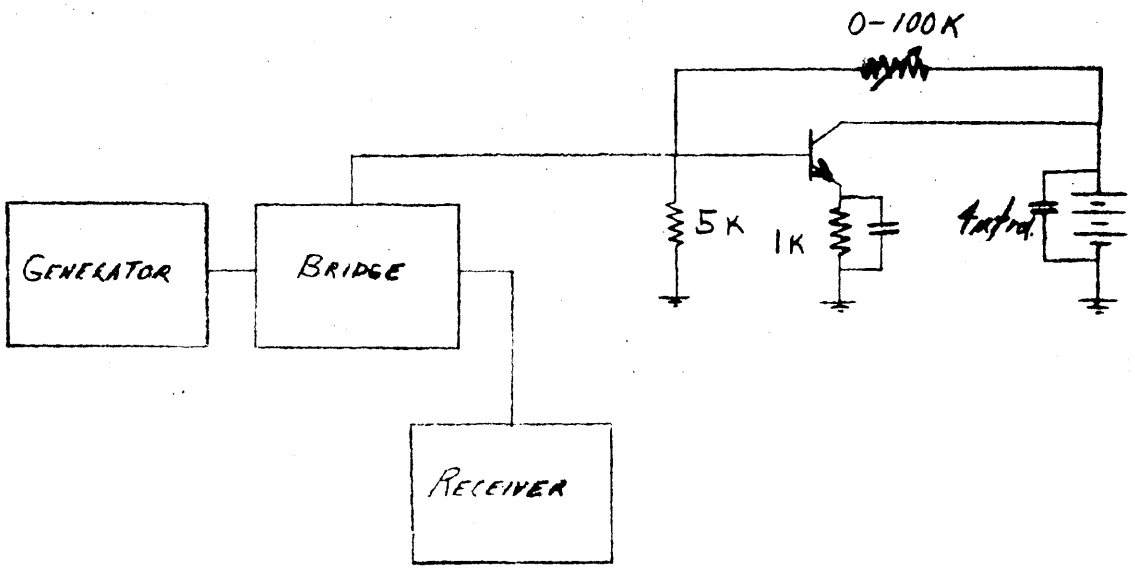
UNIT C.

Frequency	R_{in} (ohms)	C_{in} (pfrds)	R_o (ohms)	C_o (pfrds)
9.0	467	15	4700	2
9.5	489	15	2810	2
10.0	571	15	3080	2
10.5	548	15	3120	2
11.0	640	15	3250	2

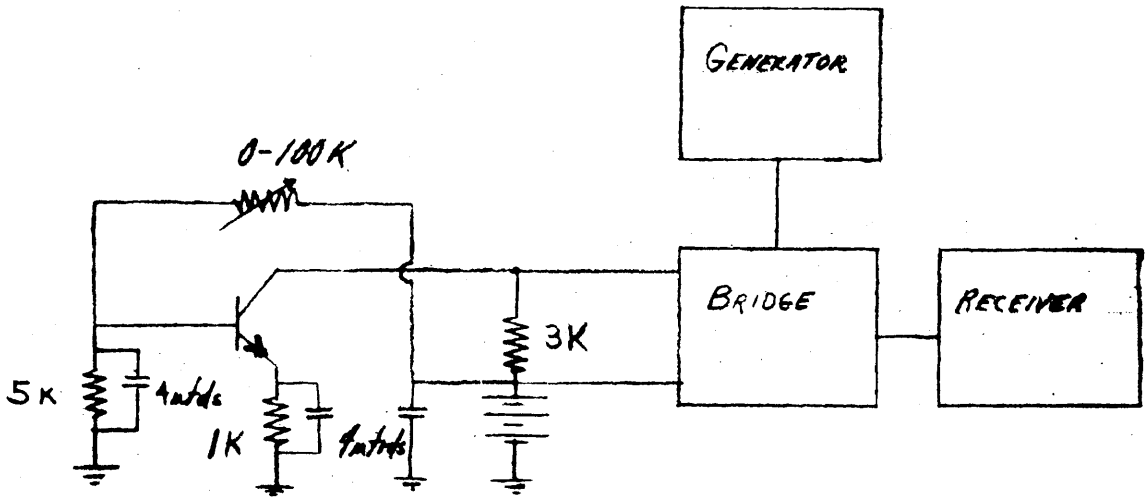
TABLE II (continued)

UNIT D.

Frequency	R_{in} (ohms)	C_{in} (pfrds)	R_o (ohms)	C_o (pfrds)
11.0	191	20	2060	2
10.5	194	20	2050	2
10.0	214	20	2350	2
9.5	201	20	2221	2
9.0	177	20	2010	2



A. DETERMINATION OF INPUT IMPEDANCE



B. DETERMINATION OF OUTPUT IMPEDANCE

FIG. 6 DETERMINATION OF INPUT AND OUTPUT IMPEDANCE

CHAPTER IV

BIAS NETWORK DESIGN

A. INTRODUCTION

There has been considerable work done on the bias stabilization of transistors. It is the purpose of this chapter to design a bias network which will afford stability over a range of temperature from 78°F. to 250°F. The method of approach to this problem has been investigated by S. K. Ghandi[5] and it is his conclusions which are used in the physical explanation.

Changes in temperature to which a transistor is subjected results in a shift in operating point and in some instances causes the transistor to destroy itself. Increasing temperatures cause electon-hole pairs to be generated in the base and collector regions. In an NPN transistor the electrons tend to migrate to the collector and the holes to the base. The result is the leakage current increases, and the base region developes a hole-excess causing base current to flow. The amount of base current which flows depends on the magnitude of the impedance in the base lead. If in a unit time only a fraction, K, of the electrons entering in

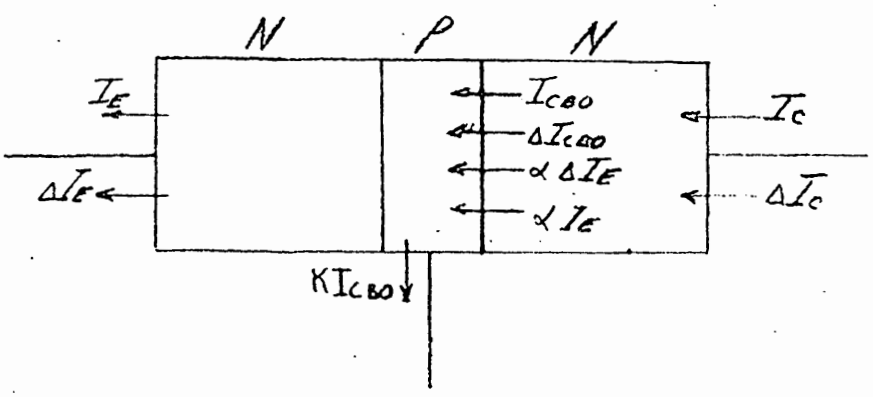


FIG. 7 TRANSISTOR CURRENTS

the base are removed the base current is K I_{CDO}. The (1-K) I_{CDO} causes electrons to be injected from the emitter, which increases the emitter current. A fraction of these electrons reach the collector and (1-α) combine with holes in the base, which results in the current relationships

$$\Delta I_E (1-\alpha) = (1-K)\Delta I_{CBO} \qquad (15)$$

$$\Delta I_C = \alpha \Delta I_E = \frac{1-K}{1-\alpha} \Delta I_{CBO} \alpha \qquad (16)$$

This increase in collector current results in increased dissipation in the collector and consequently a slightly higher temperature which causes an increase in electron-hole pair production and the process is repeated. The ambient temperature and the cooling technique utilized determines if the process increases until the transistor destroys itself, or at some elevated temperature becomes stable.

The second factor which increases the thermal sensitivity of this device is the forward resistance of the base to emitter diode. The resistance of this junction decreases as the temperature is increased resulting in a further increase in emitter current. The magnitude of this increase is dependent on the relative impedance levels of the base and emitter leads.

In general stabilization is improved if (1) The base is fed from a low impedance source ($K \rightarrow 1$); (2) The emitter is fed from a high impedance source ($\Delta I_E \rightarrow 0$).[6]

B. DESIGN CONSIDERATIONS

The previous section provides a physical explanation of the mechanism of operating point variations with temperature changes. It is necessary now to examine each factor in particular which affects the stabilization of the operating point.

The specified maximum and minimum values of current gain h_{fe} at the operating point is an important consideration since the variation in h_{fe} takes into account the change in current gain anticipated if the transistors are replaceable. The variation of h_{fe} caused by temperature changes must also

be included; this information can be obtained from graphs usually made available by the manufacturer. The variation of collector current which was discussed previously increases 6.5 - 8% per degree centigrade and doubles with a temperature change of 9-11°C. In the design of the bias network, the minimum valve of I_{CBO} is assumed zero, and the maximum value is obtained from transistor curves of I_{CBO} versus temperature.

The variation of V_{BE} must be taken into account. Under normal bias conditions V_{BE} for a silicon transistor is approximately + .7 volts but it may become necessary at elevated temperatures to reverse bias this junction to obtain low values of collector current.

Fig. 8 shows a typical grounded emitter stage which is a general circuit. This circuit was analyzed and from the results the resistive components used in the final circuit were calculated.

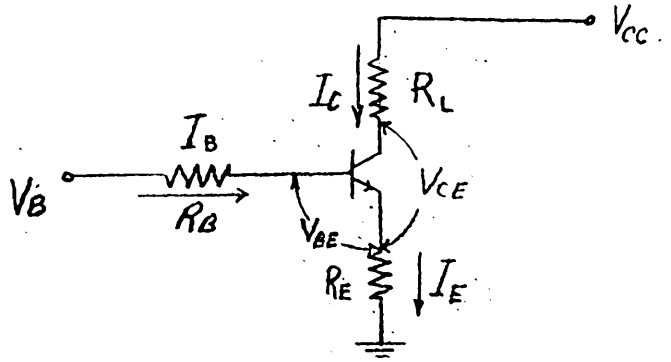


FIG. 8 TYPICAL GROUNDED EMITTER STAGE

The following equations apply to the circuit in Fig. 8.

$$h_{fb} = \frac{\alpha}{1-\alpha} \tag{17}$$

$$I_C = h_{fe} I_B + I_{CEO} = h_{fe} I_B + (h_{fe}+1) I_{CO} \tag{18}$$

$$I_C = \alpha I_E + I_{CO} \tag{19}$$

$$I_E = (h_{fe}+1) I_B + I_{CO} \tag{20}$$

$$V_B = \left[\frac{R_B}{(h_{fe}+1)} + R_E\right] I_E + V_{BE} - I_{CO} R_B \tag{21}$$

The method used to design the bias network was to obtain two equations for V_B:

1. When the temperature is at its minimum value, I_E is a minimum and the worst conditions that could occur are for $h_{fe} = h_{fe\ min}$, $V_{BE} = V_{BE\ max}$, and $I_{co} = 0$. Thus,

$$V_B = \left[\frac{R_B}{(h_{fe}+1)} + R_E\right] I_{E\ MIN} + V_{BE\ MAX} \tag{22}$$

2. When the temperature is at its maximum value, I_E is a maximum and the worst value the parameters could have are for $h_{fe} = h_{fe\ max}$, $V_{BE} = V_{BE\ min}$, $I_{co} = I_{co\ max}$. Thus,

$$V_B = \left[\frac{R_B}{(h_{fe\ MAX}+1)} + R_E\right] I_{E\ MIN} + V_{BE\ MIN} - I_{CO\ MAX} R_E \tag{23}$$

Solving Equations 22 and 23 the value of R can be calculated in terms of R and the circuit parameters. The resulting

equation is of the form

$$R_B = K R_E - C \qquad (24)$$

where K and C are constants. To convert to a single battery bias network V_B had to be determined from Equation 22. This is done in Section C.

Stability relationship. The stability factor of the bias circuit is defined as the rate of change of I_c with respect to I_{co}. This factor gives an indication as to the relative merit of the bias circuit when subjected to changes in temperature. Equation 21 is used in the determination of the stability of the network with the following substitution for base current:

$$I_B = \frac{(1-\alpha) I_c}{\alpha} - \frac{I_{co}}{\alpha} \qquad (25)$$

Making this substitution for I_B, replacing I_c by $I_B + I_E$, and neglecting V_{BE} an equation for stability is obtained by differentiating I_c with respect to I_{co}.

$$S = \frac{1}{\frac{R_E \alpha}{R_E + R_B} + 1 - \alpha} \qquad (26)$$

C. DESIGN OF THE BIAS NETWORK

Enumerated below is the procedure used in the bias circuit design.[7]

1. Range of temperature was 78°F to 250°F.
2. The values of I_{co} obtained from a graph supplied by the manufacturer was $I_{co\ max}$ = 50 micro amperes and $I_{co\ min}$ = 0.
3. The current gain was determined by using the manufacturer's tolerance and adding to the maximum specified value the variation due to temperature at the upper limit. This was determined from a plot of the transistor parameters versus temperature. The minimum value of h_{fe} remained the same because the parameter variations were normalized to 78°F. The maximum value for h_{fe} was 47, and the minimum value was 11.
4. The maximum and minimum values of emitter current were determined by the points on the I_c versus power out curve at which the gain was reduced by 1 db. The values of I_E determined were $I_{E\ max}$ = 2.76 ma. and $I_{E\ min}$ = 1.55 ma. The actual values used in the design equations were modified by a factor of 15% due to the tolerance of bias resistors. The correction resulted in $I_{E\ max}$ = 2.23 ma and $I_{E\ min}$ = 1.795 ma.
5. Using Equations 22 and 23 R_B was then solved in terms of R_E.

$$R_B = \frac{(I_{E\,MAX} - I_{E\,MIN})R_E + V_{BE\,MIN} - V_{BE\,MAX}}{I_{CO\,MAX} - \frac{I_{E\,MAX}}{h_{fe\,MAX}+1} + \frac{I_{E\,MIN}}{h_{fe\,MIN}+1}} \qquad (27)$$

Let R_E = 1000 ohms which is sufficient to swamp the base to emitter forward resistance. R_B is equal to 2.25K ohms.

The value of V_B is determined from Equation 22 which is the condition of minimum temperature. Close examination of Equation 23 shows why the V_B is determined from the equation for minimum temperature. The term $-(I_{CO}\ R_E)$ which becomes significant at high temperatures has a tendency to lower V_B. Therefore, in the design the highest value of V_B is chosen and the associated voltage divider is calculated for this particular quantity.

The bias circuit used for the amplifier is a single battery type shown in Fig. 9. R_3 is equal to R_E. The resistor R_2 may be found from the following relationship which neglects the input coil resistance.

$$\frac{R_1}{R_B} = \frac{V_{CC}}{V_B} \qquad (28)$$

also

$$R_1 = \frac{R_B V_{CC}}{V_B} = 10K\Omega \qquad (29)$$

$$R_2 = \frac{R_1 V_B}{V_{cc} - V_B} = 2.9 K\Omega \qquad (30)$$

The final bias circuit is shown in Fig. 9.

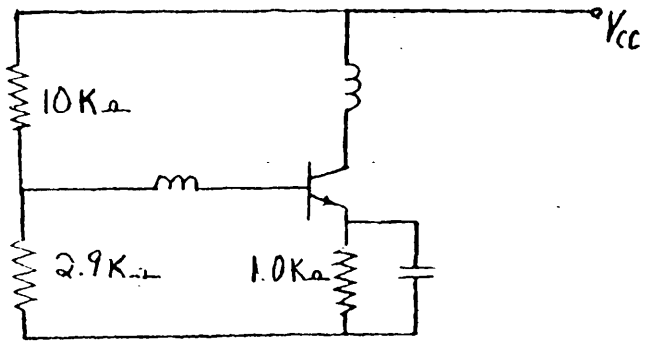


FIG. 9 BIAS CIRCUIT

D. EXPERIMENTAL RESULTS

The procedure. To check the accuracy of the design equations one of the units was subjected to a temperature change of 172°F to determined the variation of I_E. The transistor was inserted in the designed bias circuit, and the voltage across R_E was monitored by using a vacuum tube voltmeter. A heating element was connected to the transistor. The temperature was controlled by a variac which supplied power to the heat source. Temperature readings were obtained from a Weston thermometer attached to the heating element. Approximately 15 minutes was allowed for the temperature to stabilize before the initial reading of I_E was taken. The same interval of time was allowed between each successive

reading. This data shown in Table III.

Conclusions. The results are plotted graphically in Fig. 10. The variation in I_E as the temperature was changed from 84°F to 250°F was 144 micro amperes. The emitter current stayed well within the upper limit of the desired value of 2.76 ma., since, the maximum experimental value of I_E was less than 2.0 ma. The minimum value of I_E allowed was 1.55 ma. which was considerably less than the minimum obtained experimentally (1.8 ma.).

The stability predicted theoretically was 2.94, this is in close agreement with the experimental results. The graph of I_{CO} versus temperature provided by the manufacturer shows a variation in I_{CO} of 50 micro amperes over the range of temperature considered. The expected increase in I_C is S I_{CO} which is 150 micro amperes. The value found experimentally was 144 micro amperes change in I_E.

Since the network is designed for maximum protection at the higher temperatures, the value of I_C is usually lower than the optimum value of 2 ma. at which maximum power gain occurs. This problem is eliminated by increasing the size of R_2. This results in only a slight change in stability.

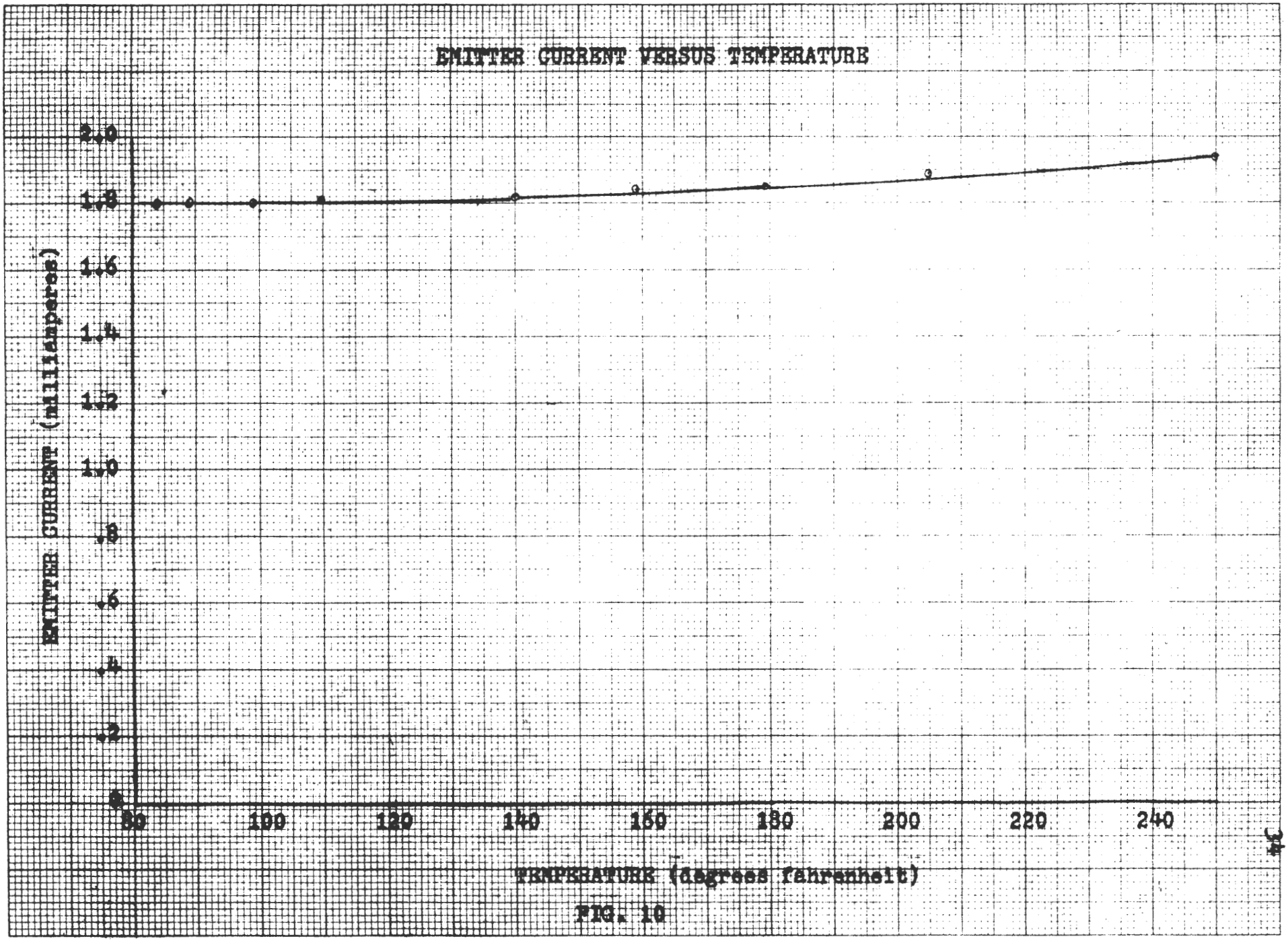

EMITTER CURRENT VERSUS TEMPERATURE
EMITTER CURRENT (milliamperes)
2.0
1.8
1.6
1.4
1.2
1.0
.8
.6
.4
.2
0
100
120
140
160
180
200
220
240
TEMPERATURE (degrees fahrenheit)

FIG. 10

TABLE III. STABILITY DATA

READING	TEMPERATURE (^{o}F)	CURRENT (ma)
1	84.0	1.80
2	88.0	1.80
3	99.0	1.80
4	109.5	1.81
5	140.0	1.82
6	159.0	1.84
7	179.0	1.85
8	205.0	1.89
9	250.0	1.94

CHAPTER V

DESIGN OF COUPLING NETWORKS

A. INTRODUCTION

The coupling networks used in the amplifier interstage networks were of the single-tuned transformer coupled type. The original design was for three staggered tuned stages separated to give a flat bandwidth between 9.5 and 10.5 Mc. Theoretically this is entirely feasible, however, practically the design of these stages proved impossible. When it was found that a one megacycle flat response could not be obtained the design requirements were changed to allow a one megacycle response between the three db points. This chapter is divided into two parts; (1) devoted to the work done in an endeavor to stagger tune the stages; (2) the final design of the single-tuned stages which were ultimately used in the amplifier.

Interstage design for stagger-tuned amplifiers. First, the center frequency and required Q for the networks was determined. This was accomplished using methods previously developed for vacuum tubes.[8] To obtain the required bandwidth, two stages with a dissipation factor of D at frequencies of $f_o\alpha$ and f_o/α were required. The third stage was tuned to

the center frequency of the cascade and had a dissipation factor of δ. The dissipation factor is defined as $1/Q_L$. Q_L is the loaded Q of the coil, and α is equal to one plus $.433\delta$.

From the design equations previously mentioned the frequencies of the tuned circuits were found to be 9.58 Mc., 10 Mc., and 10.433 Mc. with loaded circuit Q's of 20,10, and 20, respectively. The design of the two stages requiring a Q_L of 20 were impossible to fabricate with the material available.

To illustrate the difficulty encountered, consider the design of an interstage coupling network at a frequency of 10.433 Mc. This is typical of the problem which arose in attempting to secure a Q_L of 20.

The coils were wound by hand and a trial and error procedure was used to obtain the values of inductance because the permeability of the core was not known. Initially it was assumed that the coupling circuit acted as a perfect transformer which transformed impedance proportional to the square of the turns ratio. This assumption is only valid if the coefficient of coupling between the primary and secondary inductances is approximately equal to one. This assumption is verified in another section of this chapter. It is desir-

ous to match the output of a generator to the load if maximum power transfer is to be realized. This match is obtained when $R_o = Q^2 R_{in}$ where R_{in} is the input resistance to the transistor and R_o is the output resistance neglecting coil losses. The selectivity or bandwidth relation is determined by the Q_L of the circuit which is equal to

$$Q_L = \frac{f_o}{\Delta f} = \frac{2\pi R_o C_t f_o}{2} \qquad (31)$$

where C_t is the capacitance required to cause the tank to resonate at the desired frequency and $R_o/2$ is the resistance in parallel with the coil. Using the above relationship C_t was found to be equal to 247 pfrds. Having determined C_t, L_t was readily found from the relationship $L_t = 1/\omega_0^2 C_t$. L_t was found to be $.943 \times 10^{-6}$ micro henries.

The coil was then wound on a Miller #4500 adjustable ceramic form with a ferrite core. When the Q was measured on a Q Meter it was found that the coil possessed a Q of 30. However, upon further investigation it was found if the coil was wound too near the mounting nut, this fastener would act as a short circuited turn, lowering the Q of the coil by 40 to 50 percent. When the coil was properly located on the form the Q of the circuit was found to range between 50 and 60 for the three coils forms. Knowing the value of Q_u the effective shunt resistance of the coil could be found from

the equation $R_c = Q_u X_L = 58 \times 61.7 = 3580$ ohms. Q_u is the unloaded Q, that is, the Q of the coil alone. The output resistance of the transistor was found to be 2486 ohms. By matching the input to the output the effective resistance in shunt with the tank circuit is 1243 ohms, neglecting the effective coil resistance. When the resistance of the coil is taken into account an effective shunt resistance of 1243/4823 3580 = 1060 ohms is obtained. The loaded Q_L is now R_o/X_L = 1060/61.7 = 17.2. The obvious thing to do is to reduce the value of X_L. A reduction in X_L is accompanied by a reduction in R_c (shunt resistance of the coil), and it was found that no matter how much X_L was decreased the Q_L would never approach the value of Q desired. This condition is a result of initially having a low value of inductive reactance. If X_L decreases, and the X_L is large enough, the change in R_c in parallel with R_o of the transistor is not as large as the change obtained in X_L, thus, the Q_L would increase. In most cases, when the Q_L of the circuit is not too high a reduction in inductance usually compensates for the resistance of the coil.

A more thorough theoretical investigation into the feasibility of obtaining the desired selectivity characteristic with a Q_u of 50 proved interesting.[9]

If B_1' is defined as $\Delta f/f_o$, g_{01} as the output conductance of transistor one, g_{12} as the input conductance of transistor two, then an equation is developed which gives maximum power transfer efficiency as a function of B_1' and Q_u.

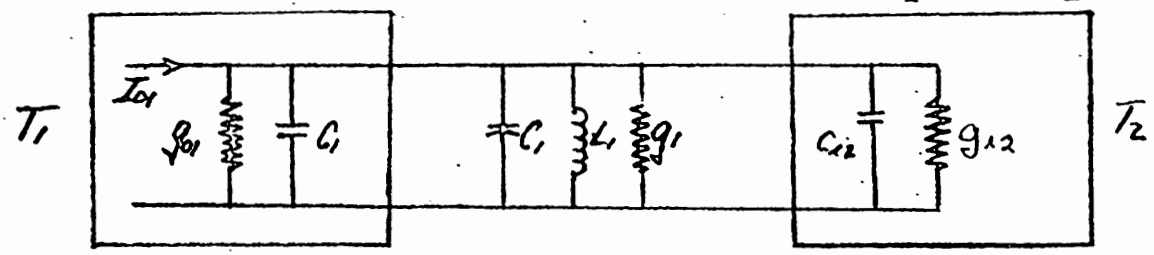


FIG. 11 COUPLING NETWORK

Referring to Fig. 11 the power available from transistor one is

$$P_1 = \frac{|I_{o1}|^2}{4 g_{o1}} \qquad (32)$$

where I_{o1} is output current of transistor one. The power delivered to transistor two is

$$P_2 = \frac{|I_{o1}|^2 g_{i2}}{(g_{o1} + g_1 + g_{i2})^2} \qquad (33)$$

Power transfer efficency is defined as

$$\eta = \frac{P_2}{P_1} = \frac{4 g_{o1} g_{i2}}{(g_{o1} + g_{i2} + g_1)^2} \qquad (34)$$

this shows that for n to be equal to unity, g_1 must be equal to zero and g_{01} equal to g_{i2}.

B_1' can also be expressed as

$$B_1' = \frac{g_{o1} + g_{i2} + g_1}{g_1 Q_u} \qquad (35)$$

Obtaining g_1 from Equation 35 and substituting into Equation 34 n is found as a function of g_{01} and g_{i2}. Differentiating n with respect to g_{i2} and equating the result to zero yields

$$\eta_{max} = \left(1 - \frac{1}{B_1' Q_0}\right)^2 \qquad (36)$$

Upon substituting values for B_1' and Q_u the efficiency is 43% of the maximum obtainable if g_1 was zero. This loss of 57% of the available power shows that even if the coupling circuit could be designed this loss of power would greatly affect the configuration of the response curve and a flat response would not be obtained.

The inability to obtain the desired Q_L and the above mentioned effect on the response curve resulted in changing the coupling circuit requirement to a 1 Mc. bandwidth between 3 db. points. This problem was a result of the authors lack of knowledge on the subject of transistors and coupling networks at the time the selectivity requirements for the amplifier were chosen.

B. DESIGN OF SINGLE-TUNED STAGES

To obtain the desired bandwidth with three cascaded stages of amplifiers single-tuned, allowance had to be made for the reduction of bandwidth due to the selectivity of

each circuit. It is intuitively evident an overall bandwidth of 1 Mc between 3 db points cannot be obtained by the use of three stages, of bandwidth equal to 1 Mc. It has been shown that n single-tuned stages have an overall bandwidth

$$B_{1n} = B_1 \sqrt{2^{1/n} - 1} \qquad (37)$$

where B_1 is equal to the bandwidth of one stage, B_{1n} is equal to the bandwidth of n stages and n is the number of stages.[10]

Solving this for B_1 with B_{1n} = 1 Mc., and n = 3 it was found that B_1 = 1.96 Mc. Equation 31 yielded a value of C_t equal to 65.3 $\mu\mu$frds. from which L was determined to be 4.64 x 10^{-6} micro henries. The Q of the coil above was 58 which yielded an equivalent R_c = 16,800 ohms. It was found that neglecting the resistance of the coil the output resistance of the amplifier was 1243.5 ohms which resulted in a loaded Q_L of 4.28. This Q was too low to meet the per stage bandwidth requirement of 1.96 Mc. Again a trial and error process was used and the L_t of the coil reduced in small steps until a L_t of 3.47 micro henries was obtained.

This value of inductance resulted in an inductive reactance which made the Q_L obtainable with a slight mismatch. The resistance of the coil ($R_c = Q\ X_L$) was combined with the output resistance of the transistor which was matched to the

input of the following stage. The parallel resistance of R_c and R_o was found to be 2080 ohms. If the input were matched to this resistance we would have 1040 ohms across the tank circuit which results in a loaded Q of 4.78. Therefore, rather than reduce X_L any further the reflected input impedance was made of such size that the required Q_L could be obtained. The value of a^2R_{in} was found to be 2380. R_{in} was equal to 408 ohms, therefore, a^2 was 5.82. The final turns ratio was 17/7.05 = 2.41 = a.

The value of inductance originally required was 4.64 micro henries, which finally became 3.47 micro henries. The factor by which the inductance was reduced was 1.34, to keep the reasonant frequency constant the capacitance was increased by 1.34, resulting in a C_t of 87.6 pfrds. To determine the capacitance actually needed in the circuit the transferred input capacitance (2.9 pfrds.), the output capacitance (3 pfrds.) and the stray wiring capacitance (0-20 pfrds.) had to be subtracted from C_t. This resulted in a physical capacitance of approximately 60 pfrds, which was obtained from a fixed capacitance of 45.3 pfrds. and a trimmer capacitor of 5 to 20 pfrds. The graphical results of the frequency response is shown in Fig. 12. The overall bandwidth is a small amount less than 1 Mc. The percent error being approximately 2.5%. Table V shows the values used in plotting the graph of Fig. 12.

Determination of the coefficient of coupling. The method of measurement of the coefficient of coupling utilized the Q Meter to determine the mutual inductance of the coils. This was accomplished by first measuring the inductance of the primary and secondary windings. Two coils which are mutually connected have a total inductance given by the expression $L_t = L_1 + L_2 \pm 2M$, the plus or minus sign is determined by whether or not the coils are connected so the mutual fluxes are aiding. If the primary and secondary are connected one value for L_t is obtained, by reversing the connections on one winding another value for L_t is obtained. The difference in these values is 4 times the mutual inductance between the two coils. Knowing the mutual, primary, and secondary inductances K could be evalulated from the relationship $K = M/\sqrt{L_1 L_2}$. Table IV shows the values of K obtained for the three units.

TABLE IV COEFFICENT OF COUPLING

United Tested	Coefficient of Coupling
1	.974
2	.965
3	.98

With the coefficient of coupling near unity the transferred

impedance of the coupling network could be assumed proportional to the square of the turns ratio. This verifies the assumption made in the design of the coupling networks.

TABLE V FREQUENCY RESPONSE DATA

FREQUENCY (Mc)	AMPLITUDE	FREQUENCY (Mc)	AMPLITUDE
8.0	.175	10.2	.9
8.2	.19	10.4	.75
8.4	.21	10.6	.58
8.8	.30	10.8	.45
9.0	.37	11.0	.35
9.2	.48	11.2	.26
9.4	.61	11.4	.22
9.6	.79	11.6	.18
9.8	.95	11.8	.14
10.0	1.00	12.0	.10

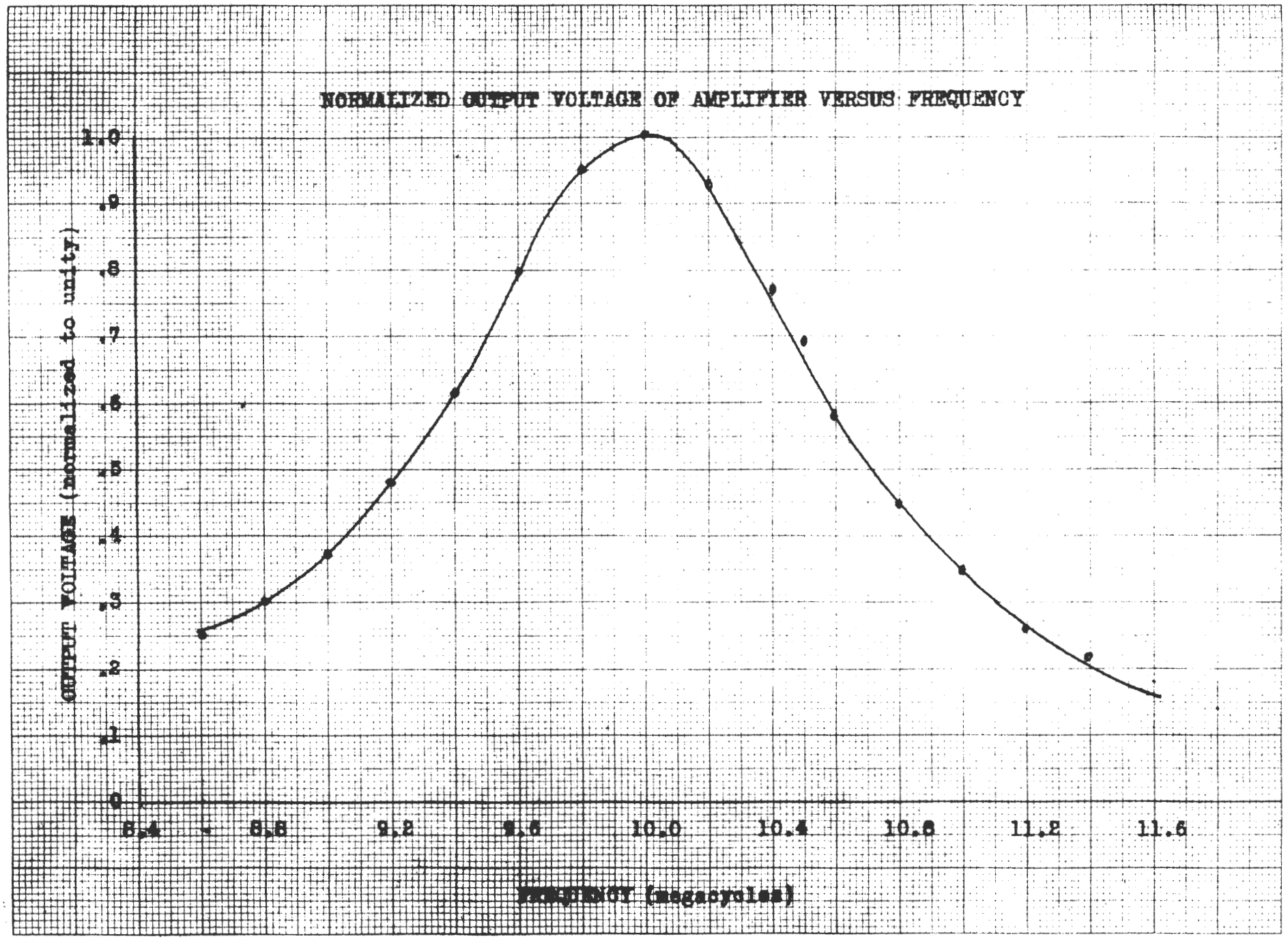

NORMALIZED OUTPUT VOLTAGE OF AMPLIFIER VERSUS FREQUENCY
OUTPUT VOLTAGE (normalized to unity)
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
8.4
8.8
9.2
9.6
10.0
10.4
10.8
11.2
11.6
FREQUENCY (megacycles)

FIG. 12

CHAPTER VI

AMPLIFIER GAIN

A. INTRODUCTION

The high frequency power gain of a transistor may be expressed in terms of fundamental device parameters. The first portion of this chapter will be devoted to the theoretical determination of high frequency power gain and then the experimental results will be evaluated. Construction of the amplifier will be considered and the problems encountered will be discussed.

Rigorous analysis by Pritchard[11] has shown that the high frequency power gain of the transistor can be expressed by the following equation

$$G = \frac{1}{25} \frac{f_{\alpha}^{co}}{f_0^2 r_b' C_c} \qquad (38)$$

Experiments have shown that this equation is valid in the following frequency range.

$$.05 - .01 < \frac{\omega}{\omega_{co}} < 2 \qquad (39)$$

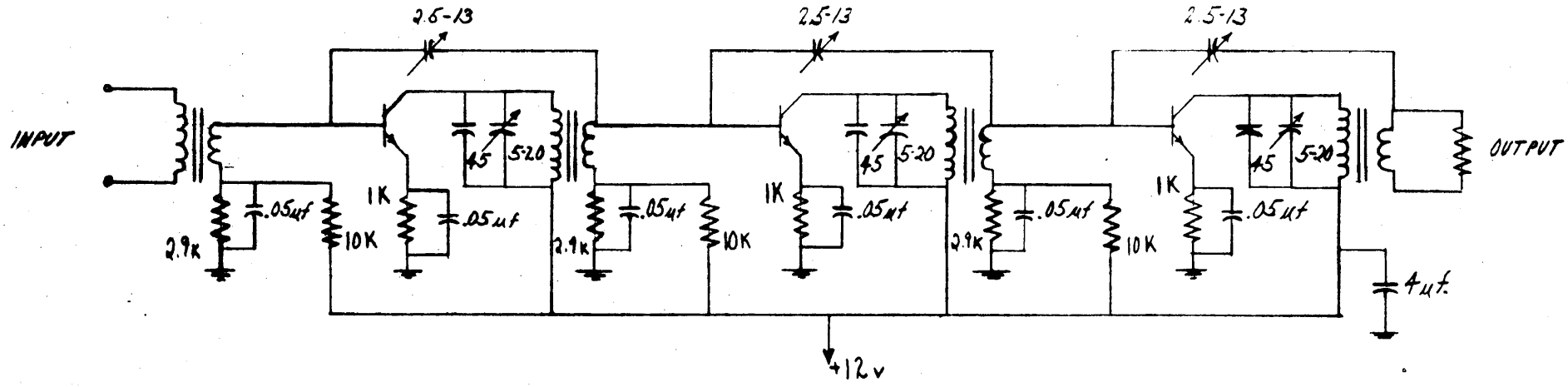
The transistor selected for use in this amplifier is a Surface Alloy Diffused-base silicon semiconductor. It has

an α_{co} frequency of approximately 60 Mc. The power gain predicted with the use of Equation 38 was a minimum of 18 db. and a maximum of 21.6 db. depending on the value of $r_b'C_c$ used in the calculation, 300 or 165 psec respectively. The above mentioned range of $r_b'C_c$ is controlled in the manufacture of the unit.

B. CONSTRUCTION

In the construction of the intermediate amplifier shown schematically in Fig. 13 a two inch wide and eight and one half inches long strip of plastic bread board material was used. Fittings could be inserted in the plastic for mounting the components and transistor easily. The circuit was constructed and a resistance check performed to ensure that no wiring errors were made. The assembled amplifier is shown in Fig. 14. The battery voltage was then applied, this caused the circuit to start a random oscillation which prevented any attempts to tune the coupling networks. This was due to a lack of neutralization. It was found that each circuit must be neutralized before these oscillations would desist. The second and third transistors were removed from the circuit and the first stage neutralized as described in Chapter II. Once this circuit was neutralized the second transistor was inserted and neutralized. This process was repeated on the third stage and oscillations did not recur. When the Stand-

THREE STAGES OF AMPLIFICATION USING THE ZN1271



NOTE: ALL CAPACITANCE IN MMF. EXCEPT WHERE INDICATED OTHERWISE.

FIG 13. 10Mc. AMPLIFIER STRIP

ard Frequency Oscillator was connected to the input, oscillations were encountered if the amplitude of the signal input was raised larger than .5 milli volts.

A.

B.

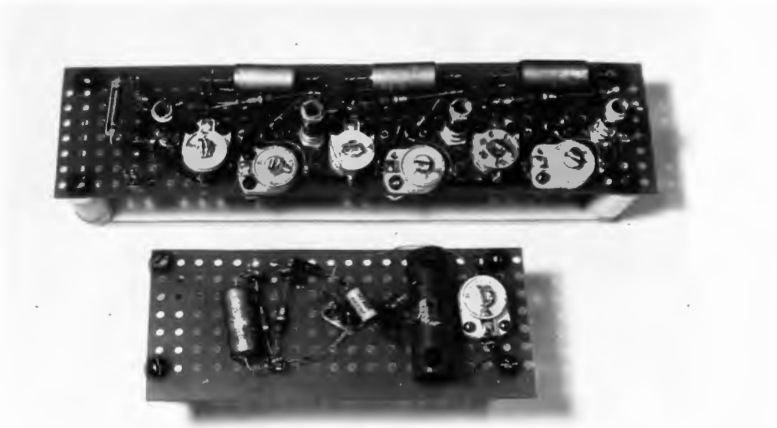


FIG. 14 ASSEMBLED UNITS

A. AMPLIFIER

B. OSCILLATOR

It was found that if the supply voltage was bypassed by a 4 ufrd tantalytic capacitor the oscillations ceased. This capacitor was put directly across the battery connections at the amplifier.

With the circuit funtioning properly the neutralization was retuned, to account for any slight variation due to the load changes since the initial adjustment was made with the circuit not terminated. Tuning was accomplished by plac-

ing the scope leads across the 427 ohm load resistance and tuning from the input to the output stage. This had the disadvantage of adding some shunt capacity to the final stage due to the 14 uuf present in the scope probe. This would be corrected in an actual circuit.

C. EVALUATION OF GAIN

The power gain of the transistors to be used in the amplifier were checked and found to have the gains shown in Table VI. These gains were obtain from a circuit which was terminated in 427 ohms.

TABLE VI POWER GAIN PER STAGE

UNIT	POWER GAIN
A	18
B	16
C	18.6

The actual power gains are somewhat less than the theoretical values due to the wide tolerances on parameters allowed in the manufacture, as an example, the variation allowed for h_{fe} is 11 to 36, a variation of over 300%. The coupling and bias networks may cause a reduction from the theoretical

power gain of .5 db. to 3 db., and the equation itself gives a slightly higher gain than can be obtained at the lower frequencies.

When the three amplifiers were cascaded the overall power gain was found to be approximately 49.4 db. There is margin for a large percentage of error in the measurement of the overall power gain due to the test equipment available. The measurement of voltages was accomplished by the use of a Techtronix Type 514 AD Scope whose vertical amplifier upper frequency limit was 10 Mc. The scope was the only voltage indicator available in that frequency range with sufficient sensitivity. The high frequency probe had to be used to keep shunt capacitance to a minimum which was 14 pfrds. The calibrated voltage range on the scope was from .03 to 50 volts peak to peak with a maximum vertical sensitivity of .03 volt per cm. The input voltage was on the order of .0015 volts. Therefore, the input voltage at best is a close approximation. The overall power gain of the three amplifiers in series was 49.4 db. Individually the amplifiers totaled to a gain of 52.6 db. which can be seen from Table VI. The power lost in the coupling networks can be computed from the equation $P_L = 10 \log_{10} 1/n$ where n is the efficiency calculated from Equation 34 Chapter V. The power lost is .66 db. and the efficiency is 86%.

Conclusions. The actual theoretical gain for the amplifier should be from 18 db to 21.6 db. Neglecting the losses in the coupling networks, the overall gain should be 54 to 64.8 db. depending on the value of $r_b'C_c$. The overall gain actually obtained was 51.38 neglecting coil losses. The gain obtained was slightly low, however, considering the limitations on the theoretical equation for power gain and parameter variations the results were reliable.

CHAPTER VII

THE VARIABLE FREQUENCY OSCILLATOR

A. INTRODUCTION

Quite frequently an alternating current energy source is required for some application, this energy can be supplied by a transistor oscillator. The purpose of this chapter is to design a radio frequency oscillator which will operate at 10 Mc. and be variably tuned. The main objective here is to obtain a design procedure, if a particular specification is desired once the procedure has been determined the design can be modified to fulfill these conditions.

B. DESIGN OF 10 MC VARIABLE FREQUENCY OSCILLATOR

Design procedure. It has been shown that the "T" equivalent circuit can be used in the analysis of transistor oscillators[12] if the effective capacitance across the collector to base region is assumed to modify the resonant frequency by its shunt capacitance. The use of the high frequency circuit in the analysis of oscillators provides accurate results in the establishing of conditions for oscillations.

The general feedback circuit is shown in Fig. 15

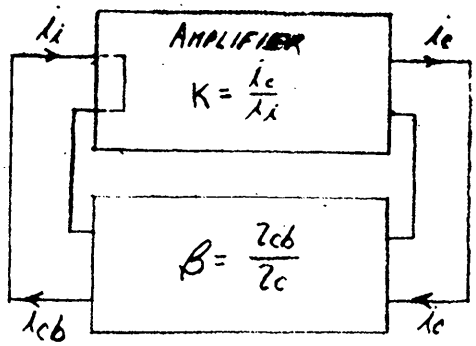


FIG. 15 GENERAL FEEDBACK CIRCUIT

The amplifier is assumed to have zero input impedance, an output impedance Z_o, a short circuit current amplification of A_i, and be unilateral. The feedback network has for a short-circuited output, an input impedance Z_i and a current amplification β.

The current amplification when the amplifier is working into the feedback network is

$$K = A_i \frac{Z_o}{Z_o + Z_i} \tag{40}$$

The starting condition for oscillation is that the total current amplification be unity, that is,

$$K\beta = A_i \left[\frac{Z_o}{Z_o + Z_i}\right] \beta = 1 \tag{41}$$

$$\beta = \frac{1}{A_i \frac{Z_o}{Z_o + Z_i}} \tag{42}$$

The transistor does not have zero input impedance, but, by combining the parameters r_b' and r_e' with the feed - back network the circuit is arranged as shown in Fig. 17.

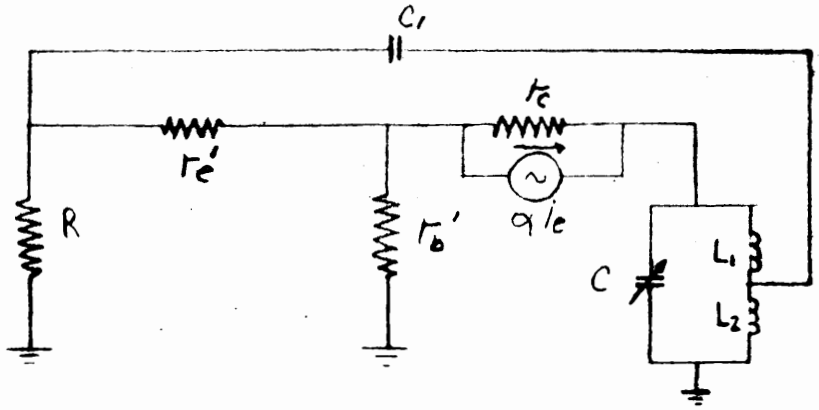


FIG. 16 HIGH FREQUENCY OSCILLATOR

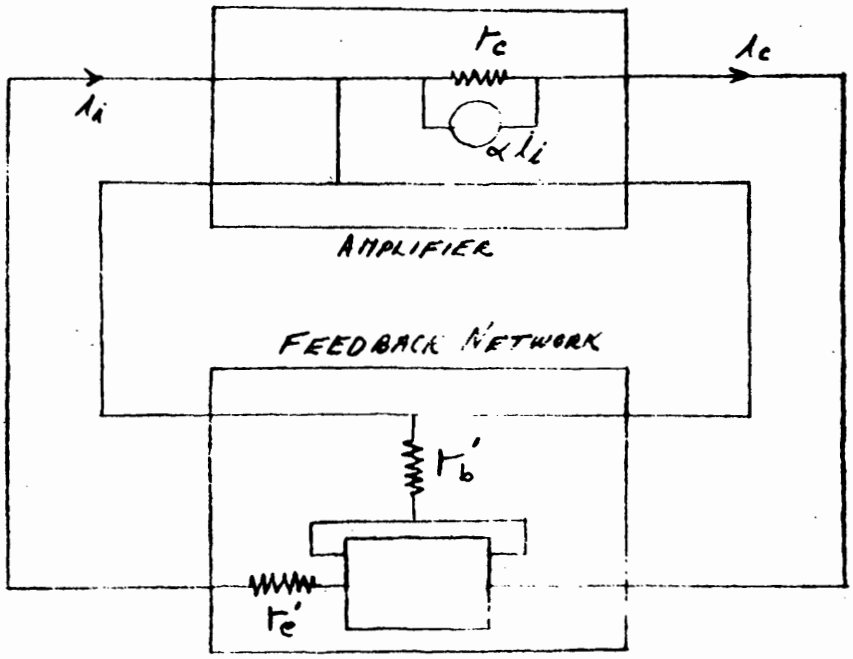


FIG. 17 GENERAL FEEDBACK DIAGRAM

If in Equation 42 r_c is substituted for Z_o and α for A_i

$$\beta = \frac{1}{\alpha}\left(1 + \frac{Z_i}{r_c}\right) \qquad (43)$$

The input impedance to the network is usually much less than r_c. With good approximation β is equal to $1/\alpha$. The feedback network can be represented as shown in Fig. 18 if $i_c = i_1$ and $i_e = i_3$

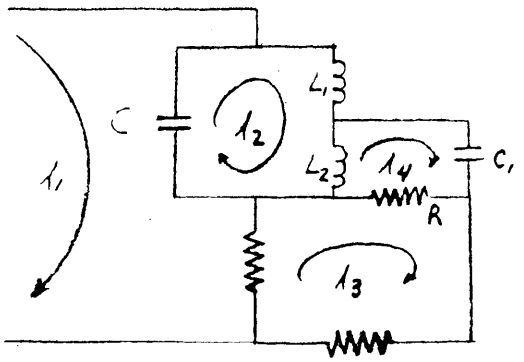


FIG. 18 FEEDBACK NETWORK

β will be equal to i_3/i_1 which is the current amplification of the feedback network. The analysis may be simplified if it is realized that the capacitance C_1 provides feedback to the emitter circuit. If X_{C_1} is made small in comparison to the input impedance of the emitter circuit it can be neglected with little loss of accuracy. The resistance R which shunts the emitter input can be neglected if it is required that R be much larger than the input impedance of the transistor. The function of R is twofold, it developes the feedback voltage, and provides bias to the amplifier. When these approximations are incorporated in the feedback network the resultant circuit is shown in Fig. 19.

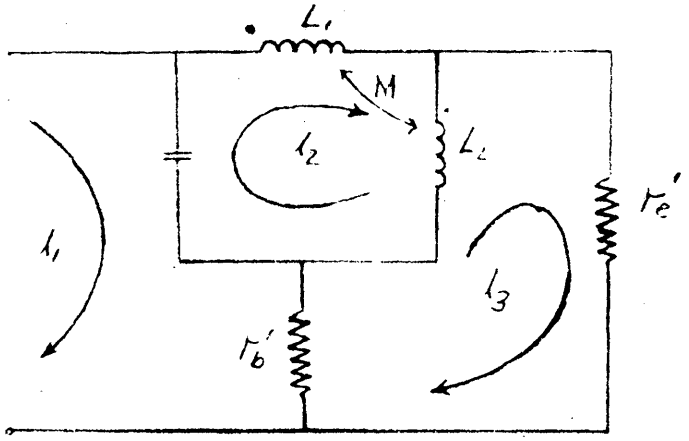


FIG. 19 APPROXIMATE FEEDBACK NETWORK

The resulting loop equations are:

$$i_2\left(\rho L_T + \frac{1}{\rho C}\right) = i_1 \frac{1}{\rho C} + i_3(\rho L_2 + \rho M) \tag{44}$$

$$i_3(\rho L_2 + r_e' + r_b') = i_2(\rho L_2 + \rho M) + i_1 r_b' \tag{45}$$

WHERE $L_T = L_1 + L_2 + 2M$

Eliminating i_2 from the above equations

$$i_1\left[\frac{L_2+M}{C} + r_b'\left(\rho L_T + \frac{1}{\rho C}\right)\right] = i_3\left[\left(\rho L_T + \frac{1}{\rho C}\right)(\rho L_2 + r_e' + r_b') - (\rho L_2 + \rho M)\right] \tag{46}$$

Solving for i_3/i_1 = the result obtained is

$$\frac{i_2}{i_1} = \frac{\frac{L_2+M}{C} + r_b'\left(\rho L_T + \frac{1}{\rho C}\right)}{\left(\rho L_T + \frac{1}{\rho C}\right)\rho L_2 - (\rho L_2 + \rho M)^2 + (r_e' + r_b')\left(\rho L_T + \frac{1}{\rho C}\right)} \tag{47}$$

In the analysis of the feedback network it was found for the loop gain to be unity a β was required which was approximately equal to $1/\alpha$. To effect this relationship Equation 47 was set equal to $1/\alpha$:

$$\frac{1}{\alpha} = \frac{(L_2 + M)/C + r_b'(\rho L_T + \frac{1}{\rho C})}{(\rho L_T + \frac{1}{\rho C})(\rho L_2) - (\rho L_2 + \rho M)^2 + (r_e' + r_b')(\rho L_T + \frac{1}{\rho C})} \qquad (48)$$

The real part of the numerator multiplied by α was set equal to the real part of the denominator, and the imaginary part of the denominator was set equal to γ multiplied by the real part of the numerator.

Equating the imaginary parts

$$\alpha r_b'(\rho L_T + \frac{1}{\rho C}) = (r_e' + r_b')(\rho L_T + \frac{1}{\rho C}) \qquad (49)$$

For this to be an equality ($pL_T + 1/pC$) must be zero. Thus, at resonance the effective series impedance of the tank circuit is zero. The resistance of the coil was neglected since the Q of the coil was approximately 150. Equating ($pL_T + 1/pC$) to zero we obtain

$$\omega^2 = \frac{1}{L_T C} \qquad (50)$$

Equating the real parts the following relationship is obtained:

$$\alpha \frac{L_2 + M}{C} = \rho L_2 (\rho L_T + \frac{1}{\rho C}) - \rho^2 (L_2 + M)^2 \qquad (51)$$

Since ($pL_T + 1/pC$) is equal to zero

$$\alpha \frac{L_2 + M}{C} = -(\rho L_2 + \rho M)^2 \qquad (52)$$

from which the magnitude of $(L_2 + M)$ relative to L_t for oscillations to start is obtained

$$\alpha = \frac{L_2 + M}{L_T} \qquad (53)$$

This means that $L_2 + M$ must be very much larger than $L_1 + M$. It was found, however, the point at which the tap for feedback was placed on the oscillator coil was not critical. Oscillations were started and sustained by the oscillator for turns ratios of $2/22 < N_1/N_2 < 22/22$. The inductance used had a value of 15.5 micro henries and was resonated with a capacitor which could be varied from 5 to 20 pfrds.

The frequency range over which the circuit was tunable was to be theoretically 9.2 Mc to 16.8 Mc. The values obtained from the circuit were 9.48 Mc and 16.65 Mc. This resulted in a 2.9% error at the low end and a 1.2% error at the high end. The instrument used in the determination of frequency was the Techtronix Type 514 AD Oscilloscope which has a maximum sweep of .1 usec/per cm. At ten megacycles a reasonable approximation to the actual signal frequency is obtained. There is a high probability of error in reading the scope face, since 1/20 th of a centermeter error in reading the scope results in a 1/2 megacycle error in frequency. The stability of the oscillator could not be deter-

mined due to the limitations of the available measuring equipment.

The tunable range of frequencies was 16.65 Mc to 2.5 Mc. The upper limit could be extended if small values of inductance were used. The lower limit could be extended if larger values of inductance were used. Decreasing the frequency to 2.5 Mc by the addition of capacitance caused a continued decrease in collector load impedance to such an extent that oscillations could no longer be sustained.

The output was taken from the voltage developed across the emitter resistor R shown in Fig. 18. If maximum output power from the unit was required it could be obtained by transformer coupling. The coupling required to effect maximum power is determined by matching the load to the output impedance of the transistor assuming Class A operation. The circuit output is determined by the maximum voltage swing of the collector. The oscillations build up until the power dissipated is equal to the power generated or until a point of nonlinearity is reached preventing a further change in collector current.

Bias network. The bias network used on the oscillator was the same one designed for the grounded emitter amplifier and provided good results. The legitimacy of using this same

network is verified if the effect on stability is examined due to a 2 K resistance in the emitter circuit. The stability is defined by Equation 30. This change in R_1 results in a value of S = 1.12 instead of 2.94.

Conclusion. The frequency output of the oscillator was described adequately by the equations developed, and the condition for oscillations to start was verified.

CHAPTER VIII

SUGGESTIONS FOR ADDITIONAL INVESTIGATION

In the course of this study on transistors the author became aware of three additional subjects which might prove fruitful if investigated. Specific problems are not presented here but, rather, a general area which might be considered for additional developement.

Intermediate frequency amplifiers to be used in a communication receiver usually must have provisions for automatic gain control. The gain control of stages is important when the input signal varies in intensity. This might be caused by radio frequency "skip" of signals which depend on the refractive effects of the ionosphere for long distance transmission.

Vacuum tube tranconductance can be easily varied by changing the operating point, providing easy control of the gain. Transistors, however, have essentially the same current gain over a wide variation of the operating point. A dependable means by which this gain can be adequately controlled presents an interesting problem.

Mixer circuits and converters are important to re-

ceivers and an investigation of the design of these two circuits would be valuable. An understanding of the design of the two circuits presented in this thesis, and the three additional subjects mentioned here, should prove helpful to an engineer considering a future in transistor circuit design.

BIBLIOGRAPHY

1. Stern, Aldridge, and Chow, "Neutralization of Transist Amplifiers," The Proceedings of the IRE, Vol. 43, pp.8 847, July, 1955.

2. Chu, G.Y., "Unilaterization of Junction Transitors," The Proceedings of the IRE, Vol. 43, pp. 1001-1006, August, 1955.

3. Philco Corp., "Tuned Amplifiers Design," Application Notes, Note 1, Form LTC 450, December 1959.

4. Angell, J.B., "High Frequency and Video Amplifiers," Handbook of Semiconductor Electronics, pp. 12-1,-12-26 McGraw Hill Book Company, New York, 1956.

5. Ghandi, S.K., "Analysis and Design of Transistor Bias Networks," Proceedings of the National Electronics Conference, Vol. 12, pp. 491-503, 1956.

6. Shea, R.F., "Transistor Circuit Engineering" pp. 55-59 John Wiley & Sons, Inc., New York, 1957.

7. Gottlieb and others, "General Electric Transistor Manual," pp. 36-39, General Electric Company, New York 1959.

8. Van Voorhis, S.M., "Microwave Receivers," Radiation Laboratory Series, Vol. 23, pp. 163-169, McGraw Hill Book Co.,

9. Shea, R.F., "Transistor Circuit Engineering," pp.160-172.

10. Sealy, S. "Radio Electronics," pp. 225-6, McGraw Hill Book Co., New York, 1956.

11. Pritchard, R.L., "High Frequency Amplifier Gain of Junction Transistors," The Proceeding of the IRE, Vol. 44, 1050-1052, August, 1956.

12. Shea, R.F., "Principles of Transistor Circuits," pp. 2 229, John Wiley & Sons, Inc., New York, 1953.

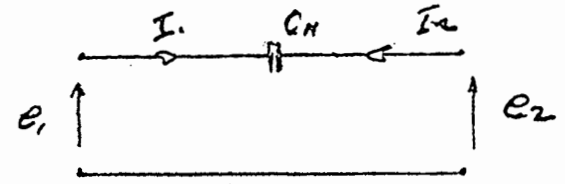
13. Shea, R.F., "Principles of Transistor Circuits," pp. 3 340.

APPENDIX I

A. PARTIALLY NEUTRALIZED OUTPUT IMPEDANCE

The following is a determination of the partially neutralized output impedance of a transistor using a high frequency equivalent circuit. The procedure presented provides a method for determination of the output impedance with a feedback path. The equations presented here are of the transistor alone and do not consider the stray capacitance which is present in a practical circuit.

The neutralizing network is shown in Fig. 20.



$$y_{11} = j\omega C_N \qquad y_{12} = -j\omega C_N$$

$$y_{21} = -j\omega C_N \qquad y_{22} = j\omega C_N$$

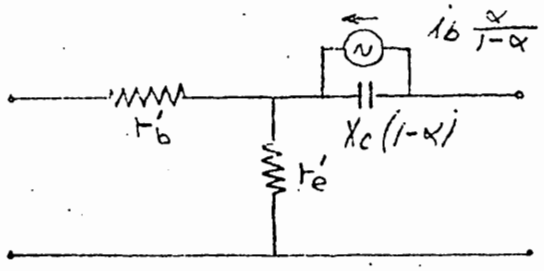
FIG. 20 NEUTRALIZING NETWORK

The short circuit admittance equations for the neutralizing circuit are

$$I_1 = e_1 y_{11} + e_2 y_{12} \tag{54}$$

$$I_2 = e_1 y_{21} + e_2 y_{22} \tag{55}$$

Fig. 21 is the high frequency equivalent circuit of the transistor.



$$Z_{11} = r_b' + r_e' \qquad Z_{12} = r_e'$$

$$Z_{21} = r_e' + j X_c \alpha \qquad Z_{22} = r_e' - j X_c (1-\alpha)$$

FIG. 21 TRANSISTOR EQUIVALENT CIRCUIT

The determinant of the open circuited z parameters in Fig. 21 is

$$\Delta_Z = Z_{11} Z_{22} - Z_{12} Z_{21} = r_b' r_e - j X_c (r_b')(1-\alpha) r_e' \quad (56)$$

The neutralizing circuit is in parallel with the transistor, therefore, if the transistor z parameters are converted to y parameters, they can be added together as shown in Equation 60.

The open circuit impedance equations are

$$e_1 = Z_{11} I_1 + Z_{12} I_2 \quad (57)$$

$$e_2 = Z_{21} I_1 + Z_{22} I_2 \quad (58)$$

Conversion of the open circuit parameters to their equivalent y parameters is shown in Equation 59.

$$[y'] = \begin{bmatrix} \frac{z_{22}}{\Delta z} & -\frac{z_{12}}{\Delta z} \\ -\frac{z_{21}}{\Delta z} & \frac{z_{11}}{\Delta z} \end{bmatrix} \tag{59}$$

The array for the short circuit admittance parameters of the neutralizing network and transistor is

$$[y''] = \begin{bmatrix} y_{11}+y_{11}' & y_{12}+y_{12}' \\ y_{21}+y_{21}' & y_{22}+y_{22}' \end{bmatrix} \tag{60}$$

The determinant of the array is

$$\Delta y'' = y_{11}''y_{22}'' - y_{12}''y_{21}'' = \frac{1}{\Delta z}\left[1 + \alpha\frac{1}{X_{cn}}(r_b' - jX_c)\right] \tag{61}$$

The output impedance with a generator admittance equal to y_g ($y_g = 1/R_g$) is

$$Z_o = \frac{y_{11}'' + y_g}{\Delta y'' + y_{11}''y_g} = \frac{2r_e' + r_b'(1-\alpha) - \alpha\left(\frac{X_c}{R_g}\left[r_e' + r_b'(1-\alpha) + 1 - \alpha\right]\right)}{2 + \frac{r_e'+r_b'}{R_g} + \alpha\frac{r_b'}{X_{cn}} - \frac{r_e + r_b'(1-\alpha)}{R_g}} \tag{62}$$

where $R_g \ll X_{cn}$.

The parameters values are $r_o' = 13.5$, $r_b' = 110$ ohms, $C_c = C_n = 1.5$ pfrds, and $R_g = 204$ ohms. The resulting value for Z_o is 12.82 - j595 ohms.

B. SHORT CIRCUIT OUTPUT IMPEDANCE

The open circuit z parameters of the transistor are shown in Equations 57 and 58. Solving for Z_o with e_1 equal to zero yields

$$Z_o = \frac{e_2}{i_2} = -\frac{Z_{12} Z_{21}}{Z_{11}} + Z_{22} \qquad (63)$$

$$= \frac{r_e' r_b'}{r_b' + r_e'} - j X_c \left[(1-\alpha) + \alpha \frac{r_e'}{r_b' + r_e'} \right] \qquad (64)$$

Substituting values as in part A the output impedance obtained is 12 - j1610 ohms

An examination of the Equations for Z_o in part A and B shows the resistive components to be approximately equal and, the capacitance to differ by 11 pfrds.

APPENDIX II

SHORT CIRCUITED INPUT IMPEDANCE DETERMINATION

The equivalent circuit used to determine the input impedance is shown below in Fig. 22.

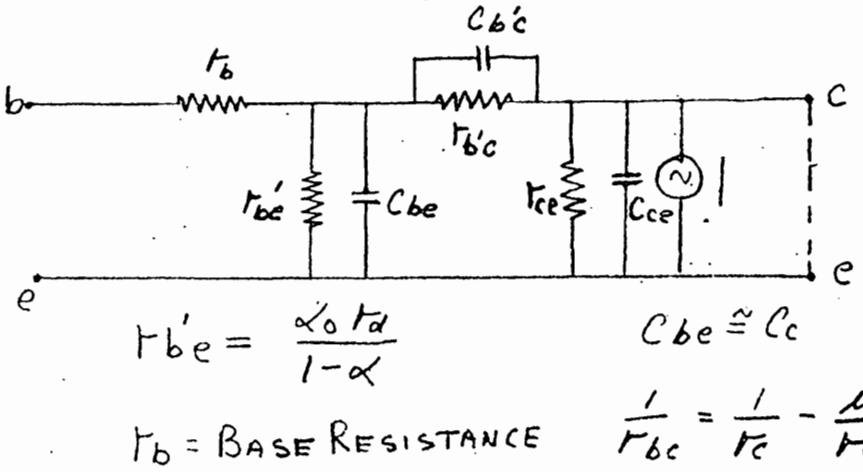


FIG. 22 TRANSISTOR EQUIVALENT CIRCUIT

When the collector and emitter are shorted the resulting input impedance is

$$Z_{IN} \cong r_b + \frac{r_{b'e}\left[-j\omega(C_{be}+C_{b'e})\right]}{r_{b'e} - j\omega(C_{be}+C_{b'c})} \qquad (65)$$

SINCE $r_{b'c} \gg r_{b'e}$

$$C_{b'c} = \frac{1}{2\pi\alpha_0 r_d f_\alpha^{co}} = 205\ \text{pfds} \qquad (66)$$

$$X_c = \frac{1}{\omega(C_{b'e} + C_{b'c})} = 78.1\,\Omega \qquad (67)$$

The input impedance calculated from Equation 65 is 486 - j71.5 ohms. The parameter values are given in Appendix I.

VITA

Robert C. McIntyre was born on June 22, 1932, in Brooklyn, New York. He attended parochial grammar school from 1938 to 1946. In 1946 he entered Brooklyn Technical High School, from which he was graduated in 1950.

After completion of high school the author was employed by the Plant Department of the New York Telephone Co. and attended Brooklyn College Evening School until December 26, 1951. On December 26, 1951 he entered the United States Air Force where he attended various electronics schools including Radar and Radio Communications. He served as a Technican and Electronics Instructor, and attended Belleville Junior College Evening School from September 1954 to June 1955. Upon completion of his military obligation he entered Belleville Junior College as a full time student. He transferred to the University of Missouri School of Mines and Metallurgy in September 1956 from which he was graduated in June of 1959 and received the Degree of Bachelor of Science in Electrical Engineering.

In January of 1959 he entered the University of Missouri School of Mines and Metallurgy as a graduate student with an assistantship in the Electrical Engineering Department. He is a member of Eta Kappa Nu, and IRE.