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HARD-SWITCHED SWITCHED CAPACITOR CONVERTER DESIGN

by

LUKAS KONSTANTIN MÜLLER

A THESIS

Presented to the Faculty of the Graduate School of

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in Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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Approved by

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ABSTRACT

Switched capacitor (SC) converters are becoming quite popular for use in DC-DC power conversion. The concept of equivalent resistance in SC converters is frequently used to determine the conduction losses due to the load current. A variety of methodologies have been presented in the literature to predict the equivalent resistance in hard-switched SC converters. However, a majority of the methods described are difficult to apply to general SC converter topologies. Additionally, previous works have not considered all nonidealities in their analysis, such as switching losses or stray inductances. This work presents a generalized and easy to use model to determine the equivalent resistance of any high-order SC converter. The presented concepts are combined to derive a complete loss model for SC converters.

The challenges of implementing output voltage regulation are addressed as well. A current-fed SC topology is presented in this work that overcomes the problems associated with voltage regulation. The new topology opens up a variety of additional operating modes, such as power sharing. These additional operating modes are explored as well.

The presented concepts are verified using digital simulation tools and prototype converters.

ACKNOWLEDGMENTS

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1. INTRODUCTION

Both the design and application of Switched Capacitor (SC) converters have received increased attention in recent years [2,3,7–9,13,15,16,19–21,24–27,30,34,36–39, 42,44,50,51,56,58–60,66]. The absence of magnetic components allows SC converters to be smaller and lighter, produce less electromagnetic interference, and feature high power densities [13, 16, 20, 25, 38, 42, 51, 59]. A large variety of SC topologies exist, allowing both voltage step-up and step-down functionality [9, 16, 24, 38].

The fundamentally different operation of SC converters prohibits the use of classical analysis approaches used in magnetic-based converters. Initially, most analysis approaches focused solely on the operation of the capacitors in SC converters. Instead of using the Volts-seconds balance in the inductors, the charge balance of the capacitors was used [60]. The resulting model was utilized to predict the output voltage and efficiency of SC converters. The capacitor-based model works well at low switching frequencies where the dynamics of stage capacitors dominate the operation of the converter. However, similar to magnetic converters, the presence of parasitic resistances, capacitances, and inductances influence the operating behavior of SC converters. For instance, at high switching frequencies the parasitic resistances of the converter switches and capacitors dominate converter operation. In this operating region, the charge-balance approach is unable to predict the performance characteristics of SC converters. Some works apply the charge-balance analysis approach to all operating areas of SC converters, resulting in improper design methodologies of SC converters [12, 28, 29]. More sophisticated methods need to be utilized to characterize SC converter operation.

One popular method used to characterize the performance of power converters is state-space averaging. State-space averaging can also be applied to SC converters, allowing output voltage and dynamic response to be accurately determined [15, 26, 27, 42, 44]. While state-space averaging offers a high degree of accuracy, it can be difficult to implement. Additionally, state-space averaging does not reveal the effects of individual stage components on overall converter performance. This makes state-space averaging more difficult to use in the initial design of an SC converter, where

appropriate components must be selected for each converter stage. Another design methodology utilizes the capacitor charge balance, as well as a model accounting for parasitic resistances in the SC converter. The charge-balance method is generally referred to as the Slow Switching Limit, and models behavior of the stage capacitors. The Fast Switching Limit is used to predict converter behavior when the effects of parasitic resistances dominate. The Slow Switching and Fast Switching Limits form asymptotes that bound the equivalent resistance of the SC converter [3, 4, 19, 30, 50]. The limits do not predict the operation of the converter in intermediate frequency regions. Curve-fits were developed based on the limits to provide an accurate and easy-to-use equation which predicts the equivalent resistance at all operating points [3,4,19,20,50]. The switching limits with their associated curve-fit have the advantage of being easy to use, allowing designers to identify the impact each component has on overall converter performance; on the other hand, the switching limits are less accurate and only predict the steady-state converter behavior. This makes the limit-based equations a preferable choice for initial SC converter designs.

Neither state-space averaging nor switching limit equations account for switching losses or standby losses in an SC converter. Therefore, they are insufficient to derive a complete performance model of an SC converter design - especially at high switching frequencies or low load levels, where standby and switching losses have a significant impact on converter performance. These losses need to be accounted for to enable a comprehensive converter design. Because conduction losses can be modeled as an equivalent resistance, the switching losses should be modeled as an equivalent circuit component. This results in a complete model accounting for all loss mechanisms in an SC converter using a simplified equivalent circuit.

Another common challenge with SC converters is output voltage regulation. Increasing the equivalent resistance of the SC converter is the most common method to realize output voltage regulation [14, 55, 67, 68]. This method, however, also leads to increased losses. Implementing a converter, which can change its equivalent topology to modify its target voltage, is a more efficient approach [9, 10, 46, 53]. Implementing this type of SC converter is more costly and complex though. Current-fed SC converters can produces a regulated output voltage, without sacrificing efficiency or ease of implementation [23,32,40,63,64]. A current-fed Cockcroft-Walton converter is

presented in this work to illustrate the design procedure for current-fed SC converters and demonstrate their operating performance.

The topics touched on in the introduction are presented in detail in the following sections. The conduction losses and equivalent resistance are derived for a simple SC converter in Section II. A way to apply the concepts shown in Section II to all types of higher SC converters is shown in Section III. Section III also discusses additional loss mechanics in SC converters, such a switching, gate driver, and standby losses. The presented equivalent resistance and switching loss calculations are used to derive an overall loss model for any order SC converters. Section IV. addresses the challenges associated with output voltage regulation. A current-fed Cockcroft-Walton multiplier is also presented in great detail in Section IV to illustrate a design methodology for current-fed SC converters. Concluding remarks are given in Section V.

2. SC EQUIVALENT RESISTANCE

Conversion efficiency is a major concern in power converter design. In the past, SC converters suffered from the stigma of a far lower efficiency than their inductor/-transformer based counterparts. This misconception originated from SC converters' fundamentally different operating characteristics. In magnetic converters the volt-second balance of the inductor is used as the primary means of deriving the steady-state behavior [17]. For basic derivations, the current through the inductor can be considered constant. In a more accurate analysis, the current waveform through an inductor is still well defined by basic circuit equations. Similarly, the voltages over the input, stage, and output capacitors are well known. The consistent and well-known operating condition of the individual components makes magnetic converters easy to analyze. Additionally, the interaction between magnetic components and capacitors are well known for traditional converter topologies.

In contrast, basic SC converters do not have any inductors or transformers that dictate the flow of current in the converter. The steady-state behavior of SC converters must be derived entirely from the charge balance of the stage capacitors [60]. Due to the lack of inductors, the current flow is dictated by RC circuit equations. While the current changes linearly in inductors, the current wave shape is exponential in an RC circuit. This non-linearity complicates the analysis. In addition, the current wave shape depends far more on the component and timing parameters in an RC circuit. The increased complexity in analyzing the operation of SC converters is the source of the common misconception about SC converter performance and operation [7, 12, 29].

The charge transfer in SC converters is analyzed in detail in this section. Many equations and methodologies exist to predict the equivalent resistance of SC converters. The concepts of a Slow Switching Limit (SSL) and a Fast Switching Limit (FSL) have proven useful in providing a rough approximation of equivalent resistance [3, 19, 30, 50]. A number of studies have used each of these concepts to provide more accurate predictions [3,19,20,50]. State-space averaging is another methodology commonly used to accurately and automatically determine the equivalent resistance

of SC converters [15, 26, 27, 42, 44]. State-space averaging, however, can be computationally intensive and does not reveal the effects a specific component has on the overall equivalent resistance of the converter. A complete, comprehensive, and easy to use derivation of well accepted SC converter concepts will be presented here. The hope is, that the work shown here clarifies the derivation of the equivalent resistance in SC converters. Additional concepts, which were not presented in previous works, are derived here as well. This allows the derivation of a complete model of equivalent resistance in SC converters for a wide operating range.

2.1. TRADITIONAL SOLUTION

As mentioned previously, there are a multitude of approaches with which one can analyze the charge transfer efficiency between capacitor. The most fundamental approach involves determining the total energy stored at the beginning and end of the charge transfer [12, 13]. To demonstrate this approach take the simple circuit shown in Figure 2.1. The circuit consists of two capacitors C_1 and C_2 as well as an

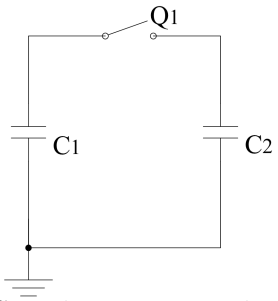

Figure 2.1. Simple capacitor charging circuit

ideal switch, denoted as Q_1. Both capacitors have the same value of capacitance, denoted as C. Initially the voltage of C_1 is equal to V_1, while C_2 has no charge, and, therefore, no voltage. The switch Q_1 is open and does not conduct any current. The capacitors are assumed to be ideal charge storage devices. They do not exhibit any self-discharge. The energy stored in the system capacitors can be found using the fundamental equation:

$$E = \frac{1}{2}CV^2 \tag{1}$$

Therefore, the energy stored in the overall system is equal to:

$$E_{total} = \frac{1}{2}CV_1^2 + \frac{1}{2}C\left(0\right)^2 = \frac{1}{2}CV_1^2 \tag{2}$$

With the initial state of the system known, Q_1 is closed to connect both capacitors in parallel. Both capacitors are in parallel, therefore, they will charge/discharge to the same voltage level. Basic circuit equations can be used to find the voltage across both capacitors to be $\frac{1}{2}V_1$. The total system capacitance is now equals to $2C$, as both capacitors are in parallel. Solving equation (1) for the new system will yield:

$$E = \frac{1}{2}2C\left(\frac{1}{2}V_1\right)^2 = \frac{1}{4}CV_1^2 \tag{3}$$

Looking at (2) and (3) it can be seen that the total energy in the system has decreased by a factor of two. Half the energy stored in the system was lost during the charge transfer between C_1 and C_2. As the capacitors were assumed to be ideal storage devices, the energy was lost in the resistive elements of the circuit. The circuit used to derive this example did not have any resistances specified though. As a matter of fact, no equations relying on any specific resistances, capacitances, or voltages were used. This demonstrates that the maximum efficiency of one capacitor charging another completely discharged capacitor is 50%. This value is independent of the resistances or capacitances encountered in the circuit, it only relies on the the fact that one capacitor is completely discharged and the system is given enough time to settle to a final value (let the first capacitor fully discharge into the other capacitor). This example demonstrates that charge transfer between two capacitors (two voltage sources in parallel) is inherently prone to loss, unlike energy transfer between a voltage source and a current source (capacitor and inductor).

The above example describes an extreme case, where C_2 was completely discharged, however, the transfer efficiency changes when the initial conditions are different. The same circuit setup as in the previous example is used, except C_1's voltage is equal to $V_{initial}$ and the voltage across C_2 is equal to $\frac{1}{2}V_{initial}$. The total energy in

this system is equal to:

$$E_{total} = \frac{1}{2}CV_1^2 + \frac{1}{2}C\left(\frac{1}{2}V_{initial}\right)^2 = \frac{10}{16}CV_1^2 \tag{4}$$

Again, switch Q_1 is closed to allow a charge transfer between C_1 and C_2. Allowing enough time for the voltage to equalize between C_1 and C_2 will result in a new steady state voltage of $\frac{3}{4}V_{initial}$. The total energy in the system, when the voltage is equalized, is equal to:

$$E_{total} = \frac{1}{2}2C\left(\frac{3}{4}V_{initial}\right)^2 = \frac{9}{16}CV_{initial}^2 \tag{5}$$

In this example, it can be seen that 90% of the energy initially in the system is still present after the charge transfer. During the charge transfer only 10% of the energy is lost compared to the 50% when the capacitor was uncharged. This demonstrates the relation between the initial voltage difference between the capacitors and the charging efficiency. This relationship is illustrated in Figure 2.2. The results presented in Figure 2.2 demonstrate that to obtain an efficient charge transfer between two capacitors, their voltages should deviate little from one another.

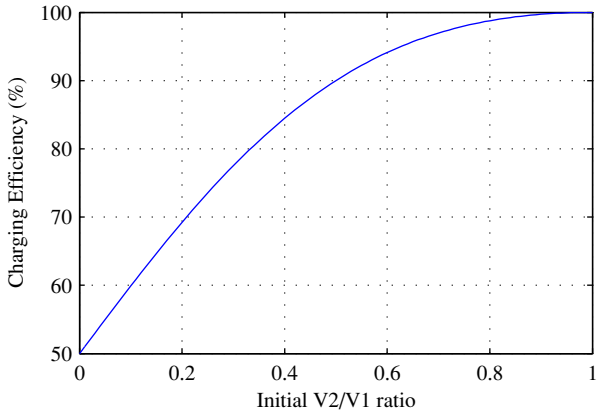

Figure 2.2. Charging efficiency vs. initial capacitor voltages

The above example illustrates a number of important aspects of capacitor charging behavior. By nature, the process is prone to loss, meaning a significant portion

of the energy in the system can be lost, if proper care is not taken. Additionally, the charge transfer efficiency can be significantly improved by reducing the voltage difference between the capacitor providing the charge and the capacitor being charged [13].

The above example is only useful as an illustration. The shown circuit is not practical as it is connected to neither a source nor a load, however, the concepts demonstrated can be used in a more practical example.

2.2. SLOW SWITCHING LIMIT

The inherent losses associated with charging capacitors from other capacitors is shown in the previous section. As traditional hard switched SC converters only have capacitors this aspect is very important. The circuit used in the previous example is a poor representation of actual SC converters, therefore, a different circuit is used for the following derivations (illustrated in Figure 2.3). This converter is the most

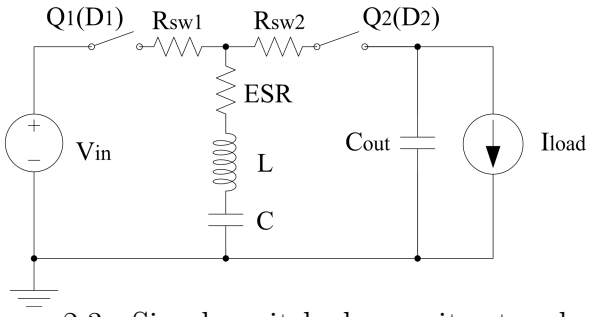

Figure 2.3. Simple switched capacitor topology

fundamental SC converter available. It is typically used for basic derivations [3, 8, 13, 19, 20, 30]. The converter is supplied by a voltage source with a voltage of V_{in}. Capacitor C_1 is the stage capacitor with a capacitance value of C. The stage capacitor does not experience any self-discharge as in the previous section. The capacitance of the output capacitor C_{out} is assumed to be large enough that its voltage remains constant [17]. The switches Q_1 and Q_2 transition instantaneously. The switch states are inverse from one another, when Q_1 is on Q_2 is off and vice versa. The interval in which Q_1 is conducting is labeled Mode 1. The duty cycle of Mode 1 is given by D_1.

Q_2 is conducting during Mode 2, with a duty cycle of D_2. There may be a Mode 3 in which neither switch is conducting. This occurs if $D_1 + D_2$ is less than 100%.

For the derivation in this section, Mode 1 and Mode 2 are long enough that the respective capacitor has enough time to be fully charged. The switching frequency of the converter is therefore low. Mode 1 and Mode 2 are of equal length, which means they have the same duty cycle. A constant load current I_{load} is drawn from the converter at all times. As the switching frequency is low, the effects of the inductor can be ignored. All resistances can be lumped into 1 resistor, R, which represents all resistances present in the circuit [30].

With these assumptions in mind, the circuit in Figure 2.3 can be simplified to the equivalent circuit shown in Figure 2.4. As in the previous section, the concept

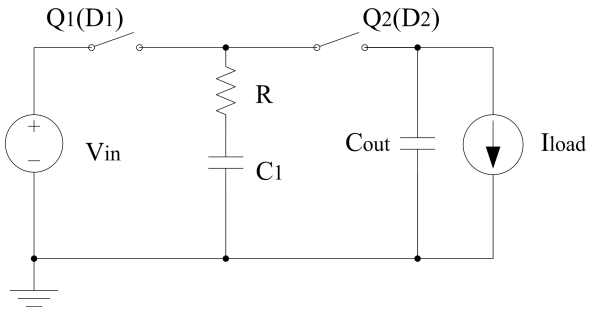

Figure 2.4. Equivalent simple SC converter model for slow switching frequencies

of charge will be used to analyze the states of the capacitors. The load draws a constant current at all times, therefore, the amount of charge extracted from the output capacitor is given by

$$Q_{out} = I_{load}\left(t_{mode1} + t_{mode2}\right) = \frac{I_{load}}{f_{sw}} \tag{6}$$

The converter is assumed to be in steady state, therefore the same amount of charge drawn from C_{out} has to be supplied to it. This guarantees that the voltage of C_{out} remains constant. The stage capacitor C_1 supplies the required charge Q_{out} to the output capacitor during Mode 2. The charge in the stage capacitor is replenished during Mode 1 by the voltage source. The frequency of the converter is assumed low

enough that the capacitors can always be fully charged, therefore, the stage capacitor C_1 will be charged to a voltage level equal to that of the input voltage source (V_{in}) during Mode 1. During Mode 2, the stage capacitor transfers charge to the output capacitor. The voltage of C_1 decreases as described by

$$\Delta V = \frac{\Delta Q}{C} = \frac{I_{load}}{f_{sw}C} \tag{7}$$

This causes the voltage of the stage capacitor to be equal to $V_{in} - \frac{I_{load}}{f_{sw}C}$ at the end of mode 2. As C_1 is charging C_{out}, the maximum voltage of C_{out} is equal C_1's voltage at the end of mode 2. The voltage across C_{out} is constant, therefore, the output voltage of the converter is equal to:

$$V_{out} = V_{in} - \frac{I_{load}}{f_{sw}C} \tag{8}$$

The efficiency of the converter is then equal to:

$$\eta = \frac{\left(V_{in} - \frac{I_{load}}{f_{sw}C}\right) I_{load}}{V_{in}I_{load}} = \frac{V_{in} - \frac{I_{load}}{f_{sw}C}}{V_{in}} = \frac{V_{out}}{V_{in}} \tag{9}$$

Equation (9) demonstrates that the power losses during the charge transfer between the stage capacitor and output capacitor causes the output voltage to drop. There are a number of publications that conclude from (9) that lower output voltages results in lower converter efficiencies [12, 28, 29]. However, in reality, lower converter efficiency results in a lower output voltage.

Equation (9) shows that the SC converter voltage and efficiency decreases with increasing load current. The loss in voltage over the stage capacitor can be rewritten as:

$$\Delta V = \frac{1}{f_{sw}C} I_{load} \tag{10}$$

Equation (10) resembles Ohm's law. Current flowing through a resistor will result in a drop of voltage. The stage capacitor is acting as a resistor in the circuit. The voltage drop is due to its equivalent resistance. Power is lost due to the presence of

the capacitor as well, however, it is important to note that the power is lost in the parasitic resistances in the circuit not the capacitor itself.

Using Ohm's law and (10) the equivalent resistance of the stage capacitor can be expressed as:

$$R_{eq,capacitor} = \frac{1}{f_{sw}C} \tag{11}$$

Equation (11) can be used to determine the equivalent resistance of a stage capacitor, as long as the initial assumptions are respected. The equation is generally referred to as the Slow Switching Limit(SSL) in the literature [3, 19, 20, 30, 37, 50]. The most important assumption is the fact that the switching frequency has to be sufficiently low to give all capacitors sufficient time to fully recharge during each switching cycle. Naturally, the question arises what time period of frequency is sufficient to insure that this fact holds. The charge characteristics of a capacitor are described by the basic RC circuit equation:

$$V_c(t) = V_{in}\left(1 - e^{\frac{-t}{RC}}\right) \tag{12}$$

where the product of RC is the time constant of the circuit. Traditionally it is assumed that $V_c(t) = V_{in}$ after 5 time constants have elapsed. Equation (12) demonstrates the role of the resistance in the circuit, which was not previously explored. At lower switching frequencies ($f_{sw} \leq \frac{1}{10RC}$) the circuit resistance does not influence the equivalent resistance of the converter, however, the resistance does influence the time constant of the circuit, which in turn influence the frequency range in which (11) is valid.

It was established that the power losses caused by the capacitor charging process can be modeled as an equivalent resistance. For switching frequencies where the charge period is longer than 10 time constants (11) can be used to model the equivalent resistance of a capacitor. This equivalent resistance value can then be used to determine the converter power losses, voltage loss and efficiency.

2.3. FAST SWITCHING LIMIT

In the previous section, the concept of equivalent resistance was established, as well as an equation derived to predict its value at low switching frequencies. However, the equation ceases to work if the switching frequency is high enough that the capacitors can no longer be fully charged during one time period.

Starting with the circuit in Figure 2.3, some assumptions can be made to modify the circuit. In this example, the switching frequency is assumed to be high enough that the stage capacitor voltage does not vary [7,19,50]. This allows all capacitors to be modeled as voltage sources with a constant voltage [7,19,50]. The resistances in the charge and discharge loop can be lumped together and modeled as one resistor with resistance R. It is assumed that the resistances in the charge and discharge loop are equal to one another, therefore R is the same for both modes. The switching frequency is high, however still low enough so that the stray inductance L is not effecting the operation of the converter. With these assumptions the circuit in Figure 2.3 can be represented by Figure 2.5.

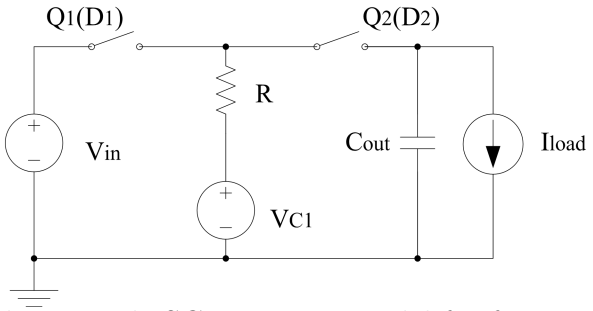

Figure 2.5. Equivalent simple SC converter model for fast switching frequencies

To guarantee steady state operation, the same charge flow characteristics have to be observed. The stage capacitor does not lose any voltage, therefore, both it and the output capacitor's voltage are constant [7, 19, 50]. The result from the previous section would predict that the voltage and power losses are now zero, however, this is not the case. During Mode 2 charge is transfered from the stage capacitor to the output capacitor. This results in a current flow from C_1 to C_{out} with a magnitude of

$$I_{charge} = \frac{I_{out}}{d} \tag{13}$$

where d is the duty cycle of mode 1. The charge current has to flow through the parasitic resistance R that is in the discharge circuit. The current flow through the resistor causes a voltage drop across it, as governed by Ohm's law

$$\Delta V = \frac{R}{d} I_{out} \tag{14}$$

There is always a voltage difference of ΔV between the stage and output capacitor. Again, this leads to a loss of output voltage, which is related to the conduction losses. The resistance presented by the circuit actively produce losses and reduces the output voltage of the converter. The parasitic resistances can be normalized to the output current by assigning them an equivalent resistance. The equivalent resistance of a parasitic resistance is then given by

$$R_{eq} = \frac{\Delta V}{I_{out}} = \frac{R}{d} \tag{15}$$

As resistance is present in both the charge and discharge circuit, the total equivalent resistance of the converter at high switching frequencies is equal to

$$R_{eq} = \frac{\Delta V}{I_{out}} = 2\frac{R}{d} \tag{16}$$

Equation (15) can be used to determine the equivalent resistance of SC converters in operating regions in which the capacitor voltage is practically constant. This assumption can be made if the charge/discharge time is a tenth of the time constant of the circuit. In the literature (15) is generally referred to as the Fast Switching Limit (FSL) [3, 19, 20, 30, 37, 50].

2.4. INDUCTIVE SWITCHING LIMIT

The effects of the converter capacitances and resistances were analyzed in the previous sections. It was shown that at low frequencies the characteristics of the capacitors dominate. At higher switching frequencies the parasitic resistances determine the equivalent resistance of the SC converter. With ever increasing switching frequencies, the operation of SC converters has to be analyzed at very high switching frequencies. Every part of a circuit features, by nature, a parasitic inductance [11, 45, 47]. In

the previously described cases, this inductance was ignored, as it hardly influenced the operation of the converter. However, at high enough frequencies this inductance comes into the picture.

The same fundamental assumption from the previous derivations are used. The circuit illustrated in Figure 2.6. was modified by adding a lumped stray inductance into the circuit. The switching frequency is high enough that the impedance of the inductors will dominate the circuit operation. This allows us to simplify the circuit by setting R equal to 0.

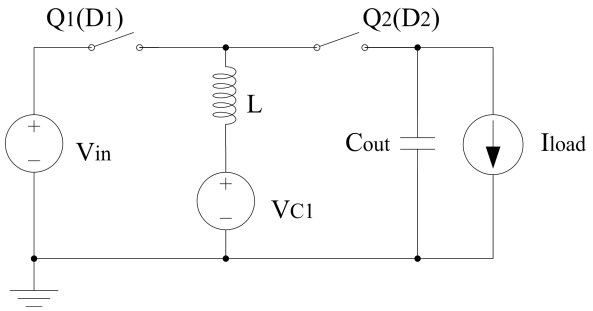

Figure 2.6. Basic SC converter for ISL derivation

The charge and current balances shown in the previous examples are still valid and can be used as is [60].The time dependent current through an inductor based on applied voltage is well-known and can be substituted into the charge balance equation [17]. This substitution will yield

$$\frac{I_{out}}{f_{sw}} = \int_0^{t_{mode}} \frac{V}{L} t \mathrm{d}t \tag{17}$$

where V is the voltage applied to the circuit, L is the total inductance, and I_{out} is the average load current. As in the previous section, the voltage of the stage capacitor is constant. Using this assumptions (17) can be rewritten as:

$$\frac{I_{out}}{f_{sw}} = \int_0^{t_{mode}} \frac{\Delta V}{L} t \mathrm{d}t \tag{18}$$

Equation (19) is the solution to the integral in Equation (18). As the converter is hard-switched, the current through the inductor is assumed to be 0 at the beginning

of each cycle. Therefore, the integration constant will be zero.

$$\frac{I_{out}}{f_{sw}} = \frac{\Delta V}{2L} t_{mode}^2 \tag{19}$$

The length of either the charge or the discharge mode is assumed to be equal to $\frac{d}{f_{sw}}$, like the previous examples. This time constant can be substituted into (19) to simplify the equation further:

$$\frac{I_{out}}{f_{sw}} = \frac{\Delta V}{2L} \frac{d^2}{f_{sw}^2} \tag{20}$$

Rearranging (20) will yield the equivalent resistance due to inductance in either the charge loop or the discharge loop:

$$R_{eq,ind} = \frac{\Delta V}{I_{out}} = \frac{2L}{d^2} f_{sw} \tag{21}$$

As the charge loop and the discharge loop have the same inductance, (21) can be multiplied by 2 to obtain the total equivalent resistance caused by the stray inductance in the SC converter. Equation (21) is the switching limit of the SC converter caused by the stray inductances, therefore it will be referred to from here on out as the Inductive Switching Limit (ISL).

The presented equation is useful to determine the equivalent resistance in operating regions where the stray inductance of the circuit dominates the circuit behavior. The equation is only valid if the frequency is high enough that the impedance of the stray inductance is much larger than the parasitic resistance encountered in the circuit.

2.5. TRANSITIONS BETWEEN OPERATING REGIONS

In the previous section, equations were derived to determine the equivalent resistance of SC converters operating at low, high, and very high switching frequencies. The switching frequency ranges were categorized by identifying the operating states of the stage capacitor and parasitic inductances. The SSL equation (11) is usable if the stage capacitor is fully charged during each cycle, meaning the frequency is low enough that the converter operates in the complete charge region [19, 37]. The FSL

equation (15) can be used if the frequency is high enough that the capacitor voltage remains constant. The converter then operates in the no charge region [19, 37]. Lastly, the ISL equation (21) can be used at extremely high switching frequencies where parasitic inductance dominates. However, the equations presented so far are only of limited use as it is difficult to identify the switching frequencies in which they work. Also, the presented equations cannot be used to model the equivalent resistance when the converter operates in an intermediated region between the SSL and FSL, or the FSL and ISL.

The valid operating regions for the different operating states can be found directly from the equations describing them. For instance, the SSL equation (11) will predict the equivalent resistance at a low switching frequency. As the switching frequency is increased the equivalent resistance decreases as depicted by (11). At a particular frequency the SSL will intercept the equivalent resistance predicted by the FSL. This interception point is where the operation of the SC converter enters a state where it can be more accurately modeled by the FSL equation (15), therefore, the corner frequency, at which the converter starts to operate fundamentally different, is given by [4]:

$$f_{c1} = \frac{2}{dRC} \tag{22}$$

The structure of (22) shows that this corner frequency is based on the time constant, as expected. If the charge and discharge time becomes less than 1 time constant the converter begins to operate more in the FSL, if it is higher, the converter operation is better modeled by the SSL.

A similar derivation can be made between the FSL and the ISL. The corner frequency is then given by:

$$f_{c2} = d\frac{R}{L} \tag{23}$$

The corner frequency between the FSL and ISL is dependent on the time constant of the RL circuit formed between the parasitic resistance and inductance. The ISL will dominate the operation of SC converters if the charge/discharge time is shorter than one RL time constant. If the time is longer than one RL time constant, the

FSL models the operation better. The equivalent resistance of the SC converter can therefore be characterized by the following equation:

$$R_{eq}\begin{cases}\frac{1}{f_{sw}C} & \text{if } f_{sw} \leq \frac{d}{2RC} \\ \frac{2R}{d} & \text{if } d\frac{R}{L} \geq f_{sw} \geq \frac{d}{2RC} \\ \frac{2Lf_{sw}}{d^2} & \text{if } f_{sw} \geq d\frac{R}{L}\end{cases} \tag{24}$$

Equation (24) gives the asymptotes for the equivalent resistance for the SC converter regardless of operating condition. Figure 2.7 shows the limits for a SC converter, however, (24) will only be accurate if the actual switching frequency is far from the corner frequency points. If the converter operates close to one of the corner

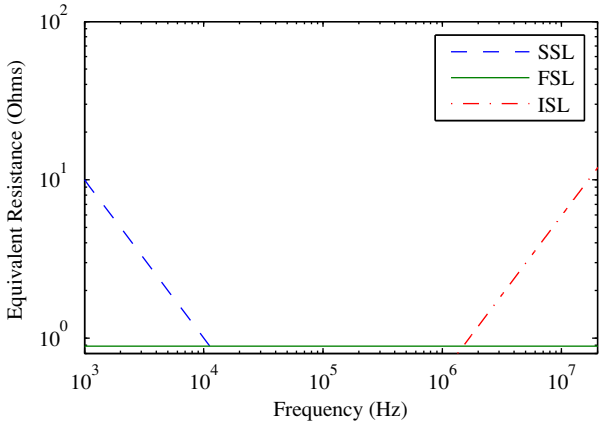

Figure 2.7. SSL, FSL and ISL for sample converter on same plot

frequencies, it enters an operating mode that is a mix of the modes it separates [4]. For instance, at f_{c1} the SC converter neither operates in the fully charged nor no charge region. Instead, the capacitors are partially charged and the equivalent resistance has to be derived from the equivalent RC circuit. Similarly, if the converter operates close to f_{c2} the equivalent RL circuit has to be used to model the circuit.

2.6. RC INTERMEDIATE CIRCUIT

The equivalent resistance of a SC converter operating between the SSL and FSL is dictated by the associated RC circuit equations. The basic RC charging equation is an exponential with the RC time constant mentioned previously:

$$V_c(t) = V_{applied} e^{-\frac{t}{RC}} \tag{25}$$

This exponential can be used as a foundation to derive an equivalent resistance equation. This procedure is shown in [30]. Assuming that the time constants and duty cycles are the same during the charge and discharge cycle, this will yield the following equation:

$$R_{eq} = \frac{1}{fC} \frac{e^{\frac{d}{RCf_{sw}}} + 1}{e^{\frac{d}{RCf_{sw}}} - 1} \tag{26}$$

The resulting equation is, unfortunately, somewhat complex and hard to visualize. The elegance of the SSL and FSL is that they are easy to calculate and utilize. Therefore, it is desirable to develop a curve fit for (26) based on the easy to use SSL and FSL. In [3] the following curve fit was proposed:

$$R_{eq} = R_{FSL} \left[1 + \left(\frac{R_{SSL}}{R_{FSL}} \right)^{\mu} \right]^{\mu} \tag{27}$$

where μ was reported to equal 2. However, in [37] it was shown that the μ value reported in [3] needed to be corrected. To accomplish this, it was assumed that the curve fit had to be corrected at the corner frequency. This was accomplished by calculating the ratio between the actual equivalent resistance at the corner frequency and the FSL equivalent resistance. As described in the derivation of (22), the value predicted by the SSL and FSL are the same at the first corner frequency, therefore, they can be used interchangeably at this operating point:

$$R_{eq,actual} = R_{FSL} \frac{e^{\frac{1}{1-d}} + 1}{e^{\frac{1}{1-d}} - 1} \tag{28}$$

The equation above can be simplified using an hyperbolic cotangent. The equation then simplifies to

$$R_{eq,actual} = R_{FSL} \coth(2d) \tag{29}$$

At the corner frequency, (29) has to be equal to (27) to insure (27) follows the proper trajectory. Using the fact that R_{FSL} and R_{SSL} are equal to one another (27) can be rewritten and set equal to (29) to solve for ratio between the actual and predicted equivalent resistance p:

$$p = \coth(2d) \tag{30}$$

Solving (30) for μ yields

$$\mu = \frac{\log(2)}{\log(p)} = \frac{\log(2)}{\log(\coth(2d))} \tag{31}$$

Substituting the equation for μ into (27) will yield a curve fit that will provide a good approximation for (26). The curve fit equation is easier to use as it only relies on the SSL, FSL and duty cycle. A comparison of (27), (26), (11) and (15) is shown in Figure 2.8.

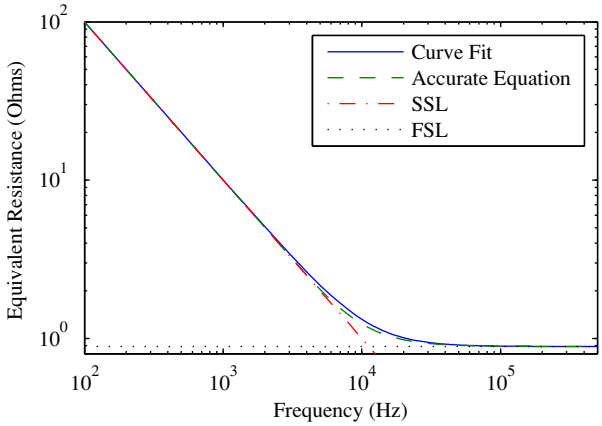

Figure 2.8. Comparison of prediced equivalent resistance from the SSL, FSL, the complete RC circuit equation, and the RC circuit curve fit

2.7. RL INTERMEDIATE CIRCUIT

The fundamental equation for an RL circuit is

$$V = L\frac{\mathrm{d}i(t)}{\mathrm{d}t} + Ri(t) \tag{32}$$

where V is the voltage applied to the RL circuit, L is the total inductance, R is the total resistance, and $i(t)$ is the instantaneous current. The applied voltage across the RL circuit (denoted as ΔV) is assumed to be constant. The solution to the differential equation in (32) becomes

$$i(t) = \frac{\Delta V}{R}\left(1 - e^{-t\frac{R}{L}}\right) \tag{33}$$

The load of the circuit is still governed by the charge balance equation. This can be used to write (32) in integral form:

$$\frac{I_{out}}{f_{sw}} = \int_0^{t_{mode}} \frac{\Delta V}{R}\left(1 - e^{-t\frac{R}{L}}\right)\mathrm{d}t \tag{34}$$

This integral can be solved to obtain

$$\frac{I_{out}}{f_{sw}} = \frac{\Delta V}{R}\left(\frac{Le^{-t_{mode}\frac{R}{L}}}{R} + t_{mode} - \frac{Le^{-0\frac{R}{L}}}{R}\right) \tag{35}$$

The length of either the charge mode or the discharge mode is substituted by $\frac{d}{f_{sw}}$. This substitution produces the following:

$$\frac{I_{out}}{f_{sw}} = \frac{\Delta V}{R}\left(\frac{Le^{-\frac{dR}{f_{sw}L}}}{R} + \frac{d}{f_{sw}} - \frac{L}{R}\right) \tag{36}$$

Equation (36) can be rearranged to obtain the equivalent resistance:

$$R_{eq} = \frac{\Delta V}{I_{load}} = \frac{R}{d - \frac{Lf_{sw}}{R}\left(1 - e^{-\frac{dR}{f_{sw}L}}\right)} \tag{37}$$

Equation (37) describes the equivalent resistance of both the parasitic resistance and the inductance in either the charge loop or the discharge loop. Setting f_{sw} to 0 will yield the FSL for the SC converter, revealing that the derived equation agrees with

previously described equations. Performing a Taylor series expansion at infinity will yield (21) as the dominant term, proving that (37) is also valid for regions in which inductances dominate. The structure of (37) demonstrates that the presence of stray inductance impedes the charge transfer in an SC converter. The reduction in charge transfer increases the equivalent resistance [30, 42].

The derived equation is useful as it accurately predicts the equivalent resistance in the FSL, ISL and in-between region. Unfortunately, this also makes the equation more complicated. As with the SSL/FSL curve fit equation, a similar equation would be desirable for this operating region. Equation (37) is exponential, therefore the same curve fit equation as in the previous section can be used. To fit the curve properly, the exponential has to be adjusted. Again the ratio between the actual resistance to the FSL at f_{c2} needs to be determined:

$$pR_{FSL} = \frac{2R}{d - \frac{Lf_{sw}}{R}\left(1 - e^{-\frac{dR}{f_{sw}L}}\right)} \tag{38}$$

The symbolic value of f_{c2} is substituted into the above equation:

$$pR_{FSL} = \frac{2R}{d - \frac{LdR}{R2L}\left(1 - e^{-\frac{2dRL}{dRL}}\right)} \tag{39}$$

This can be simplified into the following expression:

$$pR_{FSL} = \frac{4R}{d\left(1 + e^{-2}\right)} \tag{40}$$

The value for R_{FSL} can now be substituted to solve for p:

$$p = \frac{2}{1 + e^{-2}} \approx 1.76159 \tag{41}$$

With p known it can be substituted into (31) to obtain the proper exponential:

$$\mu = \frac{\log(2)}{\log\left(\frac{2}{1+e^{-2}}\right)} \approx 1.224 \tag{42}$$

The solution of (42), the R_{FSL}, and R_{ISL} can be substituted into (27) to obtain a simplified version of (37):

$$R_{eq} = R_{ISL}\left[1 + \left(\frac{R_{FSL}}{R_{ISL}}\right)^{1.224}\right]^{\frac{1}{1.224}} \tag{43}$$

A comparison of the results predicted by (43), (37) and (21) is shown in Figure 2.9. As shown the curve fit in (43) will produce the same results as (37), however it is much simpler to use as it only relies on the FSL and ISL. It is interesting to note that unlike (31), the exponential constant μ for the curve fit between the FSL and ISL is not dependent on the duty cycle d. This is due to the fact that both the FSL and the ISL account for the effects of a changing duty cycle.

2.8. COMPLETE MODEL

In this section, equations were derived to characterize the equivalent resistance of the simple SC converter shown in Figure 2.3. It was shown that the equivalent resistance is dependent on resistance, stage capacitance, stray inductance, duty cycle and switching frequency. It was also illustrated that no single equation can be used to characterize the circuit under all operating conditions, because the converter exhibits distinctly different operating modes depending on the timing of the circuit. The SSL,

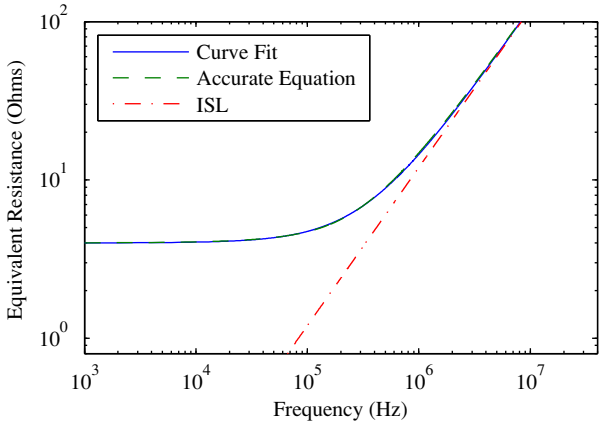

Figure 2.9. Comparison of predicted equivalent resistance from the ISL, the complete RL circuit equation, and the RL circuit curve fit

FSL and ISL can be used to determine the equivalent resistance if the converter operates in one of these distinct operating modes. In addition, the equivalent resistance is always bounded by (24) regardless of operating condition. In proximity to the corner frequencies the SC converter changes from one operating state to another. The more complex equations (26) and (32) can be used to model the resistance in those intermediate regions. The more complex version will produce the same results as the asymptotes they approach. However, using (26) and (32) are difficult to use, therefore, their respective curve fits can be used instead. This will result in the following general expression

$$R_{eq} = \begin{cases} R_{FSL}\left(1+\left(\frac{R_{SSL}}{R_{FSL}}\right)^{\mu}\right)^{\frac{1}{\mu}} & \text{for SSL \& FSL} \\ R_{ISL}\left(1+\left(\frac{R_{FSL}}{R_{ISL}}\right)^{1.224}\right)^{\frac{1}{1.224}} & \text{for FSL \& ISL} \end{cases} \tag{44}$$

where $\mu = \frac{log(2)}{log(coth(2d)}$ and the other terms equal to the ones described in the previous sections. Equation (44) can be used to obtain the accurate equivalent resistance of a hard switched SC converter under any operating condition. A plot comparing (44) with (24) is shown in Figure 2.10. The validity of the complete derived model was verified using a digital simulation. The circuit shown in Figure 2.3 was created in Simulink®with PLECS®. The duty cycle was assumed to be 45% for both the charging cycle and the discharging cycle. Lumped loop resistance was set to 0.2Ω; the lumped loop inductance equaled 30nH. The resistance and the inductance were assumed to be the same for both the charging loop and the discharging loop. The switches switched instantaneously. Figure 2.11 compares the equivalent resistance predicted by (44), the switching limits, and the results obtained from the simulation.

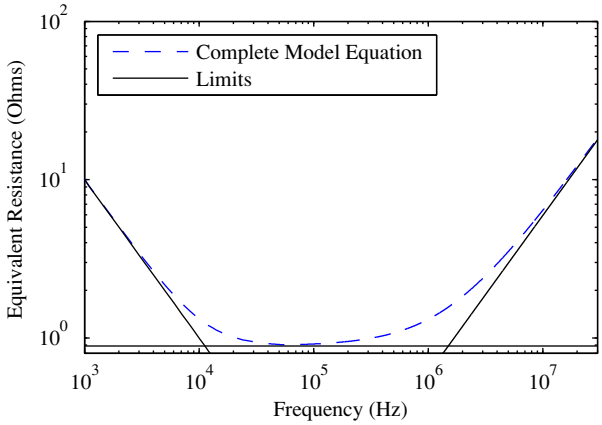

Figure 2.10. Plot comparing the curve fit equations to the switching limits

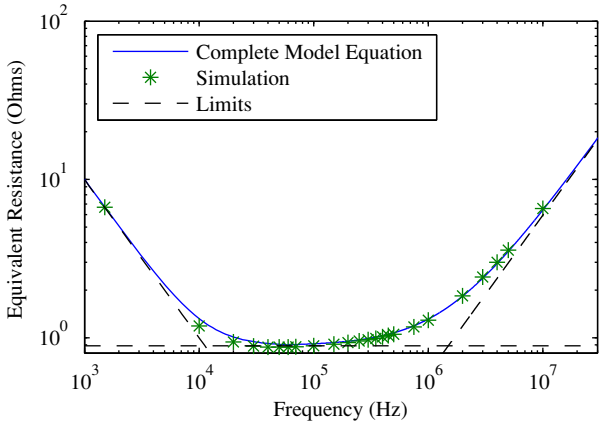

Figure 2.11. Plot comparing the curve fit equations to simulation results

3. HIGH ORDER CONVERTER

The equivalent resistance of a simple SC converter was derived in great detail in the previous section. The conduction losses of the simple SC converter can be fully characterized using equation (44). The derived equations give an insight into the general operation of SC converters, however, (44) is not useful for practical SC designs, as it is not applicable to more complex SC topologies. The losses in a SC converter are also not solely limited to conduction losses. Switching and controller losses have an impact on the converter performance as well. These losses need to be considered to arrive at a complete loss model. Once a complete model is derived, a set of design rules can be created. These rules can be used to assist with generic SC converter design.

3.1. HIGH ORDER SC CONVERTER EQUIVALENT RESISTANCE

Equation (44) is based on the SSL, FSL, and ISL. These switching limits were derived for a simple SC converter and are summarized in (24). The presented SSL, FSL, and ISL equations can be modified to work with any SC capacitor topology. Every SC topology behaves the same as the circuit in Figure 2.3. The only difference is that higher order SC converters feature more circuit components to achieve different gains. The charges transferred throughout higher order SC converter is also not constant, but vary throughout the converter. If the SSL, FSL, and ISL equations are modified to take into account the varying charge transfer ratios and increased number of components, the equations can be used for any hard switched SC converter. In addition, as (44) is only dependent on the SSL, FSL, and ISL, it can be used on high order SC converter with the modified limits.

The equivalent resistance was derived in relation to the output current of the SC converter. In the simple converter, the current through all components was equal to the output current, therefore, the output current could be substituted straight into the equation. In higher order converters, the current through a specific component might be a multiple of the output current. To account for the increased level of current (and with it charge transfer) the SSL, FSL, and ISL can be multiplied by the

ratio of the actual current to the output current. The coefficient is defined as follows:

$$a_n = \frac{Q_n}{Q_{out}} = \frac{I_n}{I_{out}} \tag{45}$$

where a_n is the charge vector of the component in stage n, I_n is the average current through that stage, and I_{out} is the output current.

At first, it would appear that the addition of the charge vector to the equivalent resistance equation would be sufficient. However, the term does not account for the voltage losses across the entire converter. Consider the following circuit operation. A SC converter consists of at least two stages with one stage capacitor each (C_1 and C_2). The loop resistance, capacitance, and inductances are lumped into one equivalent component for each stage. The converter operates at a low frequency, therefore, the SSL equation can be used to calculate the equivalent resistance of the converter stages. Both C_1 and C_2 will contribute to the total equivalent resistance of the converter.

$$R_{eq,total} = R_{eq,C1} + R_{eq,C2} \tag{46}$$

The equivalent resistance of both $R_{eq,C1}$ and $R_{eq,C2}$ can be found using the SSL equations. Stage capacitor C_1 conducts a_1 times the output current. Applying (7) to C_1 we can determine the effects of the equivalent resistance on the voltage of that stage capacitor:

$$V_{1,max} = V_{in} - a_1 \frac{I_{load}}{f_{sw} C_1} \tag{47}$$

As C_1 is conducting a_1 times the output current, it is has to charge a_1 equivalent stage capacitors. The capacitor has to charge other stages to insure the charge balance equation for the converter is satisfied. C_1 charges C_2. To simply the derivation and illustrate the effects of increase charge transfer by one stage we assume the source (V_{in}) feeding C_1 is ideal. Capacitor C_2 is then charged by an ideal source in series with C_1. The maximum voltage C_1 can charge C_2 up to is given by (47), therefore

the highest voltage on C_2 is equal to

$$V_{c2,max} = V_{in} + V_{in} - a_1 \frac{I_{load}}{f_{sw} C_1} \tag{48}$$

As capacitor C_2 itself supplies another stage higher up in the converter it will lose voltage due to a charge transfer as well. This equation is given by (7)

$$V_{c2,min} = V_{in} + V_{in} - a_1 \frac{I_{load}}{f_{sw} C_1} - a_2 \frac{I_{load}}{f_{sw} C_2} \tag{49}$$

The total loss of voltage in the converter is then given by:

$$\Delta V_{total} = \Delta V_1 + \Delta V_2 = -a_1 \frac{I_{load}}{f_{sw} C_1} - a_1 \frac{I_{load}}{f_{sw} C_1} - a_2 \frac{I_{load}}{f_{sw} C_2} \tag{50}$$

The equation above illustrates that the voltage loss of previous stages effects stage capacitors upstream. In this case, due to the voltage loss shown in (47) for C_1, a_n additional stage capacitors in higher stages will have lower voltages as well. The output voltage of the SC converter is the sum of the stage voltages, therefore, the total loss in voltage is also the sum of the voltage losses in each stage. It is easier to see the effects of a stage component if the voltage loss it causes are grouped by the charge vectors. The total voltage loss caused by C_1 can be described by:

$$\Delta V_{1,total} = a_1 \times a_1 \times \frac{I_{load}}{f_{sw} C_1} = a_1^2 \frac{I_{load}}{f_{sw} C_1} \tag{51}$$

The SSL equivalent resistance can then be generalized to:

$$R_{eq,n} = a_n \times a_n \times \frac{I_{load}}{f_{sw} C_n} = a_n^2 \frac{I_{load}}{f_{sw} C_n} \tag{52}$$

Equation (52) shows that the equivalent resistance of a stage capacitor exchanging an average current a_n times larger than the output current. The derivation of (52) relied on the voltage loss in the converter stage, which is the basis for the derivation of all equivalent resistance limits. This fact can be used to adjust (52) to be used with the FSL and ISL as well. Equation (52), therefore, shows that the SSL, FSL, and ISL can be adjusted for higher average currents by multiplying them by a_n^2. The limit equation (24) and curve fit equation (44) can be utilized as presented in any

high order converter as long as they are adjusted with the a_n^2 term to account for their current magnitude.

The derivation above also shows another important aspects of the determination of equivalent resistance in higher order converters. First, the total equivalent resistance of a SC converter can be determined by summing the equivalent resistance of the individual stages

$$R_{eq,total} = \sum_n R_{eq,n} \tag{53}$$

where $R_{eq,n}$ is the equivalent resistance of stage n of the switched capacitor converter. The summation works identically for the SSL, FSL, and ISL.

The above concept shows that the total equivalent resistance of a converter can be separated into small subsections based on the stages. Identically, the total equivalent resistance of a stage can be further separated and assigned to the individual stage components. Instead of lumping the the resistance, capacitance, and inductance into one equivalent component, each individual component is assigned an equivalent resistance, which can be summed with the other stage components to derive the total equivalent resistance. This has to be done individually for the SSL, FSL, and ISL as the different circuit components will contribute differently to the equivalent resistance at those limits.

The SSL is entirely based on the behavior of the capacitors in the stage, therefore the equivalent resistance is found by applying the already presented SSL equation. The FSL is based entirely on the operation of the resistors in the circuit. In SC converters there are resistance present in the form of equivalent series resistance (ESR) of the capacitor and the on state resistance of the MOSFET switches. The MOSFET switches only conduct during one of the two operating modes, therefore their contribution to the equivalent resistance is given by [37]:

$$R_{eq,sw} = a_{sw}^2 \frac{R_{sw}}{d_{mode}} \tag{54}$$

where a_{sw}^2 is the average current multiple of the output conducted by the switch duing one operating cycle of the converter, d_{mode} is the duty cycle of the mode in which the

switch is conducting and R_{sw} is the on state resistance of the switch. The contribution of the capacitor ESR can be found in a similar fashion. The only difference is the fact that the capacitor has to conduct current during both operating modes. The resulting equivalent resistance of a capacitor ESR is then given by [37]:

$$R_{eq,c} = a_c^2 \left(\frac{R_c}{d_1} + \frac{R_c}{d_1} \right) \tag{55}$$

where a_c is the ratio of current exchanged by the capacitor during each operating cycle and the output current, d_1 and d_2 are the duty cycles of the two modes of the SC converter and R_c is the ESR of the capacitor. The equation shows that the resistance of the capacitor influences the total equivalent resistance of a SC converter more than that of a switch. The FSL of a stage can therefore be determined from the individual circuit components by summing (54) and (55) [37].

$$R_{eq,FSL,total} = \sum_n R_{eq,c,n} + \sum_n R_{eq,sw,n} \tag{56}$$

Alternatively, the equivalent resistance of all components can be summed directly to obtain the FSL of the entire converter [20]. It is important to note that different components have different charge vector, depending on their location in the converter. The appropriate charge vector for each part needs to be used to calculate the equivalent resistance correctly.

In a similar manner to the FSL, the ISL can be determined form the different components. Again each switch and capacitor has a stray inductance associated with it. The equation for a switch would be given by:

$$R_{eq,sw} = a_{sw}^2 \frac{2 L_{sw} f_{sw}}{d_{mode}^2} \tag{57}$$

The ISL for a capacitor can be determined by:

$$R_{eq,c} = a_c^2 \left(\frac{2 L_c f_{sw}}{d_1^2} + \frac{2 L_c f_{sw}}{d_2^2} \right) \tag{58}$$

The concepts presented in this section allow the previously presented limits and curve fits to be used with all types of high order SC converters. The previously presented equations can be modified by multiplying them by the square of the ratio of average conducted to output current (a_n). In complex converter designs the equivalent resistance can be found by assigning an equivalent resistance for the individual components and then summing the values for each of the switching limits [20]. Once the switching limits are known, the curve fits can be use to obtain the equivalent resistance over the entire operating range.

3.2. CHARGE VECTOR

In the last section the charge vector a_n was introduced, which can be used to calculated the equivalent resistance in higher order SC converters. Its definition was given in (45). For a given converter topology the charge vectors of each stage have to be known to accurately calculate the equivalent resistance. There are a number of previous works that derive and describe the charge vectors for a multitude of common SC topologies [2, 36, 38, 50].

A simple graphical methodology is presented in this section to obtain the charge vectors of any high order SC converter. The method is illustrate by analyzing a 3 stage step up Fibonacci converter shown in Figure 3.1.

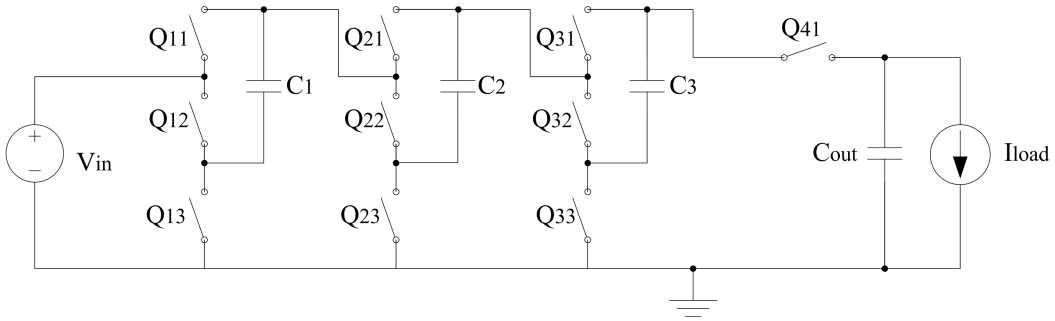

Figure 3.1. 3 stage step up Fibonacci converter schematic

The presented methodology does not rely on specific converter operating characteristics such as component values, switching frequencies, or duty cycles. Only the operating modes of the converter topology are uses. The two main operating modes

of the converter are illustrated in Figure 3.2. There is an additional operating mode in which all switches are not conducting, however, the converter is not transferring any charge in this state, therefore it does not affect the charge vector calculation.

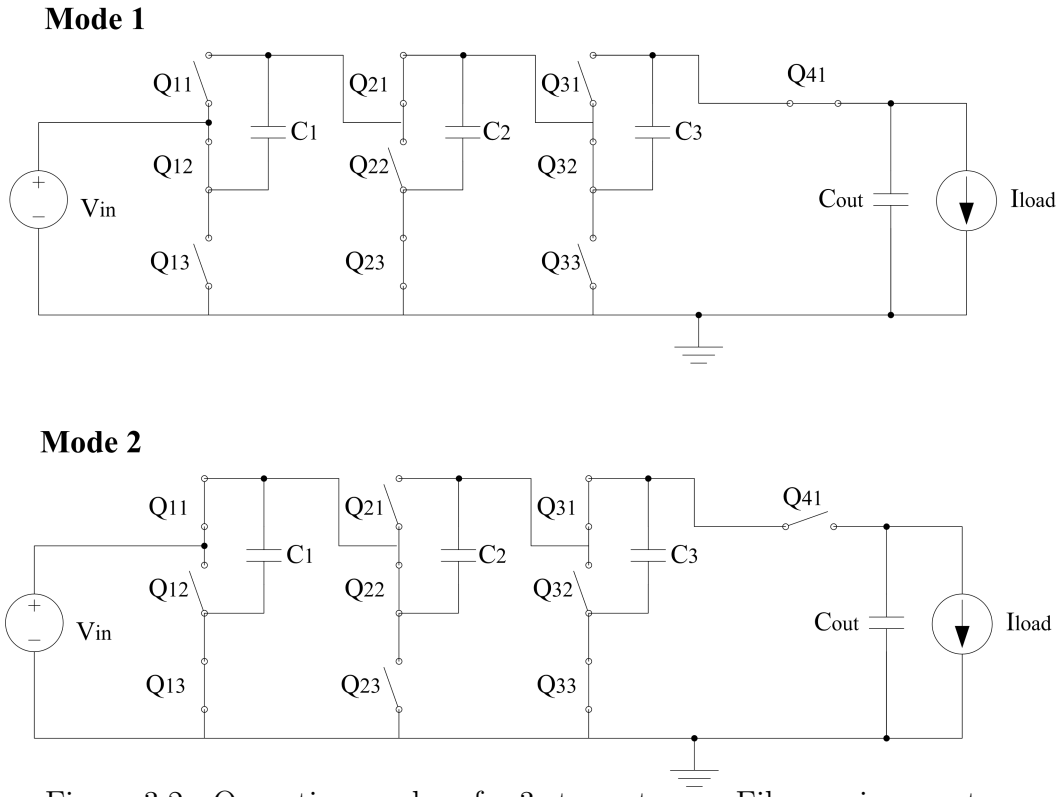

Figure 3.2. Operating modes of a 3 stage step up Fibonacci converter

During mode 1 switch Q_{41} is closed, transferring charge (in the form of a current) to the output. The load has to be supplied each switching cycle with a charge of Q_{out} to insure the converter operates in steady state, therefore during mode 1 a charge of Q_{out} is transfered through Q_{41}. The stage capacitor C_3 is in series with switch Q_{41}, therefore a charge of Q_{out} is also drawn from C_3. Switch Q_{32} is also in series with C_3, therefore it conducts Q_{out} as well. This charge transfer is illustrated in Figure 3.3. As Q_{41},C_3, and Q_{32} conduct Q_{out} Equation (45) can be used to determine that their charge vector value (a_n) is equals to 1. At this point the charge flow through the converter can no longer be determined by observing, which parts are in series, therefore we analyze the next mode. In mode 2, the output switch Q_{41} is not

conducting, therefore no charge is supplied to the output. However, a charge of Q_{out} was drawn from C_3. This charge has to be replenished to insure the capacitor voltage remains constant between switching cycles. The charge (replenishing C_3) has to flow through Q_{31} and Q_{33}, therefore their charge vector a_n is equals to one as well. In mode 2 capacitor C_2 is in series with C_3, therefore Q_{out} is supplied by C_2 in mode 2. The associated switch Q_{22} also conducts a charge of Q_{out}. The charge vector a_n for those components is again one. The analysis for this mode is exhausted, therefore the derived charge transfers are substituted into mode 1. The charger transfers derived for mode 1 previously are still valid. During mode 2 C_2 and its associated switch supplied Q_{out}. This charge has to be resupplied during mode 1 again. C_2 and C_3 both draw a charge of Q_{out} during mode 1 then. C_1, Q_{21}, and Q_{12} are in series with C_2 and C_3, therefore they have to conduct $2Q_{out}$ to satisfy the charge balance. The charge vector of those components has therefore a value of two. Switch Q_{23} only has to conduct the charge resupplying C_2, therefore its charge vector is one. A charge of $2Q_{out}$ is drawn from the input during mode 1. At this point the analysis for mode 1 is exhausted again, therefore mode 2 has to be examined again. The past charge transfers are substituted into the analysis. As described before the charge of C_1 has to be replenished. The input and switch Q_{11} are in series with the parallel combination of C_1 and C_2, therefore, a charge of $3Q_{out}$ has to be conducted through them, making the charge vector of Q_{11} equals to three. Switch Q_{13} conducts the charge that resupplies C_1, therefore its charge vector is two. At this point the charge transfer through all components is characterized. The procedure is summarized in visual form in Figure 3.3.

In the analysis, it can be seen that a total charge of $5Q_{out}$ is drawn from the input. This makes sense, as the voltage gain of a 3 stage Fibonacci converter is equal to 5. To achieve an ideal voltage magnification of 5, a 5 times higher input charge (which is related to current) has to be supplied to the input. The input to output charge can be used to insure the analysis was performed correctly. The total input charge always has a ratio equals to the ideal voltage gain of the topology higher than the output charge.

The charge vectors for any high order SC converter can be determined using the methodology above. The analysis only relies on the basic operating modes of

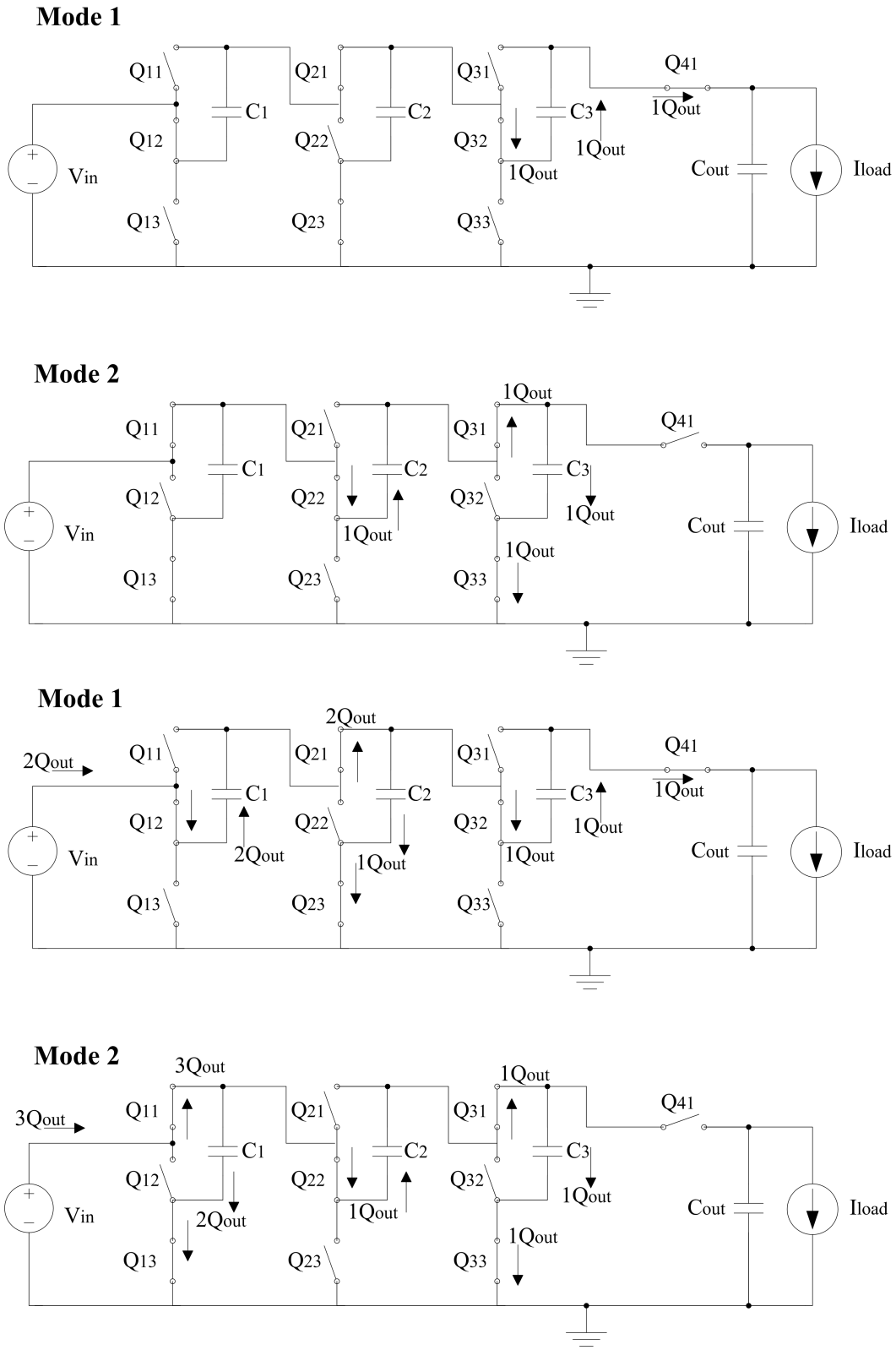

Figure 3.3. Charge flows through 3 stage step up Fibonacci converter under steady state operation

the converter, therefore the charge vectors can be used for any converter utilizing the analyzed topology.

3.3. SWITCHING LOSSES

Until now the analysis was focused on the equivalent resistance, which can be used to calculate the deviation of the output voltage from the ideal voltage or the total conduction losses of the SC converter. However, as with traditional power converters, not only conduction losses, but also switching losses contribute to the total power losses of a converter [17]. The switching losses can contribute a significant amount to the total power losses, especially at high switching frequencies [17]. The total switching losses can be separated into gate driver losses, commutation losses and stand by losses through parasitic capacitances [17]. The different loss mechanics and how they can be applied to SC converters are discussed in this section.

3.3.1. Gate Driver and Controller Losses. Standby losses are well known in traditional power converters. Traditionally, these losses include gate driving and control circuitry losses. The standby losses in SC converters are the same as they would be in traditional converters [3,34]. SC converters generally have more switches than inductor based converters therefore their standby losses are higher. The standby losses in a SC converter can be calculated using equation (59) [3, 34, 43],

$$P_{standby} = (N \times V_g \times Q_g) + P_{control} \tag{59}$$

where N denotes the number of MOSFET switches in the converter, V_g the voltage of the gate drivers and Q_g the gate charge of the used MOSFETs as specified by the manufacturer. $P_{control}$ denotes the power consumption of the control circuit of the converter.

3.3.2. Commutation Losses. Commutation losses describe the losses caused by switches transitioning from one state to another. The nonidealities of the switches further increase the equivalent resistance in SC converters. In [19] it was demonstrated that the FSL can be modified to consider the switch rise (t_r) and fall times (t_f) :

$$R_{eq}(FSL) = a_n^2 \frac{R_n}{f_{sw}\left(\frac{t_r}{2} + t_{on} + \frac{t_f}{2}\right)} \tag{60}$$

The switch transition times further reduce the amount of time available to transfer charge in the loop, effectively increasing the loop's equivalent resistance. The effects of these transition times can be incorporate into (54) and (55) by modifying the duty cycle term [19]. The effective duty cycle (d_l) is then determined by calculating the following:

$$d_l = f_{sw}\left(\frac{t_{r,l}}{2} + t_{on,l} + \frac{t_{f,l}}{2}\right) = d - \left(\frac{t_{r,l}}{2} + \frac{t_{f,l}}{2}\right) f_{sw} \tag{61}$$

The adjusted duty cycle term can be used in the FSL, ISL, and (36) to account for the increase equivalent resistance of converter switches cause by commutation losses. The curve fit associated with the FSL and ISL will still be valid with the new duty cycle. It is important to apply the new duty cycle to both limits in the calculation, or it will not produce the correct results. The effects of the switch commutation time on the equivalent resistance is shown in Figure 3.4.

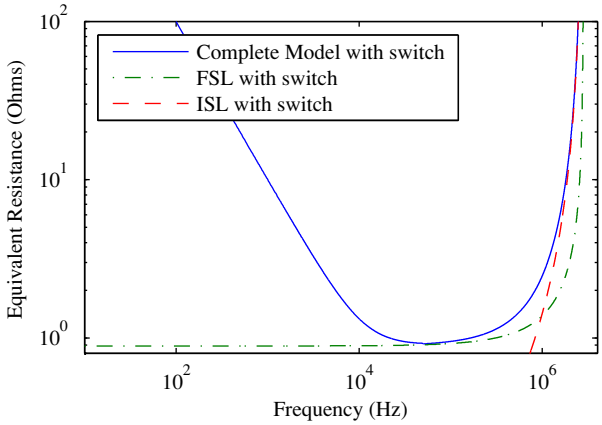

Figure 3.4. Plot illustrating the effects of switch commutation time on equivalent resistance

3.3.3. Parasitic Capacitor Losses. The standby losses caused by the parasitic capacitance of the MOSFET switches are the most challenging to determine. Traditionally, these losses were computed using the following equation:

$$P_{pc} = \frac{1}{2} C_{oss} V_D^2 f_{sw} \tag{62}$$

where P_{pc} is the power loss caused by the parasitic capacitances,C_{oss} is the output capacitance given in the manufacture datasheet for the respective switch, and V_D is the voltage across the switch when it is off. In [61] the argument is made that the C_{oss} dependent power loss term is redundant. The argument is that C_{oss} increases the power losses during turn on but decreases the power losses during turn off by the same amount, canceling out the contribution of the C_{oss} term. See [61] for a more detailed discussion on this line of argument. In contrast to what is reported in [61], a majority of papers describing the operation of charge pumps or SC converter consider the output capacitance of the power MOSFET in the switching loss calculation [3, 5, 21, 25, 34, 39, 58] or similar parasitic capacitances [35]. In [43], [65], and [31], it is argued that C_{oss} term has to be included in the switching loss calculation for all type of power converters.

As there is a general agreement that the C_{oss} term effects switching losses it will be included in the derivations in this paper. The general form of the traditional equation (62) is generally accepted, however, corrections for the C_{oss} term have been proposed. The C_{oss} term requires corrections as it is not constant over the operating voltage range of the switch. Unfortunately, the MOSFET datasheets only provide the actual C_{oss} value at one operating voltage. In [25] and [49] the following adjustment for (62) was proposed:

$$P_{pc} = \frac{1}{2}\left(C_{oss}\sqrt{\frac{V_{spec}}{V_D}}\right)V_D^2 f_{sw} \tag{63}$$

where C_{oss} is the output capacitance specified in the manufacturer data sheet and V_{spec} the voltage level at which the output capacitance was obtained.The square root term approximates the change in output capacitance with varying switching voltages. In this thesis (63) will be used for all switch loss calculations related to the parasitic switch capacitances as it has the most agreement in the literature. However, this topic is still heavily researched so designers are encouraged to review [3, 5, 17, 21, 25, 25, 31, 34, 39, 49, 58] for more information about switching losses.

3.3.4. Equivent Conductance of Switching Losses. The three switching loss types were characterized above. The losses caused by the commutation of the switches can be modeled using the already derived equivalent resistance equations.

By adjusting the duty cycle this loss can be easily considered making the overall model more accurate.

The standby control losses are relatively independent of the operating state of the converter, they only change with the switching frequency. Equation (59) can be used to model the control and gate driver circuit as a frequency dependent power loss term. If the gate drivers and the control circuit are supplied using a linear regulator, the loss can be modeled as a frequency dependent current source (I_{sb}). This constant current source would then draw from the input of the converter.

The power losses by the stray capacitances can contribute a significant amount to the losses in the switched capacitor converter, especially at low output current levels. Therefore, it is important to derive an easy to use model, similar to the equivalent resistance model, to judge their effect. The parasitic losses are independent of the load current of the converter, therefore the series equivalent resistance cannot be used. However, the parasitic loss term is voltage dependent. All the switch and stage voltages are related to the input voltage, therefore an equivalent conductance term can be defined that describes the losses caused by the parasitic capacitances. This equivalent conductance, unlike the equivalent resistance term found earlier, would be in parallel to converter input. Similar to the charge vector a_n, a voltage vector g_n needs to be defined that relates the input voltage to the switch voltages. This allows the switching losses for all switches to be related to the input voltage of the converter. The voltage gain vector can differ for each individual switch. Using this definition the equivalent conductance $G_{eq,n}$ of switch n can be described using the following equation

$$G_{eq,n} = \frac{1}{2} g_n^2 C_{oss,adj} f_{sw} \tag{64}$$

where g_n is the ratio between the applied switch voltage to the input voltage and $C_{oss,adj}$ being the output capacitance of the switch adjusted using one a method described in [3, 5, 21, 25, 25, 31, 34, 39, 49, 58, 58]. The total equivalent conductance at the converter input can then be found by summing the equivalent conductances of all

the switches in the power converter.

$$G_{eq,total} = \sum_{n} G_{eq,n} \tag{65}$$

The resulting conductance term can then be used with the input voltage to calculate the total switch losses caused by the parasitic MOSFET output capacitances. The presented stray capacitance equations may also be used for other types of stray capacitance that may be encountered in a SC converter, such as stray capacitance of PCB traces [37].

3.4. FULL LOSS MODEL

By now all possible loss mechanics in any type of SC converter were identified and analyzed. With the exception of the gate driver and control circuit losses all other losses could be defined in terms of equivalent resistance or conductance. The equivalent circuit components can be used to derive a simple circuit model that is equivalent to the SC converter. The conductance term $G_{eq,total}$ is used at the input terminals of the SC converter model. A ideal transformer is used to represent the voltage gain of the converter [37, 42]. The turns ratio of this equivalent transformer is equal to the voltage gain of the chosen SC topology. The equivalent series resistance is in series with the output terminal of the converter [19, 20, 30, 37, 42]. Any type of load model can be then connected. For this derivation a simple resistive load is used on the output. The resulting circuit is shown in Figure 3.5.

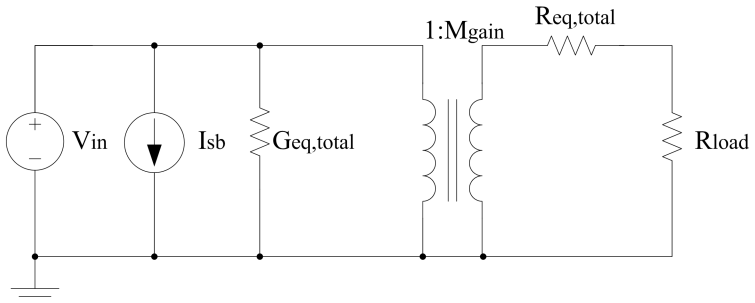

Figure 3.5. Switched capacitor equivalent circuit with ideal transformer

The voltage gain in Figure 3.5 is modeled as an ideal transformer, therefore the resistance of conductance term can be reflected to the other side using ideal transformer equations. Designers generally think in terms of the load requirements, therefore the conductance term should be reflected to the output side. This allows the conductance term to be in parallel with the equivalent resistance and the load. The reflected conductance term is then equals

$$G_{eq,ref} = \frac{G_{eq,total}}{M_{gain}^2} \tag{66}$$

where M_{gain} is the ideal voltage gain of the SC converter topology. The ideal transformer can then be replaced by an ideal voltage source with a voltage equaling the input voltage multiplied by the ideal gain of the converter topology [19, 20]. The resulting circuit model is shown in Figure 3.6.

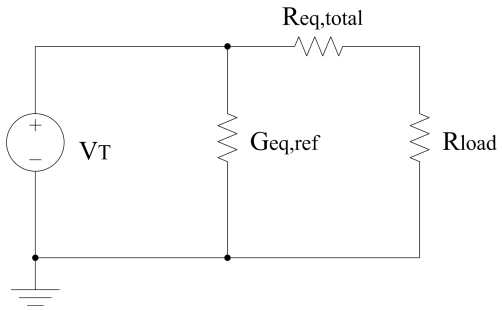

Figure 3.6. Switched capacitor equivalent circuit with ideal voltage gain and equivalent components reflected on output side

The model illustrate in Figure 3.6 is straightforward and simple, yet as accurate as the fully presented equations. The model can be used to obtain both the non ideal gain and the power efficiency of the SC converter. Assuming a resistive load the actual output voltage is determined using a voltage divider between $R_{eq,total}$ and R_{load}. The voltage gain equation is then equal to [20]:

$$V_{out} = V_{in} M_{gain} \frac{R_{load}}{R_{load} + R_{eq,total}} \tag{67}$$

Equation (67) demonstrates that the output voltage is load and switching frequency dependent. Lower switching frequencies will result in higher equivalent resistances, lowering the output voltage. This relation is illustrated in Figure 3.7.

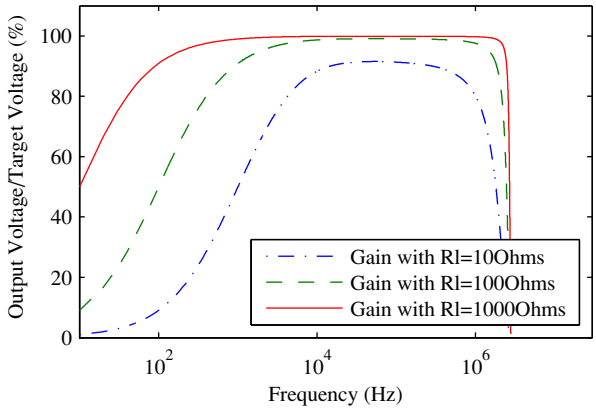

Figure 3.7. Actual output voltage compared to the target voltage of an SC converter with varying switching frequencies and load levels

In a similar manner the power efficiency of the converter can be determined using the following equation

$$\eta = \frac{P_{out}}{P_{in}} = \frac{R_{load}}{R_{load} + R_{eq,total}} \frac{1}{\frac{G_{eq,total}}{M_{gain}^2}(R_{load} + R_{eq,total}) + 1} \tag{68}$$

The first term in (68) is equal to (67), demonstrating that the output voltage of the converter is related to the efficiency of the converter. This first part represents the efficiency of the charge transfer. The second part of the equation accounts for the loss of efficiency due to losses in parasitic capacitances. Many previous works have stated that the efficiency of SC converters is related to the non-ideal voltage gain of SC converters [12, 20, 28, 29, 52, 67]. However, as shown in (67) and (68) only the efficiency of the charge transfer is related to the output voltage of SC converters [7]. Lower charge transfer efficiencies cause the lower output voltage not vice versa as implied in previous works.

The converter efficiency for different load levels over the entire operating frequency region is shown in Figure 3.8. The efficiency of a SC converter is heavily

dependent on both the load level and switching frequency. At low load levels switching losses are a major contributer to the overall power losses in the converter. The load current is low, therefore higher equivalent series resistance will not cause very high power losses. Therefore, the switching frequency in SC converters should be lowered at light loads to improve the overall efficiency. At high load level the opposite is true, high current draws makes it important to reduce the equivalent series resistance of the converter to a minimum. However, the rise and fall times of the power MOSFETs limit the converter's maximum operating frequency. The converter should never be allowed to operate close to the limit set by the commutation losses as it has detrimental effects on the equivalent series resistance and with it the efficiency. The convert frequency should only be set as high as necessary to minimize the equivalent series resistance of the converter.

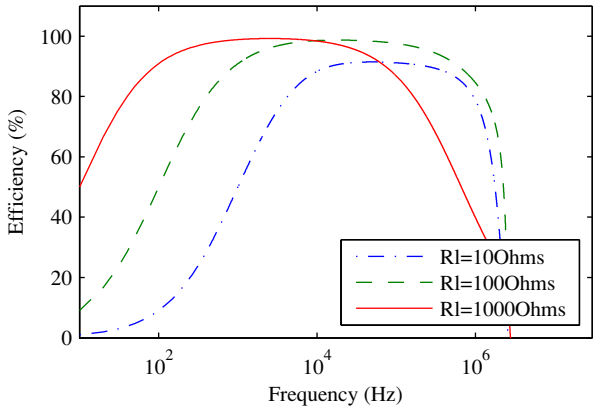

Figure 3.8. Efficiency of SC converter with varying switching frequencies and load levels

3.5. OUTPUT VOLTAGE REGULATION

In general, it is desirable to control the output voltage of a DC/DC converter to a specific voltage level. As shown in (67), the output voltage of a SC converter can be adjusted by varying the equivalent resistance of the converter. In this mode it operates like a linear regulator, dissipating power to lower the voltage. If the load of the SC converter can be modeled as a resistor and its resistance is known, (67) can be

used with (24) or (44) to control the output voltage. To control the output voltage the SC converter should either be operated in the SSL region, or the FSL region. If the converter operates in the SSL region, the switching frequency can be adjusted to change the equivalent resistance and with it the output voltage. In the FSL region, the duty cycle of the converter can be adjusted to regulate the output voltage of the converter.

Implementing voltage regulation in the SSL is generally more efficient, especially for light loads. This comes from the fact that the switching losses will be much lower as the converter operates at a lower frequency. This is illustrated in (68) and Figure 3.8. The variable switching frequency can cause EMI problems though making this control scheme problematic. Control in the FSL can be realized at a fixed switching frequency, similar to traditional power converters, by adjusting the duty cycle. The ease of implementation comes at the price of slightly lower efficiencies as mentioned. It is important to keep in mind that either control scheme relies on increasing the power losses in the converter to lower the output voltage. Therefore, using a SC converter for voltage regulation results in much higher losses than a traditional magnetic power converter.

3.6. EXPERIMENTAL VERIFICATION

A number of concepts and equations were introduced in this section. The equivalent resistance equations from the last section were adapted to work with high order SC converters. The effects of switching resistance on the converter performance was explored as well. Based on the presented equations, an equivalent model was derived that captures the major loss mechanics in a SC converter. The presented model was compared to a prototype 5 stage Fibonacci converter with a gain of 13. The commanded duty cycle for both modes was equals to 0.45. The different voltage and current levels throughout the converter necessitate different component stages for the individual stages. An overview of the used components is shown in Table 3.1. The component parameters published in the manufacturer datasheet were used for all calculations.

The curve fit equation (44) was verified in Figure 3.9. The proper charge vector term a_n was included for all stage components. The duty cycle was also adjusted as

Table 3.1. 5 stage prototype Fibonacci converter component overview

Stage	Capacitor	Switch
Stage 1	5x FFV34E0107K - 100μF Film	SIR870ADP-T1-GE3 N-CH100V 63A
Stage 2	3x B32524Q1686K - 68μF Film	SIR870ADP-T1-GE3 N-CH100V 63A
Stage 3	2x FFV34F0656K - 65μF Film	BSC320N20NS3 N-CH 200V 36A
Stage 4	1x C4ATDBW5600A30J - 60 μF Film	SIHP22N60S-E3 N-CH 600V 22A
Stage 5	1x B32774D4226K - 22μF Film	SIHP22N60S-E3 N-CH 600V 22A
Output Stage	1x B32798G2756K - 75μF Film	C3D10060G SiC Schottky 600V 10A

described in (61) to account for switching losses. The presented equivalent resistance equation matched the measurements from the prototype converter well. The measured resistance was lower than the calculated values in the intermediate switching frequency range. In one instance, the measured value was lower than the value predicted by the FSL which is the theoretical minimum resistance. Therefore, it is most likely that the Fibonacci converter operated in a resonant mode as resistances lower than the FSL can be achieved that way. For more information about resonant operation of SC converters see [8, 30, 33, 51]. Figure 3.9 shows that the presented model can be used to estimate the actual equivalent resistance of a high order converter.

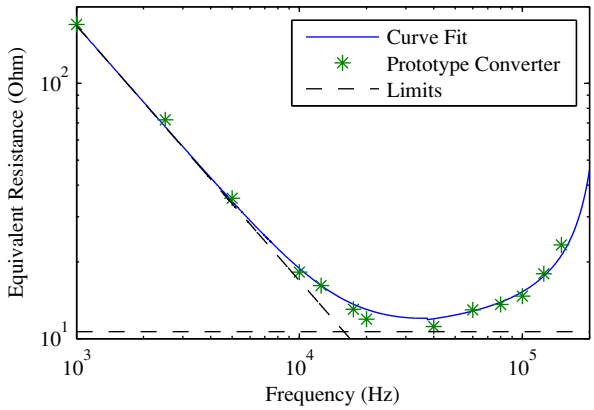

Figure 3.9. Comparison of calculated and measured equivalent resistance of a 5 stage Fibonacci converter

The complete loss model illustrated in Figure 3.6 was verified with the prototype converter as well. Using the equivalent model the efficiency of the converter can be calculated using equation (68). Figures 3.10, 3.11, and 3.12 show the calculated and predicted efficiency of the 5 stage Fibonacci converter at various switching frequencies and output resistances. The same graphs are shown in Figures 3.13, 3.14, and 3.15 using a output load conductance instead of a resistance. This is done to better illustrate the relationship between supplied converter power and converter efficiency. The results show that (68) can be used to approximate the efficiency of the practical converter with a good degree of accuracy.

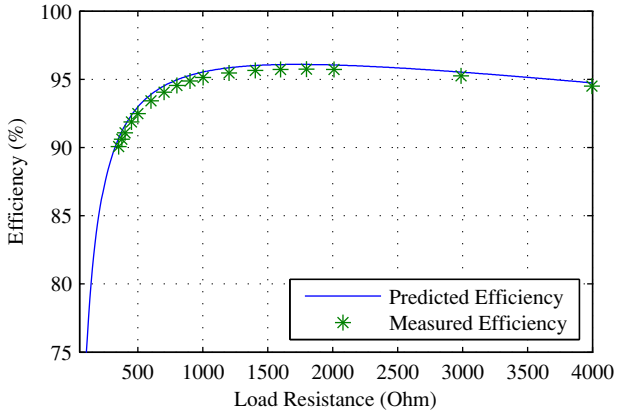

Figure 3.10. Predicted and measured efficiency of a 5 stage Fibonacci converter operating with an input voltage of 25V, a switching frequency of 5kHz, and a load resistance

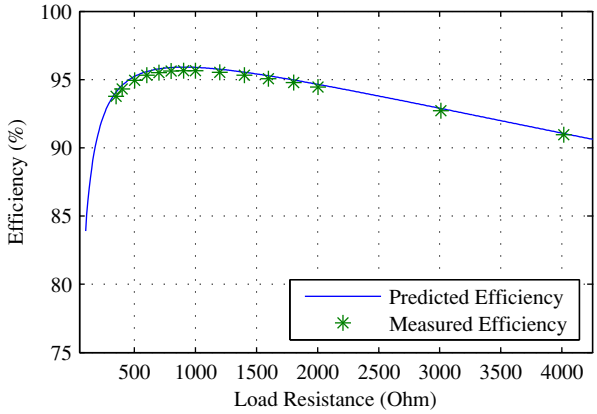

Figure 3.11. Predicted and measured efficiency of a 5 stage Fibonacci converter operating with an input voltage of 25V, a switching frequency of 10kHz, and a load resistance

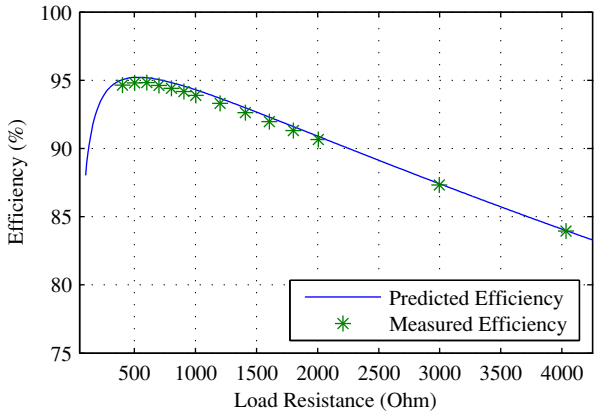

Figure 3.12. Predicted and measured efficiency of a 5 stage Fibonacci converter operating with an input voltage of 25V, a switching frequency of 20kHz, and a load resistance

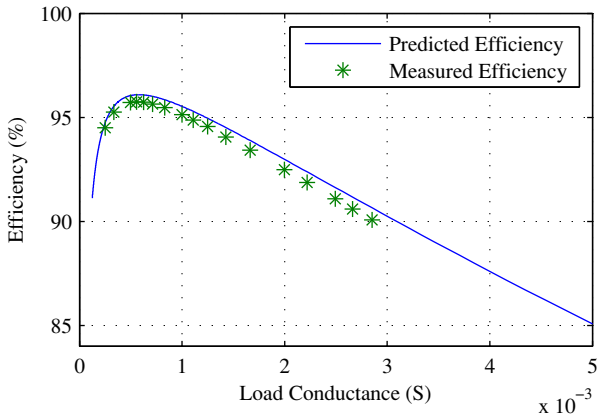

Figure 3.13. Predicted and measured efficiency of a 5 stage Fibonacci converter operating with an input voltage of 25V, a switching frequency of 5kHz, and a load conductance

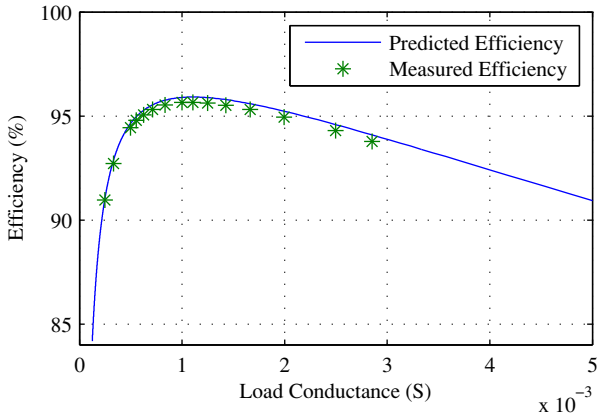

Figure 3.14. Predicted and measured efficiency of a 5 stage Fibonacci converter operating with an input voltage of 25V, a switching frequency of 10kHz, and a load conductance

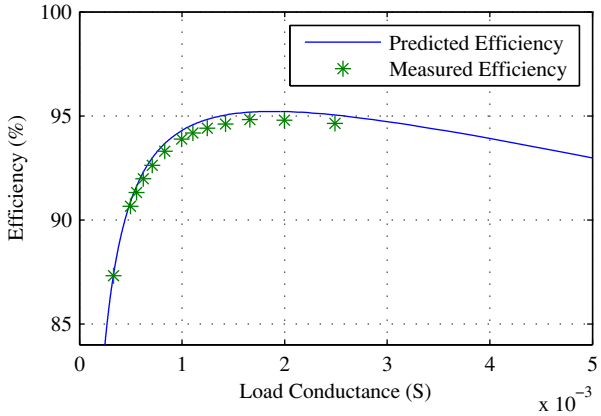

Figure 3.15. Predicted and measured efficiency of a 5 stage Fibonacci converter operating with an input voltage of 25V, a switching frequency of 20kHz, and a load conductance

4. CURRENT-FED SC CONVERTERS

4.1. INTRODUCTION

A complete loss model for SC converters of any order were derived in the last section. It was also demonstrated that output voltage regulation could only be realized by increasing the equivalent series resistance of the converter. By increasing the equivalent resistance the power losses in the converter are increased as well though. For output voltage regulation this makes SC converters lossy similar to linear regulator [14, 55, 67, 68]. The maximum attainable efficiency with output voltage regulation is given by:

$$\eta = \frac{V_{out}}{V_T} \tag{69}$$

A number of solutions have been presented to this fundamental problem. One such solutions involves switched capacitor converter topologies that can adjust their target voltage based on the required output voltage [9, 10, 46, 53]. This is done by including a large number of additional switches in each switching cell to modify the converter topology to produce the most desirable target voltage. The output voltage is controlled between the available target voltage levels by adjusting the equivalent series resistance. This method allows for better converter efficiencies, especially if a wide range of output voltages are desired. However, it is also required a large number of additional components making it more expensive and complex to implement. Additionally, the converter efficiency is still impacted when regulating the output voltage between the available target voltages.

Another proposed method was to utilize the switched capacitor converter cell as an unregulated converter that is supplemented by a traditional magnetic converter to perform the voltage regulation. In this approach the SC converter could always be operated at its maximum efficiency point regardless of required output voltage. The magnetic converter can be designed to regulate the output voltage using the SC converter as an input. This approach promises good converter performance, however, it also poses a number of design challenges. This solution requires two dedicated

converters to perform the action generally done by one. This will greatly increase the implementation cost and space requirements. In addition, the designer needs to ensure that the output impedance of the SC converter is lower than the input impedance of the connected converter to insure stable operation [1, 22, 41, 42, 54]. This can greatly complicate the controller design of the magnetic based converter or necessitate the use of a large DC link capacitor between the converters.

The third approach is to include an inductor into the SC converter to act as a current sources, either at the input or output [23, 32, 40, 63, 64]. It is important to keep in mind that the inductor is used as a current source, not a resonant element. A number of resonant switched capacitor topologies were proposed in which uses small inductor throughout the converter to shape the capacitor charge and discharge currents. The current through those types of inductors varies greatly throughout each switching cycle, therefore they could not be modeled as a current source. For more information about soft-switching SC converters see [8, 30, 33, 51].

To perform voltage regulation, an inductor with a reasonably high inductance is used to keep the current flowing through it approximately constant throughout each switching cycle. Having the inductors as a current sources at the inputs or output allows a constant current to be supplied to or drawn from the SC converter. If the inductor is on the output side the output voltage of the converter can be directly controlled by adjusting the current through the output. If the output of the SC converter is a fixed resistance the output voltage would be given by:

$$V_{out} = I_{out} R_{load} \tag{70}$$

If the output current can be directly controlled, the output voltage can be adjusted as shown in (70). However, as the inductor in this case is directly connected to the output of the SC converter without any DC link bulk capacitors only a bucking action could be performed. Additionally, the operation of the inductor would be tied to one operating mode of the SC converter.

Inductors can also be added to the input of a SC converter to control the total input current. As shown in the previous section, the SC converter can be modeled as an ideal transformer with a series resistor on the output. The switching losses are

ignored as they do not affect the output voltage directly. The equivalent circuit for this configuration was shown in Figure 3.5. The ideal transformer changes the input current in a similar manner as it changes voltage, therefore the output current can be related to the input current by

$$I_{out} = \frac{I_{in,L}}{M_{gain}} \tag{71}$$

where $I_{in,L}$ is the current set by the input inductor and M_{gain} is the ideal voltage gain of the chosen SC converter topology. The output voltage is then given by (70). The output voltage is controlled indirectly through the input current, as the output current ideally has a constant relation to the output voltage. The gain will not be ideal due to the charge losses in the stray capacitances of the switches, however a compensator network with an integrator can be used to correct for the small current error.

By controlling the current flow, the output voltage can be controlled directly. This control scheme does not rely on the SC converter dissipating any excess power in the equivalent resistance, allowing them to be operated at their optimal operating point. Inductors are inherently current driven devices, therefore they can be commanded a constant current through an appropriate control scheme. Current mode control strategies, such as peak or average current mode control, can be adapted to work with SC converters.

The greatest challenge in adding the current sources to the SC converters is integrating them seamlessly into the existing SC topology. The inductor has to act as a current source as it interfaces with the converter. No bulk DC link capacitors can be added in between the inductor and the SC converter as this will create an equivalent voltage source. Another challenge is that the voltage over the inductor has to be varied to control its current. The voltage variation is controlled through a switch that changes the voltage applied over the inductor.

In the traditional boost converter a switch controls the connection between the inductor and the ground. When the switch is conducting the source voltage source is applied directly over the inductor, increasing the current flow through it. When the switch is off the voltage across the inductor is negative as it supplies current to

the output, this causes the current to ramp back down. If the output capacitor is removed from the boost converter then the system outputs a pulsating current with controllable magnitude. The current magnitude is controlled by varying the switch duty cycle. A boost like circuit with the output capacitors removed can therefore be used as a current source for a SC converter that works with a discontinuous input currents. There are a variety of SC converters with a discontinuous input current like the the Cockcroft-Walton multiplier or the Dickson charge pump. Adding a boost converter like stage to each input allows the output voltage of the SC controller to be accurately controlled by varying the current through them.

A traditional buck converter can act like a current source in a similar manner to a boost converter. However the boost converter will produce a constant output current while drawing a discontinuous input current. If the input capacitors of the buck converter are removed this buck cell can be used with a SC converter that produces a discontinuous output current. The pulse width of the output current (which can be adjusted by changing the discharge pulse with of the highest capacitor group) can then be adjusted to control the output current magnitude.

The discontinuous current waveforms at either the input or the output of SC converters are a normal part of the operation of the SC converter. They are caused by the switching action of the SC converter. If the current source cells are pared in such a way that the discontinuous current waveform is either supplied by or fed into the SC converter the need for additional switches are reduced.

A number of current fed SC converters have been proposed in the literature. The majority of them rely on a boost like stage feeding current into an SC converter. Cockcroft-Walton type converters are the very popular with current-fed SC converters as all the stage switches can be realized using diodes. This eliminates the need for the boost converter stage switch to be synchronized with the switches inside the SC converter. A dual input current-fed Cockcroft Walton multipler was derived based on previously presented current-fed SC converter topologies. In this section the operation of the converter is presented in detail to elaborate on the concepts presented above.

4.2. CURRENT-FED COCKCROFT WALTON MULTIPLIER

A current-fed SC converter is presented in this thesis (see Fig.4.1). The four switch configuration presented in [63] was not utilized in this design. In [63] one inductor was used to act as the current source for the input voltage. By switching it in an H Bridge style configuration the current through it could be controlled very tightly, however it made the circuit implementation very difficult. In this design an interleaved boost converter was used as the input stage. The total input current is then controlled by the total current through the two inductor. This both reduces the converter's complexity and allows it to perform dual input operation, if desired. The dual input operation enables the controller to perform three different operation modes. These modes are MPPT on two separate power sources, power sharing between two power sources while maintaining a controlled output voltage, or interleaved operation with a single power source.

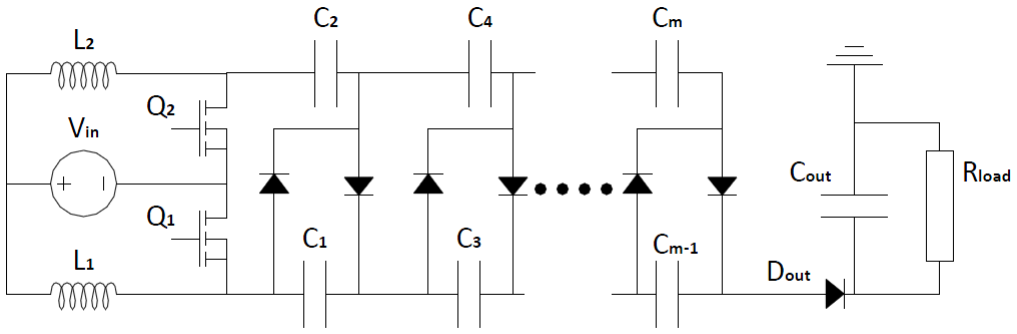

Figure 4.1. Current-fed Cockcroft Walton multiplier schematic

4.3. STEADY STATE ANALYSIS

4.3.1. Converter Operation Modes. The converter's operation can be separated into four distinct operation modes. Figure 4.2 illustrates the current flow in the converter during each mode. Figure 4.3 presents the voltage and current profiles during different operation modes.

1. **Mode1:** Both switches (Q_1 and Q_2) are conducting. Both boost inductors (L_1 and L_2) are directly charged by the input source, increasing their currents. The

ladder capacitors' voltages remain virtually unchanged as all diodes block the flow of current, preventing them from discharging. The output diode operates

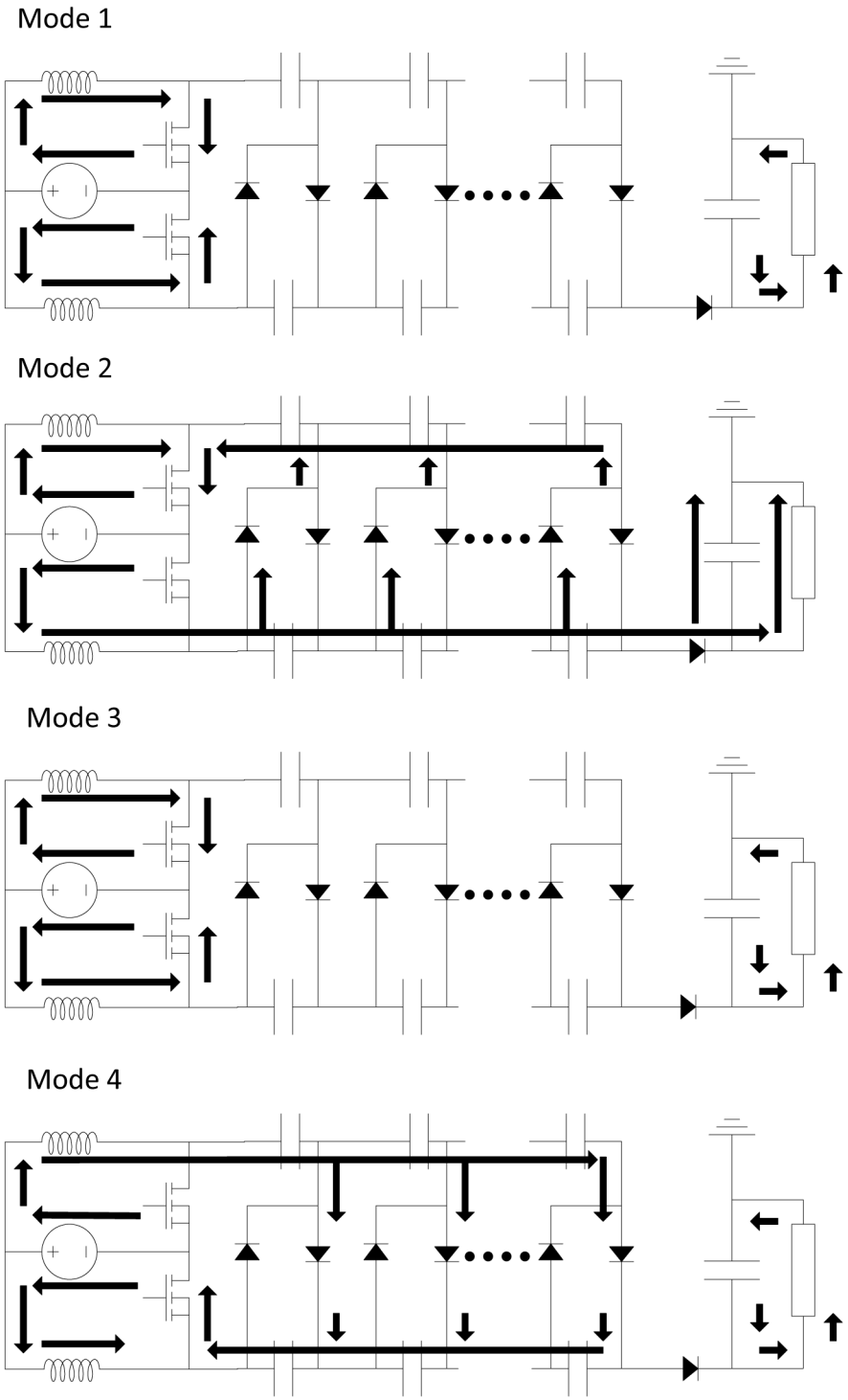

Figure 4.2. CFCW multiplier current flow diagram

in reverse bias as the output capacitor is at a higher potential than either the top or the bottom capacitor chain. The load is supplied by the output capacitor.

2. **Mode2:** At time $(d_1 - 0.5)\,T$, switch Q_1 stops conducting, forcing the current in the L_1 boost conductor to flow into the capacitor ladder. The bottom terminal of the capacitor ladder assumes a high potential while the top terminal remains at ground potential. This results in a flow of current from L_1 through Q_2 to the ground. In mode 2, both the input boost inductor and the bottom row of capacitors are connected in series. The resulting potential is high enough to force the output diode to conduct and charge the output capacitor. The bottom row of capacitors is discharged during this mode. The returning

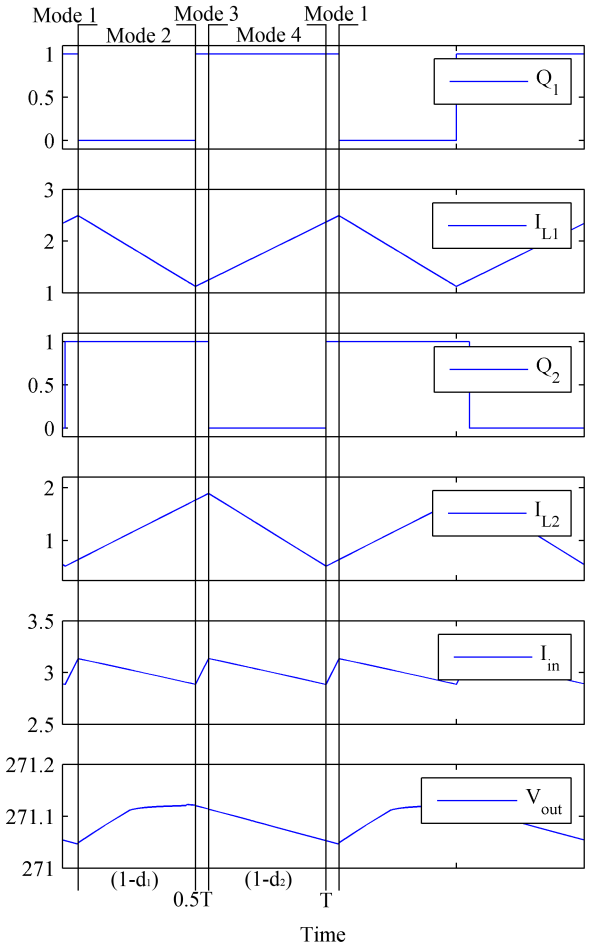

Figure 4.3. CFCW multiplier waveforms

current-to-ground conducted through the top row of capacitors recharges the top ladder.

3. **Mode 3:** After time $0.5T$, switch Q_1 begins conducting again, and the converter operates in the same state as Mode 1.

4. **Mode 4:** At time d_2T , switch Q_2 stops conducting, forcing the current in the boost conductor L_2 to flow into the capacitors. The top terminal of the capacitor ladder assumes a positive potential, and the bottom terminal remains at ground potential. The polarity over the capacitor ladder is inverse to Mode 2, creating the required alternating signal on the multiplier. The combined voltage of the source, boost inductor L_2 and the top capacitors do not exceed the output voltage, causing the output diode to remain in reverse bias. The entire boost inductor current L_2 is conducted through the top capacitors discharging them. The bottom capacitor row is recharged in Mode 4.

4.3.2. Derivation of Ideal Static Gain. The presented converter consists of two building blocks: an interleaved boost converter and a CW multiplier. The ideal voltage of both converters are well known. Therefore, they can be combined to obtain the ideal voltage gain of this topology.

$$V_{out,target} = \frac{1+N}{1-d_1}V_{in,1} + \frac{N}{1-d_2}V_{in,2} \tag{72}$$

with N being the total number of stages in the Cockcroft-Walton multiplier and $d_1 + d_2 \geq 1$. The combined duty cycle of the boost converter switches has to be greater than 100% to insure the CW multiplier always has connection to ground. The converter's gain can be adjusted by changing either of the switch duty cycles. Power converters are, in general, operated in a symmetrical mode. In the presented converter, both switches can be operated with the same duty cycle, having the Q_2 command signal delayed by 180° .This will simplify the equations describing the gain of the converter. The voltage gain for the converter in a symmetrical operation mode is given by

$$V_{out,target} = \frac{2N+1}{1-d}V_{in} \tag{73}$$

4.3.3. Component Voltage Stresses. Components with both the appropriate voltage and current ratings need to be selected for a practical converter to be designed. The voltage stresses across the converter devices can be easily obtained from the ideal voltage gain derivation. Primary switches Q_1 and Q_2 have a steady-state voltage stress equal to the output voltage of their respective boost stages. Equation (72) can be used to calculate these voltage stresses. These, however, only describe the steady-state stress; they do not consider the switching overshoot. Appropriate margins of safety must be applied in accordance with the MOSFET manufacturer specifications.

The maximum voltage stress over the individual stage component is the same as the stage voltage calculated in the ideal voltage derivation. Each stage capacitor and diode must have a withstand voltage of at least

$$V_{stress,stage} = \frac{1}{1-d_1} V_{in,1} + \frac{1}{1-d_2} V_{in,2} \tag{74}$$

The only exception to (74) is C_2 and the first diode in the ladder. These devices will only see the output voltage of the bottom boost stage. Therefore, they need to be able to withstand the voltage produced by the bottom boost stage.

Under normal operating conditions, the steady-state voltage stress of the output diode is equal to $V_{in,1}$. If the converter is connected to a dc bus with a fixed voltage, as in grid-tie solar energy systems, the output diode should still be rated for the full output voltage. This would protect the converter from damaging voltages when it is not operational or during start-up.

4.3.4. Component Current Stresses. The current stresses for all components need to be determined to aid the designer in selecting the most appropriate components. The peak, average, and RMS currents are of interest to the designer when selecting components with the appropriate rating. These values can also be used in both efficiency calculations and thermal design.

The average currents through the converter's components can be derived from the charge transfers described in a CW multiplier. The charge supplied by the converter to the output can only travel through the stage diodes in the converter [40]. Therefore, the average current through all diodes in the converter is equal to the

converter output current [40]. The average current through the stage capacitors can be determined using the charge each capacitor must transfer each cycle. This will yield the following average capacitor current equation:

$$I_{Cap,m} = 2(N + 1 - m)I_{out} \tag{75}$$

where m is the index of the stage component.

The average currents through the boost inductors can be found using conservation of charge:

$$I_{L1} = \frac{N+1}{1-d_1} I_{out} \tag{76}$$

$$I_{L1} = \frac{N}{1-d_2} I_{out} \tag{77}$$

Similarly, the average currents through the primary switches can be determined using the following equations:

$$I_{Q1} = \left(\frac{N+1}{1-d_1} d_1 + N \right) I_{out} \tag{78}$$

$$I_{Q1} = \left(\frac{N}{1-d_2} d_2 + N \right) I_{out} \tag{79}$$

The peak currents through the switches, diodes, and capacitors are limited by the peak current through the input inductors [63]. The peak current through the respective boost inductor can be found using

$$I_{pk,1} = \frac{N+1}{1-d_1} I_{out} + \frac{V_{in,1} d_1}{L_1 f_{sw}} \tag{80}$$

$$I_{pk,2} = \frac{N}{1-d_2} I_{out} + \frac{V_{in,2} d_2}{L_2 f_{sw}} \tag{81}$$

The peak current through all even diodes and the output diode is equal to (80). The peak current through the odd diodes is equal to (81). The peak current through the capacitors is either (80) or (81); whichever one is larger. The peak current through Q_1 and Q_2 is less than the sum of the peak inductor currents.

The designer should also know the RMS currents as these dictate the losses in resistive elements. The RMS current through the input inductors can be easily obtained as the current flow through them is clearly defined. The RMS current in them will be equal to that in a traditional boost converter. Finding the exact RMS current through the remaining components, however, is extremely difficult. These currents are dependent on the conduction state of the diodes in the converter. Both the nonlinear behavior and the fact that they are not controlled externally makes the exact current waveforms through the converter components hard to determine [6]. This makes an accurate analytic solution for the RMS currents impossible [6].

A method commonly used to eliminate this problem involves assuming that only one diode conducts at any given time in the CW multiplier [62, 63]. This, however, is only an approximation as it assumes the absence of an output rectifier and the use of ideal diodes in the converter [40]. The RMS current calculations can be further simplified if they are based on the average current conducted through the components. The following RMS current equations can be derived from these assumptions:

$$I_{rms,diode(even)} = \frac{\sqrt{N+1}}{\sqrt{1-d_1}} I_{out} \tag{82}$$

$$I_{rms,diode(odd)} = \frac{\sqrt{N}}{\sqrt{1-d_2}} I_{out} \tag{83}$$

$$I_{rms,cap(m)} = \sqrt{(N+1-m)\left(\frac{N+1}{1-d_1} + \frac{N}{1-d_2}\right)} I_{out} \tag{84}$$

$$I_{rms,Q1} = \sqrt{\frac{(N+1)^2}{(1-d_1)^2} d_1 + \frac{N^2}{1-d_2}} I_{out} \tag{85}$$

$$I_{rms,Q2} = \sqrt{\frac{N^2+2N}{(1-d_1)} + \frac{N^2}{(1-d_2)^2} d_2} I_{out} \tag{86}$$

In general, the derived rms current equations overestimate the actual RMS current magnitudes throughout the converter. These equations can thus be used to verify that the selected components can withstanding the current stresses encountered when the converter is operating.

4.3.5. Component-Based Voltage Gain. Many publications only present the ideal voltage gain of the converter under consideration. The actual gain of a switch capacitor based converter, however, is greatly dependent on its load, the switching frequency, and the selected components [6, 7, 30, 50]. This dependence is much greater than it would be in a conventional inductor-based converter. Additionally, non-idealities of the input boost stage will cause the actual output voltage to deviate even further from the ideal value [48]. This is especially true for high-duty cycles, which would be common when operating the converter presented here.

The duty cycle of the boost stage greatly influences the voltage gain of the overall converter. As with a traditional boost converter, the voltage gain of the boost stage will eventually collapse if either the duty cycle or the load is too high. Therefore, selected components in the boost stage greatly impact the converter's performance. The non-ideal voltage gain equation of the boost stage used in the presented converter, including inductor resistance R_L and transistor resistance R_Q, is

$$V_{out,boost} = \frac{1}{1-d}\frac{V_{in}}{1+\frac{R_L+dR_Q}{(1-d)^2R_{load}}} \tag{87}$$

Equation (87) can be used to modify the ideal voltage gain equation to account for the voltage degradation of the boost stage at ether high duty cycles or high load levels (small values of R_{load}). The non-idealities of the CW multiplier cause the output voltage to deviate further from the ideal equation. The equivalent resistance effect of the capacitors (observed in CW multipliers) further reduces the maximum possible output voltage. The capacitors act as frequency, duty cycle, and capacitance dependent series resistors in the converter [7,68]. The decrease in output voltage due solely to the charging and discharging process is

$$\Delta V_{out,cap} = -\sum_{1}^{N} 2\frac{I_{out}}{C_m f_{sw}}(N+1-m)^2 \tag{88}$$

This loss is the same as that for other current fed CW multipliers [63]. Equation (88) is similar to the SSL presented in previous sections.

The capacitors equivalent series resistances (ESR) need to be included as well to determine the capacitors full effect on the converter performance. Because the

accurate current waveforms of the stage capacitors are unknown, the exact voltage drops cannot be determined. If an infinite switching frequency is assumed, a useful analytic equation can be found with the previously stated approximations. Voltage losses due to resistive elements in an SC converter are at their maximum when the switching frequency is high [7,30]. Thus this approximation is useful as it determines the worst possible voltage loss due to the capacitor ESRs:

$$\Delta V_{out,ESR} = -\sum_{1}^{N} \left(\frac{N+1}{1-d_1} + \frac{N}{1-d_2} \right) (N+1-m)\, ESR_{cap,m} I_{out} \tag{89}$$

Equations (87) and (89) can be summed to determine the voltage loss in the converter based on the stage capacitor characteristics.

The stage diodes' voltage drops must be considered in addition to the non-ideal behavior of the capacitors. As the output charge travels through each stage diode, the output voltage is diminished by the sum of their forward voltage drops. Again, the nonlinear behavior of the diodes makes it extremely challenging to determine the exact forward voltage drop of each diode [6]. Many diode manufactures provide approximate forward voltage drops for specific operating conditions. These approximations can be used as provided to approximate the forward voltage drop of each diode. In this instance the following would describe a drop in output voltage as a result of the diodes:

$$\Delta V_{out,diode} = -(2N+1) V_{fw(I)} \tag{90}$$

Alternatively, a piecewise linear model can be used to approximate the voltage forward drop for the average current magnitude [6]. Using the piecewise linear model will yield the following equation to determine the voltage loss due to the diodes:

$$\begin{aligned} \Delta V_{out,diode} = &-\sum_{1}^{N} 2\frac{I_{out}}{C_m f_{sw}} (N+1-m)^2 - 2NV_{fw} \\ &- NR_{diode,m} \left(\frac{N+1}{1-d_1} + \frac{N}{1-d_2} \right) - V_{fw,out} - R_{diode,out} \frac{N+1}{1-d_1} \end{aligned} \tag{91}$$

The equivalent resistances can be determined with the forward voltage curves provided by the manufacturer. Again, the actual forward voltage of a real diode follows an exponential curve, not a straight line. As a result, the resistance can only be approximated.

Equations (87)-(90) can be combined to obtain a load-dependent output voltage equation:

$$\begin{aligned} V_{out} =& \frac{N+1}{1-d_1}\frac{V_{in,1}}{1+\frac{R_L 1+dR_Q 1}{(1-d_1)^2 R_{load}}} + \frac{N}{1-d_2}\frac{V_{in,2}}{1+\frac{R_L 2+dR_Q 2}{(1-d_2)^2 R_{load}}} \\ & - \sum_{1}^{N} 2\frac{I_{out}}{C_m f_{sw}}(N+1-m)^2 - (2N+1)V_{fw(I)} \\ & - \sum_{1}^{N}\left(\frac{N+1}{1-d_1}+\frac{N}{1-d_2}\right)(N+1-m)\,ESR_{cap,m}I_{out} \end{aligned} \tag{92}$$

Equation (92) considers the effects that all converter components have on the output voltage, with approximations necessitated by the nonlinearities of the diodes. Although it is only an approximation, equation (92) is sufficiently accurate in most conditions, especially for the operating conditions encountered in a real, physical implementation of the converter. This equation allows to the designer to verify that the intended voltage gain is achieved with the selected components for either a given load level or switching frequency.

4.3.6. Output Voltage Ripple. The output voltages calculated in both (72) and (92) represents only the converter's maximum output voltage. The converter's output stage is identical to that of a traditional boost converter. Therefore, the output capacitor must supply the load whenever Q_1 is conducting. Equation (93) (for the boost converter) can be used to calculate the converter's output voltage ripple:

$$\delta V_{out} = \frac{d_1 I_{load}}{C_{out} f_{sw}} \tag{93}$$

4.4. CONVERTER CONTROL SCHEMES

The input of the converter presented is formed by two individual boost converters. Traditionally current mode control schemes are utilized for boost type converters

to improve the dynamic response. Current mode control has the additional benefit of simplifying the required controller implementation. The dual input nature of the converter allows for a variety of different control schemes depending on the desired operation of the converter. Two possible control schemes are presented in this section: dual input power sharing current mode control with output voltage regulation and dual maximum power point tracking using Perturb & Observe (P&O) [18]. The presented controls schemes are fundamental enough that they can be modified to suit different application areas.

4.4.1. Current Mode Control. Using current mode control the current through each boost inductor can be controlled to a set level. The CW multiplier is a charge pump, therefore the input and output current (and with it charge) are related to another. Assuming an ideal converter the current relation can be expressed by

$$I_{out} = \frac{1-d_1}{N+1} I_{1,in} + \frac{1-d_2}{N} I_{2,in} \tag{94}$$

where $I_{1,in}$ and $I_{2,in}$ are the current magnitude through the bottom and top inductor respectively. The output voltage of the converter is a function of the output current and the load resistance. Therefore, the ideal steady state output voltage can be written by:

$$V_{out} = R_{load} \left(\frac{1-d_1}{N+1} I_{1,in} + \frac{1-d_2}{N} I_{2,in} \right) \tag{95}$$

Equation (94) shows that controlling either input current to a reference value allows the output voltage to be controlled to a set level. As with all current mode control schemes, an outer loop voltage compensation network is used to set a reference input current. By adjusting the reference input current the output voltage is controlled as shown by (95). The difference is that the required input current can come from either $I_{1,in}$ or $I_{2,in}$. The proposed power sharing feature is realized by adjusting which input loop delivers the required input current. For instance, a ratio between input currents can be defined to set a ratio of the power drawn from each input. If the input voltages of each supply are constant and equal, the power delivered by the inputs are given by

$$\frac{P_1}{P_2} = \frac{I_1}{I_2} \tag{96}$$

A block diagram of this control scheme is shown in Figure 4.4. Alternatively, a voltage

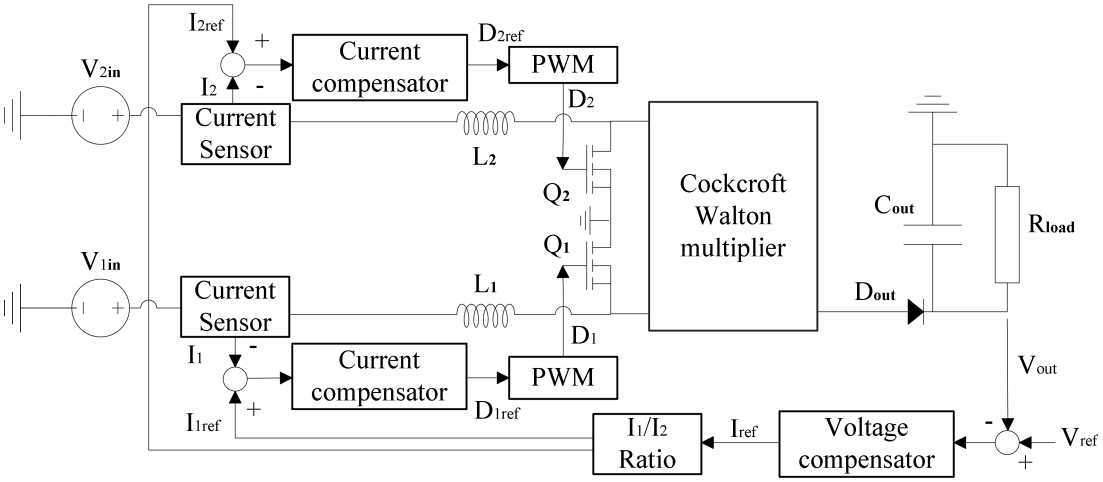

Figure 4.4. Dual current mode control scheme

sensing network can be added to the desired input. This would allow a controller to determine the required current magnitude of of a specific loop to extract a fixed amount of power from it. The converter only has 2 control parameters, therefore the input power of one input can be controlled to an exact value while still maintaining a regulated output voltage. The converter operation is also still restricted by the duty cycle requirements ($d_1 + d_2 \geq 1$) and the converter losses that may occur at very high or low duty cycle values.

4.4.2. Dual Maximum Power Point Tracking. The power sharing feature discussed above can be further modified to allow individual maximum power point tracking for both inputs. The ability to regulate the output voltage is sacrificed to allow for power control on each loop. As step-up converters for renewable systems generally feed into a fixed DC bus the loss of output regulation does not present a problem.

There is a large variety of MPPT algorithms available that can be used to control the converter. The popular P&O MPPT algorithm can be implemented by adding a voltage measurement to each input (shown in Fig. 4.5). The two P&O controllers then monitors the input power by multiplying the voltage and current measurements. The power extracted is maximized by changing the duty cycle of the switch until the

maximum amount of power is delivered by the source. As both inputs are individually controlled, the power extracted from each can be maximized independently of the operating state of the other input. This holds true within the operating limits of the converter. Again, the combined duty cycle of the input switches has to exceed 100%. Also if the converter feeds into a fixed DC load the following needs to be satisfied:

$$V_{link} = \frac{1+N}{1-d_{range}} V_{1,range} + \frac{N}{1-d_{range}} V_{2,range} \tag{97}$$

where V_{link} is the DC link voltage the converter feeds into, d_{range} is the allowable duty cycle range and $V_{x,range}$ is the voltage range of the respective source in which MPPT can still be performed.

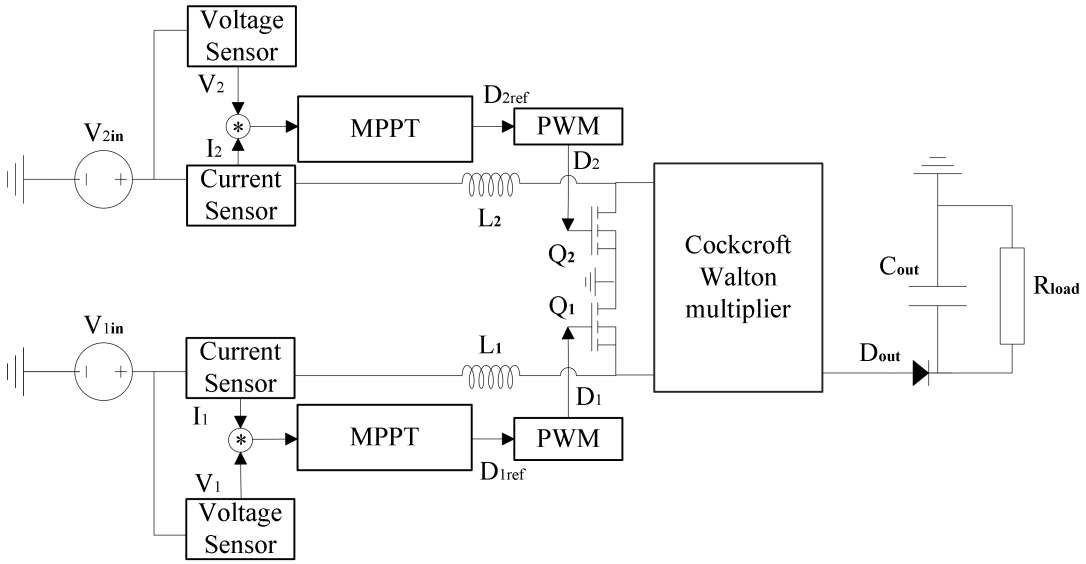

Figure 4.5. Dual MPPT control scheme

Other MPPT algorithms can as be modified to work with the converter such as Fractional Short-Circuit Current MPPT. Refer to [18] for an overview of potential MPPT algorithms.

4.5. RESULTS

An experimental, two-stage, current fed CW multiplier was built to validate the presented design equation. The converter is rated for 450 W with a maximum output

voltage of 400 V. Both the capacitance and the resistance of each stage capacitor greatly influence the overall converter operation as shown in (92). Electrolytic capacitors have the largest capacitance per volume. However they also have high ESRs, poor high frequency characteristics and reliability issues [57]. Additionally, because the entire current through the capacitors is in an ac ripple form, an aluminum electrolytic capacitor able to handle the encountered currents can be difficult to locate. Thus, film capacitors were chosen for all stage capacitors as they have much lower ESRs and higher current ratings. An overview of the used stage components is shown in Table 4.1. The component parameters published in the manufacturer datasheet were used for all calculations. The converter was controlled by an Atmel ATmega 328P 8-bit AVR microcontroller operating at 16MHz. Both the dual current mode control and dual MPPT algorithm were realized on the ATmega. The dual current mode control scheme was implemented as shown in Figure 4.4. The 328P sampled the output voltage and used a PI compensator to generate a reference input current. A ratio of the required input current was commanded to each current compensator. The commanded current of loop 1 and 2 have to equal the commanded input current. The ATmega then sampled the input current of each loop and executed a current compensator for each loop. The PI loops adjusted the duty cycle of Q_1 and Q_2 to obtain the desired input current. The complete microcontroller code for the dual current mode control scheme is given in Appendix A. The dual MPPT algorithm was implemented as shown in Figure 4.5 and described in [18]. A standard P&O algorithm was used, with the exception that the microcontroller insured that the combined duty cycle of both switches exceeded 100% as required by the topology. Appendix B shows the dual MPPT code for the ATmega 328P.

A digital simulation was also created in Simulink®with PLECS®to verify the presented design equations. The parasitic elements such as capacitor ESRs were included in the PLECS model to simulate the actual physical system.

To verify equation (92) the converter was run with a fixed duty cycle. Both inputs were connected to the same source with a voltage of 25V. The ideal gain for the converter in this configuration is equal to 11.1. Figure 4.6 shows the predicted value using equation (92), the simulated and experimental results. The difference between the experimental results and voltage predicted by the equation and simulation is due

Table 4.1. 2 stage prototype current fed Cockcroft-Walton converter component overview

Stage	Passive Component	Switch
Input	60B104C - 100μH Inductor	FDMS86200 N-CH150V 49A
Stage 1	C4ATDBW5600A30J - 60μF Film Capacitor	MBRB20200CTG Si Schottky 200V 20A
Stage 2	C4ATDBW5300A30J - 30μF Film Capacitor	MBRB20200CTG Si Schottky 200V 20A
Output	B32774D4226K - 22μF Film Capacitor	C3D04060E SiC Schottky 600V 4A

to the non-linearities of the stage diodes [6]. The efficiency of the converter using different duty cycle values is shown in Figure 4.7.

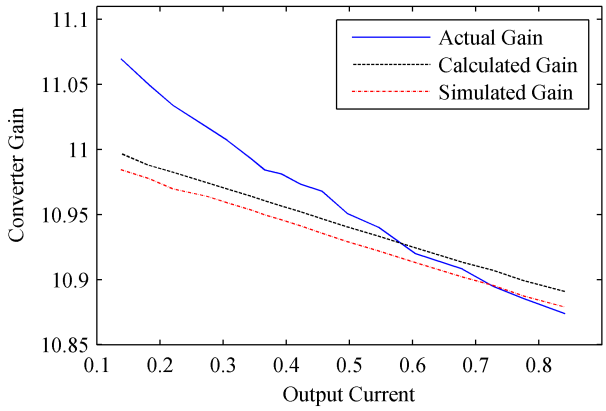

Figure 4.6. Static voltage gain of a 2 stage current-fed Cockcroft Walton multiplier

The ratio between the duty cycles impacts the converter's efficiency. Higher current magnitudes in one of the boost inductors (caused by the power sharing) will result in higher RMS currents. These higher RMS currents cause higher losses in the resistive elements of the circuit, reducing the efficiency of the overall converter. Adjusting the duty cycles to ensure equal currents in both boost inductors can increase the efficiency by lowering the RMS currents. However, this operation state is only an option if both inputs of the converter are connected to the same source.

The control and power sharing capabilities of the converter were verified as well. Figure 4.8 shows the output voltage and current through the individual loops. Initially the controller is set to command equal current from both loops. At $t = 213$ loop 1 was assigned a higher and loop 2 a lower ratio of the required input current. Figure 4.8. verifies that the output voltage can be maintained when the input current to each loop is changed.

As described in the previous section the converter is capable of performing maximum power point tracking on two panels simultaneously. Each input of the converter is connected to a 80W solar panel. The converter is feeding into a 180V constant voltage bus. The power flow from each solar panel is shown in Figure 4.9. Initially only solar panel 2 is connected to the converter. Panel 1 is disconnected to

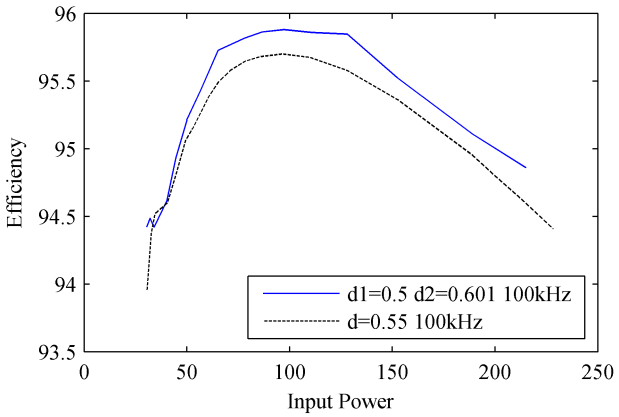

Figure 4.7. Efficiency of a 2 stage current-fed Cockcroft Walton multiplier

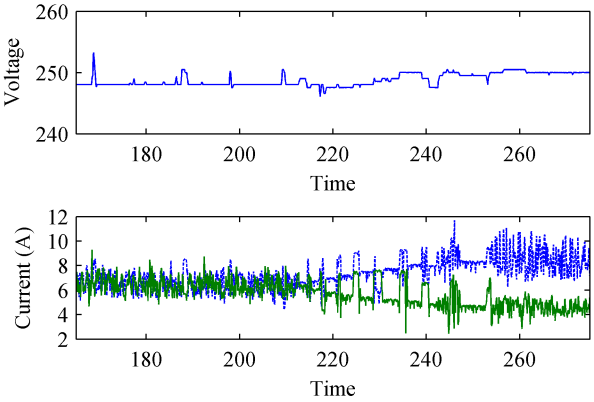

Figure 4.8. Current-fed Cockcroft Walton multiplier with regulated output voltage and power sharing

simulate a the panel being inoperable. Panel 2 is capable of delivering almost 100% of its maximum power despite a 100% missmatch between the panels. At $t = 106$ panel 1 is connected to the converter. At this point panel 1 is covered in a 2 mil translucent plastic sheet to simulate the panel being shaded. The power output of both panel 1 and panel 2 increase after an initial settling period. The converter is now capable of operating panel 2 at its maximum power point as the voltage gain of the converter is high enough to allow variation of the duty cycle. Before panel 1 was connected, the gain of the converter had to be maximized to allow the high 180V output voltage to be met. This did not allow for variation of the duty cycle to perform maximum power point tracking. This fact is described by equation (97). At $t = 195$, the sheet is removed to allow panel 1 to receive full sunlight. With both panels unshaded, the converter is capable of operating them at their maximum power point. This is shown between $t = 225$ to $t = 245$. At $t = 245$ panel 1 is unplugged once more. After a brief settling time, the converter adjusts the duty cycle of panel 2 to allow it to operate close to its maximum power point again.

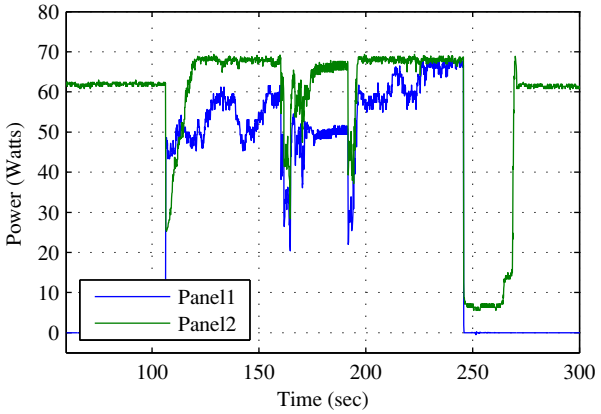

Figure 4.9. Dual maximum power point operation

4.6. CONCLUSION

Current fed SC converter topologies were discussed in brief in the beginning of this section. A current-fed Cockcroft Walton multiplier was presented in great detail

to illustrate the difference in the design process. Many SC converters have inherently multiple inputs from which the draw power discontinuously. This fact can be used to generate current-fed SC converter that support multiple input operation. This feature was discussed and demonstrated with the CW multiplier as well.

While the inclusion of inductors somewhat offsets the benefits of SC converters, they are still a viable alternative to transformer based converters. A large selection of premade inductors exist that can be easily included in a converter design. In contrast, high frequency transformers have to be custom designed and made, which greatly increases the cost and the design complexity.

5. CONCLUSIONS

The static performance of hard-switched switched capacitor converters was described in great detail in this thesis. The previously presented SSL and FSL was reexamined to correct misconceptions from previous works [12, 28, 29]. A new switching limit, the ISL, was derived as well to model the equivalent resistance of the converter at very high switching frequencies. The previously presented RC circuit equation and the newly derived RL circuit equations were simplified using a curve-fit proposed in [3, 37]. The correction term proposed in [37] was further refined to generate a generalized curve-fit for both equations. The equations were combined to obtain a complete model of the equivalent resistance of hard-switched switched capacitor converters.

The equivalent resistance model was generalized for any high order SC converter using charge vectors. An expression describing the switching losses through an equivalent conductance was derived as well. The equivalent resistance and conductance were combined to obtain an equivalent circuit capable of predicting the total power and voltage losses in a hard-switched SC converter. The challenges of implementing a regulated output voltage for SC converters was described as well.

The prospects of using a current-fed SC converter were examined. A current-fed Cockcroft-Walton converter was derived in full, providing all the required design equations. The multiple input configuration of most SC converters allows for power sharing in current-fed SC converters. Potential control algorithms were presented and verified on a prototype converter.

A number of research projects can stem from the concepts presented in this thesis. The complete loss model presented in this thesis can be used to realize a variable frequency control scheme to maximize SC converter efficiency under all operating conditions. In [42] a dynamic model for hard-switched SC converter operating either in the SSL or FSL was presented. A similar derivation to [42] can be done using the ISL to obtain a dynamic model of hard-switched SC converters operating either in the FSL or ISL. The dynamic response of current-fed SC converters can be analyzed along those lines as well.

APPENDIX A

CURRENT SHARING MICROCONTROLLER CODE

```
#include "TimerOne.h" //Timer 1 PWM Library
#include "FrequencyTimer2.h" //Timer 2 Interrupt Library
#include <avr/io.h>
#include <stdint.h>

//Setting up constants
const uint8_t PWM1_PIN = 9; //PWM1 on Pin9
const uint8_t PWM2_PIN = 10;//PWM2 on Pin10
const uint8_t Vout_Pin = 3; //Vout Measurement ADC Pin
const uint8_t V1_Pin = 4; //V1 Measurement ADC Pin
const uint8_t V2_Pin = 1; //V2 Measurement ADC Pin
const uint8_t I1_Pin = 0; //I1 Measurement ADC Pin
const uint8_t I2_Pin = 5; //I2 Measurement ADC Pin
const int PWM1_Max = 800;// 80% Max Duty cycle
const int PWM1_Min = 200;// 20% Min Duty cycle

//PI Controler Tuning Constants
const float KpV = 0.25; //Gain term for Vout PI loop
const float KiV = 0.25; //Integral term for Vout PI loop
const float KpI = 1; //Gain term for Iout PI loop
const float KiI = 1; //Integral term for Iout PI loop
float Voutset = 250.0; //Set point for output voltage
float Iref = 0; //Reference Input current for both current
// loops

//Different Prescaler Settings for ADC
const unsigned char PS_4 = (1 << ADPS1);
const unsigned char PS_8 = (1 << ADPS1) | (1 << ADPS0);
const unsigned char PS_16 = (1 << ADPS2);
const unsigned char PS_128 = (1 << ADPS2) | (1 << ADPS1)
| (1 << ADPS0);
```

```
//Setting up program memeory
volatile int PWM1 = 600; //Current PWM1 value starts at 60%
volatile int PWM2 = 400; //Current PWM2 value starts at 60%
float PWM1d = 600;
float PWM2d = 400;
int IntVout = 0; //Current ADC value of output voltage
int IntV1 = 0; //Current ADC value of input voltage 1
int IntV2 = 0; //Current ADC value of input voltage 2
int IntI1 = 0; //Current ADC value of input current 1
int IntI2 = 0; //Current ADC value of input current 2
int incomingByte = 0; //Serial Buffer Variable
volatile float RealVout = 0; //Real value of current
//output voltage
volatile float RealV1 = 0; //Real value of current
// input voltage 1
volatile float RealV2 = 0; //Real value of current
//input voltage 2
volatile float RealI1 = 0; //Real value of current
//input current 1
volatile float RealI2 = 0; //Real value of current
//input current 2
float Vouterror = 0; //Output Voltage error
float Voutintegral = 0; //Current integral value
float I1error = 0; //Loop 1 Current error
float I1integral = 0;//Loop 1 integrator
float I2error = 0; //Loop 2 Current error
float I2integral = 0;//Loop 2 integrator
float Gain1 = 0.5; //Ratio of commanded input current to I1
float Gain2 = 0.5;//Ratio of commanded input current to I2
float time = 0.001;
//Time constant for integration based on ISR time interval
volatile float realtime = 0;//Hold current time for data
```

```
//logging

void setup(){
  Serial.begin(115200); //Set Serial to fastest
  //possible speed

  //Configure output pins
  pinMode(PWM1_PIN, OUTPUT);
  pinMode(PWM2_PIN, OUTPUT);
  Timer1.initialize(10);//Sets PWM freqeuncy to 100kHz
  Timer1.pwm(PWM1_PIN,PWM1);//Starts PWM1 with default
  //duty cycle
  Timer1.pwm(PWM2_PIN,PWM2);//Starts PWM2 with default
  //duty cycle

  //Sets up ISR to execute PI loop at fixed time interval
  FrequencyTimer2::setPeriod(1000);//Set up ISR period
  FrequencyTimer2::enable();//Initialize ISR timer
  FrequencyTimer2::setOnOverflow(controller);//Enable ISR

  //Sets up ADC for faster read than Default Analog Read
  ADCSRA &= ~PS_128; //Clears ADC Pre-Scaler
  ADCSRA |= PS_16;
  //Change Pre-Scaler to allow fastest possible ADC
}

void controller() //Controller ISR
{
  //Updates PWM
  Timer1.pwm(PWM1_PIN,PWM1);
  Timer1.pwm(PWM2_PIN,PWM2);
  //Pull new measured values
```

```
IntVout = analogRead(Vout_Pin); //ADCsingleREAD(Vout_Pin);
IntV1 = analogRead(V1_Pin);//ADCsingleREAD(V1_Pin);
IntV2 = analogRead(V2_Pin);//ADCsingleREAD(V2_Pin);
IntI1 = analogRead(I1_Pin);//ADCsingleREAD(I1_Pin);
IntI2 = analogRead(I2_Pin);//ADCsingleREAD(I2_Pin);
//Convert values to real number to make computations
RealVout=IntVout*(500.0/1024.0);
RealV1=IntV1*(50.0/1024.0);
RealV2=IntV2*(50.0/1024.0);
RealI1=(IntI1-528)*(5.0/1024.0)*15.625;
//polarity on I2 is reverse!
RealI2=(528-IntI2)*(5.0/1024.0)*15.625;
//Run outer PI loop for Output voltage
Vouterror=Voutset-RealVout;
Voutintegral=Voutintegral+Vouterror*time;
Voutintegral=constrain(Voutintegral,-100,100);
Iref=KpV*Vouterror+KiV*Voutintegral;
//Run PI loop for both inner Average Current Mode loops
//Loop 1
I1error=Iref*Gain1-RealI1;
I1integral=I1integral+I1error*time;
I1integral=constrain(I1integral,0,1024);
PWM1d=KpI*I1error+KiI*I1integral;
//Loop 2
I2error=Iref*Gain2-RealI2;
I2integral=I2integral+I2error*time;
I2integral=constrain(I2integral,0,1024);
PWM2d=KpI*I2error+KiI*I2integral;
//Insures duty cycle limitation of CFCW multiplier
PWM1=(int) PWM1d;
PWM2=(int) 1024.0-PWM2d;
PWM1=constrain(PWM1,PWM1_Min,PWM1_Max);
```

```
  PWM2=constrain(PWM2,200,(1100-PWM1));
  realtime += 0.001;
  //Done with controller execution,
 //wait for next iteration to update controller
}

//Main Program, handles data-logging only
//as controller is time sensitive
void loop(){
Serial.print(realtime);
Serial.print(",");
Serial.print(RealVout);
Serial.print(",");
Serial.print(realtime);
Serial.print(",");
Serial.print(RealI1);
Serial.print(",");
Serial.print(realtime);
Serial.print(",");
Serial.print(RealI2);
Serial.print(",");
Serial.print(realtime);
Serial.print(",");
Serial.println(Gain1);

//Changes the current distribution of the input loops
//if a character is received over the serial port
while (Serial.available()) {
  incomingByte = Serial.read();
  if(incomingByte==61){
    Gain1 = 0.7;
    Gain2 = 0.3;
```

```
    }
    else if(incomingByte==114){
      Gain1 = 0.5;
      Gain2 = 0.5;
    }
  }
  }
```

APPENDIX B

DUAL MPPT MICROCONTROLLER CODE

```
#include "TimerOne.h"
#include "FrequencyTimer2.h"

const int PWM1_PIN = 9; //PWM1 on Pin9
const int PWM2_PIN = 10; //PWM2 on Pin10
const int AVG_NUM=30;
//Average measurement over specified number
int Delta1 = 5; //Duty cycle step change 1
int Delta2 = 5; //Duty cycle step change 2
//unsigned long Power1c = 0; //Current Power Measurement 1
float Power1p = 0; //Last Power Measurement 1
//unsigned long Power2c = 0; //Current Power Measurement 2
float Power2p = 0; //Last Power Measurement 2
int PWM1 = 600; // Start PWM1 at 60%
int PWM2 = 400; // Start PWM2 at 60%
int PWM_Max1=800; //80% Max duty cycle
int PWM_Min1=200; //20% Min duty cycle
int Current1 = 0; //Current Measurement1
int Current2 = 0; //Current Measurement2
int Voltage1 = 0; //Voltage Measurement1
int Voltage2 = 0; //Voltage Measurement2
int incomingByte = 0; //Serial Buffer Variable
float V1actual = 0; //Float representation of
//control variables
float V2actual = 0;
float I1actual = 0;
float I2actual = 0;
float P1actual = 0;
float P2actual = 0;
volatile float ctime = 0;//Time stamp for data logging

//Define different ADC prescaler
```

```
const unsigned char PS_4 = (1 << ADPS1);
const unsigned char PS_8 = (1 << ADPS1) | (1 << ADPS0);
const unsigned char PS_16 = (1 << ADPS2);
const unsigned char PS_128 = (1 << ADPS2) | (1 << ADPS1)
 | (1 << ADPS0);

void setup(){
 Serial.begin(9600);
 Timer1.initialize(10); //Set PWM to 100kHz
 Timer1.pwm(PWM1_PIN,PWM1);
 Timer1.pwm(PWM2_PIN,PWM2);
 //change timer interrupt to generate a time stamp
//every 1ms
 FrequencyTimer2::setPeriod(1000);//Set up ISR period
 FrequencyTimer2::enable();//Initialize ISR timer
 FrequencyTimer2::setOnOverflow(time);//Enable ISR

 ADCSRA &= ~PS_128;
 ADCSRA |= PS_16; //Change Pre-Scaler to allow faster ADC
 }

//Function to return the average of a sensor reading
int read_adc(int channel){
    int sum = 0;
int temp;
 int i;
  for (i=0; i<AVG_NUM; i++) {
  // loop through reading raw adc values AVG_NUM number
  // of times
    temp = analogRead(channel);
    // read the input pin
    sum += temp;
```

```
    // store sum for averaging
    //delayMicroseconds(100);
    // pauses for 100 microseconds
  }
   return(sum / AVG_NUM);
  // divide sum by AVG_NUM to get average and return it
}

void time()
{
  ctime+=0.001;
}

void loop(){ //Main Program
//See if Data is coming over the serial communication
  while (Serial.available()) {
                // read the incoming byte:
                incomingByte = Serial.read();
  }
  if(incomingByte==61){ //If a "=" is sent over serial,
  //Sweep program will plot the I-V characterisitc of the
  //attached  solar panel
     Serial.print("Beginning Sweep:Panel 1");
     Serial.println();
    PWM1=450; //Reset PWMs to fixed values (PWM=45%)
    PWM2=400; //(PWM2= 60%)
     Timer1.pwm(PWM1_PIN,PWM1);
     Timer1.pwm(PWM2_PIN,PWM2);
     while(PWM1<=750){ //Sweep first panel by increasing duty
     //cycle by 1% until at 80%)
        delayMicroseconds(100);
        //wait 100uS to let the converter settle
```

```
    //and get a clean measurement
    // Read Current and voltage from Panel 1
    Current1 = read_adc(0);
    Voltage1 = read_adc(1);
    //Sent I&V information for panel 1
    Serial.print("{C1,T,");
    Serial.print(Current1);
    Serial.print("}{V1,T,");
    Serial.print(Voltage1);
    Serial.print("}");
    Serial.println();
   PWM1+=10; //Increase duty cycle by 1%
    Timer1.pwm(PWM1_PIN,PWM1);
 }
 PWM1=600; //Reset duty cycle to fixed values
\\(PWM1=60%)
 PWM2=550; //(PWM2=45%)
 Timer1.pwm(PWM1_PIN,PWM1);
 Timer1.pwm(PWM2_PIN,PWM2);
 Serial.print("Beginning Sweep:Panel 2");
 Serial.println();
 while(PWM2>=308){//Sweep second panel until
 //80% duty cycle)
    delayMicroseconds(100);
    Current2 = read_adc(2);
    Voltage2 = read_adc(3);
    //Sent I&V information for panel 2
    Serial.print("{C2,T,");
    Serial.print(Current2);
    Serial.print("}{V2,T,");
    Serial.print(Voltage2);
    Serial.print("}");
```

```
        Serial.println();
        PWM2-=10; //Increase duty cycle by 1%
        Timer1.pwm(PWM2_PIN,PWM2);
      }
   incomingByte=0; //Reset Buffer variable
   PWM1=600; //Reset PWM duty cycles to default values
   PWM2=400;
   Timer1.pwm(PWM1_PIN,PWM1);
   Timer1.pwm(PWM2_PIN,PWM2);
 }
//If command isn't sent regular MPPT is executed
Current1=read_adc(5);
Voltage1=read_adc(4);
Current2=read_adc(0);
Voltage2=read_adc(1);
V1actual=Voltage1*(50.0/1024.0);
V2actual=Voltage2*(50.0/1024.0);
I1actual=(528-Current1)*(5.0/1024.0)*9.090909;
I2actual=(Current2-528)*(5.0/1024.0)*9.090909;
P1actual=V1actual*I1actual;
P2actual=V2actual*I2actual;
if(P1actual>=Power1p){ //P&O Sweep algorithm
  PWM1+=Delta1;
}
else{
 Delta1= (-Delta1);
PWM1+=Delta1;
}
if(P2actual>=Power2p){
  PWM2+=Delta2;
}
else{
```

```
    Delta2 = (-Delta2);
   PWM2+=Delta2;
}
PWM1=constrain(PWM1,PWM_Min1,PWM_Max1);
PWM2=constrain(PWM2,200,(1100-PWM1));
Timer1.pwm(PWM1_PIN,PWM1);
Timer1.pwm(PWM2_PIN,PWM2);
//Sent current state data for data logging
Serial.print(ctime);
Serial.print(",");
Serial.print(PWM1);
Serial.print(",");
Serial.print(PWM2);
Serial.print(",");
Serial.print(I1actual);
Serial.print(",");
Serial.print(V1actual);
Serial.print(",");
Serial.print(P1actual);
Serial.print(",");
Serial.print(I2actual);
Serial.print(",");
Serial.print(V2actual);
Serial.print(",");
Serial.print(P2actual);
Serial.println();
Power1p=P1actual; //Save states for next iteration
Power2p=P2actual;

}
```

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