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Constructing conducted emission models for integrated circuits

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CONSTRUCTING CONDUCTED EMISSION MODELS FOR INTEGRATED CIRCUITS

by

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ABSTRACT

Conducted emissions, noise conducted out of integrated circuit pins, play an important role in determining the system level EMC performance. Characterizing conducted emissions from ICs is investigated and the corresponding noise models are developed in this thesis. Both simulation IBIS and measurement based methods for noise-model construction are studied. The constructed noise source model for a test IC is applied in system-level simulations and the calculated far field radiation is validated with measurements. The agreement in the simulated and measured results demonstrates the effectiveness of the constructed model for characterizing the conducted emissions from an IC I/O pin.

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1. INTRODUCTION

In high-speed digital or mixed RF/digital designs, digital ICs are the main contributors to the noise and interference issues, including system-level EMI, and RF interference from digital to wireless. Concerning about the significant role of IC emission, the system level electromagnetic emissions (EMEs) characterization techniques are developed at IC-level [1], [2]. Several standards are created regarding EME, IEC 61967-4 [6]. The nature of the digital circuits requires frequent logic transitions of the internal gates inside a digital IC to achieve functionalities and transfer data [3]. The transient currents related to the logic transitions cause noise, which can be propagated conductively out of the pins of the IC (denoted conducted emissions), or coupled to other PCB radiators through electric or magnetic field, or even directly radiated out (denoted radiated emissions) [3],[4], as illustrated in Figure. 1.1. It is critical to accurately understand the noise sources at the IC, in order to better control, and predict more effectively, the system-/board-level EMC performance [5]. The noise models of the IC can also be used to understand the noise mechanisms inside the IC and provide useful guidelines for IC/package designs. Thus, IC modeling in terms of EME is desired.

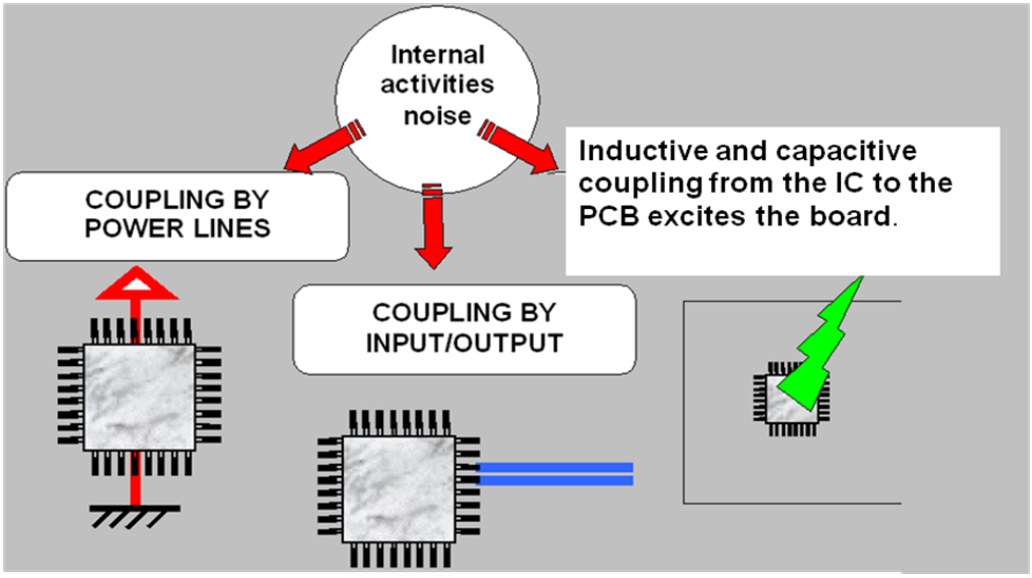


Figure 1.1 Digital IC is the main noise source in an electronic system. Noise generated due to the internal activities can be conducted out from the IC pins, or coupled to PCB radiators either inductively or capacitively, or directly radiated out.

Noise models for conducted emissions can be developed based on both measurements and modeling. When some information is available for an IC from the IC vendor, modeling methodologies are very powerful to generate effective conducted emissions models. However, in most of the cases, IC information is proprietary and may not be available to PCB/system design engineers. Then, model extraction procedures from measurements are highly desirable.

There are established international standards for IC conducted emissions measurements, the 150 Ω method for I/O pin, 1 Ω method for power/ground pin and the magnetic probe method [6] [7] [8]. Based on these established measurement procedures, simple noise source models can be assumed for IC conducted emissions by measuring the spectra of off-chip current [3]. However, in the paper of Villavicencio [5], it is pointed out that these methods for modeling conducted emissions are not accurate enough. And these methods cannot support high frequency measurement, because in high frequency the parasitic inductance plays a dominate role for the resistance, no matter it is 1 ohm resistance or 150 resistance. This parasitic inductance with destroy the measurement and

these method won't work anymore. In terms of these, new measurement method is studied for extracting noise source in high frequency. Based on the structure of real product, total voltage at the output of IC pin is measured. This total voltage contains information about IC and the structure. The conducted emission can be estimated based on this total voltage in full-wave simulation, the model of which is the structure from output of IC pin.

Besides measurement based noise source extraction, modeling-based noise-source extraction is studied when some information of the IC under study is available. Similar approaches as the ones for noise-source extraction from measurements will be used based on modeling. For I/O pins, IBIS models for the I/O pins of the IC under study are investigated. The IBIS models [11] [12], excellent for signal integrity simulations [13][14], will give a good estimation of the I-V relationship at the I/O pins that can also be used to extract the Thevenin equivalent voltage sources. The V-I curve from IBIS model captures rise/fall time information when the IBIS model is generated [15][16][17]. So it can be extracted as an accurate IC emission model. Also besides Thevenin's equivalent source, a total voltage can be obtained like did in measurement. And this total voltage is noise source correlated with the certain structure.

To extract noise source from IBIS model, the specification of IBIS model is introduced. IBIS (Input/Output Buffer Information Specification) is behavior model. It is used to describe the behavior of input, output from IC. IBIS is the buffer which contains a set of V/I, V/T curves and these can be used for SI, EMI simulation. IBIS model provide at least two V/T curves, which represent high level output and low level output. V/I curves include the nonlinear effect of ESD diodes, transistor. V/T curves provide information about the speed to change from low to high and from high to low. The advantage of IBIS model is that it doesn't provide IC logic function, as SPICE model does. And from SPICE model the IC logic can be extracted. In order to protect secrete in IC, vendors usually provide IBIS model instead of SPICE model. Another advantage is simulation by IBIS model costs 10 times less than SPICE model because of its simply structure.

In this paper, the IC is a output buffer and the IBIS model includes 3 parts, as shown in Figure 1.2. The first part is NMOS and PMOS transistors. They represent the

high level and low level output. The second part is ESD diodes. They represent the IC protection circuits. The third parts are package inductance, resistance, capacitance and total capacitance of IC pad, diodes and transistors.

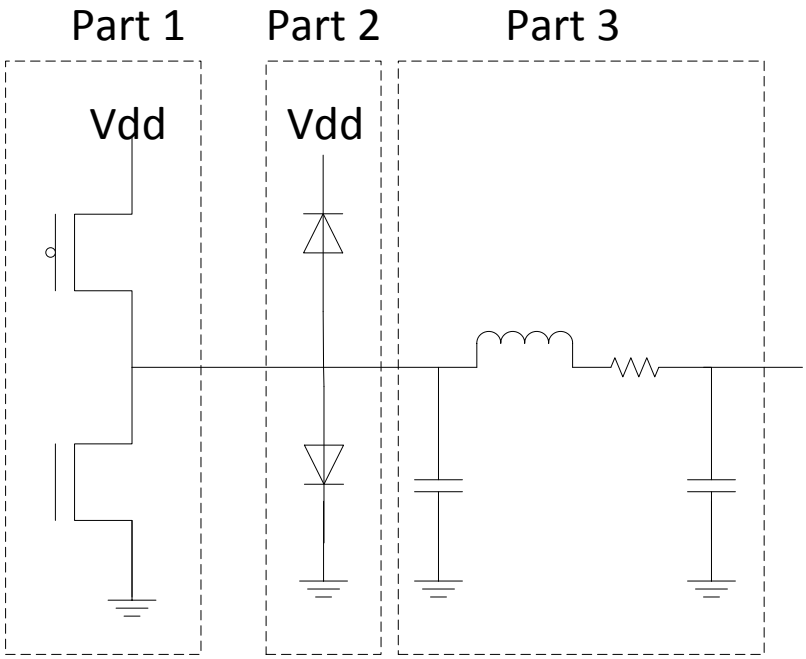


Figure 1.2. Output IBIS model structure

In general, different processes are possible for modeling IC emissions: established international standards and the two novel methods used in this paper.

More in detail, IC emission model is extracted in three methods: Measured total voltage correlated with certain structure, IBIS Thevenin's equivalent source and IBIS total voltage correlated with certain structure. The advantage of the total voltage in measurement is that no resistors are needed to mount on the testboard. The total voltage is measured by active probe, which is with high input impedance and will not change the current at the IC pin. Also the probe tip is very small so that the parasitic inductance is quite small and can be used to very high frequency, up to 10 GHz. The advantage of IBIS

Thevenin's equivalent noise model is that the model is independent of structure connected with IC pin, which means once the model is extracted it can be used in any structures for modeling IC emission. The trace, load, PCB structure has nothing to do with this source model.

For the measurement of total voltage, a testboard is designed. A clock/data buffer is the IC to be modeled. The output of the IC is connected to a long trace, which is a 53 Ohm micro-stripline and the same model is built in full-wave simulator HFSS. The total voltage is measured by active probe right at the output of IC. The IC drives the trace to radiate and far field of this testboard is measured.

For IBIS Thevenin's equivalent source, IBIS model is used in ADS and different load is used to calculate equivalent voltage and impedance for the IBIS model. After extracting the noise source, it is applied in the HFSS model built before for far field simulation. The far field results are compared with measurement for validation.

For IBIS total voltage, the S-parameter from the HFSS model is extracted and used in ADS as the load of IBIS model. Then total voltage is obtained at the output of IBIS model. This total voltage is also applied in the same HFSS model for far field simulation and the results are compared with those from other two methods.

In this paper, the section one is introduction. Section two is about studying how to apply IBIS model in the two methods: IBIS total voltage source and IBIS Thevenin's equivalent source. Section three is about how to extract total voltage source from measurement. Section four is about how to extract IBIS Thevenin equivalent source and total voltage from IBIS model. Section five gives the far field measurement from the testboard. Section six is about far field simulation from IBIS Thevenin's equivalent source and IBIS total voltage source.

2. STUDY OF NOISE SOURCE EXTRACTION FROM IBIS MODEL

In this section, how to apply IBIS model to extract IC sources is studied. Two approaches are carried out. The approach one is to extract total voltage from IBIS model, correlated with certain structure s-parameter. The approach two is to extract Thevenin's equivalent source with IBIS model.

2.1. APPROACH ONE: TOTAL VOLTAGE METHOD

IBIS is a behavior model representing IC product [12]. And it can be utilized to extract IC noise model. After that the far field radiation can be obtained in full-wave simulation. IBIS model is V-I curves buffer and it cannot be used in full-wave simulation directly. So co-simulations are carried out in order to apply IBIS models in full-wave simulation. For this part, the approach one is discussed.

As shown in Figure 2.1, first of all, a structure without load and sources is built and they interconnect with ports in the full-wave model. In real design, this structure is the layout connecting each component in the board. It is the signal path in real board. Secondly, the S-parameters are extracted from full-wave simulation and imported into circuit simulator, ADS. In ADS IBIS model can be applied and load in real board is added in. Finally, Voltage at interconnection between IBIS model and SNP file is obtained. The voltage used as voltage source is applied on full-wave model in HFSS; and then near or far field can be calculated in full-wave simulation.

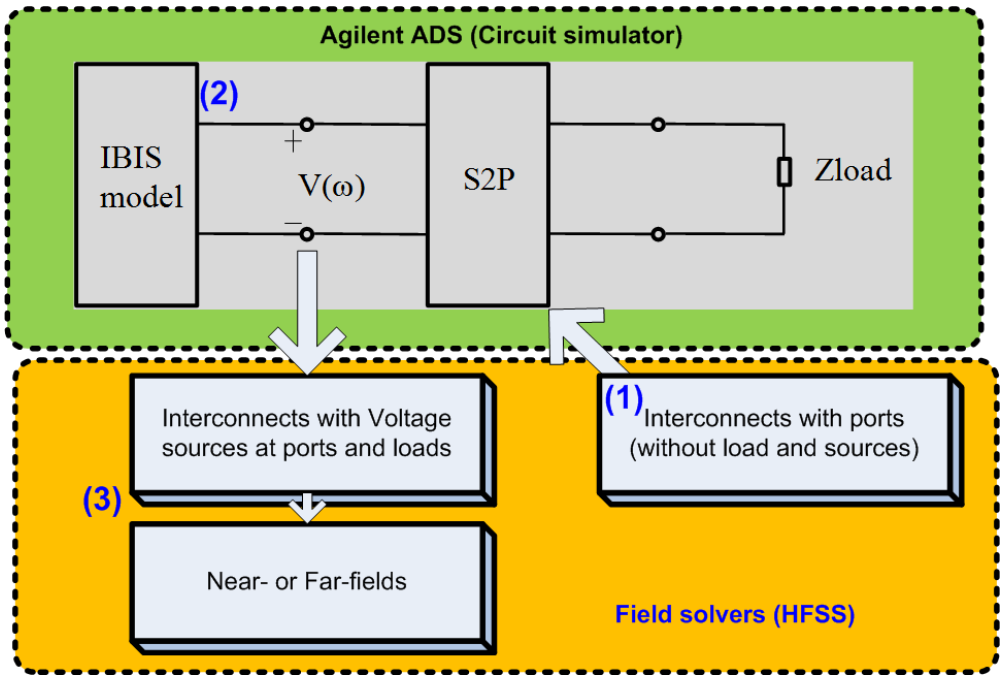


Figure 2.1. Approach one procedure

In order to study these two approaches, a test structure as shown in Figure. 2.2, is built. The slot length is set to ½ wave length at 1.6GHz so that there will be maximum radiation, as shown in Figure.2.3. Mesh in HFSS simulator should be increased because the default mesh is not dense enough, the difference is shown in approach 2.

For the first step in approach 1, the structure, connecting sources which are represented by IBIS models, is simulated in HFSS. All the ports in full-wave model are where sources locate. S-parameters can be extracted and it contains all information of the structure in frequency domain.

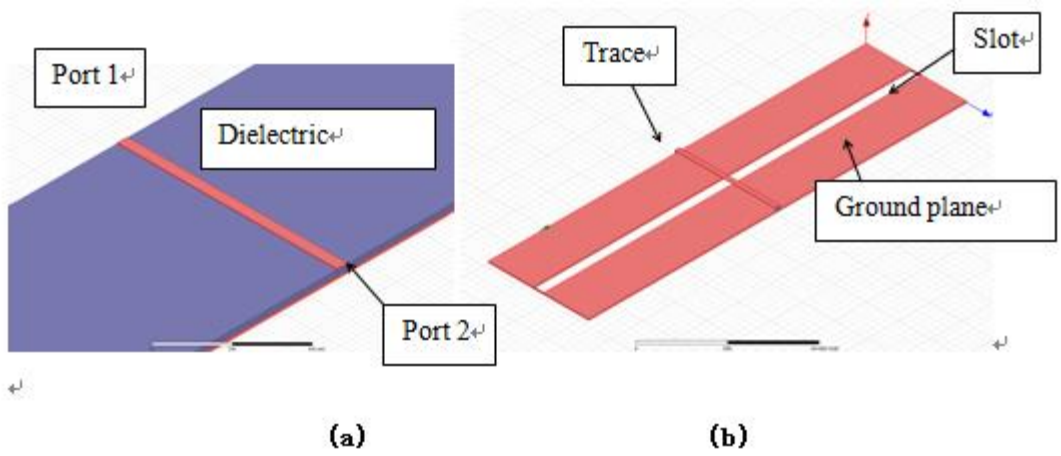


Figure 2.2. Full-wave simulation structure (a) view with dielectric (b)view without dielectric

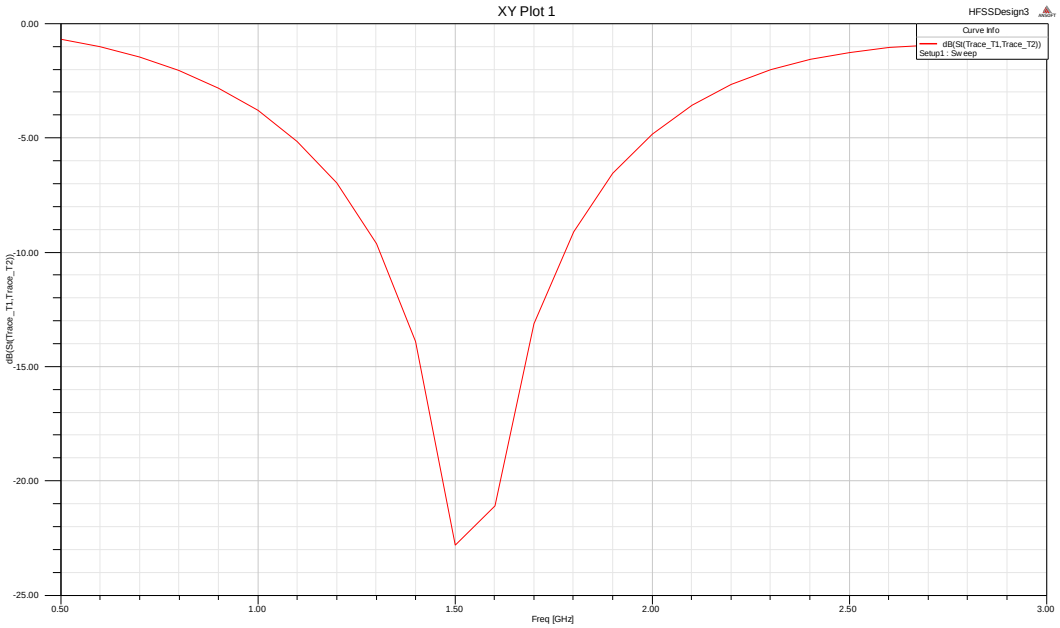


Figure 2.3. Resonate at 1.6GHz

In second step, IBIS model is applied in ADS as shown in Figure 2.4. The trigger for IBIS model is clock wave with period 0.625ns so that the fundamental frequency is

1.6GHz, rise/fall time 0.1ns, high voltage 1.5V, low voltage 0V. In order to achieve accurate total voltage in frequency domain simulation time should be large enough. And the step in time domain simulation is set to 1/10 of the rise/fall time which means there are 10 sampling points during rise/fall time. It meets the Nyquist law. In this step, total voltage at the output of IBIS model is obtained and transferred from time domain to frequency domain. Then this frequency domain total voltage is to be applied in the full-wave simulation.

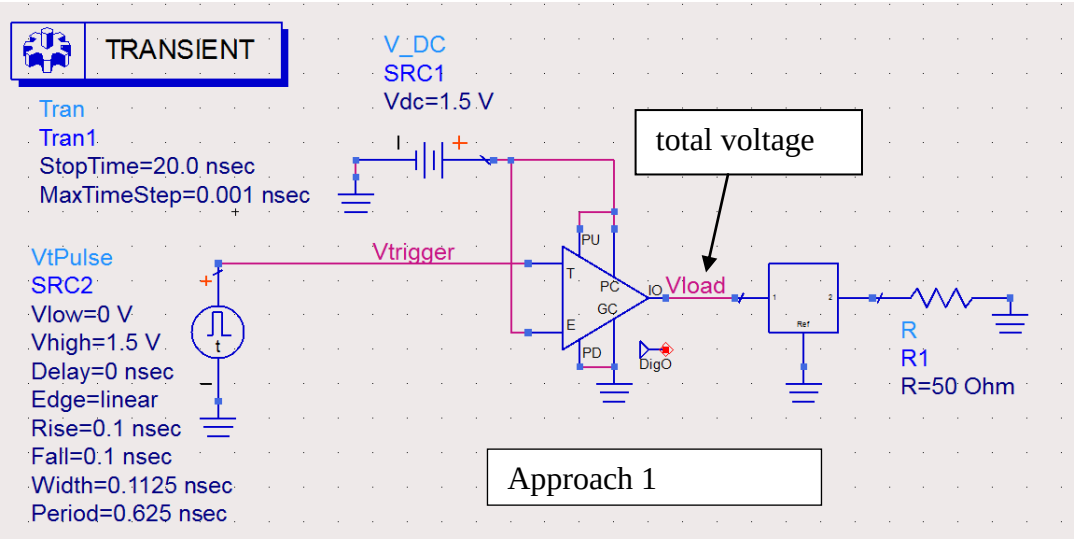


Figure 2.4. approach 1 schematic

In the third step of approach 1, total voltage (frequency domain) obtained is applied as total voltage in the lumped port in HFSS structure. Also load is applied to the HFSS structure, as shown in Figure.2.5. In this case, voltage at 1.6 GHz is used in HFSS model, as shown in Figure. 2.6. What's more, if all the frequency components are needed to be taken into consideration, "pwl" function can be used to do this operation. Frequency domain total voltage can be written into database by pwl function, as shown in Figure. 2.7. And it is written into a "xx.tab" file with frequency in the first column, unit in Hz

and magnitude or phase in the second column, unit in V or deg. After setting sources, a sphere with 3 meter radius is created, shown in Figure 2.8. After simulation in HFSS, far field is obtained on this 3 meter sphere, shown in Figure 2.9.

In conclusion, total voltage is extracted in from IBIS model related with HFSS s-parameter, in ADS. Then this source is applied in HFSS as total voltage in Lumped port. After simulation, the far field on the sphere defined is obtained. In this way IC model is extracted and it is used to get far field.

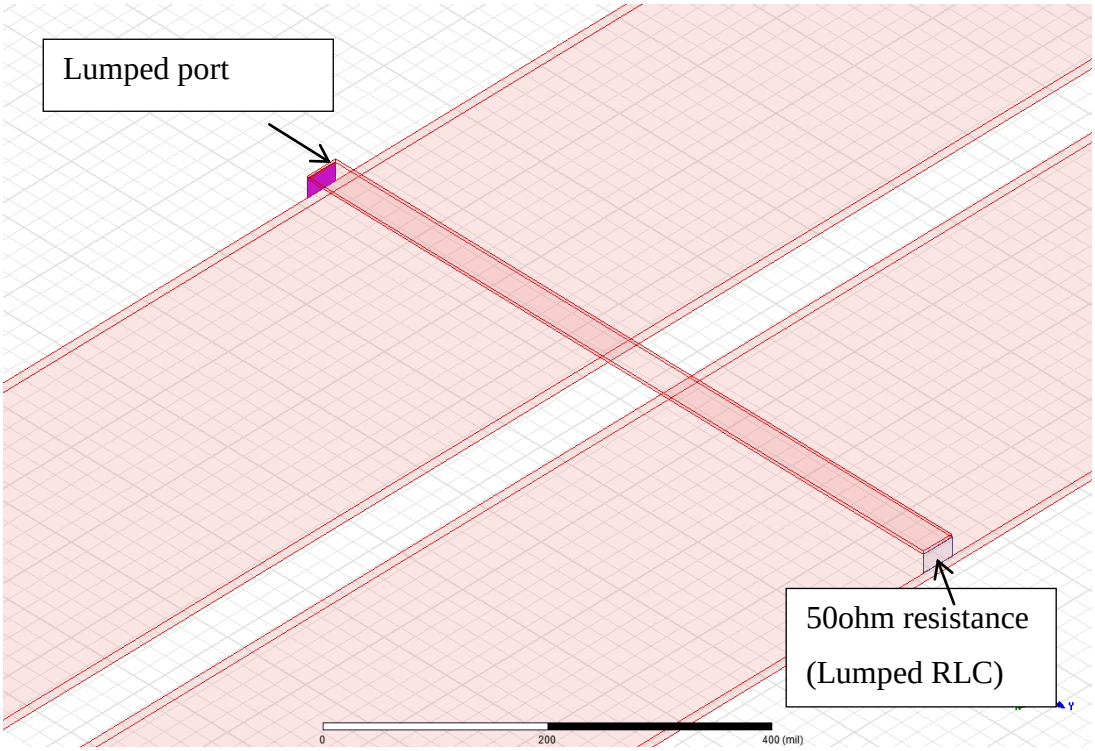


Figure 2.5. Port and port settings

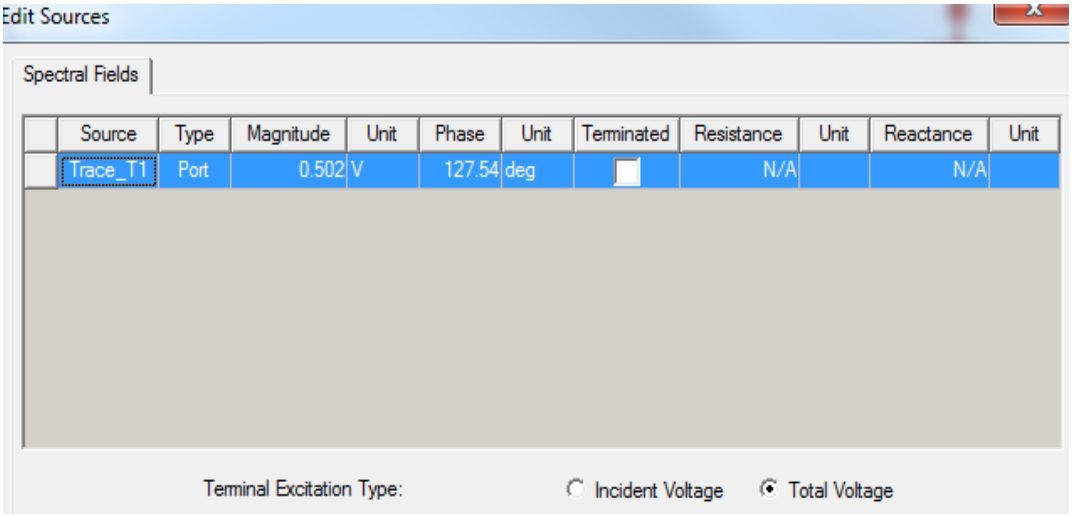


Figure 2.6. Voltage source at fundamental frequency

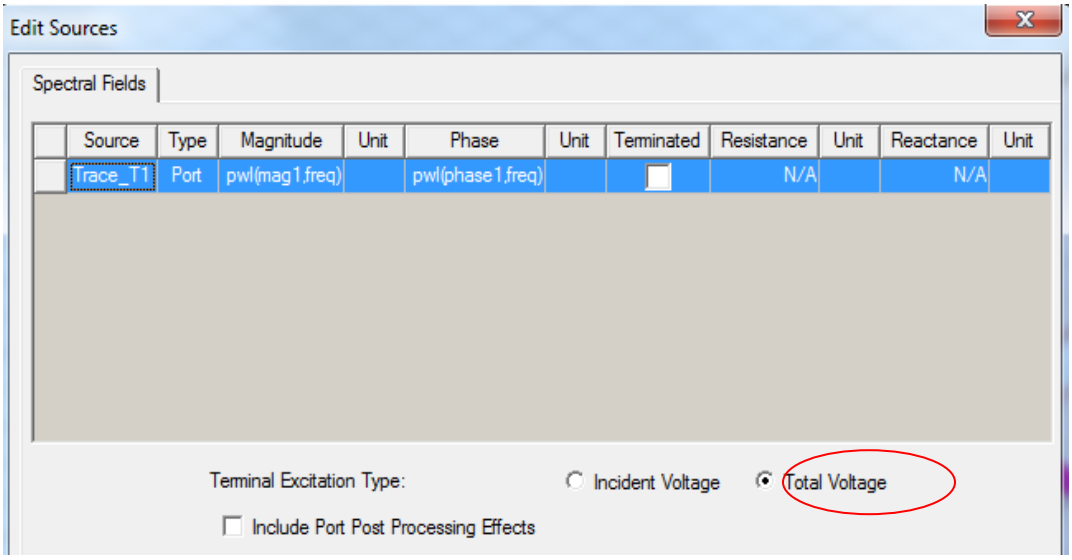


Figure 2.7. Total voltage is applied in lumped port by pwl function

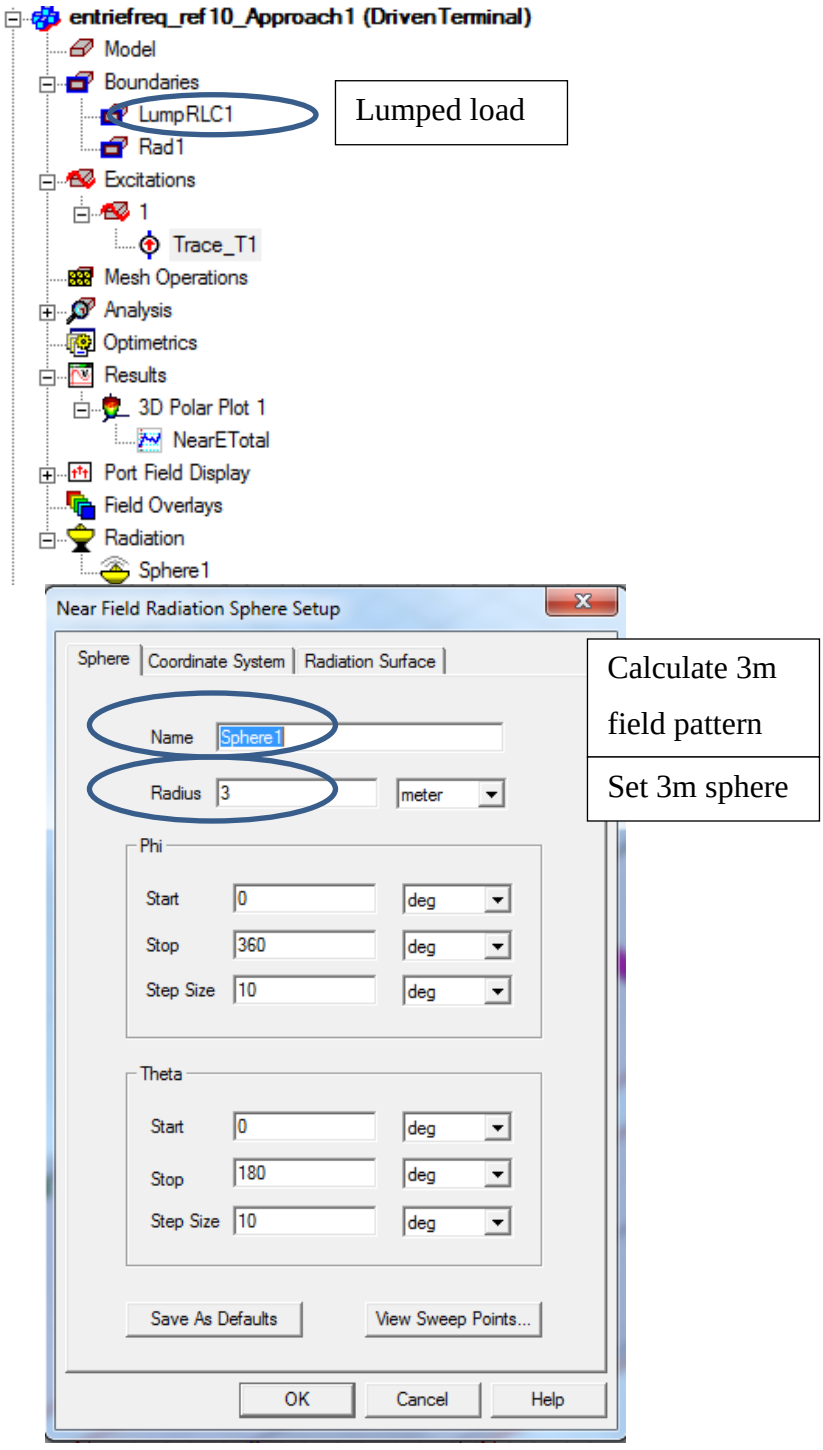


Figure 2.8. Settings of lumped load and 3m field sphere for far field pattern

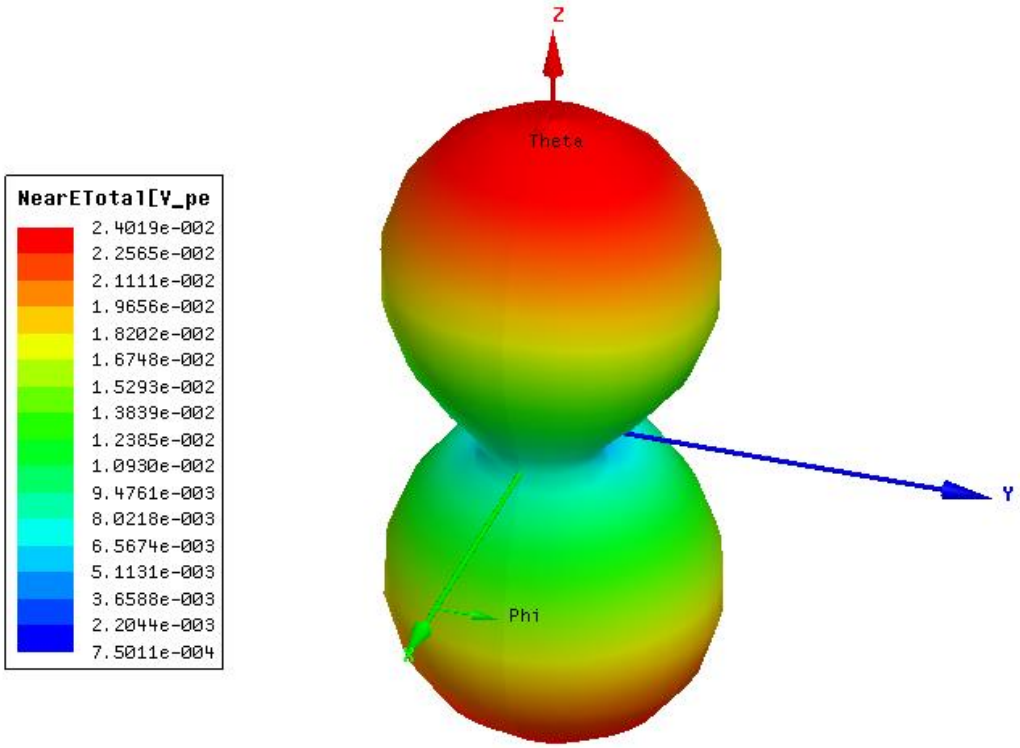


Figure 2.9. Field pattern in 3m far field

2.2. APPROACH TWO: THEVENIN EQUIVALENT SOURCE

Thevenin's theorem indicates that any circuit sources and impedance can be transformed to Thevenin equivalent. In approach 2, IBIS model is treated as sources and applied with different loads to calculate equivalent source voltage and impedance in frequency domain. And apply the equivalent sources in full-wave simulation to obtain 3m far field pattern. The method is shown in Figure.2.10.

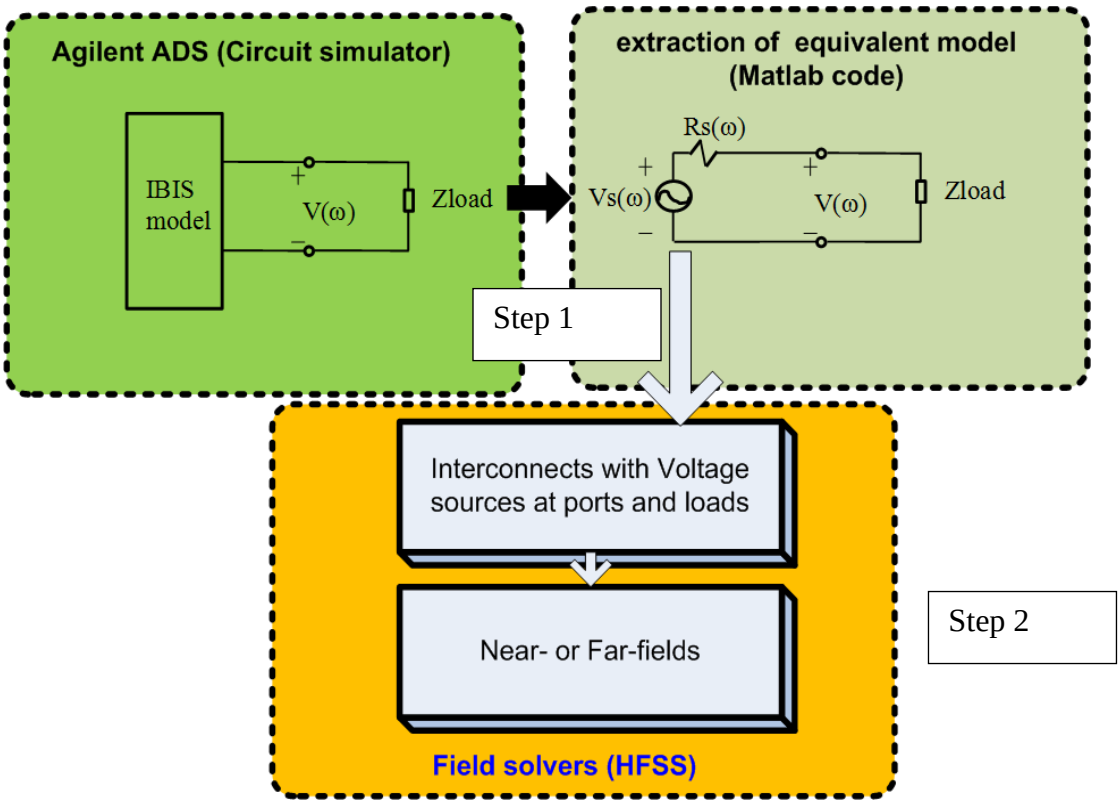


Figure 2.10. Procedure of approach 2 to obtain far field pattern

For the first step, IBIS model is imported in ADS and it is applied with different loads. Then by Thevenin's theorem, equivalent voltage and impedance are calculated, as shown in Figure 2.11. Assume load voltage are V1,V2 and load impedance are Z1, Z2, respectively. Then equivalent voltage and impedance can be calculated by the following equations (2.1):

$$\begin{cases} V_1 = \dfrac{V_s}{Z_s + Z_1} Z_1 \\ V_2 = \dfrac{V_s}{Z_s + Z_2} Z_2 \end{cases} \Rightarrow \begin{cases} V_s = \dfrac{V_1 V_2 (Z_2 - Z_1)}{V_1 Z_2 - V_2 Z_1} \\ Z_s = \dfrac{(V_2 - V_1)}{\dfrac{V_1}{Z_1} - \dfrac{V_2}{Z_2}} \end{cases} \tag{2.1}$$

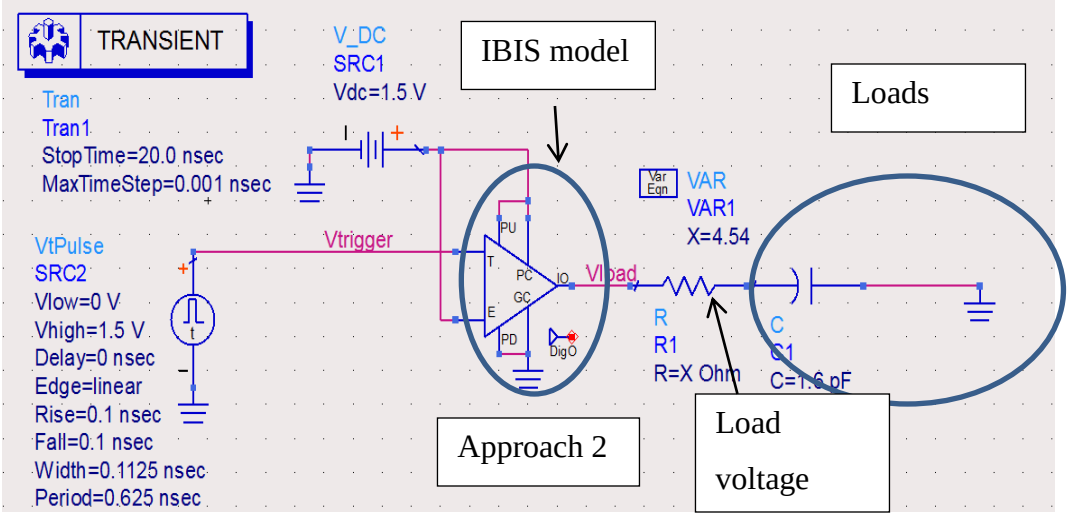
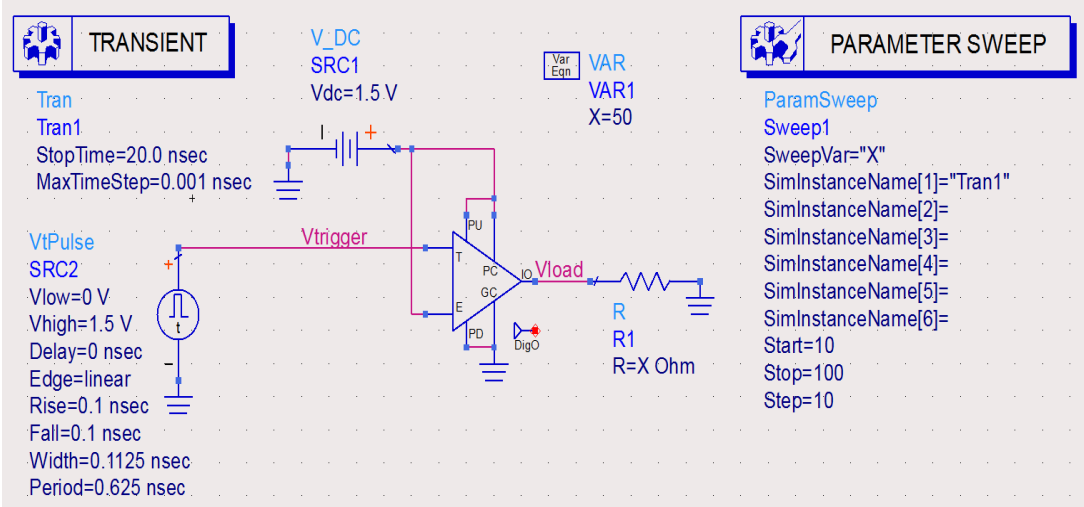
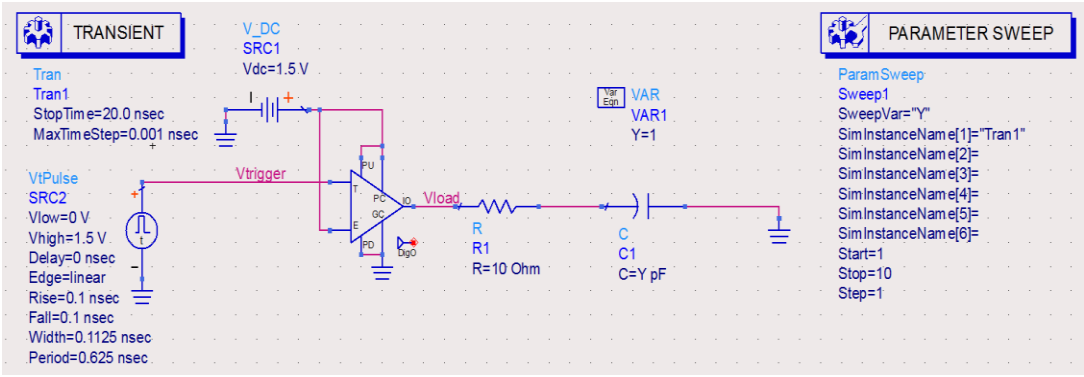


Figure 2.11. Approach 2 schematic with complex load(Zin)

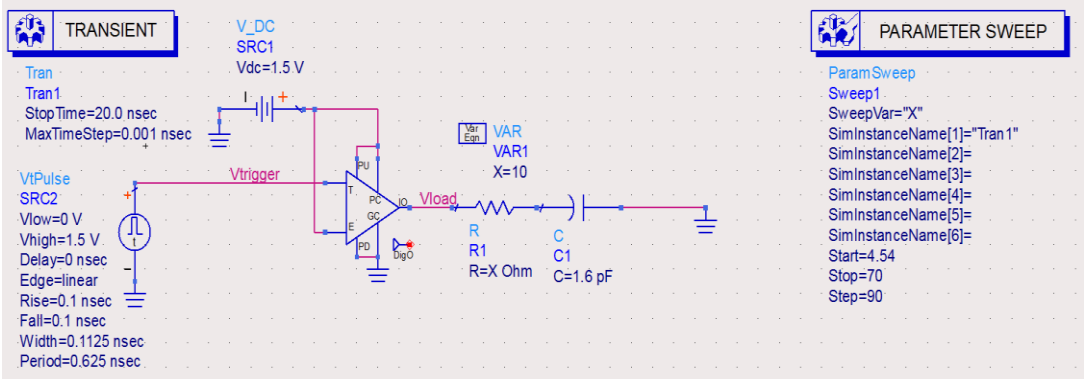
And three different kinds of loads are used to calculate equivalent source, pure resistance load, complex load and load from input impedance of HFSS model, as shown in Figure. 2.12. The calculated equivalent voltage and impedance is shown in table 2.1. The equivalent sources calculated are different between these three kinds of loads. This is because this IBIS model contains non-linear components and it takes time for capacitance to charge on. So the non-linear will contribute mismatch between these three methods. And there is one point should be mentioned that simulation time should be long enough for the result to converge, as shown in Figure. 2.13.



(a)



(b)



(c)

Figure 2.12. Three different loads to calculate equivalent source (a) pure resistance load (b) complex load (c) input impedance from HFSS model

Table 2.1. Equivalent sources calculated from 3 different loads

Zin	Rs_real	Rs_imag	Vs_mag	Vs_phase
R=4.75Ω,70Ω,C=1.6pF	38.744	-24.951	0.792	115.202
Resistance	**Rs_real**	**Rs_imag**	**Vs_mag**	**Vs_phase**
10,100Ω	38.175	-44.575	0.760	107.988
20,90Ω	38.338	-48.973	0.766	106.638
30,80Ω	38.468	-47.134	0.765	107.167
40,70Ω	38.255	-45.347	0.762	107.735
50,60Ω	38.175	-44.574	0.760	107.988
Complex	**Rs_real**	**Rs_imag**	**Vs_mag**	**Vs_phase**
R=10Ω,C=1pF,10pF	31.127	-32.192	0.802	109.959
R=10Ω,C=2pF,9pF	32.554	-34.168	0.836	109.601
R=10Ω,C=3pF,8pF	33.364	-35.009	0.853	109.602
R=10Ω,C=4pF,7pF	33.631	-35.245	0.858	109.622
R=10Ω,C=1pF,6pF	33.576	-35.102	0.857	109.656

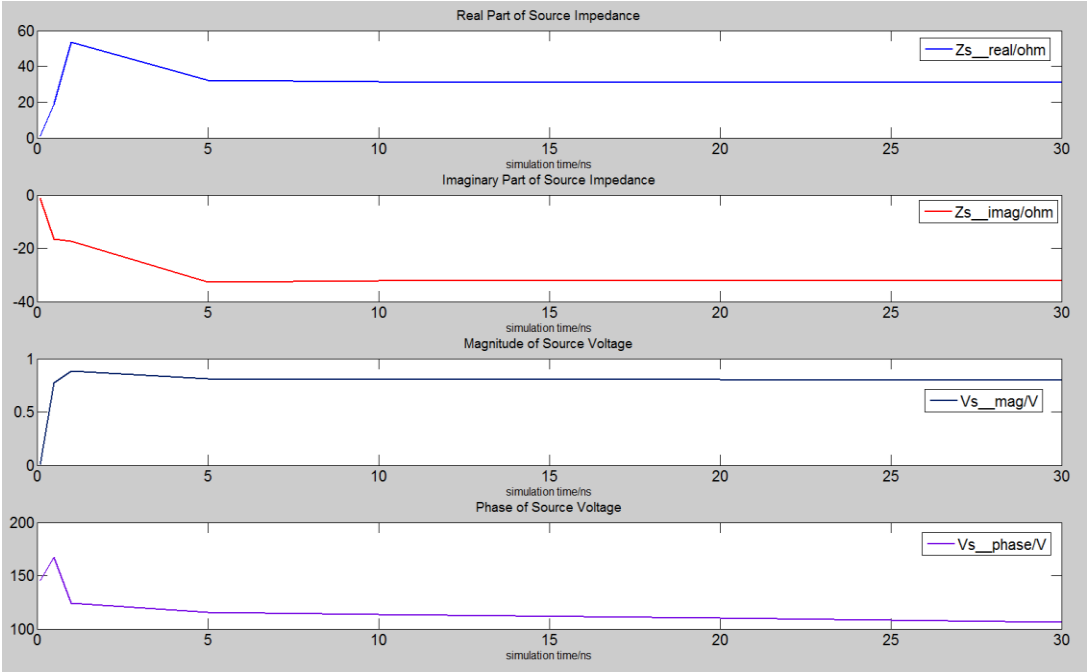


Figure 2.13. Steady state by long time simulation

In the second step of approach 2, three methods of applying equivalent source in full-wave simulation are studied: 1)transfer to lumped incident voltage, 2)add Lumped resistance by the port and then use lumped total voltage, 3)add Lumped resistance by the port and use total voltage excitation. The 3m far field patterns are generated, and then compared with the pattern in approach 1.

1) lumped port incident voltage application, equivalent voltage should be changed by the following equations:

$$V_{port\_total} = \frac{Z_{in}}{Z_s + Z_{in}} V_s \tag{2.2}$$

$$V_{port\_total} = V_{incident}(1+\Gamma) = V_{incident}\left(1+\frac{Z_{in}-Z_s}{Z_{in}+Z_s}\right) \tag{2.3}$$

The port total voltage in circuit world should be equal to that in wave world:

$$V_{incident}\left(1+\frac{Z_{in}-Z_s}{Z_{in}+Z_s}\right)=\frac{Z_{in}}{Z_{in}+Z_s}V_s \Rightarrow V_{incident}=\frac{1}{2}V_s \tag{2.4}$$

So the incident voltage applied in the HFSS should be half of the source voltage and full port impedance in HFSS is the source impedance.

The equivalent source is calculated from Zin. And the values are in table 1. The details port settings are shown in Figure.2.14. Voltage at the port is calculated by calculator in HFSS, in Figure.2.15. The port voltage is compared with the voltage in approach 1 and approach 2 in ADS circuit simulation, shown in table 2.2. The result shows that the transition from circuit world to wave world is correct. The field pattern is generated in 3m sphere and it is compared with the pattern from approach 1, shown in Figure.2.16. The differences of maximum E-field value and load voltage between these two approaches are listed in table 2.3.

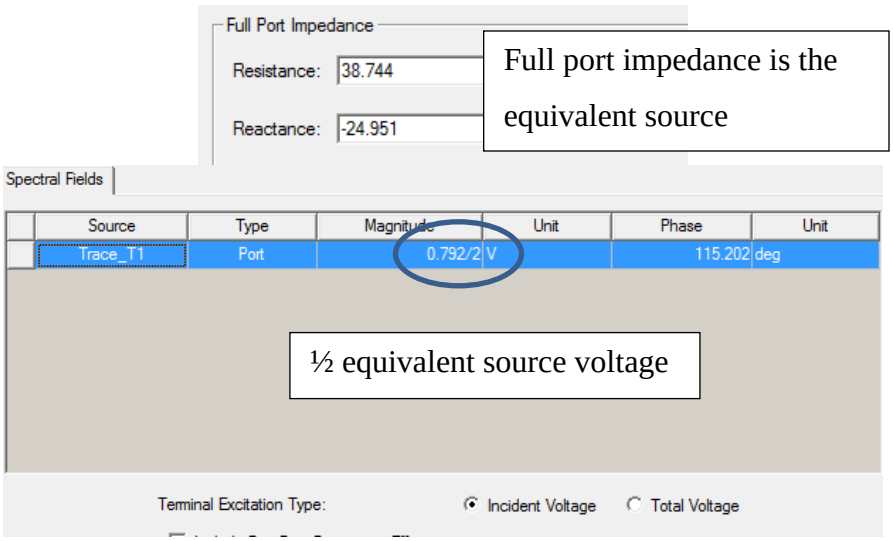


Figure 2.14. Port settings in HFSS for lumped port incident voltage

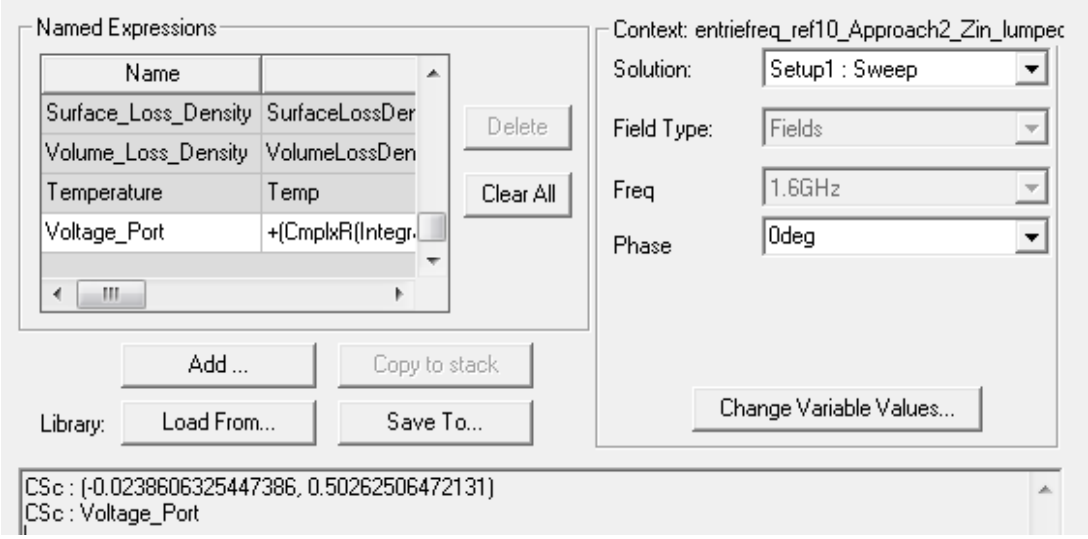


Figure 2.15. Port voltage in calculator

Table 2.2. Comparison of load voltage between approach 1 approach 2

	Load voltage(mag/phase)
Approach 1	0.443/95.134
Approach 2	0.503/92.729

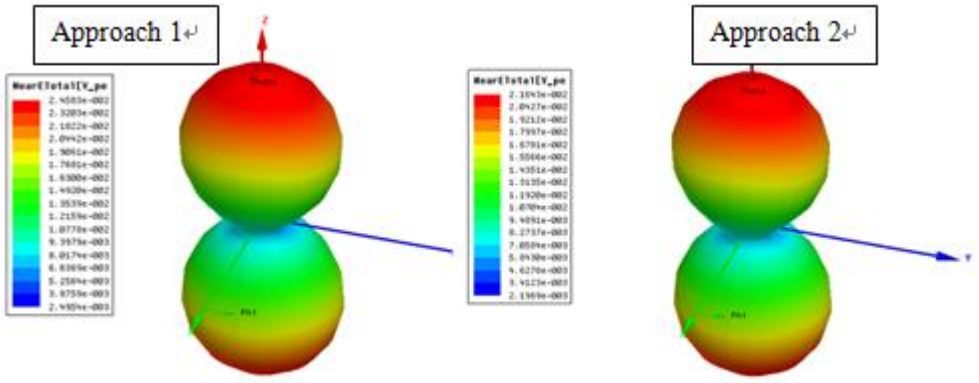


Figure 2.16. Far field pattern comparison between approach 1 and approach 2

Table 2.3. Load voltage difference and max E-field difference

	Approach 1	**Approach 2**	**Relative difference**
Load voltage(mag/phase) in ADS	0.443/95.134	0.503/92.729	13.4%
Max E field in HFSS	2.1643e-2	2.4583e-2	13.58%

2) lumped port total voltage is another method to apply equivalent source to HFSS full-wave simulation, shown in Figure.2.17. A lumped RLC element should be added by the port with impedance as equivalent source impedance. Voltage is applied as total voltage in lumped port. At the top/bottom side, PEC sheet is used to connect

top/bottom lumped port with lumped RLC sheet/bottom plane. In this method, the E-field values don't match with approach 1, as shown in Figure 2.18. It is not accurate as lumped incident voltage.

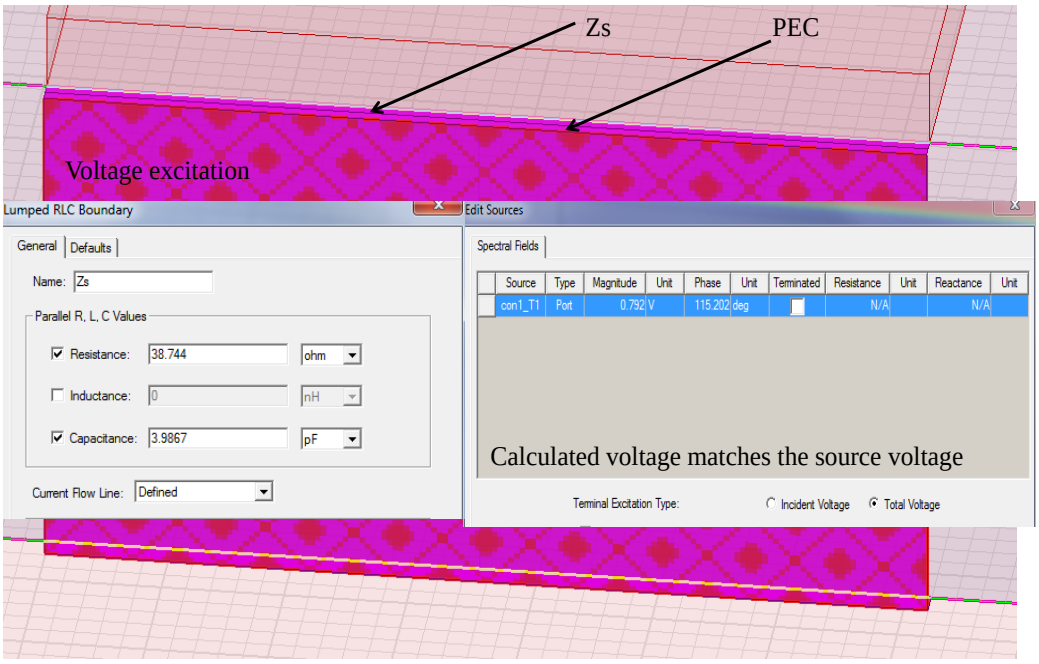


Figure 2.17. Lumped port settings for total voltage

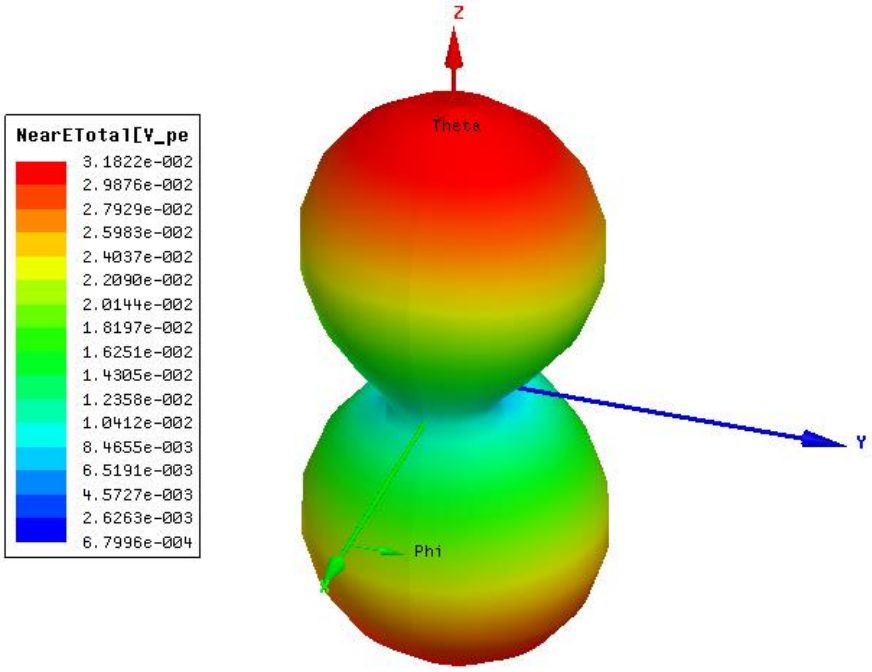


Figure 2.18. Field pattern of lumped port total voltage

3) Another method to apply equivalent source in HFSS is voltage excitation. A Lumped RLC sheet with impedance of equivalent source impedance is also used, shown in Figure 2.19. However, the field pattern also mismatches with approach 1, Figure 2.20.

In conclusion, it is better to use the first method which is lumped incident voltage to apply equivalent sources into HFSS model. The advantage of applying Thevenin's equivalent source by incident voltage is that the source is independent of loads when it is extracted and when it is used as incident voltage, it is independent of structures. So The Thevenin's equivalent source can be used for any structures for emission simulation.

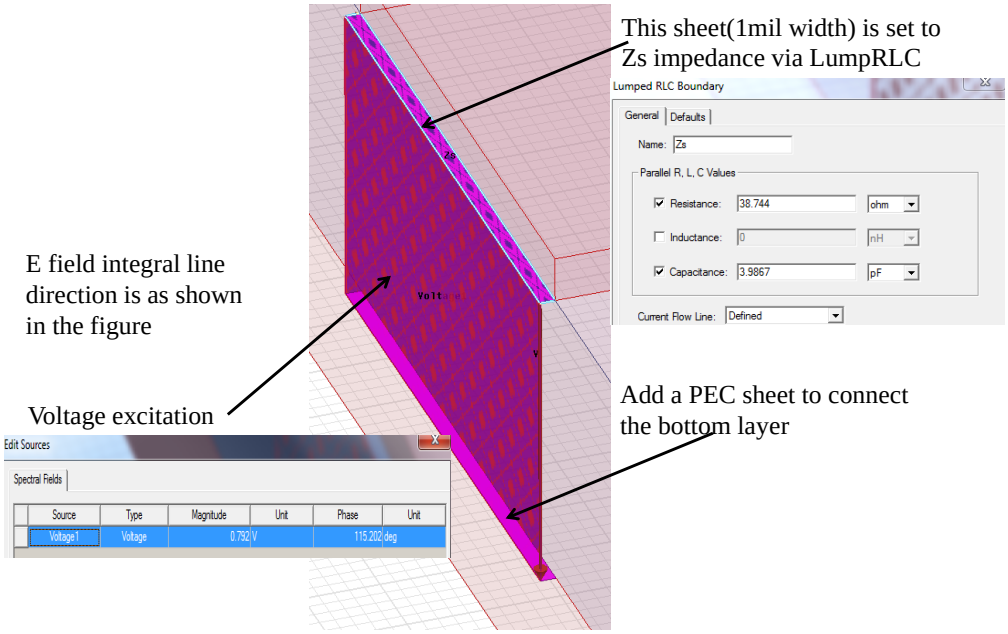


Figure 2.19. Total voltage excitation port settings

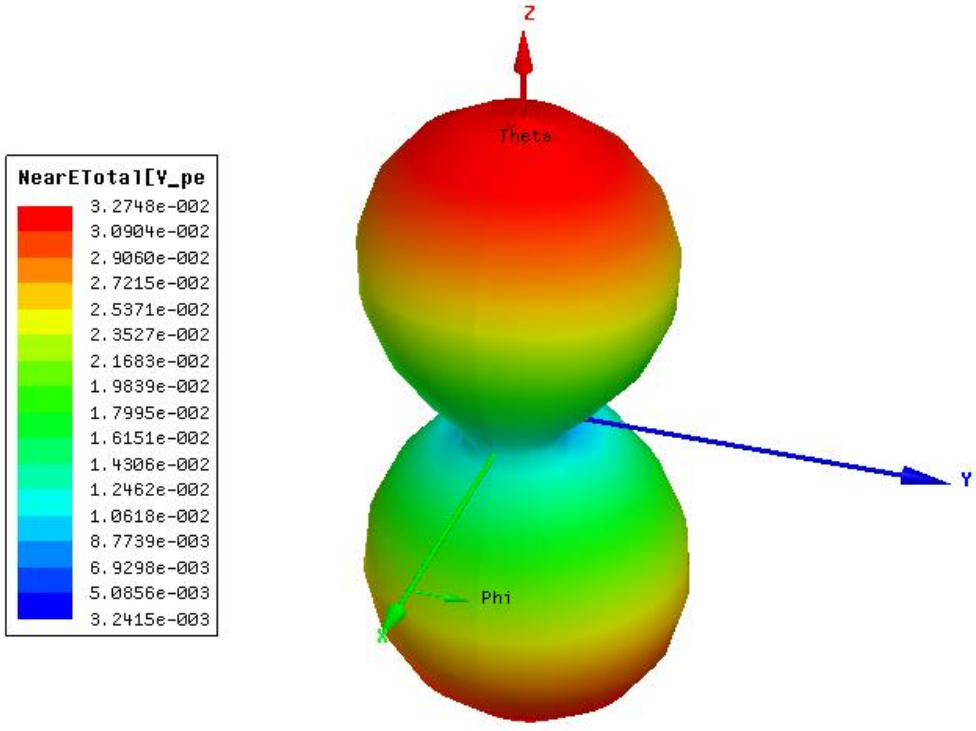


Figure 2.20. Field pattern of voltage excitation

2.3. IMPROVED SOURCE

In the previous methods, the data rate is too fast for the load to achieve steady state. So a slower data rate is set, shown in Figure 2.21. The maximum data rate for model DQ 34 1333 is 1333Mbps, so the period in the trigger is set to 1.5ns, with rise/fall time 0.25ns, pulse width 0.75ns. It is 50% duty circle. The time step is 0.01ns so there are at least 25 points in the rise/fall time. 150 ns simulation time means 100 periods for the whole simulation. Different sets of load are used to calculate equivalent source.

For pure resistance, load voltage of one set of resistance load is shown in Figure 2.22. The voltage reach steady which means reactance component in IBIS model is fully charged/discharged. With the similar calculation discussed before, equivalent voltage and impedance is calculated, shown in table 2.4.

Table 2.4. Equivalent Source

Resistance	Rs_real /Ω	Rs_imag/Ω	Vs_mag/V	Vs_phase/deg
20Ω,200Ω	45.349	-16.111	0.979	175.106
40Ω,180Ω	37.857	-13.435	0.952	175.626
60Ω,160Ω	34.666	-12.663	0.941	175.771
80Ω,140Ω	33.053	-12.393	0.935	175.826
100Ω,120Ω	32.206	-12.368	0.929	175.850

The result shows that equivalent voltage in different load is almost the same but equivalent impedance changes.

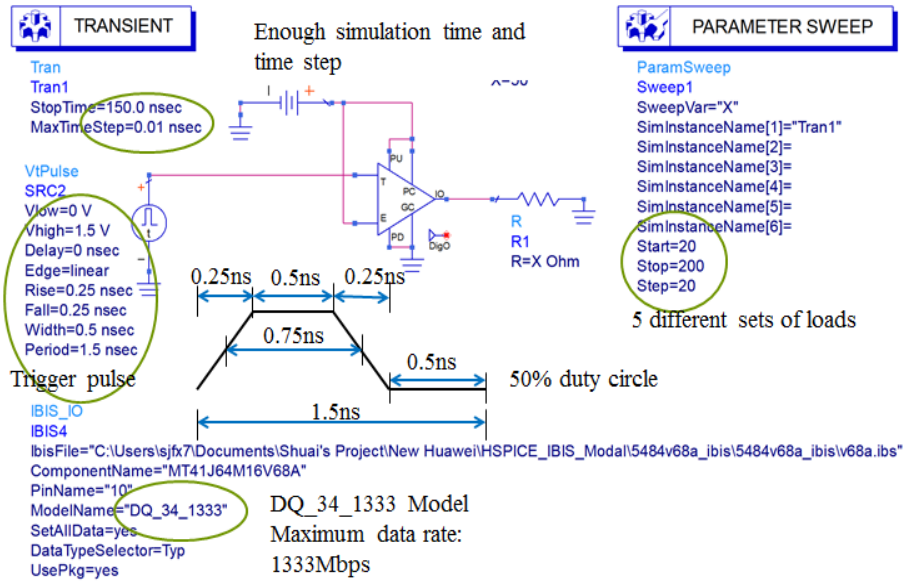


Figure 2.21. New source for approach 2

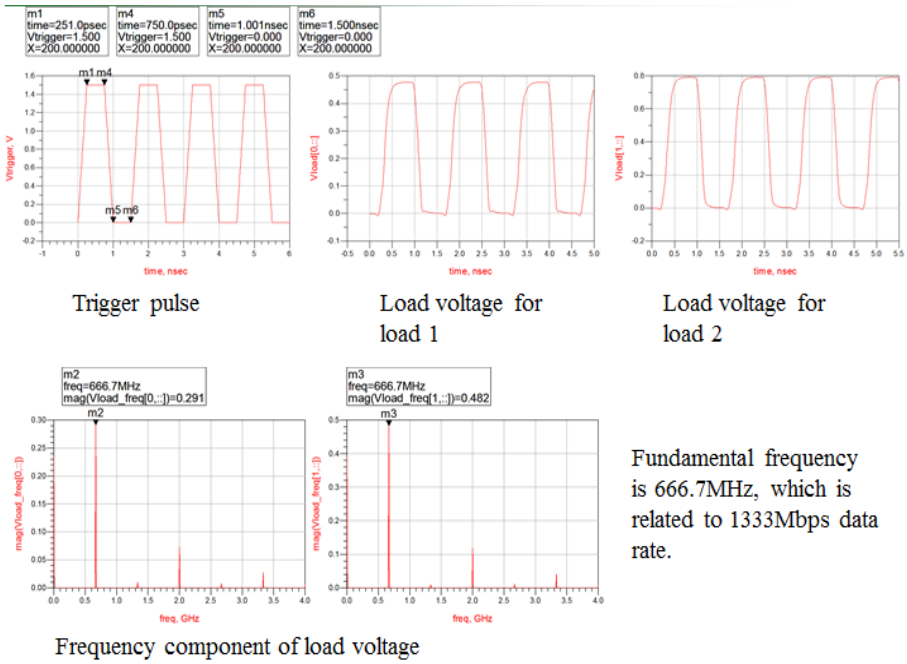


Figure 2.22. Trigger voltage and load voltage

Complex loads are also used to calculate equivalent source, shown in Figure 2.23. The trigger pulse is the same with pure resistance. Equivalent source are shown in table 2.5. The equivalent voltage from complex load is almost the same with that from pure resistance load. However, the impedance especially imaginary part of impedance is quite different.

In conclusion, it is better to used resistance as load, because it has no charging and discharging issues. And also the simulation time should be large enough for the time domain signal reach steady state so that the frequency information can be accurate.

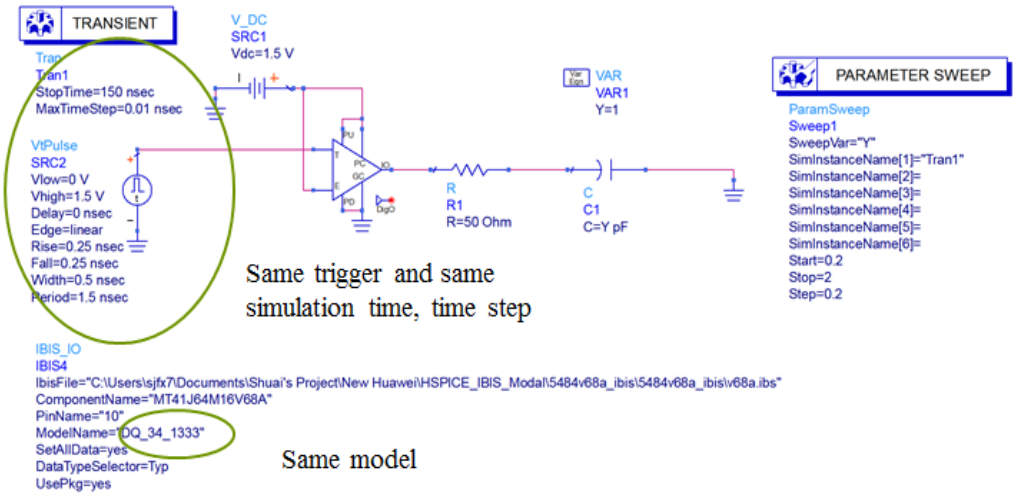


Figure 2.23. Complex load schematic

Table 2.5. Equivalent source form complex load

Complex load	Rs_real/Ω	Rs_imag/Ω	Vs_mag/V	Vs_phase/deg
50Ω; 0.2pF, 2pF	34.991	-4.311	0.902	174.949
50Ω; 0.4pF,1.8pF	34.559	-4.447	0.900	174.643
50Ω; 0.6pF,1.6pF	34.292	-4.510	0.899	174.439
50Ω; 0.8pF,1.4pF	34.134	-4.541	0.899	174.310
50Ω; 1pF,1.2pF	34.065	-4.551	0.898	174.249

3. SOURCE EXTRACTION FROM MEASUREMENT OF TESTBOARD

3.1. CIRCUIT DIAGRAM

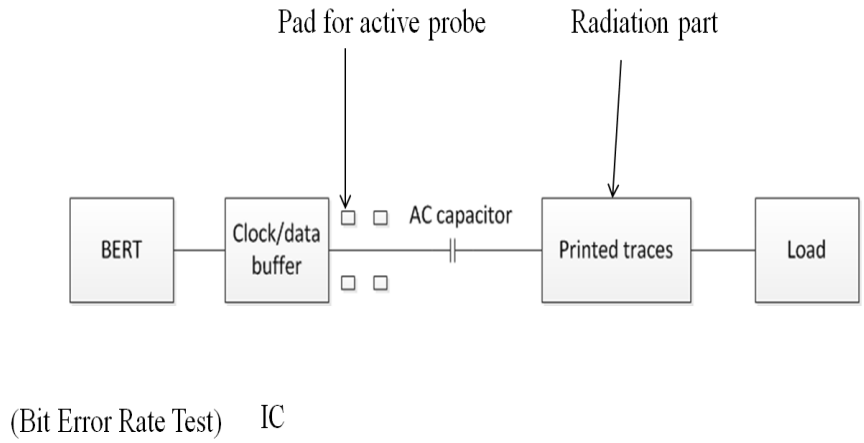


Figure 3.1. Circuit diagram for extracting source from measurement

A testboard is desired to extract source by measurement and also validate the simulation results by far field measurement. A diagram is drawn in Figure 3.1. In this testtard BERT (Bit Error Rate Test) is used as trigger. A clock/data buffer is used to provide source for the trace to radiate. It is better to choose a clock/data buffer with one input and one output. And the clock/data buffer should have IBIS model for simulation. At the output of the clock/data buffer there are test pads to extract total voltage from measurement. Then the total voltage can be used in full wave simulation for far field information. And the far field simulation results can be compared with far field from IBIS source. Because conducted emission is to be measured, so for the test board, the only radiation source should be the trace. In terms of this point, all the IC and other component should be placed on different layers with the trace, which means the trace

should be placed on top layer. The IC and other component are placed on bottom layer. Besides this testboard, a calibration board with only trace on it is desired for extracting s-parameters, and this s-parameters is used in approach one to extract total voltage from IBIS model.

3.2. TEST BOARD DESIGN

In order to study conducted emission, the most important point is the source from IC. To simplify the simulation and measurement, a clock buffer is chosen. It has one input one output. At the same time it has IBIS model so that the IC can be used in simulation to extract source. ADCLK905 offers 95 ps propagation delay and it can achieve as fast as 10 Gbps data rate. The random Jitter is as low as 60 fs. For AC-Coupled input the application circuit is as shown in Figure 3.2. For layout convenience, the input pin is selected as /D so that the V_{ref} will not cross the input trace. But the phase will be opposite. In this test board it is ok for 180 degree phase difference.

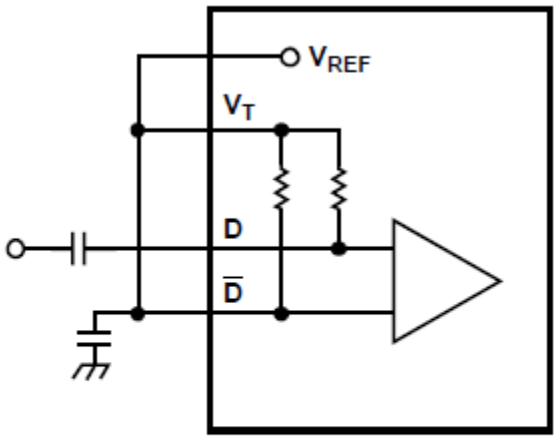


Figure 3.2. AC-Coupled Application Circuit

For the test board, BERT (Bit Error Rate Test) is used as trigger for the clock buffer. It is Microwave Logic Transmitter and the max data rate from the output of the BERT is 1.4 Gbps. In order to provide stable power supply, instead of using DC voltage source directly, a linear voltage regulator is selected for the test board. The output can be set to 3.3 V, as shown in Figure 3.3.

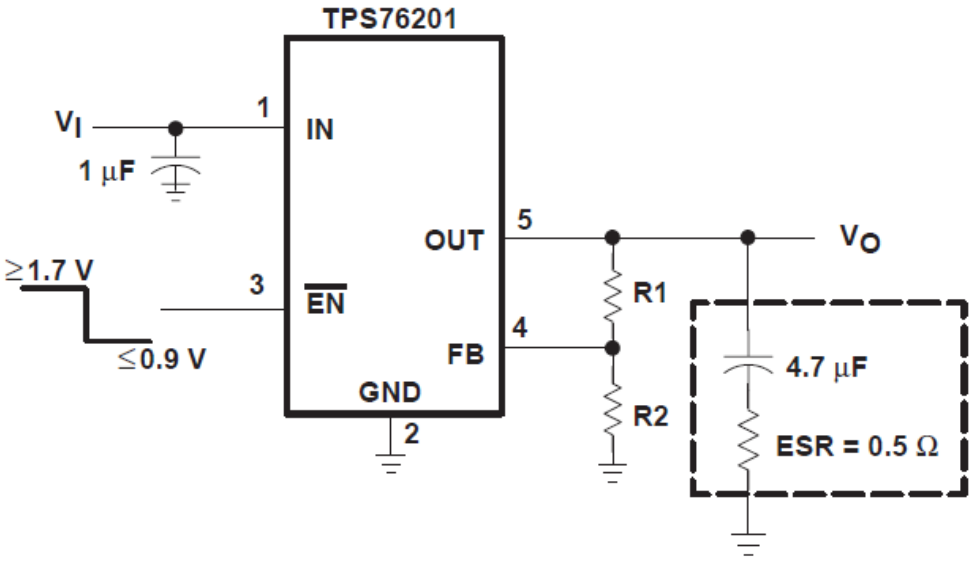


Figure 3.3. Voltage regulator application circuits

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \tag{3.1}$$

Where V_{ref} is 0.6663 V. In order to provide 3.3 V voltage, the ratio of R_1 and R_2 should be 4.

On the test board bulk decoupling capacitors are placed by the voltage regulator so that the power supply from voltage regulator is stable without high frequency. Around the IC VCC power pin, smooth decoupling capacitors are also placed along the power trace in to the IC. With these decoupling capacitors the clock buffer will work properly. The board is shown as Figure. 3.4.

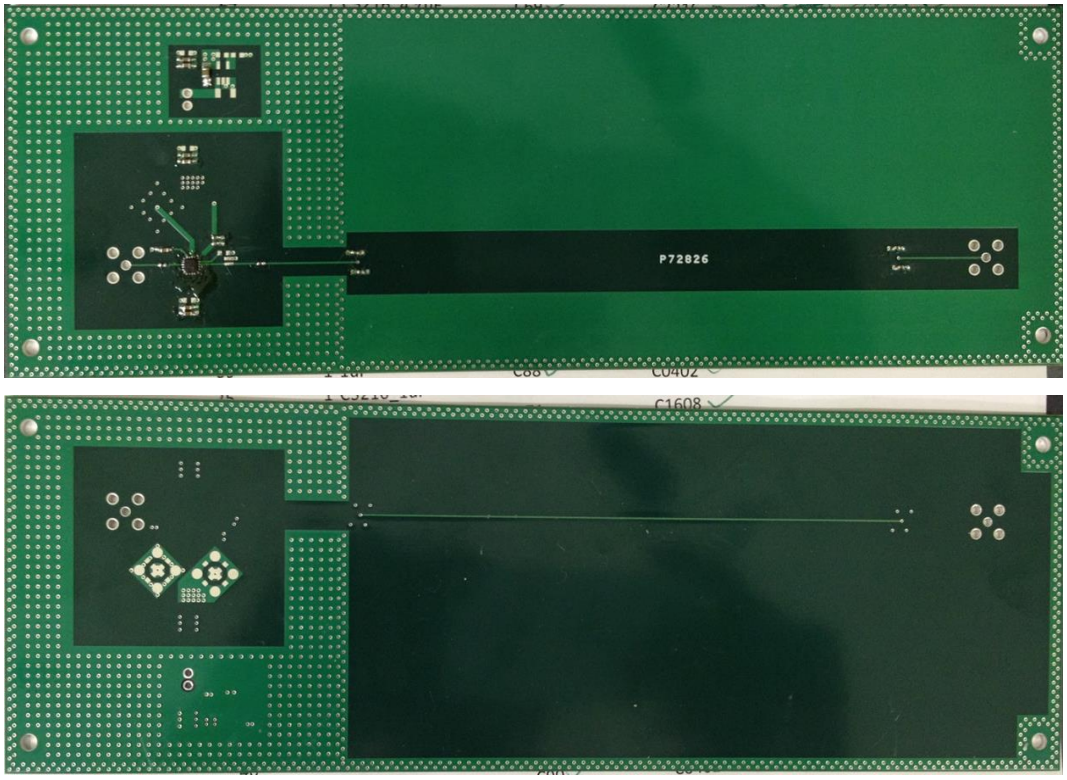


Figure 3.4. Top view and back view of the test board

3.3. TOTAL VOLTAGE EXTRACTION

The BERT (Bit Error Rate Test) is set to 100 MHz with 1V amplitude for the input trigger of the clock/data buffer, as shown in Figure. 3.5.

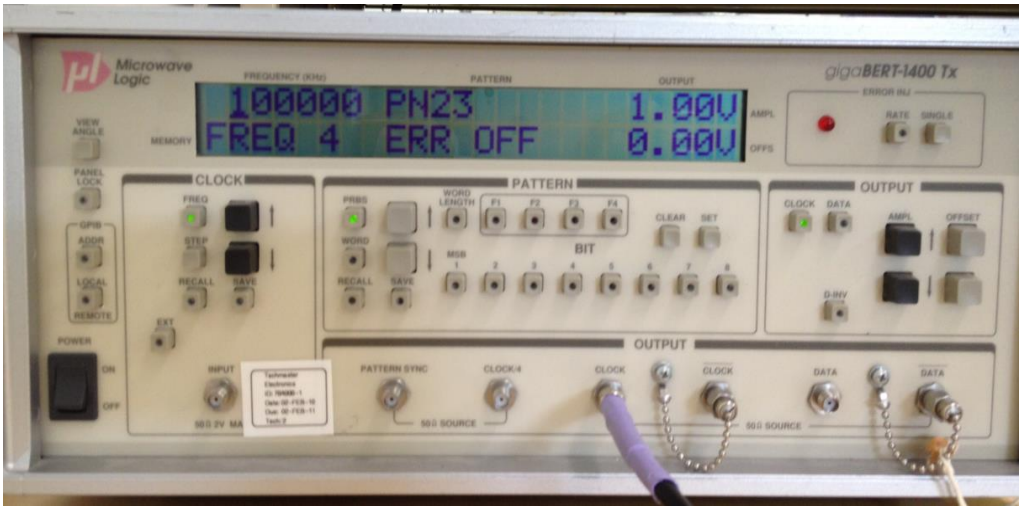


Figure 3.5. BERT settings

With oscilloscope the output from BERT is measured. And the waveform from BERT is shown in Figure. 3.6. The oscilloscope is with bandwidth of 6GHz and 20GSa/s.

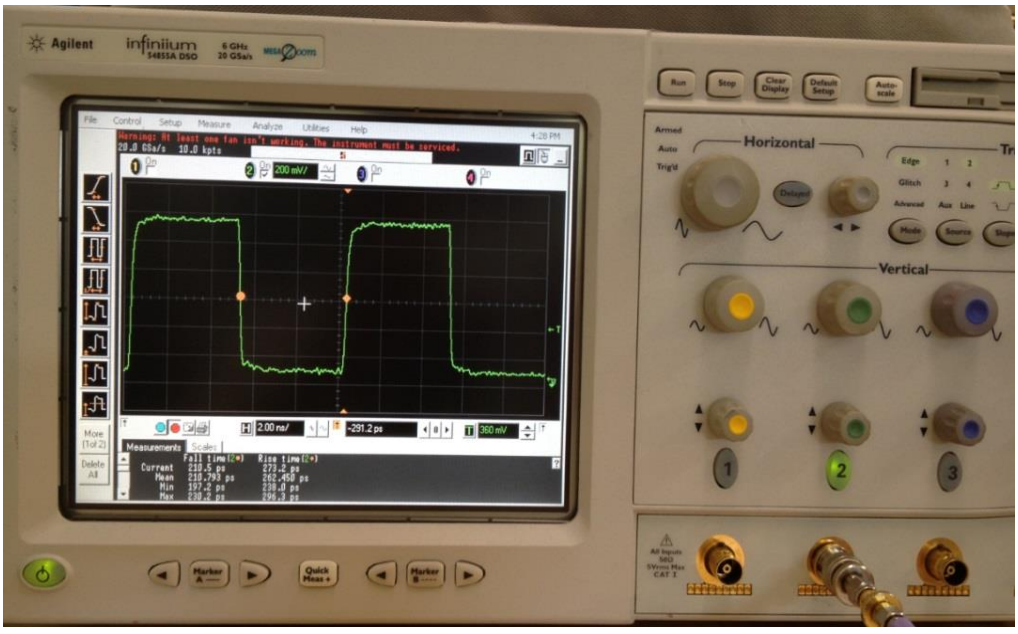


Figure 3.6. BERT output waveform

In total voltage measurement, active probe is used to measure total voltage. And before starting the measurement, the active probe should be validate it is working correctly. In order to test active probe, a microstripe line is used. One port of the trace is connected to the BERT source and the load is connected to oscilloscope to measure the signal on the trace. Active probe is soldered on the trace between signal and ground so that if the active probe works well, the signal measured from active probe should be the same with waveform shown in oscilloscope, with some phase shift. The microstripe line structure and TDR measurement is shown in Figure. 3.7. The TDR shows that the trace is a 50 ohm trace.

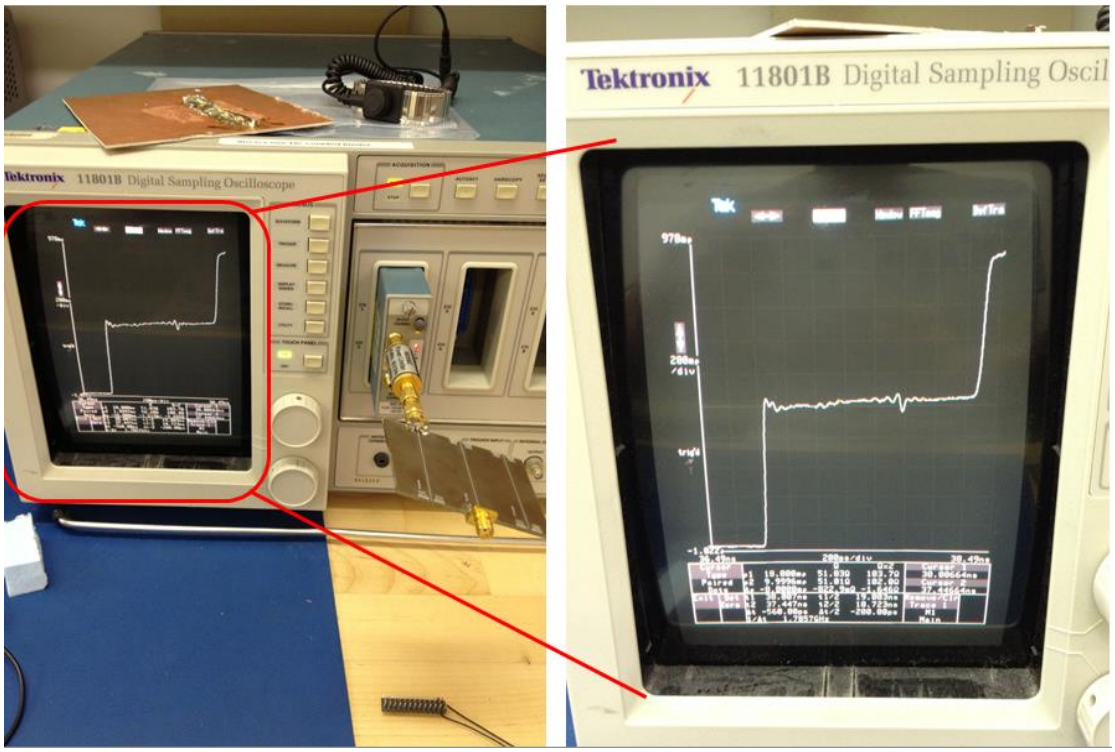


Figure 3.7. TDR measurement for the trace

Active probe is soldered on the trace as shown in Figure. 3.8. The result is shown in Figure. 3.9. The results show that the signal on the trace and measured signal form active probe are the same. So the active probe works well to measure signal on the trace and it will be used to measure the voltage on the output of the clock/data buffer.

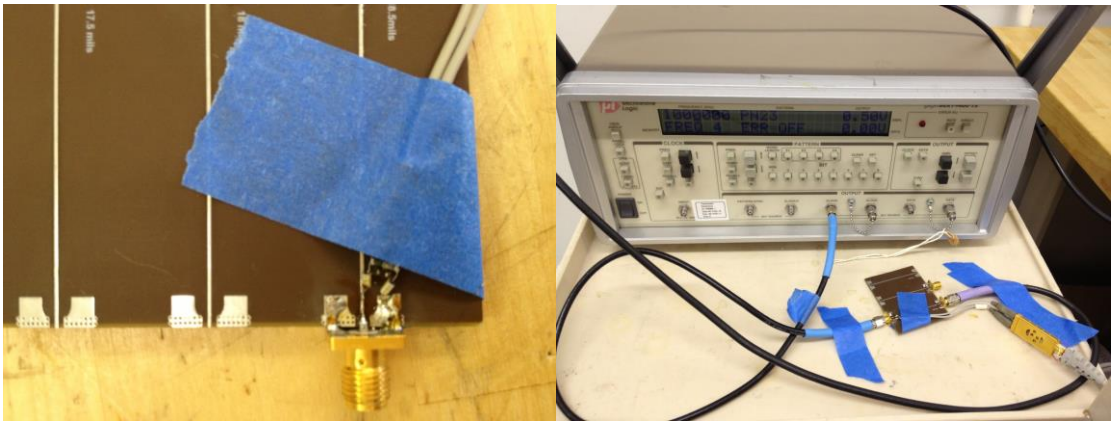


Figure 3.8. Active probe soldered on the trace

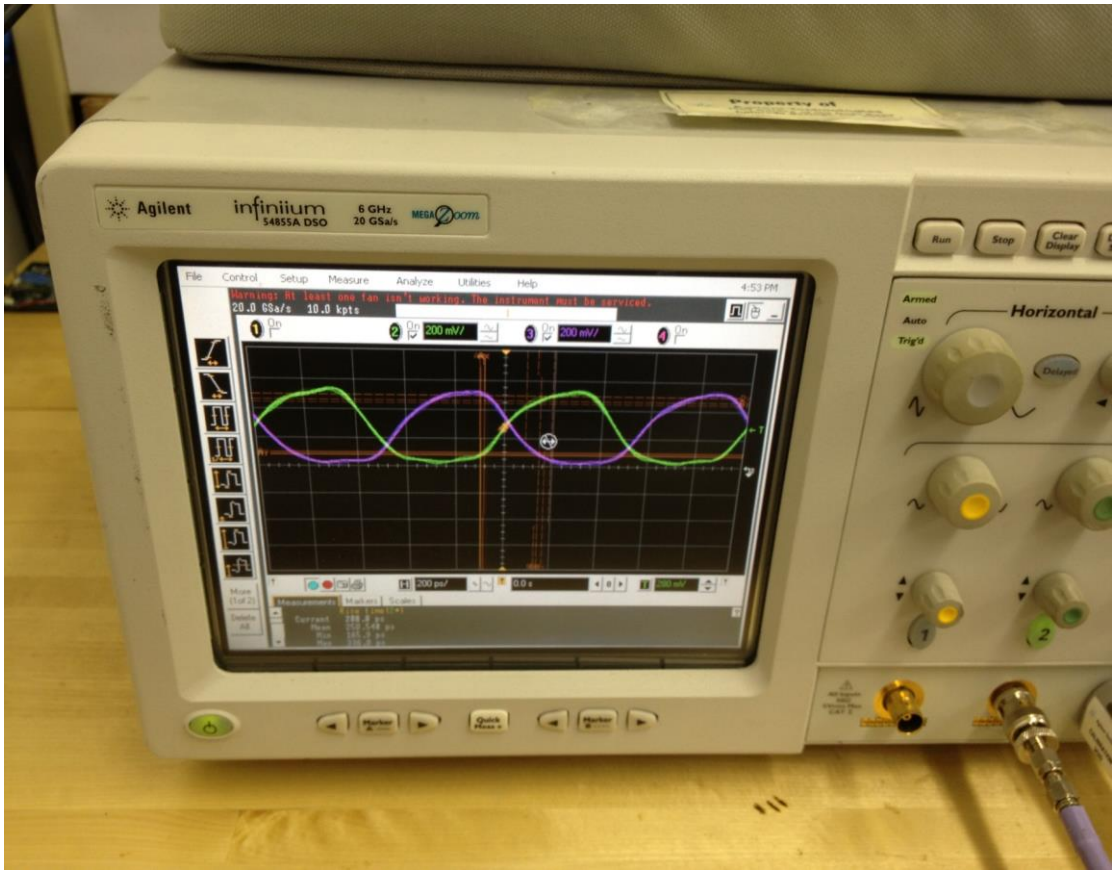


Figure 3.9. Measurement from active probe

On the test board, active probe is soldered on the test pad and measure the waveform from data/clock buffer, as shown in Figure. 3.10. The total voltage will be transfer to frequency domain to get harmonic values. And this total voltage will be used for simulation in full-wave software, HFSS to get far field result. This far field simulation result can be used to compare with far field result from IBIS source simulation. If the results match, then it means both methods can be used to extract sources and used for far field simulation.

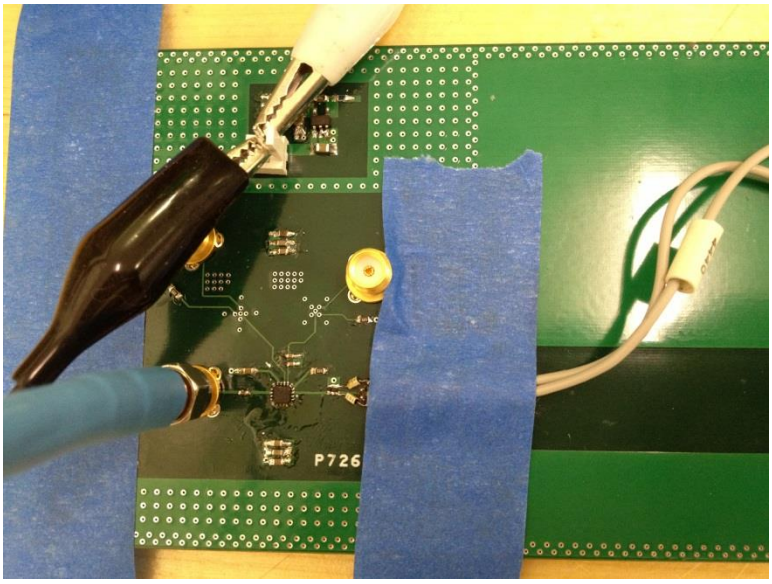


Figure 3.10. Measuring total voltage from IC

Total voltage is measured from output of the IC, the waveform is shown in Figure 3.11. The total voltage is transferred to frequency domain so that it can be applied in frequency domain full wave simulator, HFSS. The harmonic values are listed in Table 3.1.

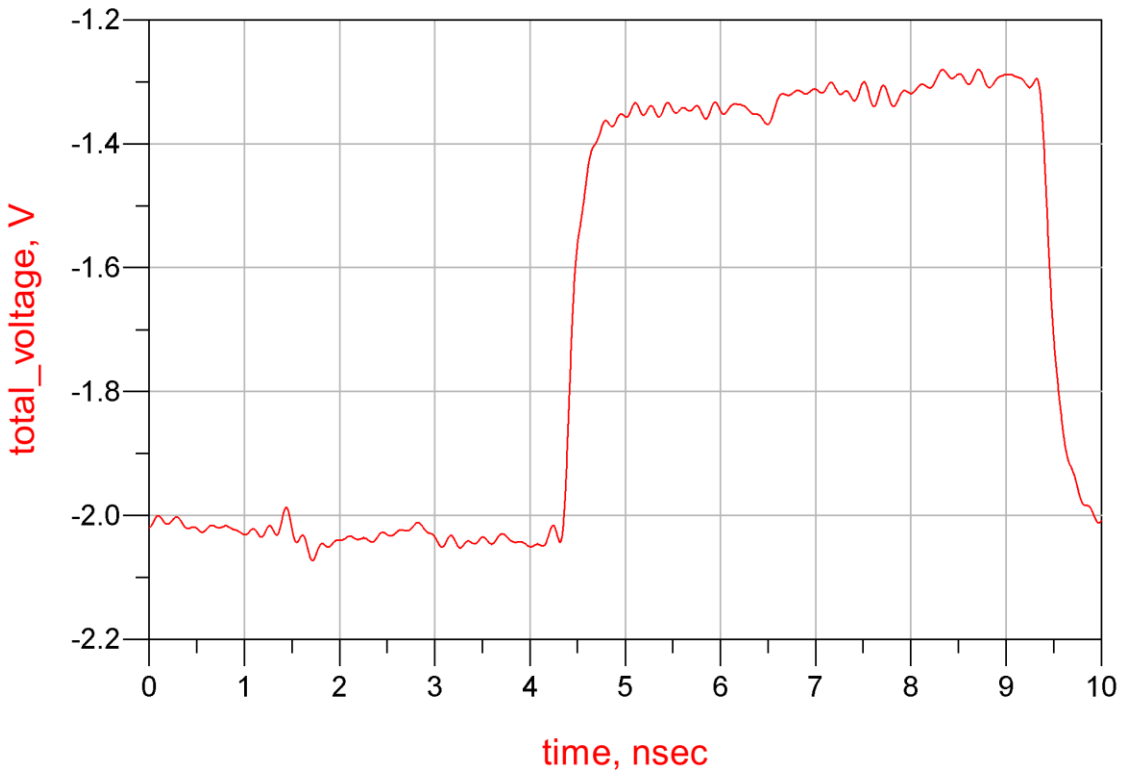


Figure 3.11. Measured IC output

Table 3.1. Total voltage harmonic values.

100 MHz	300 MHz	500 MHz	700 MHz	900 MHz
0.449 V	0.144 V	0.087 V	0.049 V	0.042 V

In conclusion, IC model can be extracted from measurement. And this measurement based IC model can be compare with IC model extracted from IBIS model. If they match, it means the IC model from IBIS is correct. And it is discussed in section five. This total voltage is also applied in HFSS to do far field simulation. The results are compared with measurement. This part is discussed in section six.

4. SOURCE EXTRACTION FROM IBIS MODEL

Based on studies on section 2, two approaches can be used to extract IC models. And after that the IC models are applied in HFSS to simulate for the emission. In this section, IC source model is extracted from the IBIS of the IC used in test board.

4.1. APPROACH ONE TOTAL VOLTAGE

In order to extract total voltage from IBIS, s-parameters of the structure is desired. The s-parameter is extracted from calibration board. And it is imported into ADS to get total voltage.

As studied in previous sections, IBIS model can be used to extract total voltage. In ADS, IBIS model is imported as output buffer and it is triggered by the same signal, from BERT, as did in test board. The output of IBIS model is connected with S-Parameters extracted from HFSS model. After extracting total voltage from ADS, total voltage will be used in full-wave simulation and to get far field results.

ADS schematic is shown in Figure. 4.1. The BERT clock waveform is used as input trigger. S-parameter is measured from calibration board. Then the total voltage is extracted from the output of the clock buffer. It is used as source into HFSS full-wave simulation. Total voltage waveform is shown in Figure. 4.2. And it is converted to frequency domain to get values at harmonic frequencies. The result is listed in Table 4.1.

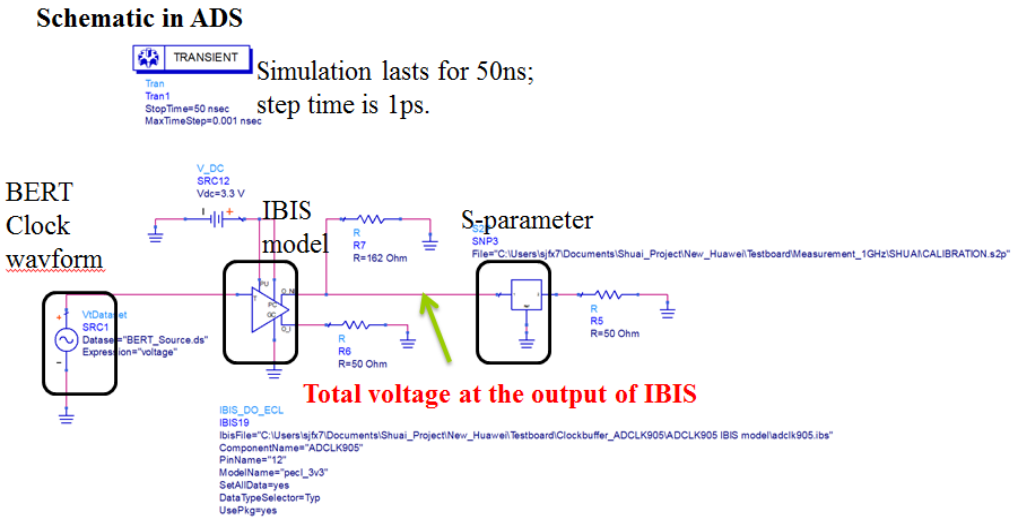


Figure 4.1. Total voltage extraction schematic

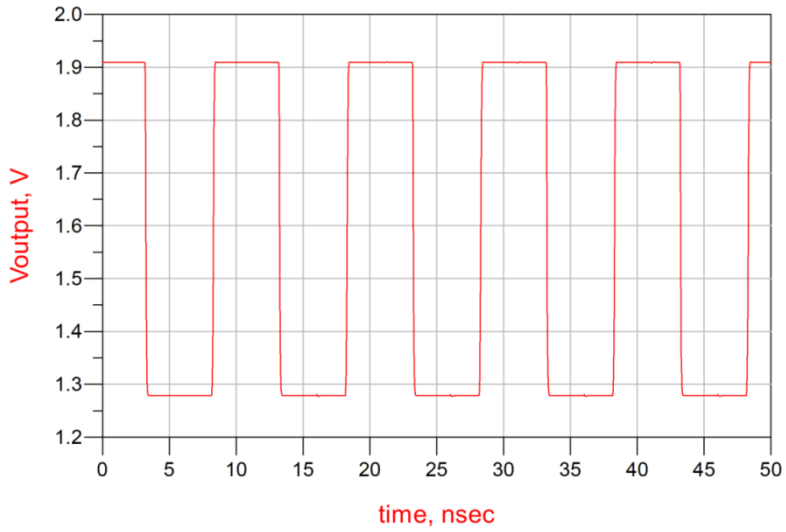


Figure 4.2. Total voltage waveform

Table 4.1. Harmonics Frequency Values

100 MHz	300 MHz	500 MHz	700 MHz	900 MHz
0.401 V	0.133 V	0.079 V	0.056 V	0.043 V

4.2. APPROACH 2 THEVENIN EQUIVALENT SOURCE

IBIS model can be represented as a voltage source plus source impedance. This equivalent source is extracted in ADS simulation by applying different loads to the IBIS model and the Thevenin equivalent source is obtained from equation 4.1. The block diagram is shown in Figure 4.5.

$$\begin{cases} V_1 = \dfrac{V_s}{Z_s + Z_1} Z_1 \\ V_2 = \dfrac{V_s}{Z_s + Z_2} Z_2 \end{cases} \Rightarrow \begin{cases} V_s = \dfrac{V_1 V_2 (Z_2 - Z_1)}{V_1 Z_2 - V_2 Z_1} \\ Z_s = \dfrac{(V_2 - V_1)}{\dfrac{V_1}{Z_1} - \dfrac{V_2}{Z_2}} \end{cases} \tag{4.1}$$

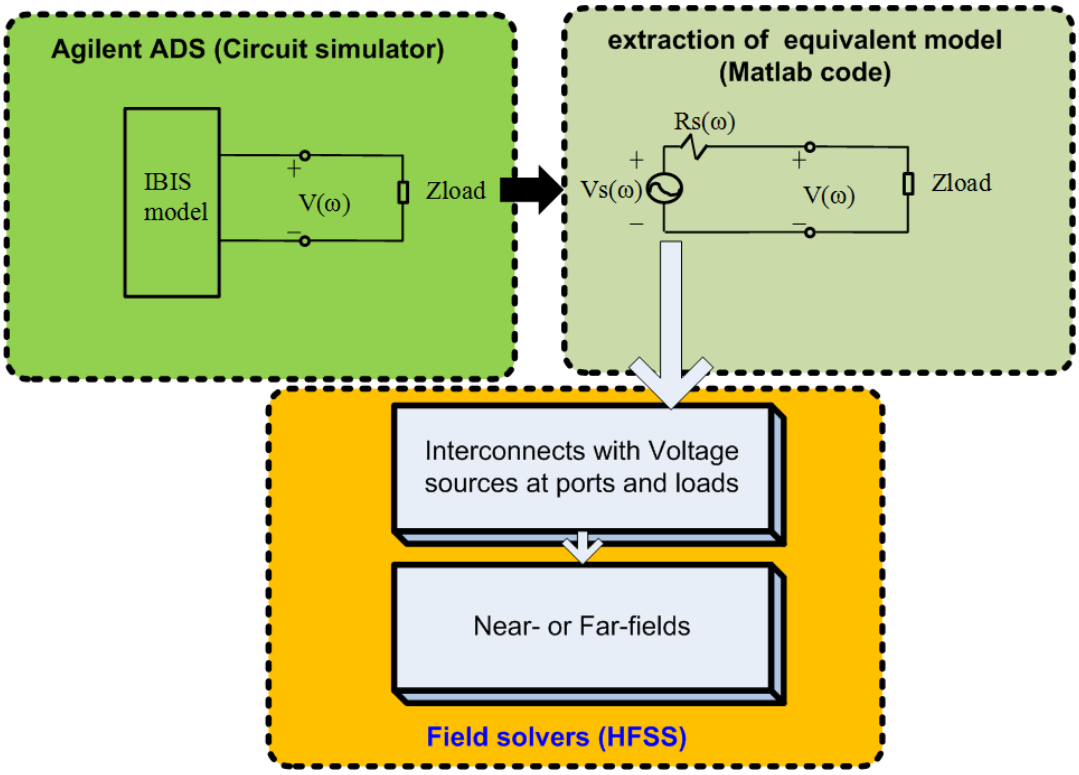


Figure 4.3. Block diagram for approach two

In ADS the trigger for IBIS model is the signal from BERT. The power supply voltage is 3.3 V. At the load, different values of resistors are added to get different load voltage and then by using equation 4.1 source voltage and source impedance is obtained by Thevenin's theorem. ADS schematic is shown in Figure 4.6. The different load waveform is shown in Figure. 4.7. Calculated equivalent source is listed in Table 4.2 for harmonic frequencies.

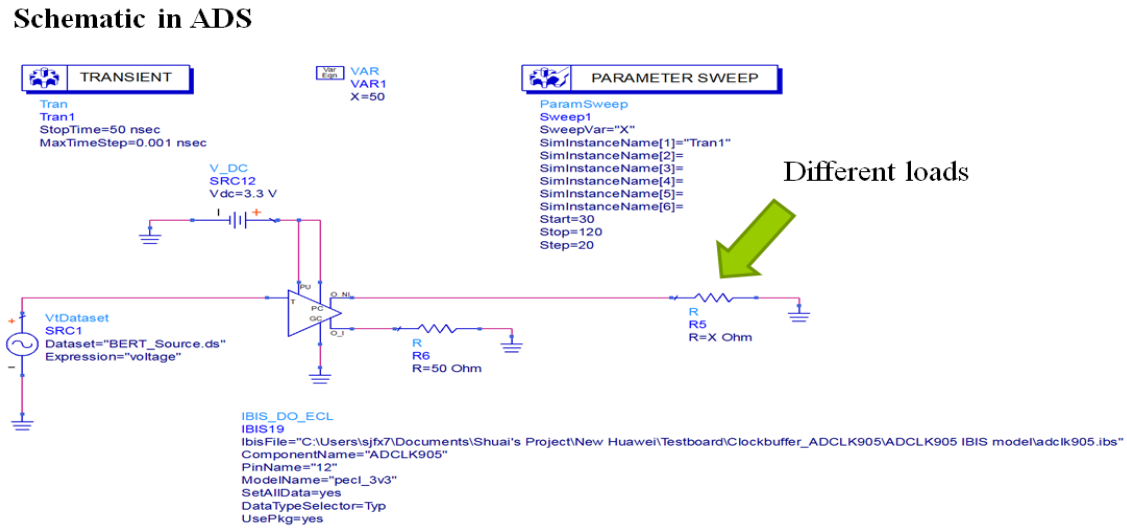


Figure 4.4. Schematic to obtain equivalent source.

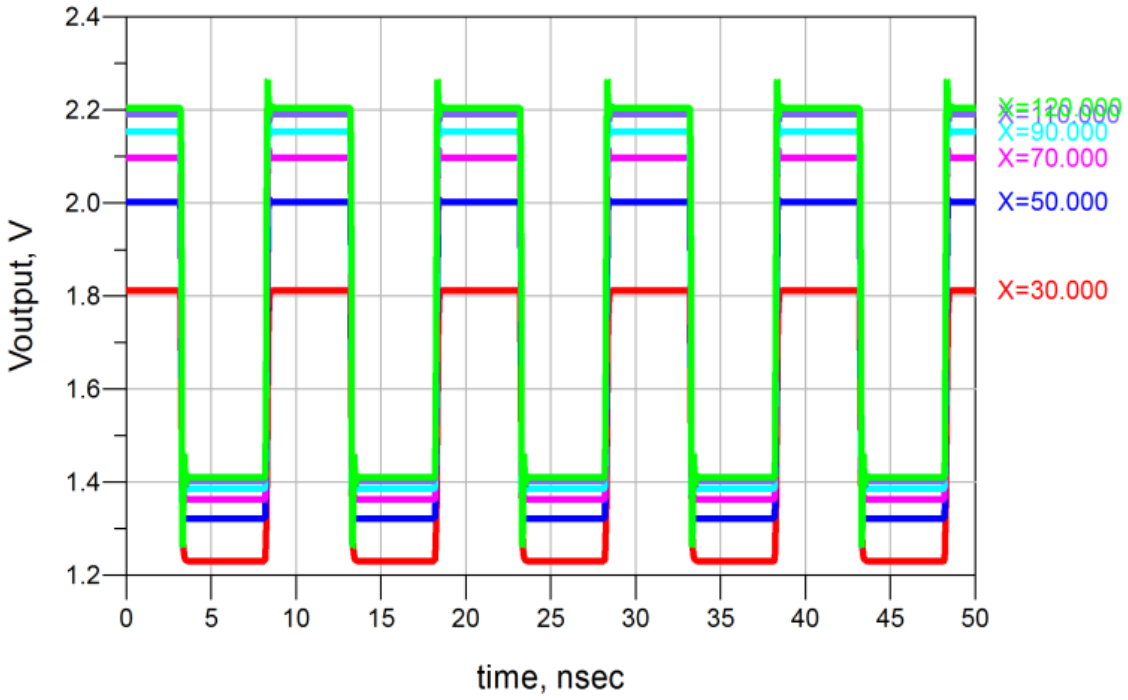


Figure 4.5. Load voltage waveform

Table 4.2. Thevenin equivalent source

Frequency	Real (Zs)/ohm	Imag (Zs)/ohm	Mag (Vs)/V	Phase (Vs)/deg
100 MHz	16.543	1.518	0.576	-26.207
300 MHz	16.652	4.57	0.192	101.382
500 MHz	16.871	7.673	0.116	-131.02
700 MHz	17.205	10.864	0.083	-3.406
900 MHz	17.66	14.181	0.065	124.299

In conclusion, in this part IBIS model is used to extract IC models in two approaches. The first one is to extract total voltage associated with structure s-parameters.

And the total voltage from IBIS matches with that from measurement. .The second approach is to apply different load to IBIS and to extract Thevenin's equivalent source. And the Thevenin's source is preferred, because the source is independent of load or structures.

5. FAR FIELD MEASUREMENT WITH TEST BOARD

In this section far field measurement is done with the test board. Calibration and data post-processing method is involved. This measured far field is to validate the IC model extracted from measurement and IBIS model.

5.1. SERTUP AND POST PPROCESSING PROCEDURE

In the far field measurement BERT is set to 100 MHz with amplitude of 1 V. Spectrum analyzer is used to capture frequency domain information. The frequency span is from 50 MHz to 1GHz. Sweep points is 1601. RBW is 10 K. Sweep time is 36.6 ms. an amplifier is used to increase the SNR because the radiation from trace is quite small. Before doing measurement calibration needs to be done first. A block diagram for calibration is shown in Figure 5.1. First of all, cable connected to the antenna is removed from antenna and connect with another cable which attached to the output of spectrum analyzer. The internal source of spectrum analyzer is set to -40 dBm. Because the amplifier has a 26 dB gain so in order to protect spectrum analyzer the internal source is set to a relative low power output. Secondly, the power at the input of spectrum analyzer is measured and after adding the source power -40 dBm the S21 of the channel is obtained. Finally, the additional cable is attached to the input and output of spectrum analyzer. The additional cable S21 is measured. After subtracting the total S21(dB) with additional cable S21(dB), the channel gain from antenna through power amplifier to spectrum analyzer is obtained. The real connection relationship is shown in Figure 5.2.

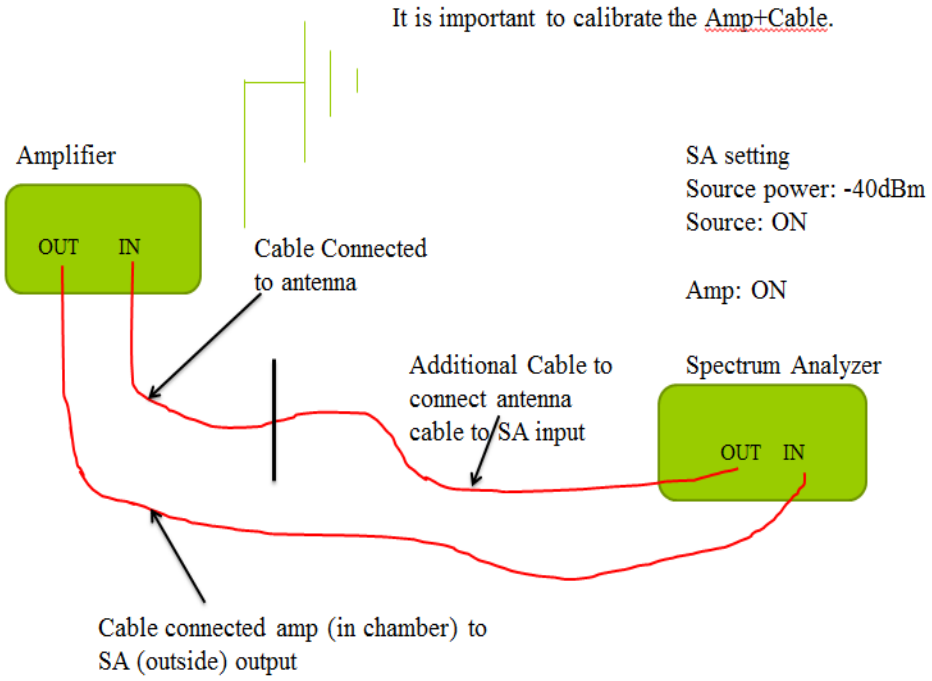


Figure 5.1. Calibration procedure

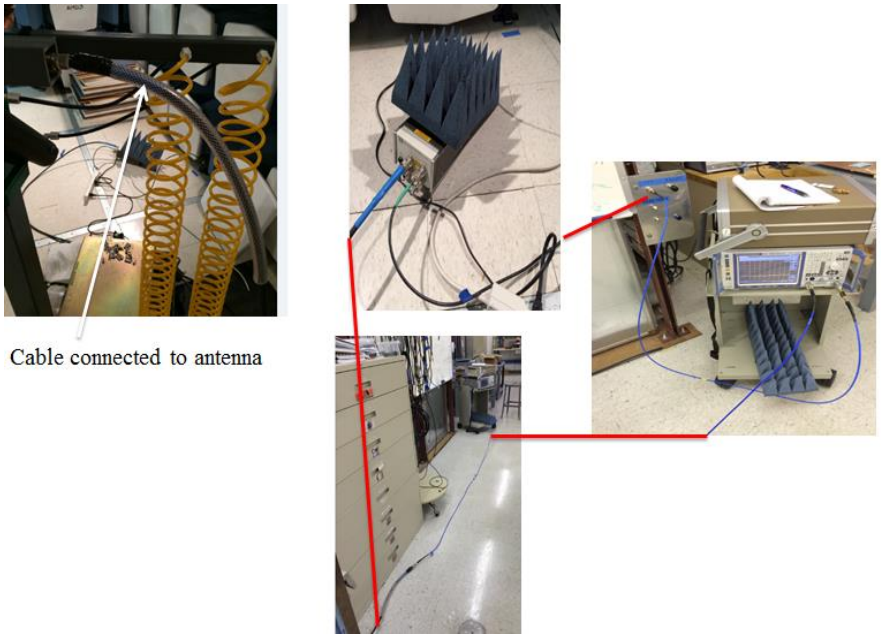


Figure 5.2. Real product connection illustrated by red line

After calibrating the power amplifier and cable loss, the measurement can be processed. After measuring the far field, spectrum analyzer data should be processed to calculate the E field measured at the antenna. The equations are shown from 5.1-5.6. It means the power measured in spectrum analyzer should subtract the S21 of the amplifier channel, plus the antenna factor and plus 107, then the result is the E field measured by the antenna.

$$\left|S_{21}\right|^2 = G_a - L_{cable} = \frac{P_{meas}}{P_r} \tag{5.1}$$

$$P_r = \frac{P_t G_t G_r \lambda^2}{\left(4\pi R\right)^2} \tag{5.2}$$

$$P_D = \frac{P_t G_t}{4\pi R^2} = \frac{E_r^2}{\eta} \tag{5.3}$$

$$AF = 20\log 10\left(\frac{9.73}{\sqrt{G_r}\lambda}\right) \tag{5.4}$$

$$E_r^2 = 4\pi\eta \frac{P_{meas}}{\left|S_{21}\right|^2 G_r \lambda^2} \tag{5.5}$$

$$E_r\left(dBV/m\right) = \left[10\log 10\left(4\pi\eta\right) - 20\log 10\left(9.73\right)\right] + P_{meas}\left(dBW\right) - S_{21}\left(dB\right) + AF\left(dB\right) \tag{5.6}$$

$$E_r\left(dB\mu V/m\right) = 107\left(dB\right) + P_{meas}\left(dBmW\right) - S_{21}\left(dB\right) + AF\left(dB\right) \tag{5.7}$$

5.2. FAR FIELD MEASUREMENT

The only radiation needed is the radiation from trace. And other parts should be shielded well to achieve the goal. In terms of this a shielding box is necessary. The shielding box is shown in Figure. 5.3. In order to eliminate cavity mode in the box, absorbing material is attached. The PCB board is placed at the top surface of the box and

the gap between PCB board and box is filled with gasket for shielding purpose. It is shown in Figure. 5.4.

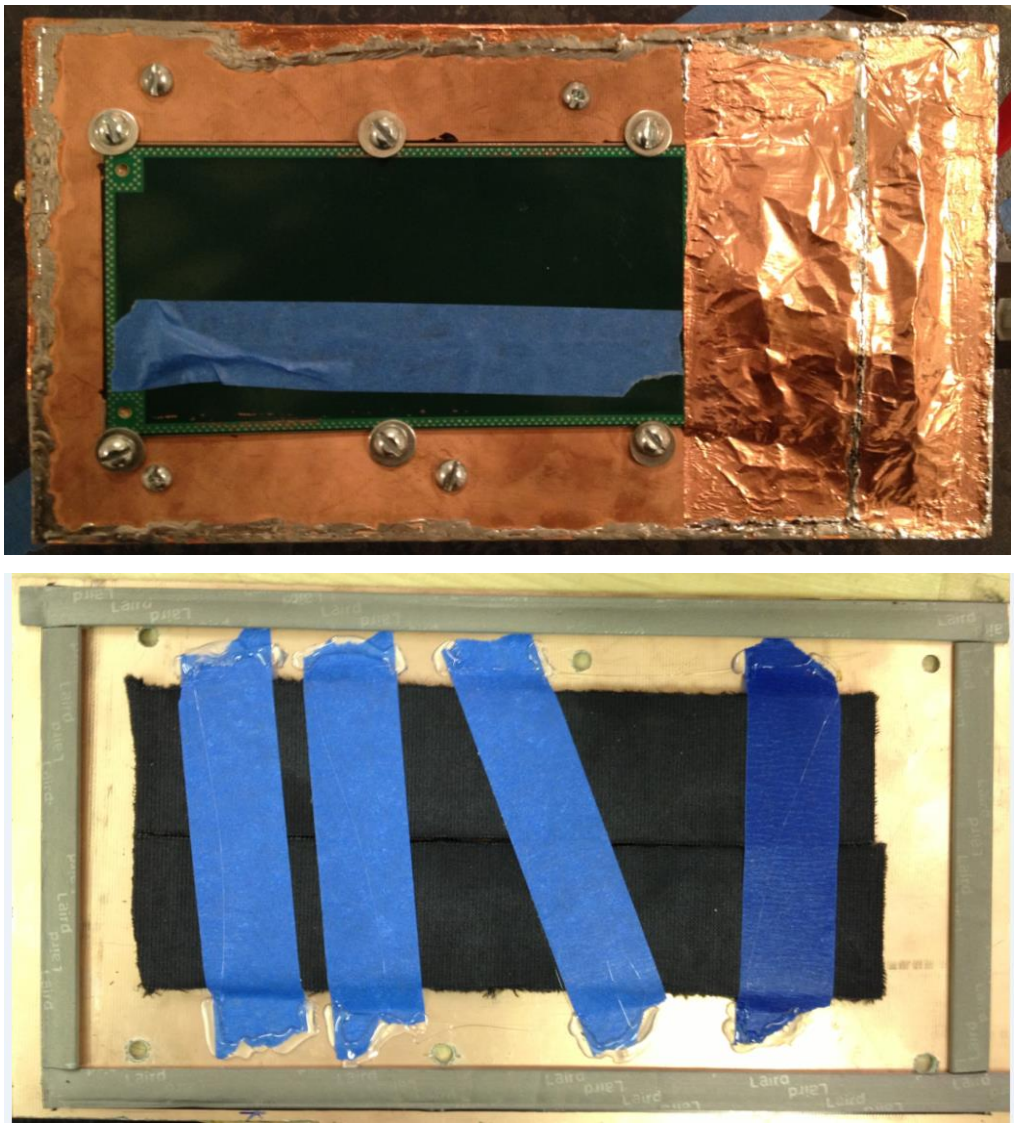


Figure 5.3. Top and inner bottom.

Figure 5.4. Different views of the shield box

In order to make sure there is no radiation from shielding box when it is fully covered, all slots are soldered and attached to ground on the turn table, as shown in Figure. 5.5. The antenna is set to 1 m height and the DUT is placed at the center of the turn table, shown in Figure 5.6. After measurement the far field is measured and it is almost noise floor shown in Figure 5.7.

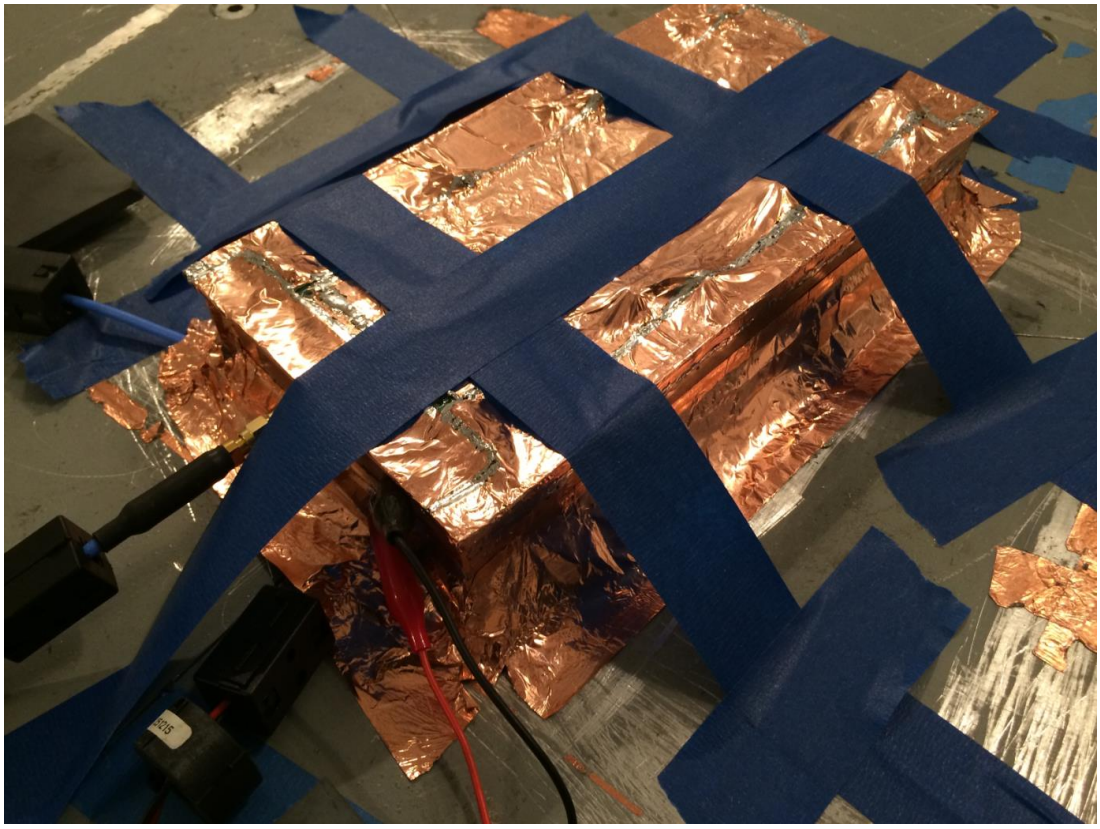


Figure 5.5. DUT Covered with copper tape

Figure 5.6. Far field measurement setup

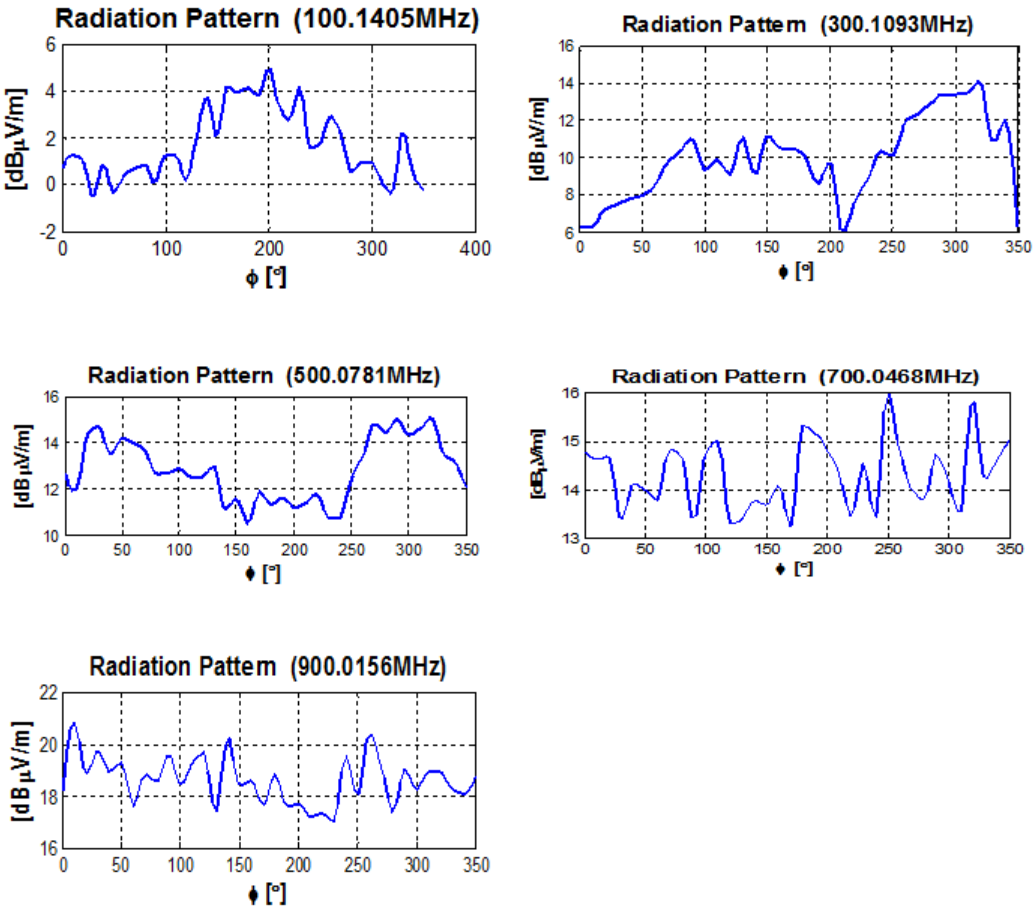
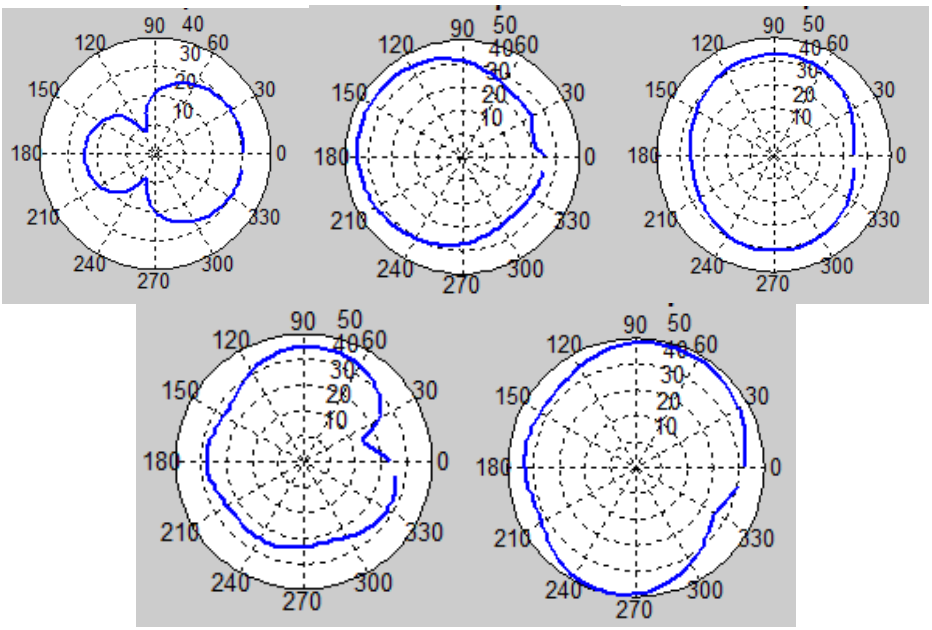


Figure 5.7. Far field measured with box fully covered

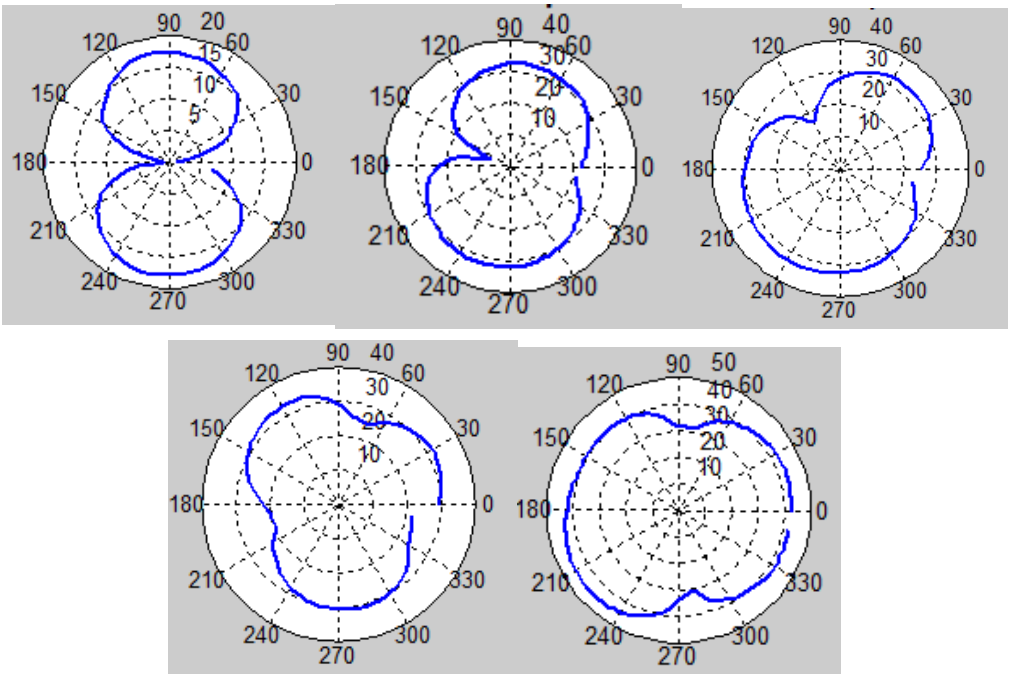
When the board is fully covered, there is no radiation from far field measurement. After that the trace area is opened and the silkscreen on the edge of PCB board is removed. And the edge of the PCB board,where ground vias located, is soldered with copper tape covered so that the radiation will not escape from the the box. The only radiation source is the trace. It is shown in Figure. 5.8.

Figure 5.8. Radiation measured from trace

After post-processing with the measured data, far field pattern is obtained with antenna height of 1 m and horizontal distance of 3 m. The results are shown in Figure. 5.9. The peak values of these patterns are listed in Table 5.1.



Ez at 100 MHz - 900 Mhz



Eφ at 100 MHz – 900MHz

Figure 5.9. Far field Ez and Eφ from radiated trace

Table 5.1. Far field radiation

	100MHz	300MHz	500MHz	700MHz	900MHz
Measure Ez (dBuV/m)	30.77	44	43	45	49.7
Measure Eφ (dBuV/m)	18	32.7	32.8	33	45

The pattern is different from simulation; the reason is investigated by using H-field probe to check if there is leakage field from the box. It is found that at the load connector part, there is radiation. In order to eliminate the effect of the connector, trace is cut off by the end of the transition signal via and soldered with 50 Ohm resistor to GND. Then solder all the pins of the connector to GND by copper tape, as shown in Figure. 5.10.

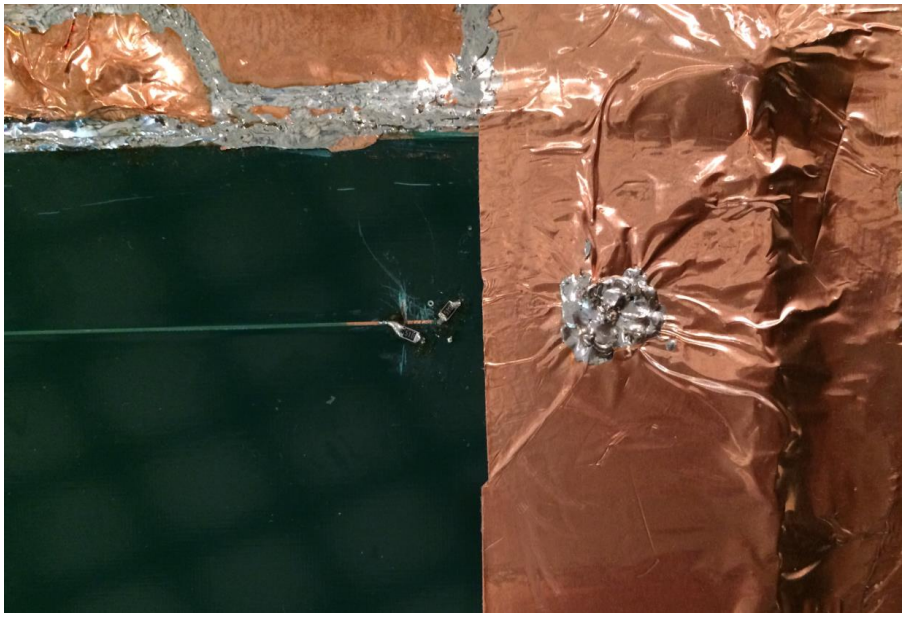


Figure 5.10. Cut off trace and shield the connector part

After shielding the connector the far field pattern becomes better, as shown in Figure. 5.11. And max far field values are listed in table 5.2.

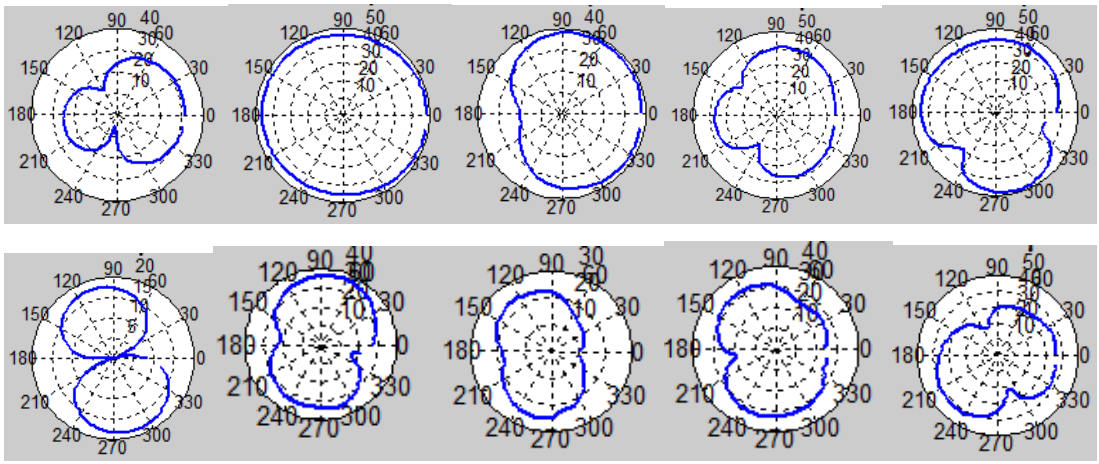


Figure 5.11. Ez and Eφ from measurement with connector covered

Table 5.2. Max far field values with connector covered

	100MHz	300MHz	500MHz	700MHz	900MHz
Measure Ez (dBuV/m)	31.58	48.56	38.79	41.15	48.49
Measure Eφ (dBuV/m)	18.53	36.79	25.2	33.28	41.86

After doing the far field measurement the Ez pattern at 300 MHz is still not good. When using H-field probe to measure the field at the edge of the PCB board, there is always peak at 300 MHz, shown in Figure 5.12.

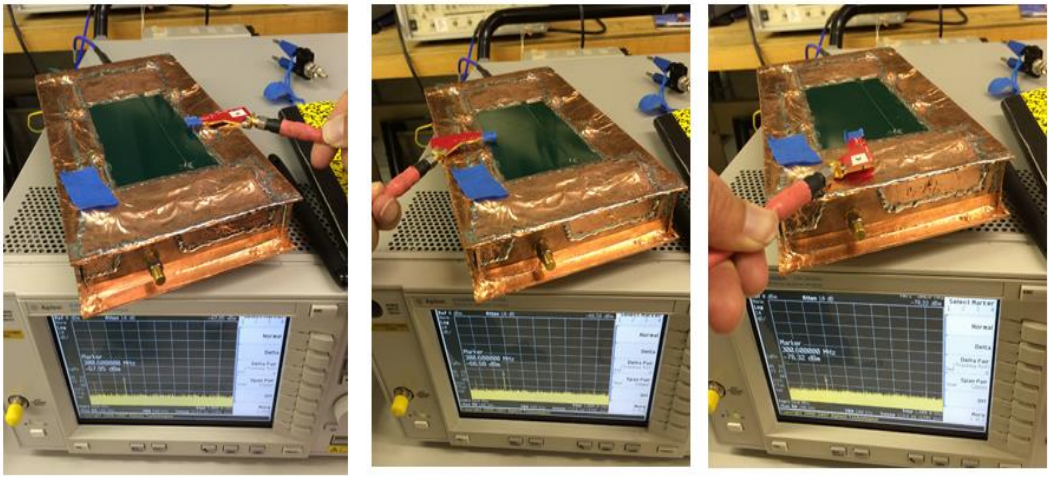


Figure 5.12. There is always a peak at 300 MHz

When the edge of the PCB board is milled, it is found that the layer below the trace is PWR plane instead of GND plane which is different from my design. The manufactury make a mistake! This is the reason why there are offset between simulation and measurement and the simulation results are matched well. Further work will be done when the new board comes.

6. FAR FIELD SIMULATION

6.1. FAR FIELD OF IBIS MODEL TOTAL VOLTAGE SOURCE

A full-wave structure same as real test board is needed for far field simulation. Because the testboard is shielded by box, so a box needs also to be created in HFSS. The real testboard with shielding box is shown in Figure 6.1. The test board in HFSS model is simplified as a microstripline because the only radiation part is the trace on the top layer and the other parts are shielded. So the PCB board can be represented as a microstripline. Lumped port is applied in this model, as shown in Figure. 6.2.

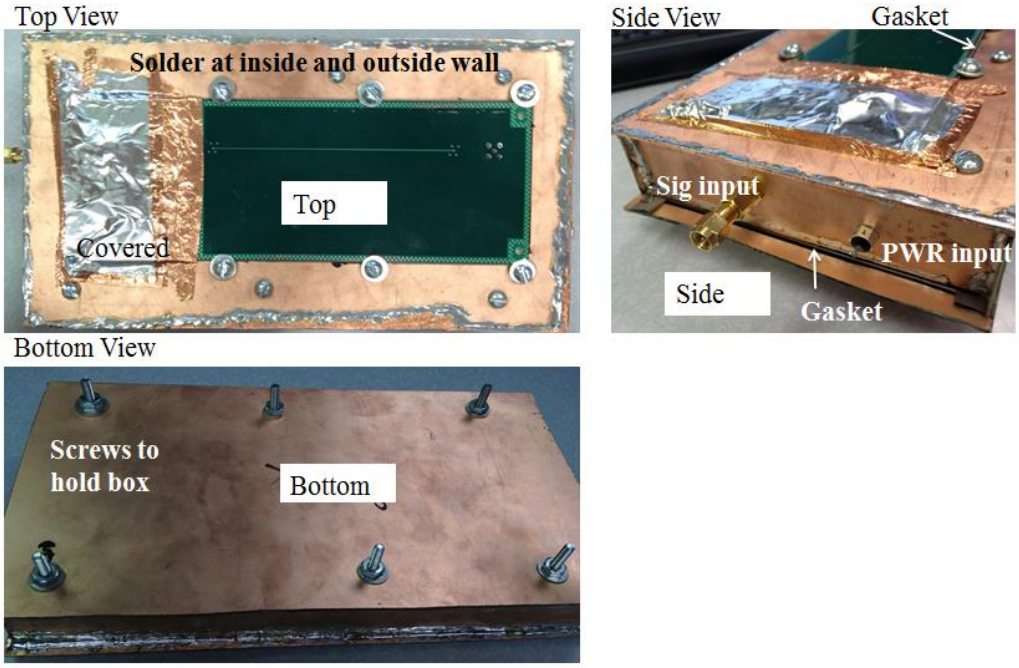


Figure 6.1 Shielding box

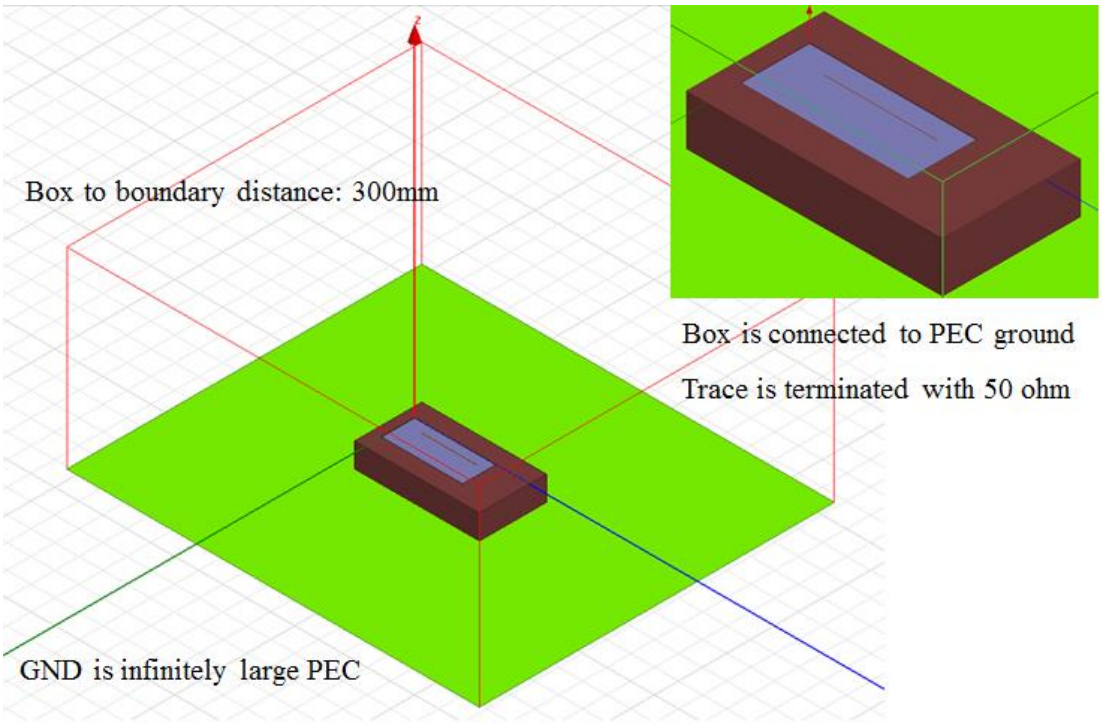


Figure 6.2 Full-wave model for PCB board and shielding box

As mentioned in section 3, the total voltage is obtained from IBIS model and the total voltage is transferred from time domain to frequency domain. The total voltage from IBIS model matches with that from measurement, in table 6.1. Then it is applied into HFSS for far field simulation. Port setting is shown in Figure 6.3. For approach one, a uniform 1 V total voltage is used. In the post processing after simulation, the real simulated far field should be that multiplied by the actual total voltages of different harmonics listed in the table 6.1

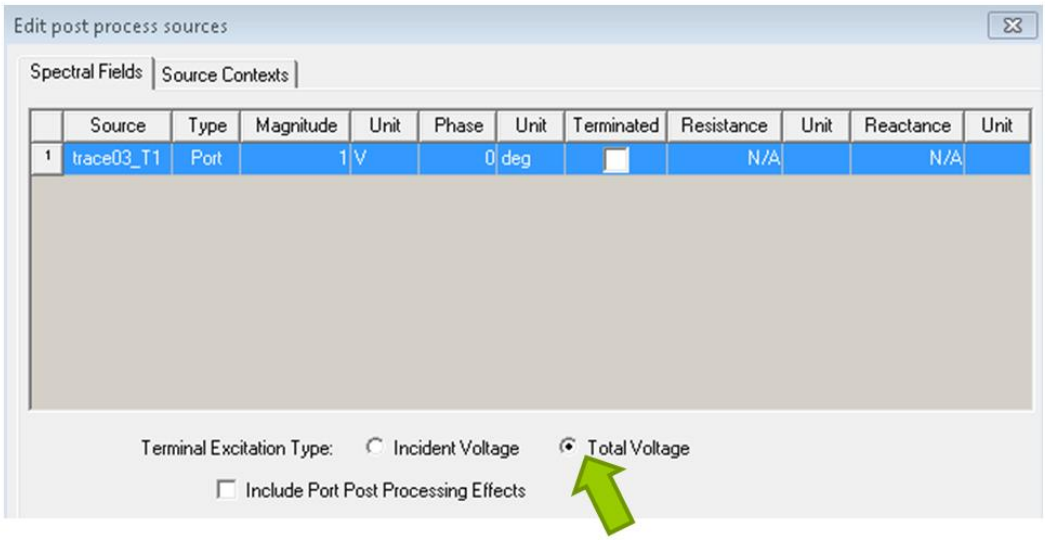


Figure 6.3. Apply total voltage in HFSS

Table 6.1. Total voltage from measured IC output and IBIS output

	100 MHz	300 MHz	500 MHz	700 MHz	900 MHz
Measured total voltage	0.449 V	0.144 V	0.087 V	0.049 V	0.042 V
IBIS Total volage	0.401 V	0.133 V	0.079 V	0.056 V	0.043 V

From the table 6.1, the measured total voltage is almost the same with IBIS total voltage. After simulation, the far field pattern can be obtained. The measurement is done in cylindrical coordinate and the far field sphere is defined in spherical coordinate so the

sphere radius in the HFSS simulation should be modified to sqrt(3^2+1^1), as shown in Figure 6.4.

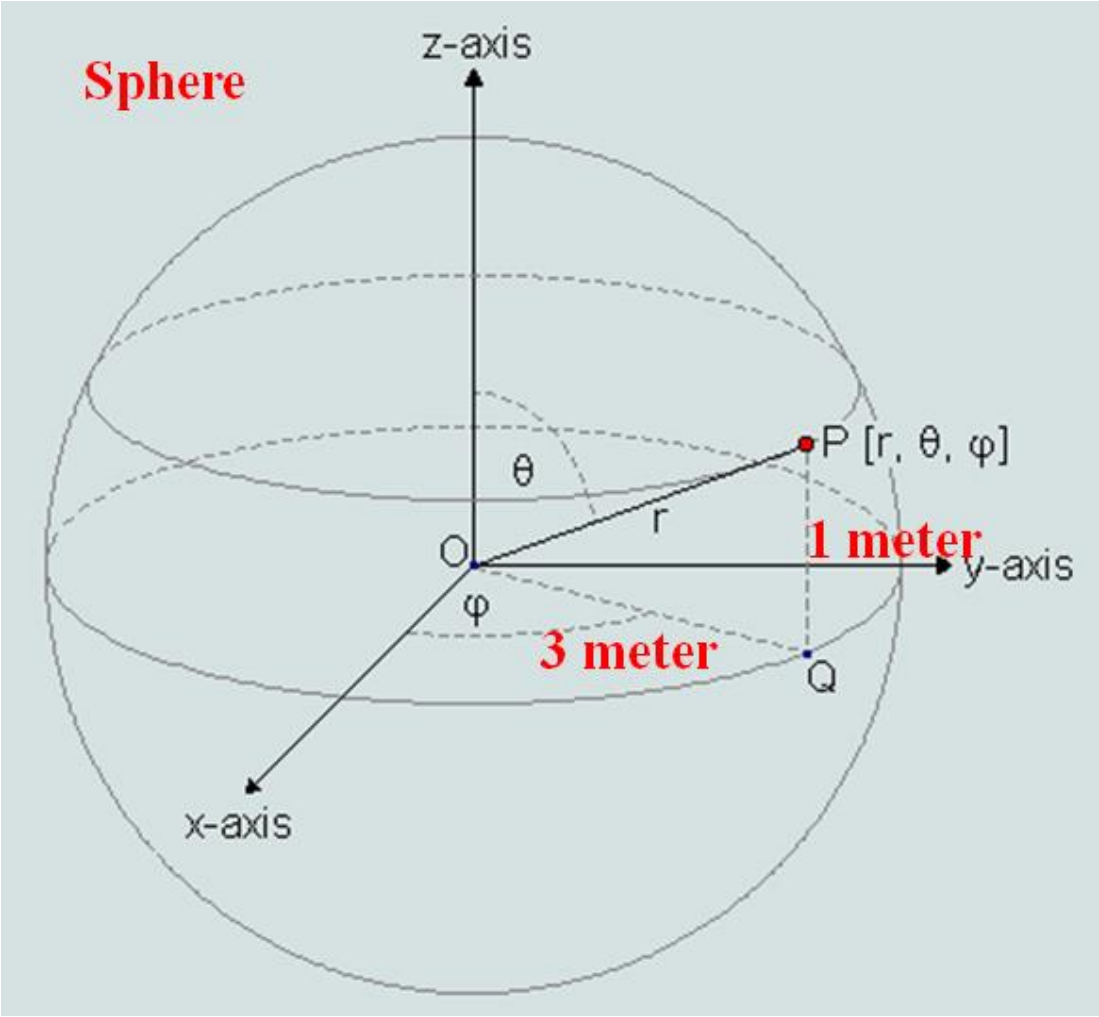


Figure 6.4. Sphere defined in HFSS

The far field radiation pattern from measured total voltage is shown in Figure 6.5-Figure 6.8. And the peak value is shown in Table 6.2. The total voltage from IBIS

matches with that from measurement. The far field simulation from IBIS also matches with that from measured source, shown in table 6.2.

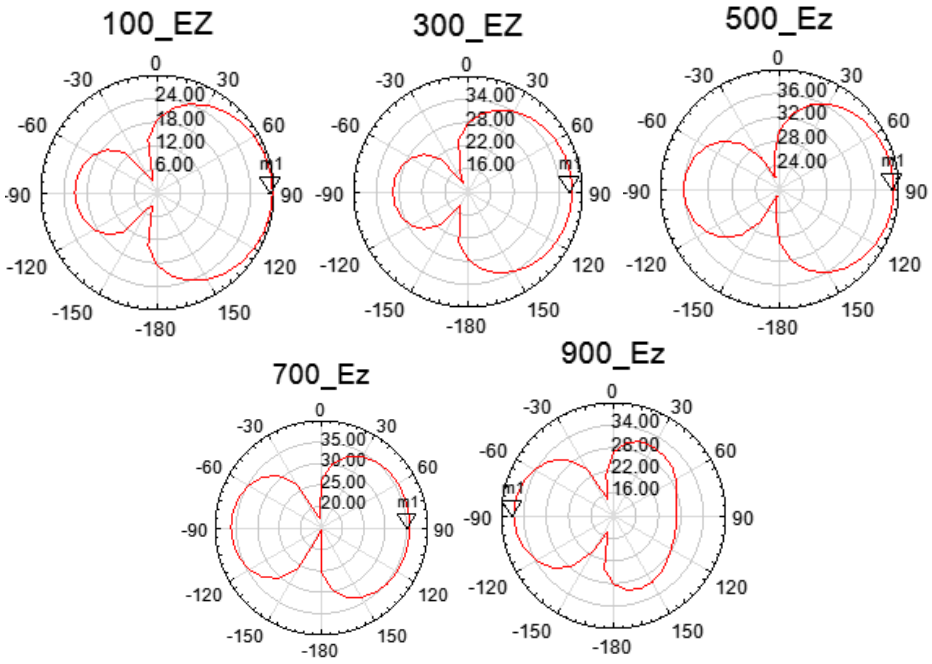


Figure 6.5. Ez far field pattern from measured total voltage

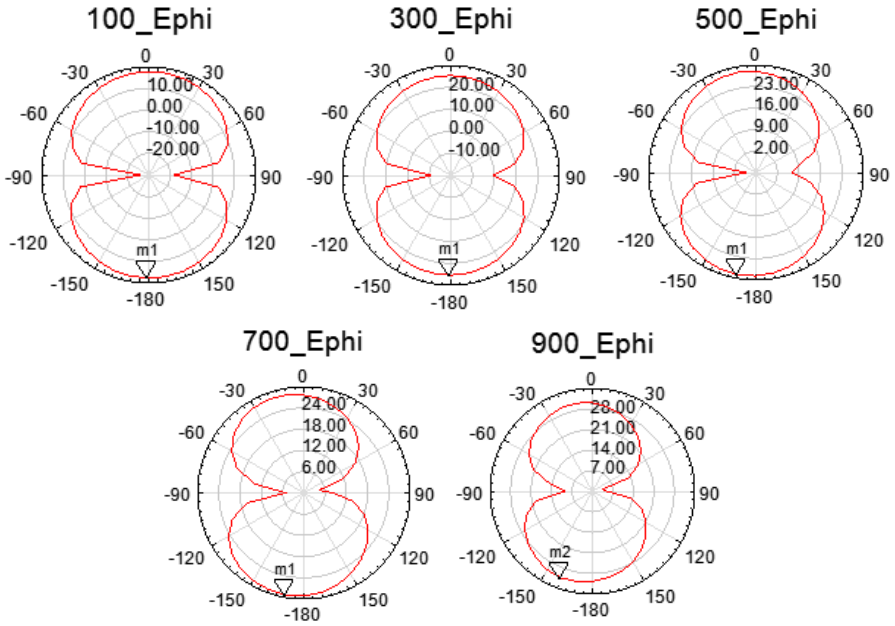


Figure 6.6 Eφ far field pattern from measured total voltage

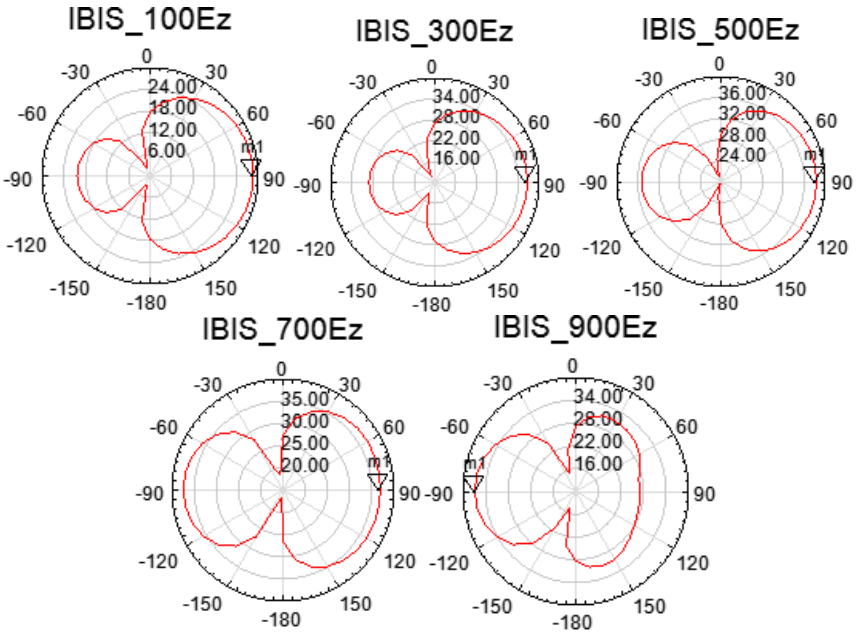


Figure 6.7. Ez far field pattern from IBIS total voltage

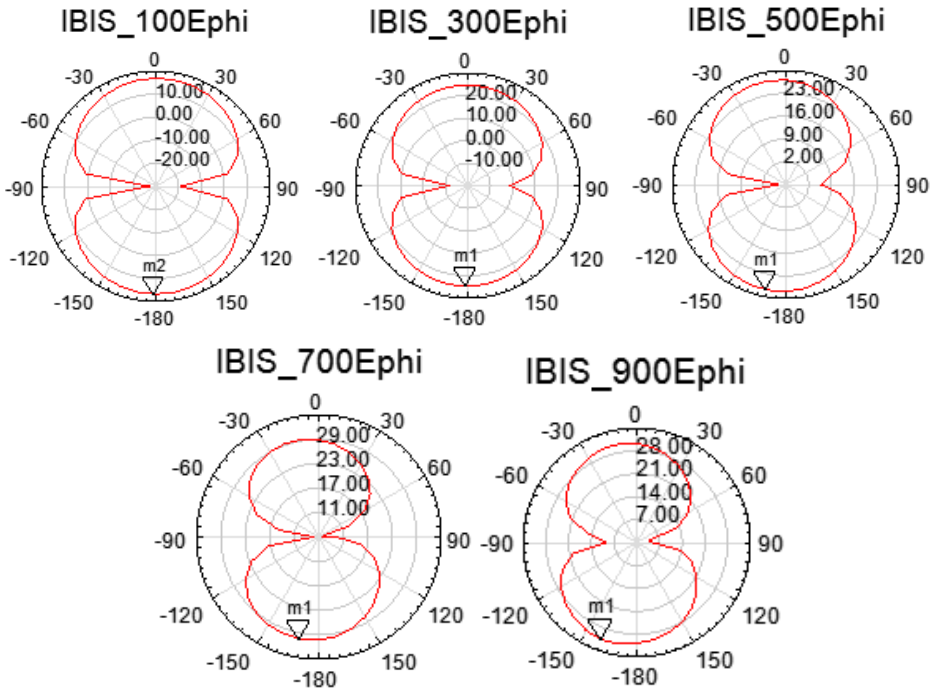


Figure 6.8. Eφ far field pattern from IBIS total voltage

Table 6.2. Total voltage from measured IC output and IBIS output

	total voltage	100 MHz	300 MHz	500 MHz	700 MHz	900 MHz
Ez(dBuV/m)	measured	29.7	37.4	39.2	35.8	36.7
	IBIS	28.7	36.7	38.4	36.9	36.9
E_{φ}(dBuV/m)	Measured	17.7	25.4	28.7	29.3	31.4
	IBIS	17	25	28	30.4	31.6

6.2. FAR FIELD OF IBIS THEVENIN EQUIVALENT SOURCE

When the Thevenin's equivalent source is obtained from section 4, in ADS simulation, the source can be applied as incident voltage in HFSS simulation for far field. The advantage of this method is that the equivalent source is independent of structures it

is applied, which means once the equivalent source is obtained it can be used in any structures.

To apply the equivalent source from lumped world to wave world, there is a transition, shown in Equation 6.1- 6.3. From the equation incident voltage in lumped port should be half of the Vs and the port impedance is Zs. Also the advantage of using incident voltage instead of total voltage is that incident voltage is independent of Zin which is dependent on the structure. So the Thevenin equivalent source can be applied as incident voltage to any structures.

$$V_{port\_total} = V_{incident}(1 + \Gamma) = V_{incident}\left(1 + \frac{Z_{in} - Z_s}{Z_{in} + Z_s}\right) \tag{6.1}$$

$$V_{port\_total} = \frac{Z_{in}}{Z_s + Z_{in}} V_s \tag{6.2}$$

$$V_{incident}\left(1 + \frac{Z_{in} - Z_s}{Z_{in} + Z_s}\right) = \frac{Z_{in}}{Z_{in} + Z_s} V_s \Rightarrow V_{incident} = \frac{1}{2} V_s \tag{6.3}$$

After applying Thevenin equivalent source in HFSS simulation, the far field radiation pattern can be achieved, shown in Figure 6.9 and Figure 6.10. The shapes of the patterns at 900 MHz have a little difference. This is because of mesh in HFSS simulation. So the pattern has some difference. The peak values are listed in Table 6.3. Compared with far field simulation results from approach one, the far field match well.

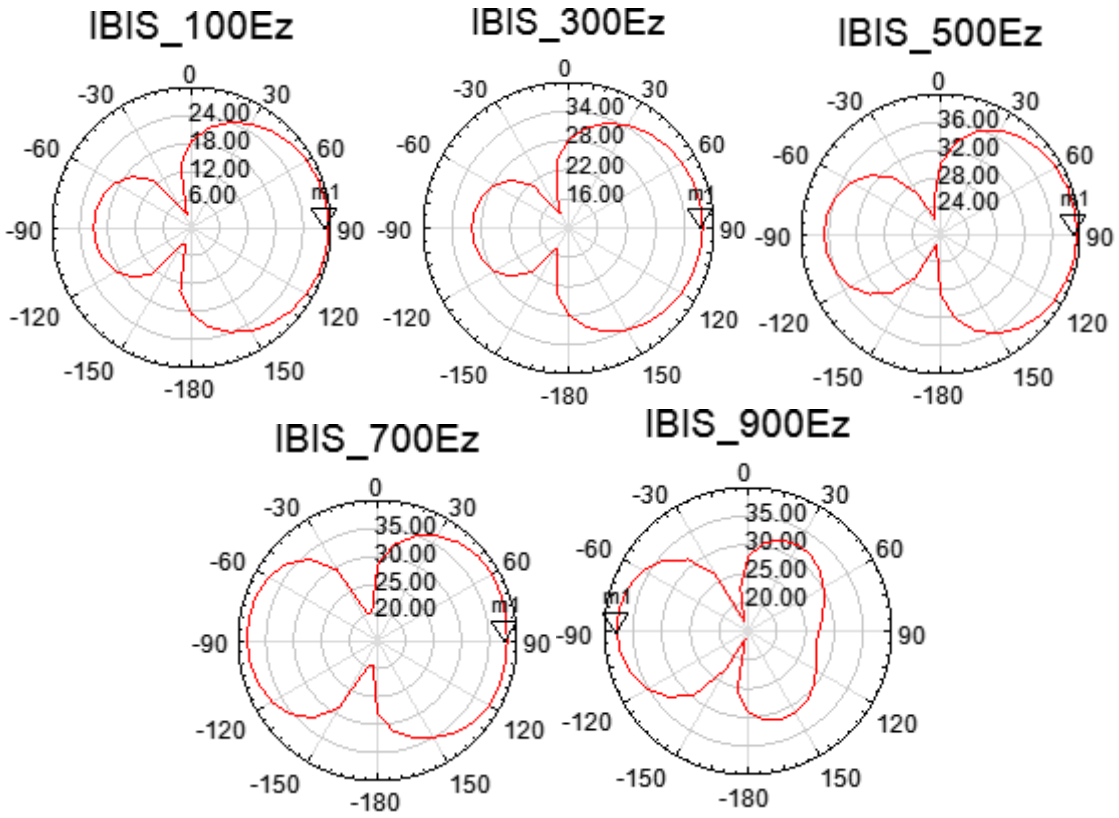


Figure 6.9. Ez far field pattern from IBIS equivalent source

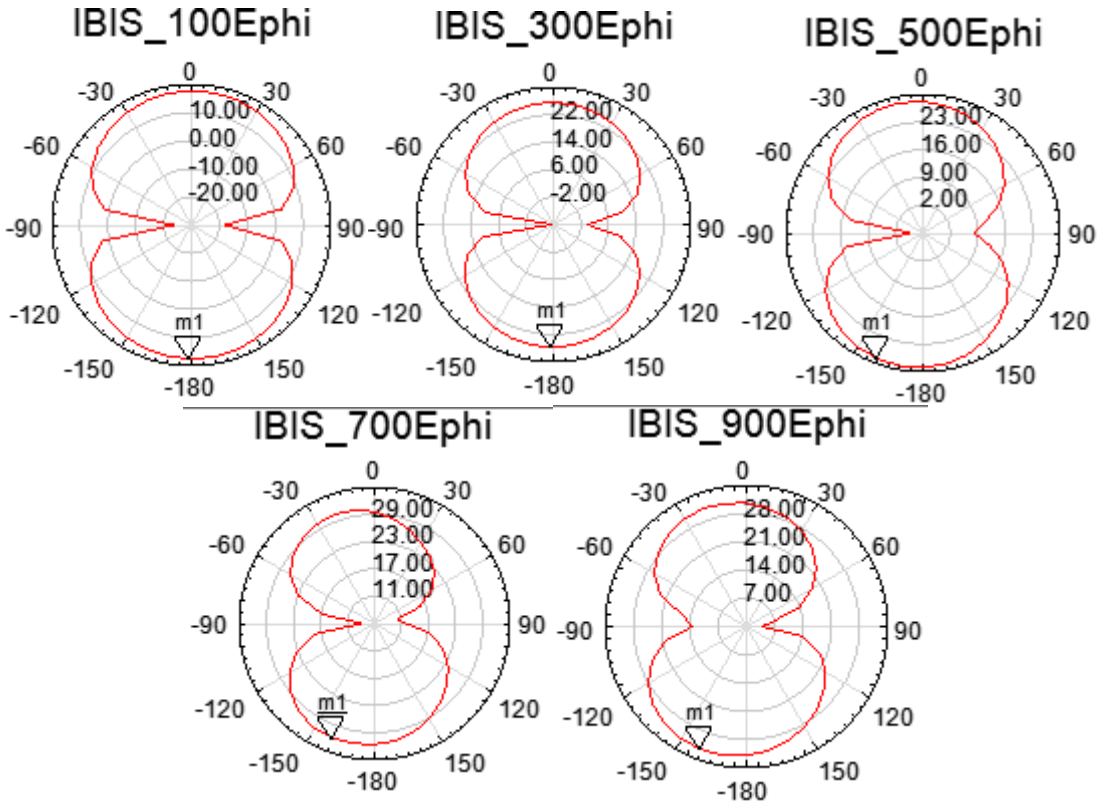


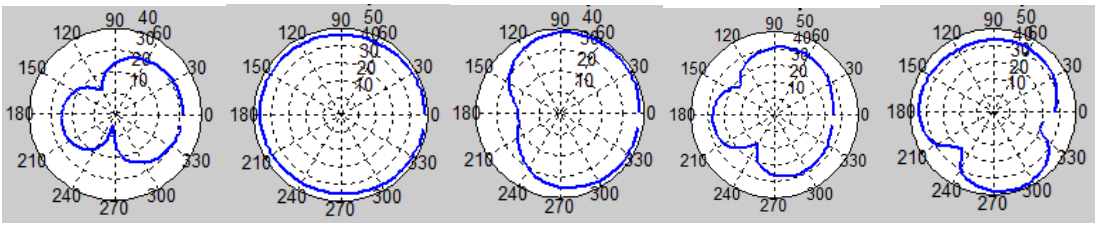
Figure 6.10. Eφ far field pattern from IBIS equivalent source

Table 6.3. Maximum E field from IBIS equivalent source

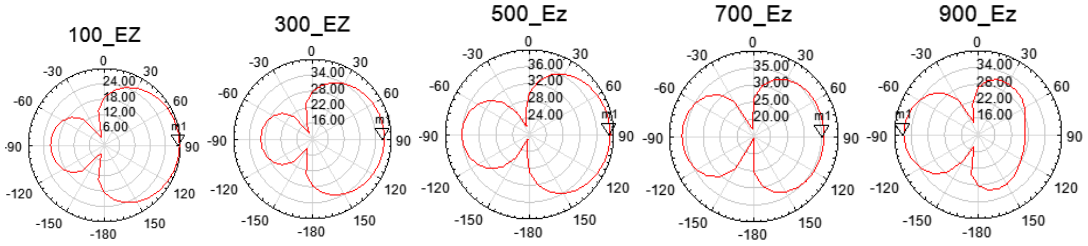
	100 MHz	300 MHz	500 MHz	700 MHz	900 MHz
Ez(dBuV/m)	29.6	37.7	39.6	38.3	37.8
E_{φ}(dBuV/m)	17.6	25.8	29	31.9	32.4

7. CONLUSION

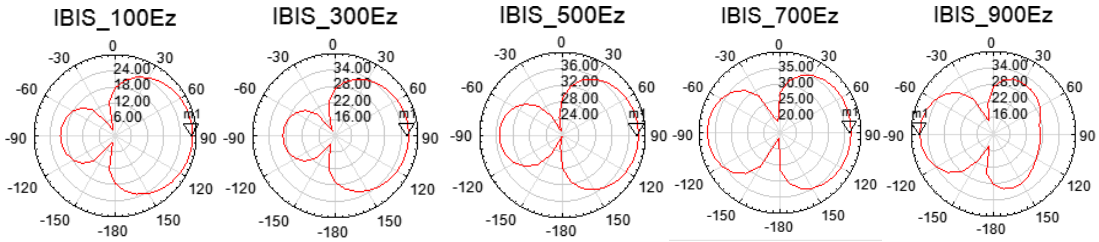
Simulation and measurement are compared in the following Figure 7.1 and Figure 7.2 and the comparison of maximum radiation values is listed in Table 7.1. From the comparison, the pattern from simulation match well; however the pattern between simulation and measurement has some offset in high frequency. For the maximum radiation values, the simulation results match well with each other and have some difference with measurement. It means IBIS model can be used to extract equivalent source and applied into HFSS to do simulation for far field. Besides measurement method, IBIS is good to construct IC conducted emission model.



(a) Ez far field from testboard measurement

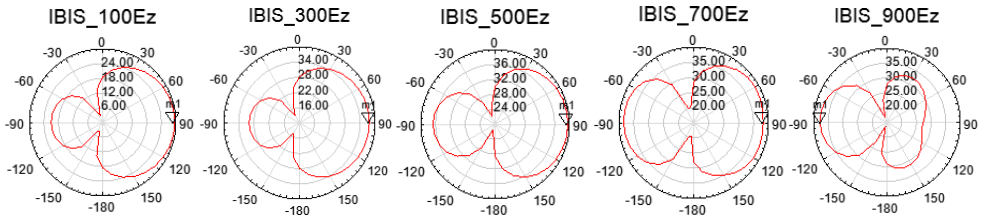


(b) Ez far field pattern from simulation of measured total voltage



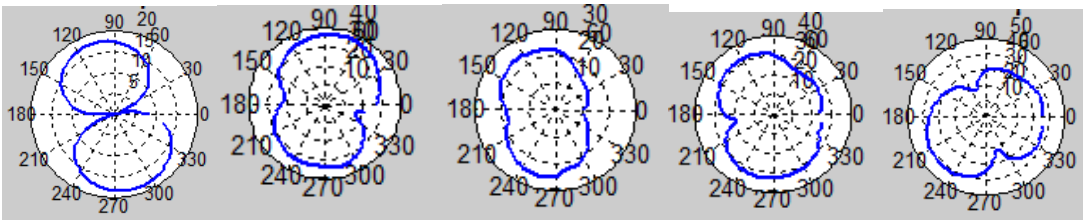
(c) Ez far field pattern from simulation of IBIS total voltage

Figure 7.1. Far field pattern comparison.

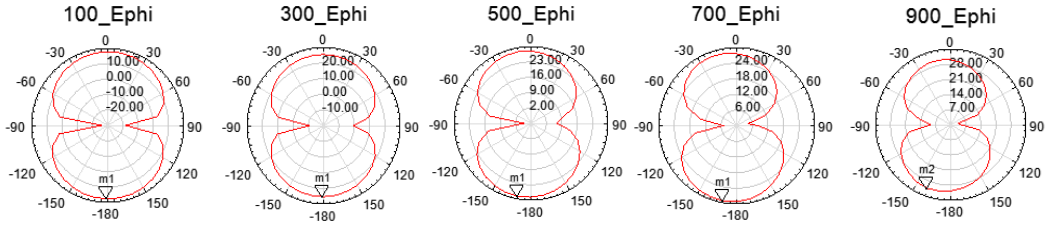


(d) Ez far field pattern from simulation of IBIS equivalent source

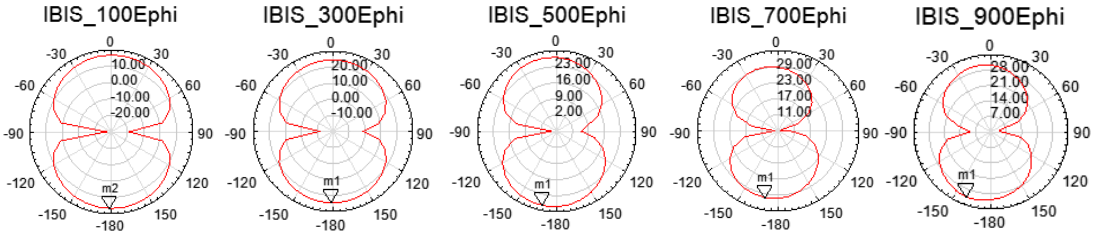
Figure 7.2. Far field pattern comparison(cont.)



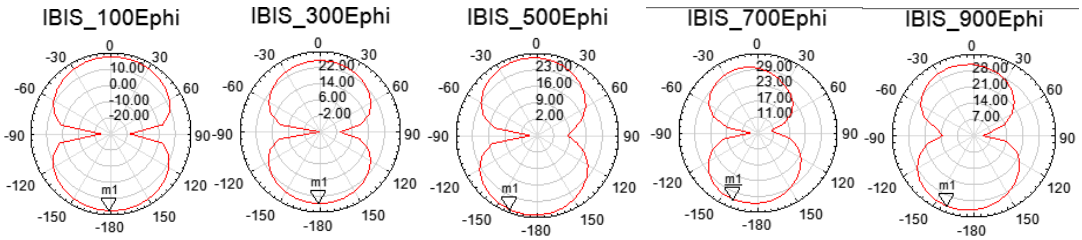
(a) Eφ far field from testboard measurement



(b) Eφ far field pattern from simulation of measured total voltage



(c) Eφ far field pattern from simulation of IBIS total voltage



(d) Eφ far field pattern from simulation of IBIS equivalent source

Figure 7.3. Far field pattern comparison.

Table 7.1. Maximum values of radiation pattern

			100 MHz	300 MHz	500 MHz	700 MHz	900 MHz
Ez (dBuV/m)	measurement		31.58	48.56	38.79	41.15	48.49
	simulation	Measured total voltage	29.7	37.4	39.2	35.8	36.7
		IBIS total voltage	28.7	36.7	38.4	36.9	36.9
		IBIS Thevenin voltage	29.6	37.7	39.6	38.3	37.8
E_{φ} (dBuV/m)	measurement		18.53	36.79	25.2	33.28	41.86
	simulation	Measured total voltage	17.7	25.4	28.7	29.3	31.4
		IBIS total voltage	17	25	28	30.4	31.6
		IBIS Thevenin voltage	17.6	25.8	29	31.9	32.4

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