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Investigation of decoupling capacitor connection methods using PEEC and study of alien crosstalk from a BroadR-Reach® protocol based system

Tamar Makharashvili

Department:

INVESTIGATION OF DECOUPLING CAPACITOR CONNECTION METHODS USING PEEC AND STUDY OF ALIEN CROSSTALK FROM A BROADR-REACH® PROTOCOL BASED SYSTEM

by

TAMAR MAKHARASHVILI

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Dr. Daryl Beetner, Advisor
Dr. Albert Ruehli
Dr. James L. Drewniak

ABSTRACT

Power Distribution Network (PDN) for Printed Circuit Board (PCB) design requires proper power integrity analysis. In order to deliver a low-ripple DC voltage from a Voltage Regulator Module (VRM) to an Integrated Circuit (IC), a certain target input impedance should be achieved. Developing simple physics-based equivalent circuit models are essential for understanding how a system works and making crucial design decisions. In this work, the input impedance of a decoupling capacitor due to traces, pads and via discontinuities are investigated using the Physics-based Model Size Reduction (PMSR) method. Various decoupling capacitor connection methods are compared and design guidelines are provided for reducing the equivalent inductance to meet target impedance requirements. It is shown that a shared pad having 179 pH equivalent L_{above} loop inductance is a better design choice as compared to a doublet or shared via design with 218 pH and 406 pH L_{above} loop inductance respectively.

The second part of this thesis relates to BroadR-Reach® technology, a point-to-point Ethernet Physical Layer (PHY) standard, which is used in automotive applications. This technology allows full-duplex communication between two devices over a single, Unshielded Twisted wire Pair (UTP) cable. Here, alien crosstalk in a 6 UTP bundle is investigated for meeting electromagnetic compatibility requirements. The performance of Alien Near-End and Far-End Crosstalk of two different UTPs with and without an inline Circular Plastic Connector (CPC) are compared to standard limits. An inline connector in the middle of a 15 m 6 UTP cable bundle, with a 25 cm untwisted region fails the PSANEXT standard limit by 4 dB at 100 MHz, while the same bundle without the connector passes the standard by a margin of 8 dB at 100 MHz.

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1. INTRODUCTION

System level modelling and standard regulations are two of the main research areas in Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC). At first it may seem like system level modelling and standard regulations are two different topics, however it should be noted that they are strongly related to each other under the concept of EMI/EMC. System level modeling helps us to understand which part of the system contributes towards EMI/EMC problems, which may result in a failure under standard requirements.

A Power Distribution Network (PDN) should deliver a low-ripple DC voltage from a Voltage Regulator Module (VRM) to an Integrated Circuit (IC). Global and local decoupling capacitors are used for power noise regulation in VRM designs. Via connections throughout the PCB layers are used for connecting decoupling capacitors to power and ground layers or fills. The input impedance looking from the IC into the PDN structure determines the voltage ripple. Analyzing the equivalent circuit of the PDN assists in the design of Printed Circuit Boards (PCB). Observing the system response does not give a good idea about how to change the PDN design which makes it difficult to make decisions on design changes in the system. The main objective of the modeling problems studied here is to investigate various decoupling capacitor connection methods and provide design guidelines for reducing the equivalent inductance and meeting target impedance requirements. Simple physics-based equivalent circuit models are essential for understanding the underlying physics that causes the resulting inductance. Partial Element Equivalent Circuit (PEEC) method transfers an electromagnetic domain problem to a circuit level problem. A Physics-based Model Size Reduction (PMSR) method, based on this PEEC solution, was previously proposed and applied for DC capacitor block modeling for power electronic systems [1]. PMSR technique generates small, equivalent circuits based on the geometry of the structure. As this method is physics driven, each element of the circuit can be easily related to a corresponding geometry in the structure. This method is used here to better understand the causes of inductance associated with various decoupling capacitor connection methods.

Another contribution of this work is towards the investigation of alien crosstalk in a BroadR-Reach® protocol based system. Alien crosstalk represents an unknown source coupling into the link segment. BroadR-Reach® technology is a point-to-point Ethernet Physical Layer (PHY) standard which is used in automotive connectivity applications. This is an upcoming technology, which allows full-duplex communication between two devices over a single, Unshielded Twisted Pair (UTP) cable. The BroadR-Reach® protocol realizes simultaneous transmission and reception operations through an UTP cable at 100Mb/s. Thus the frequency range for the PHY is significantly increased compared to the previous Controller Area Network (CAN) standard, where data transmission speed is limited to 10Mb/s. It is necessary for systems with a BroadR-Reach® Ethernet PHY to meet the EMC requirements for automotive applications.

A particular application involving a bundle of 6 UTP's gives rise to a scenario with one victim pair and 5 aggressors. Alien crosstalk is generally present when cables are bundled together. This crosstalk noise may also occur from unknown sources outside the cable bundle that can couple into the link segment via electric and magnetic fields. For meeting new standard requirements, different automotive cables and connectors were tested to check if they meet the standard requirements. A methodology and testing procedure for Power Sum Alien Near-End Crosstalk and Power Sum Alien Equal Level Far-End Crosstalk was developed. Two cables with and without an inline Circular Plastic Connector (CPC) were tested for their compliance towards the standards. The effect of the untwisted region at the connector was also investigated.

The overall structure of the thesis is as following. Section 2 relates to the effect of PCB planes and via discontinuities on the input impedance looking into a decoupling capacitor. Various decoupling capacitor connection methods are compared and design guidelines are provided based on equivalent circuits obtained using the PMSR method. Section 3 demonstrates the methodology, the testing procedure, and experimental results for Power Sum Alien Near-End Crosstalk and Power Sum Alien Equal Level Far-End Crosstalk considering a simple test structures.

2. PHYSICS-BASED MODEL SIZE REDUCTION

2.1. INTRODUCTION

A high speed Printed Circuit Board (PCB) requires proper power integrity analysis. One of the important considerations for a high speed PCB is the design of the Power Delivery Network (PDN). The PDN should deliver a low-ripple DC voltage from a Voltage Regulator Module (VRM) to an Integrated Circuit (IC). Global and local decoupling capacitors are used for power noise regulation in VRM design. Via connections throughout the PCB layers are used for connecting decoupling capacitors to power and ground layers or fills. The input impedance looking from the IC into the PDN determines the voltage ripple from the VRM [2], [3]. There is a lot of ongoing research regarding the input impedance calculation. One such approach is to create an equivalent circuit of the PCB PDN layers using the cavity model [4]. In this paper, the input impedance due to the PCB planes and via discontinuities was investigated. Various decoupling capacitor connection methods were compared and design guidelines were provided so as to reduce the equivalent inductance and thus meet the target impedance requirements. However, the equivalent inductance for these models does not include the inductance of the decoupling capacitors and connecting traces and pads. Here, L_{above} refers to the total equivalent inductance above the top GND plane looking into the decoupling capacitor, while L_{below} refers to the total equivalent inductance below top GND plane through all the PCB layers till the IC (Figure 2.1). In some cases L_{above} dominates L_{below}, especially when the PCB thickness is small or when there are long traces between the pads and vias. Thus a thorough investigation of the different capacitor connection configurations is necessary.

Developing simple physics-based equivalent circuit modes are essential for understanding the physics of the system. The Partial Element Equivalent Circuit (PEEC) method converts an electromagnetic domain problem into a circuit problem. However, the resulting circuit model is so complex that it prevents the designer from having an intuitive understanding of the underlying causes of problems. There are several other reduction techniques developed for obtaining small, accurate equivalent circuits. The well-known Model Order Reduction (MOR) technique [5] is very effective for reducing

large PEEC circuit models. However, the circuit generated does not relate to the geometry, because the reduction is purely mathematical. In [6] and [7], an equivalent SPICE circuit model is obtained from impedance parameters determined using 3D full-wave simulations, where model reduction is obtained based on the equivalent circuits for the dominant eigenvalues of a structure. Derived Physically Expressive Circuit Model (DPECM) [8], [9] uses the Y-to-Δ transformation to combine all insignificant internal nodes in a coupling circuit model so that a resultant circuit contains only the essences of the original. DPECM method seems to work on narrow band RF models only. Different equivalent circuits are required for different frequency range using DPECM. Most power electronics models need a DC solution. So do Power Distribution Network (PDN) circuits. Recently, Physics-Based Model Size Reduction (PMSR) method was proposed and applied for a DC capacitor block in [1]. The equivalent circuit obtained using PMSR method is strongly correlated to the real geometry. This technique is used here to study decoupling capacitor connection methods. Efficiency is not an issue in this problem, but it is essential to understand the underlying physics to drive design guidelines and improved connection strategies.

In this work, the L_{above} of three different designs for decoupling capacitor connection methods are investigated and characterized. For better understanding of the physics involved, the equivalent circuits are developed using PMSR technique.

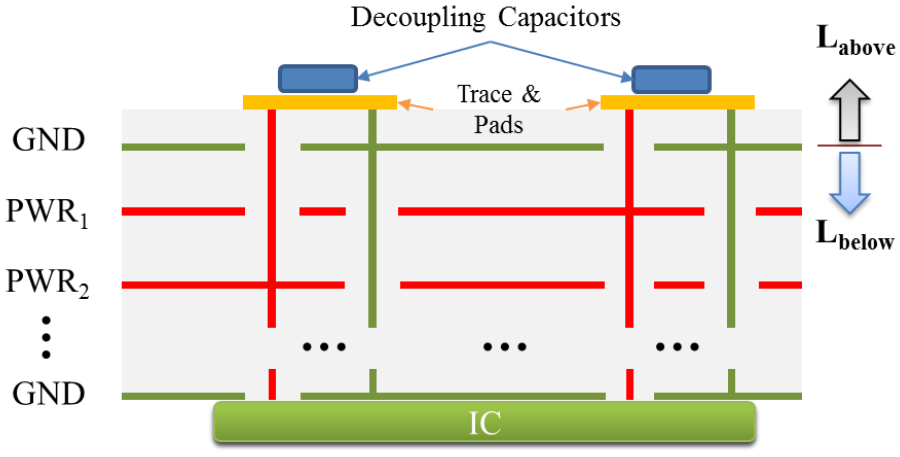


Figure 2.1. PCB PDN cross-section

2.2. PEEC FORMULATION

The Partial Element Equivalent Circuit (PEEC) Method was developed by Dr. Ruehli, starting as early as 1972 [10]. Since then PEEC modeling is widely used in Electromagnetic (EM) problem solving. A lot of research has been done on using the PEEC method in the time and frequency domain. PEEC converts an electromagnetic domain problem into the circuit domain, where SPICE-like circuit solvers can be applied for equivalent circuit analysis. PEEC models electric field interactions as capacitances and magnetic field interactions as inductances. The advantage of the method is that an interconnect geometry can be represented as a circuit model, where linear and non-linear elements can be later added and solved. Moreover, by using the PEEC method it is easy to separate the resistive, capacitive and inductive effects.

To apply the PEEC method, all of the conductors in the problem must first be subdivided into N canonical primitive structures, such as rectangular cells, for which formulas for capacitance, resistance, partial self and mutual inductances are known. There are two different capacitive and inductive cells as shown in Figure 2.2. It is assumed that currents in vertical (J_x) and horizontal (J_y) inductive cells and charge densities (q) in the capacitive cells are uniform. Solution accuracy increases for smaller mesh cells where assumption of current and charge uniformity holds good. Potential coefficients (inverse of capacitance matrix) calculated from charge density over each capacitive cell are defined at the nodes. Each inductance in a branch, between the nodes, is obtained from the current over vertical and horizontal inductive cells. The resistance and partial self-inductance of each branch is computed along with the partial mutual-inductance between each pair of branches. An example of a classic PEEC cell is shown on Figure 2.3. For n number of capacitive cells and m vertical and horizontal branches, resistive and inductive $m \times m$ matrices and capacitive $n \times n$ matrix are assembled.

By satisfying Kirchhoff's voltage (KVL) and current laws (KCL), a solver for the PEEC method can be constructed. The solution of PEEC models is based on the Modified Nodal Analysis (MNA) method. The MNA is one of the well-known general formulation methods based on KVL and KCL, which is widely used in circuit simulators such as SPICE [14]. The MNA matrix for a simple PEEC circuit can be expressed with passive

RLGC elements, independent current and voltage sources and unknown nodal voltages and branch currents in a matrix equation as in (1).

$$(s\mathbf{C}+\mathbf{G})\mathbf{X}(s)=\mathbf{X}_{in}(s) \tag{1}$$

where RLGC elements are defined in $(s\mathbf{C}+\mathbf{G})$, $\mathbf{X}(s)$ is vector of unknown nodal voltages and $\mathbf{X}_{in}(s)$ is independent current and voltage sources as denoted in (3), (4) and (5) respectively.

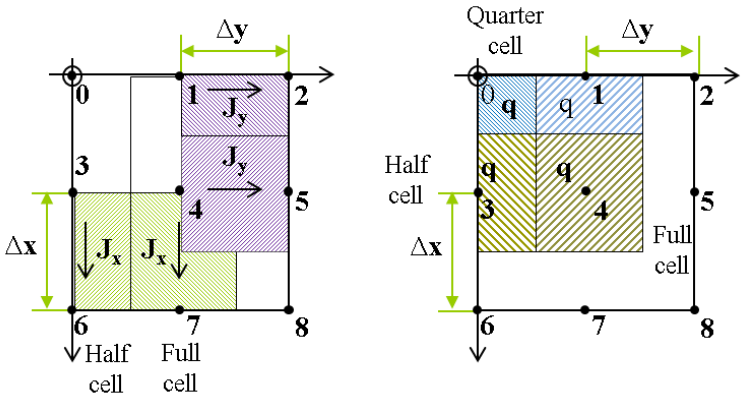


Figure 2.2. The meshing of the PEEC cells [1]

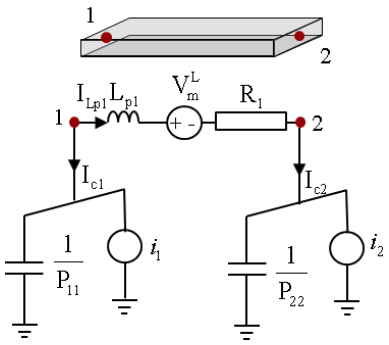


Figure 2.3. A “fundamental loop” of classic PEEC cell [1]

The PEEC tool used in this study is based on the analytical closed form solutions for the partial elements of a zero thickness conductor [10]. Retardation effect is not taken into account for the power integrity applications studied here, as the structures are small compared to a wavelength.

2.3. PMSR METHOD

The Physics-based Model Size Reduction (PMSR) method aims to reduce a conventional PEEC model into a macromodel such that key electro-physical characteristics can be represented with a relatively simple circuit structure [1]. PMSR starts with a complex PEEC model solution that is effective up to the highest frequency of interest. Based on the geometry, nodes are selected within the original PEEC model which will remain in the reduced model. Lumped RLGC elements will be estimated at or between these nodes from the original model. Once the PMSR model is obtained, all the non-parasitic lumped elements (not associated with the PEEC model) are added to the circuit to form the "final" model. The connectivity matrix, $\mathbf{A}_r$, for a reduced equivalent circuit is defined. Calculation of reduced RLC circuit matrices are performed separately.

2.3.1. Resistance and Inductance Matrices Reduction. As mentioned above, reduction is based on the original PEEC model. Equation (2) shows the general form of the MNA for impedance formulation with only current sources.

$$\begin{bmatrix} s\mathbf{C} & \mathbf{A} \\ \mathbf{A}^T & -(s\mathbf{L}+\mathbf{R}) \end{bmatrix} \begin{bmatrix} \Phi_p \\ \mathbf{I}_L \end{bmatrix} = \mathbf{B} \begin{bmatrix} \mathbf{I}_{in} \\ 0 \end{bmatrix} \tag{2}$$

where $\mathbf{C}$, $\mathbf{L}$ and $\mathbf{R}$ matrices contain capacitive, inductive and resistive elements respectively which are calculated based on PEEC formulation; $\mathbf{A}$ is the connectivity matrix with relation between nodes and branches; Φ_p are unknown nodal potentials; $\mathbf{I}_L$ are unknown branch currents; $\mathbf{B}$ is an input selector matrix; $\mathbf{I}_{in}$ is the known input current source vector matrix; $s = 2\pi f$ in frequency domain.

Based on (3), (4) and (5), equation (2) can be expressed as (6).

$$\begin{bmatrix} s\mathbf{C} & \mathbf{A} \\ \mathbf{A}^T & -(s\mathbf{L}+\mathbf{R}) \end{bmatrix} \equiv s\mathbf{C}+\mathbf{G} \tag{3}$$

$$\begin{bmatrix} \Phi_p \\ \mathbf{I}_L \end{bmatrix} \equiv \mathbf{X}(s) \tag{4}$$

$$\begin{bmatrix} \mathbf{I}_{in} \\ \mathbf{0} \end{bmatrix} \equiv \mathbf{X}_{in}(s) \tag{5}$$

$$(s\mathbf{C}+\mathbf{G})\mathbf{X}(s) = \mathbf{B}\mathbf{X}_{in}(s) \tag{6}$$

The port impedance of (6), looking from known current source locations, can be found using (7).

$$\mathbf{Z}_{port} = \mathbf{B}^T(s\mathbf{C}+\mathbf{G})^{-1}\mathbf{B} \tag{7}$$

The general form of the MNA for the reduced circuit is shown in (8), with the assumption that the capacitance matrix equals to zero ($s\mathbf{C}=0$).

$$\begin{bmatrix} 0 & \mathbf{A}_r \\ \mathbf{A}_r{}^T & -(s\mathbf{L}_r+\mathbf{R}_r) \end{bmatrix} \begin{bmatrix} \Phi_{pr} \\ \mathbf{I}_{Lr} \end{bmatrix} = \begin{bmatrix} \mathbf{I}_{in} \\ 0 \end{bmatrix} \tag{8}$$

Equation (8) can be rewritten as a set of linear equations as shown in (9).

$$\begin{cases} \mathbf{A}_r\mathbf{I}_{Lr} = \mathbf{I}_{in} \\ \mathbf{A}_r{}^T\Phi_{pr} - (s\mathbf{L}_r+\mathbf{R}_r)\mathbf{I}_{Lr} = \mathbf{I}_{in} \end{cases} \tag{9}$$

Multiplying $\mathbf{A}_r{}^T$ to both sides in the first equation in (9) yields (10).

$$\mathbf{A}_r{}^T\mathbf{A}_r\mathbf{I}_{Lr} = \mathbf{A}_r{}^T\mathbf{I}_{in} \tag{10}$$

$\mathbf{I}_{Lr}$ can be found from (10) and is expressed as in (11), with the assumption that the inverse of $\mathbf{A}_r^T\mathbf{A}_r$ exists.

$$\mathbf{I}_{Lr} = (\mathbf{A}_r^T\mathbf{A}_r)^{-1}\mathbf{A}_r^T\mathbf{I}_{in} \tag{11}$$

By substituting (11) into the second equation of (9), equation (12) is obtained.

$$\mathbf{A}_r^T\Phi_{pr} - (s\mathbf{L}_r + \mathbf{R}_r)(\mathbf{A}_r^T\mathbf{A}_r)^{-1}\mathbf{A}_r^T\mathbf{I}_{in} = \mathbf{I}_{in} \tag{12}$$

Equation (12) is rewritten for unknown nodal voltages, which is equal to the product of the impedance and the source current in (13).

$$\mathbf{A}_r^T\Phi_{pr} = (s\mathbf{L}_r + \mathbf{R}_r)(\mathbf{A}_r^T\mathbf{A}_r)^{-1}\mathbf{A}_r^T\mathbf{I}_{in} \tag{13}$$

The main idea under the PMSR method is that the reduced model voltages at the ports are the same as the PEEC original model (Φ_{pr} and Φ_p). Thus (13) is equal to the port impedance of the original PEEC model and can be expressed as (14).

$$\mathbf{A}_r^T\Phi_{pr} = (s\mathbf{L}_r + \mathbf{R}_r)(\mathbf{A}_r^T\mathbf{A}_r)^{-1}\mathbf{A}_r^T\mathbf{I}_{in} = \mathbf{A}_r^T\mathbf{Z}_{port}\mathbf{I}_{in} \tag{14}$$

From (14), it can be shown that port impedances of the reduced and original models are equal to each other as in (15).

$$\mathbf{Z}_{port} = (s\mathbf{L}_r + \mathbf{R}_r)(\mathbf{A}_r^T\mathbf{A}_r)^{-1} \tag{15}$$

Reduced circuit inductance and impedance matrixes are determined from (15) and are shown in (16).

$$s\mathbf{L}_r + \mathbf{R}_r = \mathbf{A}_r^T\mathbf{Z}_{port}\mathbf{A}_r = \mathbf{A}_r^T\mathbf{B}^T(s\mathbf{C} + \mathbf{G})^{-1}\mathbf{B}\mathbf{A}_r \tag{16}$$

The PMSR inductance matrix reduction is based on the assumptions that the capacitance in the system is equal to zero, or is negligible and port impedances before and after the reduction models are equal.

2.3.1.1 The reduced system nodes. The reduced system nodes remain in the reduced model from the original PEEC. By selecting several nodes for the equivalent circuit, the accuracy of the circuit behavior compared to the original circuit is decreased, especially at high frequencies. In [6] a limitation of the equivalent circuit representation is well described. One of the factors is that the electric circuit cannot describe a wave phenomena. Secondly, the equivalent circuit has an upper limit in the frequency domain for which it is accurate. For some applications, however, capturing the high frequency behavior may not be required.

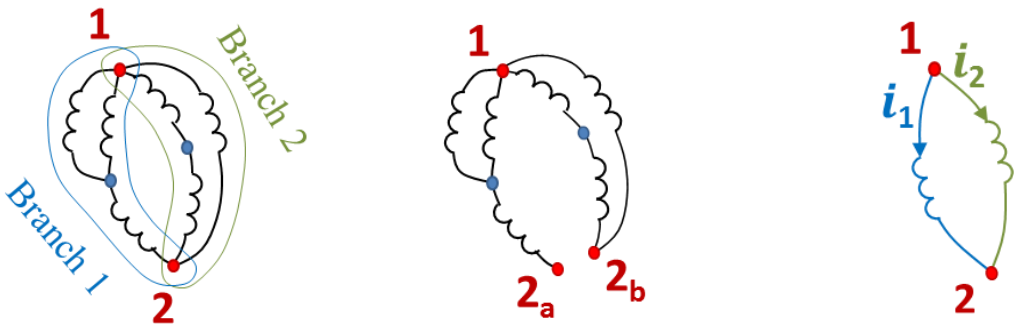
The location and number of reduced system nodes are decided by the user according to the desired equivalent circuit model. For example, reduced system nodes are placed where lumped elements and ports are located. In the case when an inductive effect dominates, the reduced system nodes should be placed along the current path.

2.3.1.2 Breaking the loop. The reduction technique is about finding the port impedance between two selected system nodes, which is defined by the potential difference between the points divided by the current. In case there are two current paths between the two reduced system nodes in the reduced model (Figure 2.4 a), $\mathbf{A}_r^T \mathbf{A}_r$ is not invertible. The reduced connectivity matrix $\mathbf{A}_r$ is singular, because its columns are linearly dependent on each another. In this situation, the PMSR technique provides a possibility to define equivalent partial inductance models for two current paths by breaking the loop.

The process of breaking the loop is to create temporary additional reduced system nodes, so that two inductive branches are independent and the current path between nodes in the intermediate model can only go through one set of independent branches (Figure 2.4 b). Breaking the loop makes $\mathbf{A}_r^T \mathbf{A}_r$ invertible. In the final stage, the inductive branches are reconnected again (Figure 2.4 c).

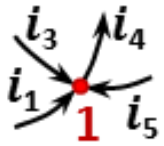
Breaking the loop in the MNA matrix is implemented in the following way. In the original connectivity $\mathbf{A}$ matrix (Figure 2.5) an additional row is created for the

temporary node. Branches connected to the original node are split between these two nodes (Figure 2.6).



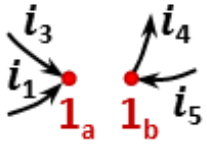
a) b) c)

Figure 2.4. a) Example of the part of the circuit where two current paths are defined between two reduced system nodes. b) Intermediate model with broken loop. c) The final reduced model with reconnected inductive branches



$$A = \begin{matrix} i_1 & i_2 & i_3 & i_4 & i_5 \end{matrix} \\ \begin{bmatrix} 1 & 0 & 1 & -1 & 1 \end{bmatrix}$$

Figure 2.5. Original connectivity A matrix



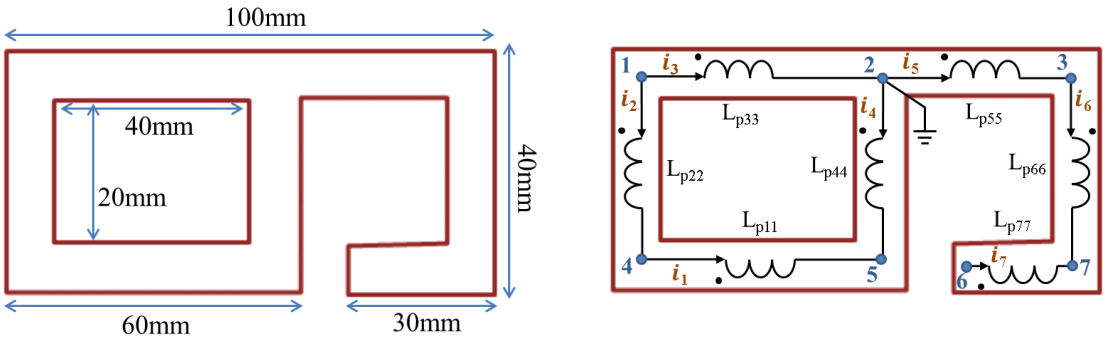
$$A = \begin{matrix} i_1 & i_2 & i_3 & i_4 & i_5 \end{matrix} \\ \begin{bmatrix} 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 \end{bmatrix}$$

Figure 2.6. Connectivity A matrix with additional temporary node

Breaking the loop is not always necessary. It is required only when more than one current path is defined between two reduced system nodes in the reduced model. In other cases, even with closed loops, breaking is not mandatory.

Breaking the loop is not only for making $\mathbf{A}_r^T\mathbf{A}_r$ invertible. It also gives physical meaning to the reduced model, which is the main objective of this technique.

The PMSR technique can be applied to a simple structure with both a closed and a semi closed layout as shown in Figure 2.7 a. This structure provides a good example of why breaking the loops is required for maintaining the physical insight into the system. First, the PEEC method is applied and the partial RLC elements are obtained. Figure 2.7 b shows the partial inductance circuit super imposed on the layout. Using PMSR technique the original circuit in Figure 2.8 a is simplified and reduced to an equivalent circuit as shown in Figure 2.8 b. Self and mutual inductance terms for the original circuit model are listed in Table 2.1.

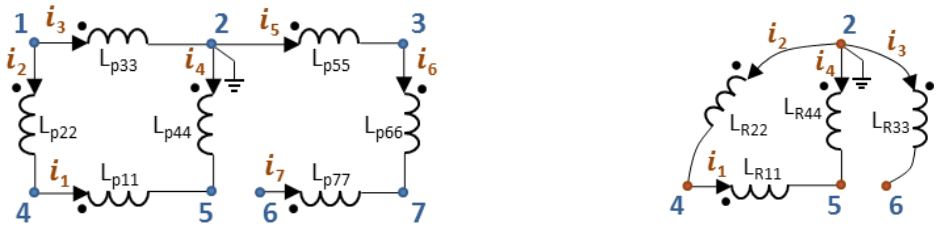


(a) (b)

Figure 2.7. a) Simple structure with a closed and a semi closed loop [1]; b) Partial inductance circuit super imposed on the layout

Nodes 2, 4, 5 and 6 of the original model are selected as reduced system nodes. In this case, breaking the loop is not necessary for reduction, because $\mathbf{A}_r^T\mathbf{A}_r$ is invertible. The reduced circuit elements without the intermediate breaking loop stage are listed in Table 2.2. For maintaining the physical insight to the reduced model, the original circuit

model should be broken at the # 4 reduced system node. In the original PEEC model, breaking the loop is done as shown in Figure 2.9. Branches are separated with additional temporary nodes, so that the two current paths are isolated from each other. The equivalent circuit elements when the loop is broken at reduced system node # 4 at the intermediate stage are listed in Table 2.3. For validation purposes, the original circuit can be analytically simplified to the reduced model as shown on Table 2.4.



(a) (b)

Figure 2.8. a) Original PEEC model; b) Reduced model

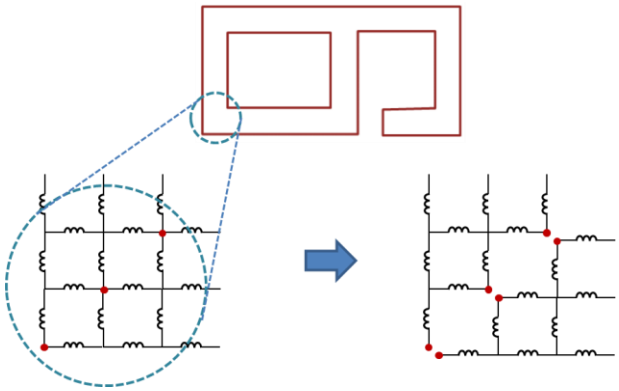


Figure 2.9. Breaking the loop based on the geometry

Regardless of whether the loop was broken, the total input impedance between node 5 and 6 are the same as shown in Table 2.5. However, the equivalent circuit

inductances are different. The values of inductance found analytically for the reduced model validates the correctness of the values obtained by first breaking the loop.

It should be noted that if node 2, 4 and 6 were selected as reduced system nodes, breaking the loop would be necessary regardless. This is so as the two current paths would have been defined between node 2 and node 4, thus $\mathbf{A}_r$ matrix is singular.

Table 2.1. Partial inductances of the original model in [nH]

L_{p11}	L_{p22}	L_{p33}	L_{p44}	L_{p55}	L_{p66}	L_{p77}
36.5	18.3	30.4	24.3	24.3	18.3	18.3

L_{p13}	L_{p15}	L_{p17}	L_{p24}	L_{p26}	L_{p35}	L_{p37}	L_{p46}	L_{p57}
6.5	3.9	3.8	2.3	0.9	4.2	2.1	2.8	2.8

Table 2.2. The reduced equivalent circuit inductances without breaking the loop in [nH]

L_{R11}	L_{R22}	L_{R33}	L_{R44}
26.7	31.4	55.1	19.0

L_{R12}	L_{R13}	L_{R14}	L_{R23}	L_{R24}	L_{R34}
-19.5	1.4	7.2	0.5	11.9	1.9

Table 2.3. The reduced equivalent circuit inductances with broken loop at node 4 in [nH]

L_{R11}	L_{R22}	L_{R33}	L_{R44}
36.5	48.7	55.3	24.3

L_{R12}	L_{R13}	L_{R14}	L_{R23}	L_{R24}	L_{R34}
-6.5	0.1	0	-1.2	2.3	2.8

Table 2.4. Analytically solved reduced model

Element	Equals to	Value [nH]
$\mathbf{L_{R11}}$	L_{p11}	36.5
$\mathbf{L_{R22}}$	$L_{p22} + L_{p33}$	48.7
$\mathbf{L_{R33}}$	$L_{p55} + L_{p66} + L_{p77} - 2L_{p57}$	55.3
$\mathbf{L_{R44}}$	L_{p44}	24.3
$\mathbf{L_{R12}}$	$-L_{p13}$	-6.3
$\mathbf{L_{R13}}$	$L_{p15}-L_{p17}$	0.1
$\mathbf{L_{R14}}$	0	0
$\mathbf{L_{R23}}$	$L_{p26} - L_{p35} + L_{p37}$	-1.2
$\mathbf{L_{R24}}$	L_{p24}	2.3
$\mathbf{L_{R34}}$	L_{p46}	2.8

Table 2.5. Equivalent loop inductance between node 5 and 6

Before Reduction	Reduced circuit with broken loop	Reduced circuit without breaking the loop
36.08 nH	36.08 nH	36.08 nH

2.3.2. Capacitance Matrix Reduction. For capacitance model reduction, it is proposed that capacitive cells can be grouped around the reduced system nodes – the same reduced system nodes that are used for inductance model reduction [1]. Reduction is done by assuming that the group member nodes have the same potential. The groups around the reduced system nodes are formed based on the voltage distribution over the geometry.

For illustration, the voltage distribution over a metal plate was calculated using a complete PEEC model as shown in Figure 2.10. Four groups around four reduced system nodes are generated and color coded in Figure 2.11.

Capacitive groups grow around reduced system nodes. Reduction is done by mapping the same potential within a group in the following way:

- Voltage distribution for a chosen frequency is calculated based on the original PEEC model.
- A neighboring nodes of the reduced system nodes are found from connectivity A matrix
- The neighboring node with voltage V_{node} is considered a part of group of reduced system node with V_{base} value, if condition (17) is satisfied.

$$\left| \frac{V_{node} - V_{base}}{V_{base}} \right| < \varepsilon_{tol} \tag{17}$$

where V_{node} is nodal voltage of the neighboring node of the reduced system node where nodal voltage is V_{base} and ε_{tol} is tolerance.

- Groups spread simultaneously until all cells belong to a group.

Considering a simple test case with n capacitive cells and dividing them into two groups with the same potential each, the relation between potentials and charges are expressed in (18).

$$\begin{cases} c_{s11}\Phi_1 + c_{s12}\Phi_2 + \ldots + c_{s1n/2}\Phi_{n/2} + \ldots + c_{s1n}\Phi_n = q_1 \\ c_{s21}\Phi_1 + c_{s22}\Phi_2 + \ldots + c_{s2n/2}\Phi_{n/2} + \ldots + c_{s2n}\Phi_n = q_2 \\ \vdots \\ c_{sn1}\Phi_1 + c_{sn2}\Phi_2 + \ldots + c_{snn/2}\Phi_{n/2} + \ldots + c_{snn}\Phi_n = q_n \end{cases} \tag{18}$$

The same potential can be set to one half of the n cells and another potential to another half of the cells (in order to get two distinct groups), by assigning Φ' and Φ'' potentials to each group as in (19), (20).

$$\Phi_1 = \Phi_2 = \ldots = \Phi_{n/2} = \Phi' \tag{19}$$

$$\Phi_{n/2+1} = \Phi_{n/2+2} = \ldots = \Phi_n = \Phi'' \tag{20}$$

Considering assumptions (19) and (20) the system in (18) can be rewritten as (21).

$$\begin{cases} \sum_{i=1}^{n/2}\sum_{j=1}^{n/2} c_{ij}\Phi' + \sum_{i=1}^{n/2}\sum_{j=n/2+1}^{n} c_{ij}\Phi'' = \sum_{k=1}^{n/2} q_k \\ \sum_{i=n/2+1}^{n}\sum_{j=1}^{n/2} c_{ij}\Phi' + \sum_{i=n/2+1}^{n}\sum_{j=n/2+1}^{n} c_{ij}\Phi'' = \sum_{k=n/2+1}^{n} q_k \end{cases} \quad (21)$$

The resulting reduced capacitance matrix consists of two self and two mutual capacitances expressed in equation (21).

$$\begin{cases} \sum_{i=1}^{n/2}\sum_{j=1}^{n/2} c_{ij} & \sum_{i=1}^{n/2}\sum_{j=n/2+1}^{n} c_{ij} \\ \sum_{i=n/2+1}^{n}\sum_{j=1}^{n/2} c_{ij} & \sum_{i=n/2+1}^{n}\sum_{j=n/2+1}^{n} c_{ij} \end{cases} \quad (22)$$

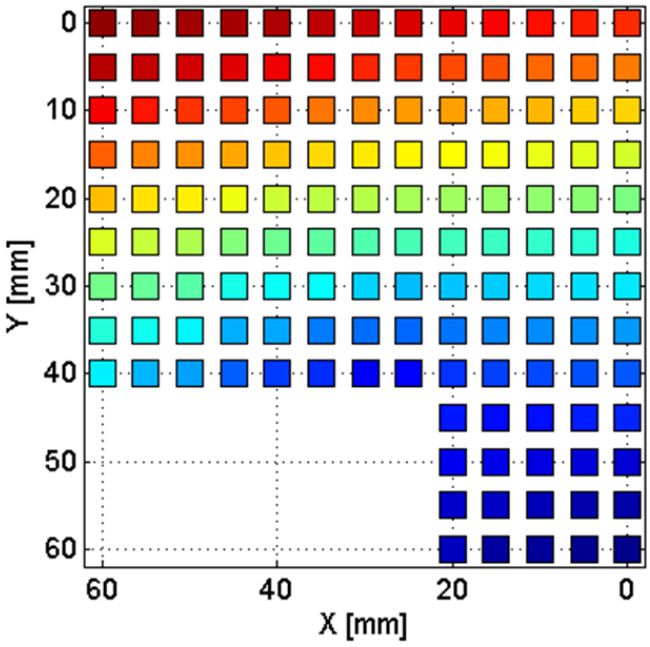


Figure 2.10. Voltage distribution over metal plate

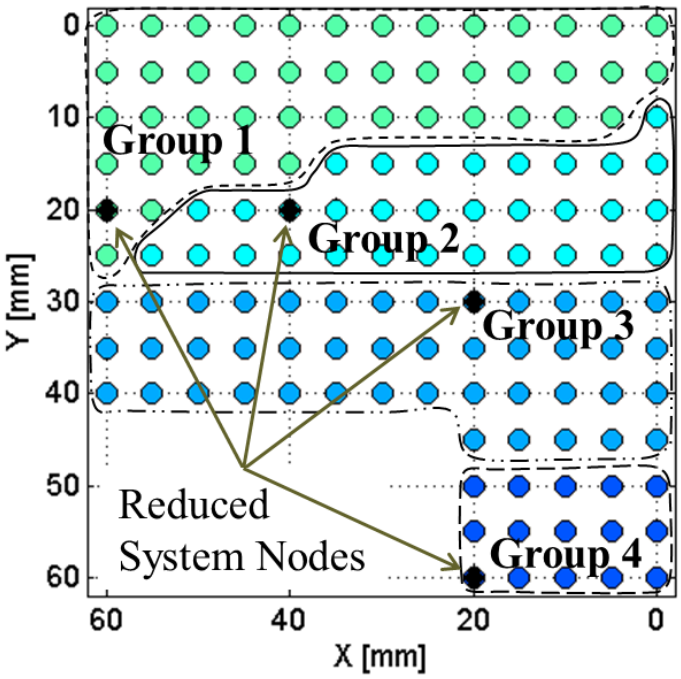


Figure 2.11. Capacitance grouping example based on voltage distribution

The same approach is used for more than two groups. Using such a grouping method, the capacitance model is significantly reduced while preserving the relation between elements in the reduced model and geometry. Using this grouping approach a reduced model for capacitance is obtained.

It should be noted that capacitance groups are based on voltage distribution, which changes with a change in the frequency. Thus capacitance groups are highly dependent on the selected frequency; here it is referred as a reduction frequency. An example of two parallel plates is investigated as shown in Figure 2.12.

The input impedance looking from the current source is analyzed. Reduction is tested for three different reduction frequencies. Impedance before and after reduction are compared from frequencies of 10 MHz up to 1 GHz as shown in Figure 2.13, for different reduction frequencies used to group the capacitances.

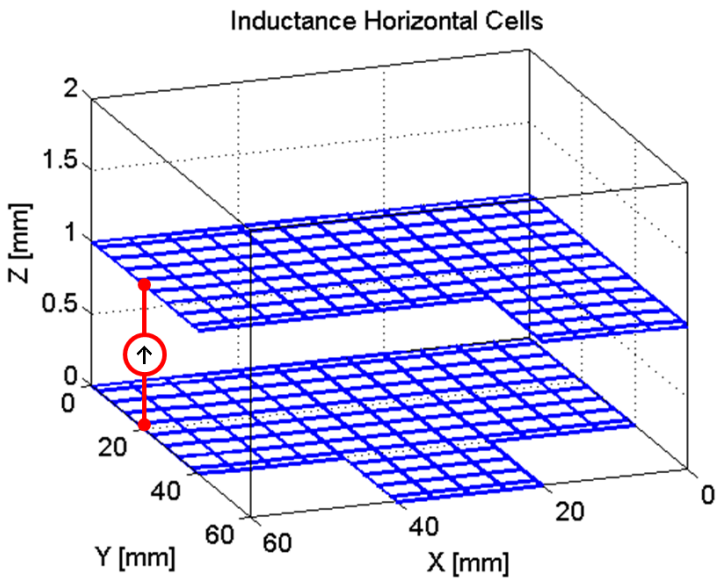


Figure 2.12. PEEC inductance horizontal cells of the test geometry with two parallel plates

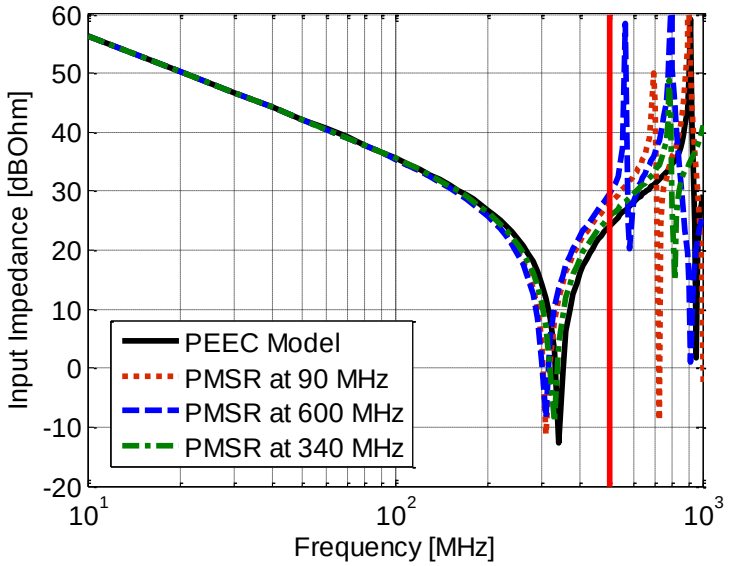


Figure 2.13. Input impedance before and after reduction of the test geometry. The cutoff frequency is shown with a red line

According to Figure 2.13, the reduced model shows good accuracy until 500 MHz if the capacitance reduction is performed at structure resonant frequency. Projectional groups are created at the resonance frequency – that is, where the geometry of groups on the top plate match the geometry of groups on the bottom plate. This grouping is due to a standing wave in the structure. At the resonance frequency, a similar voltage distribution appears on the upper and lower conductors. It is recommended to use system resonance frequency for obtaining projectional capacitance groups.

One important feature of the grouping method is that the resulting capacitances are "real", in the sense that the self-capacitances in the reduced model is positive so long as the self-capacitances in the original model are positive. Using a fine mesh improves the likelihood that the capacitances are positive, and thus are physically meaningful. Using a course mesh to generate the original model (perhaps in an attempt to keep the original model simple) may result in negative capacitance values, which detracts from the usefulness of the model.

2.4. L ABOVE INDUCTANCE CALCULATION USING PMSR METHOD

In this section, the PMSR method is used to obtain an equivalent circuit for different designs of decoupling capacitor connection methods. As mentioned earlier, L_{above} refers to the total equivalent inductance above the top GND plane, including the capacitor parasitic inductance, trace inductance, and pad and via inductances. The objective of this work is to better understand and improve methods of placing decoupling capacitors. Here the capacitor internal inductance is ignored as this does not have an effect on the design of the connection. Including the capacitor's internal inductance will increase the overall inductance value in the system, but the trend with and without this internal inductance will remain the same.

In article [13], circuit macromodels for decoupling capacitors including the local environment were constructed. It is shown that a decoupling capacitor model is highly influenced by the connections and other mounting details, such as the distance to the nearest ground plane. To keep the computational time reasonably low, a simplified 3 layer 0402 capacitor model shown in Figure 2.14 is studied.

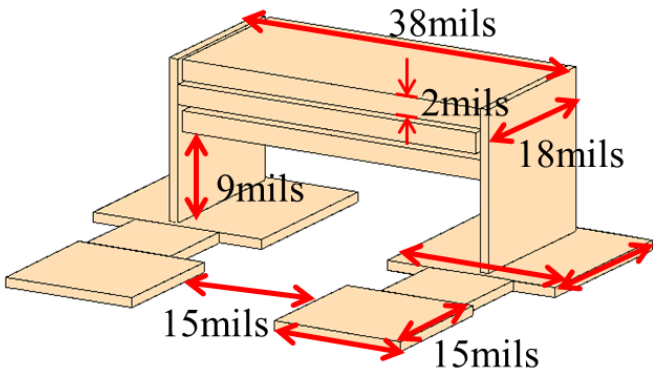


Figure 2.14. The simplified 3 layer 0402 capacitor model with traces and pads

The impact of the ground plane under the capacitor macromodel is analyzed using the full-wave PEEC tool. It was observed that the total inductance which includes the pad, trace and internal capacitor inductances are influenced by the ground plane. These values are listed in the Table 2.6.

Table 2.6. Comparison of macromodel inductances of 0402 capacitor model

Model Details	Spacing to ground	Total Inductance
PEEC model with ground plane	5 mils	340 pH
PEEC model with ground plane	30 mils	390 pH
PEEC model without ground under capacitor	∞	570 pH

2.4.1. Shared Via Design. One of the ways of placing two decoupling capacitors is using shared vias is shown on Figure 2.15. Decoupling capacitors are often referred to as decaps. Here they are placed 0.1702 mm above the reference plane.

Power and ground vias with drill sizes of 0.254 mm, pad dimeters of 0.538 mm and anti-pad diameters of 0.762 mm, connect traces to the reference plane. Decoupling capacitors are shorted with a 1.25x2.52 mm Perfect Electric Conductor (PEC) plate. Design

dimensions are defined for 0805 package size capacitors in Figure 2.15. Shared via configuration top and side views are shown in Figure 2.15 and Figure 2.16 respectively.

The shared via design was modeled using quasi-static PEEC tool using the Free Space Green's Function. Due to PEEC tool limitations of solving cylindrical shape geometries, analytical expressions (23) and (24) are used for via partial self and mutual inductance calculations respectively [14]:

$$L_{p11,via} \approx \frac{\mu_0 l}{2\pi}\left(\ln\left[\frac{l}{a}+\sqrt{1+\left(\frac{l}{a}\right)^2}\right]+\frac{a}{l}-\sqrt{1+\left(\frac{a}{l}\right)^2}\right) \tag{23}$$

$$L_{p12,via} \approx \frac{\mu_0 l}{2\pi}\left(\ln\left[\frac{l}{S}+\sqrt{1+\left(\frac{l}{S}\right)^2}\right]+\frac{S}{l}-\sqrt{1+\left(\frac{S}{l}\right)^2}\right) \tag{24}$$

where l is length of the a radius drill size via and S is separation between two vias.

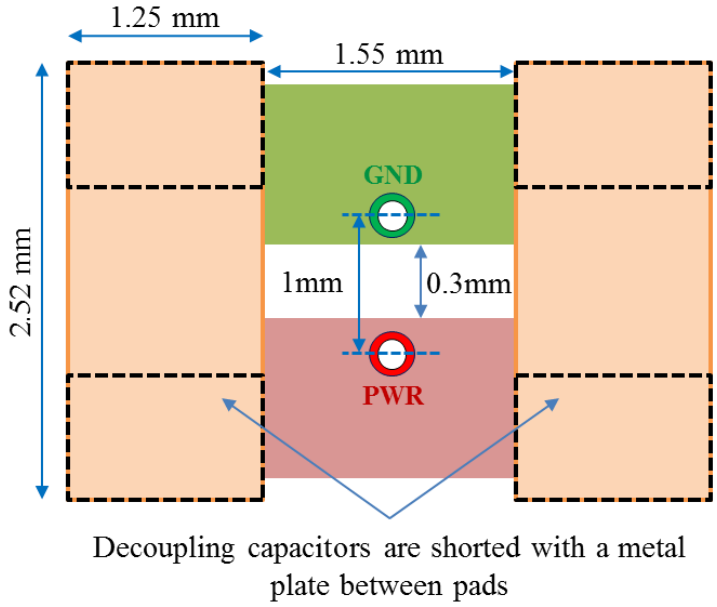


Figure 2.15. Top view of the shared via decoupling capacitors connection method. The decoupling capacitor was modeled as a metal plate

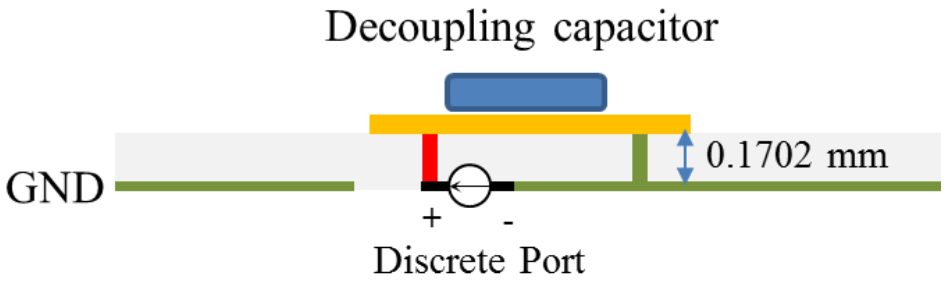
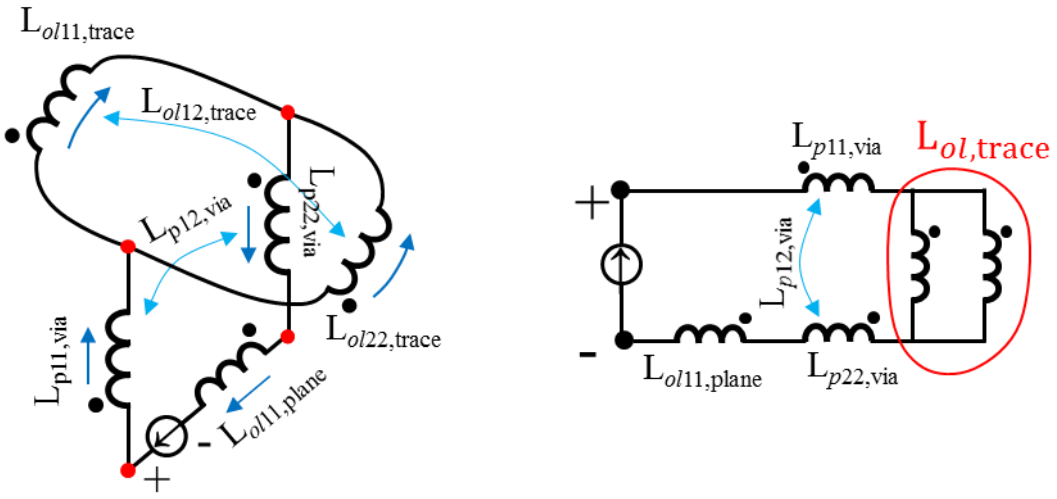


Figure 2.16. Side view of the shared via decoupling capacitors connection method

PEEC model was reduced to an equivalent simplified circuit model using the PMSR technique as shown in Figure 2.17 a. In Figure 2.17 b the circuit diagram of the equivalent model is presented in an intuitive way. It should be noted that the equivalent model is strongly related to the geometry of the structure as shown in Figure 2.18.



a) b)

Figure 2.17. a) Physics-based reduced equivalent circuit for the shared via design; b) Circuit diagram for the shared via design

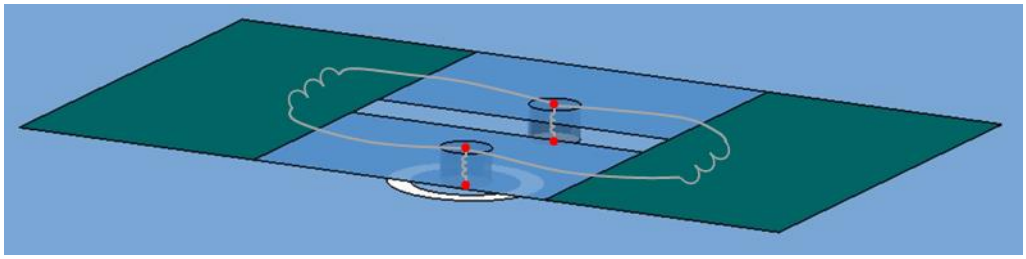


Figure 2.18. Equivalent model super imposed on the shared via geometry

All the self and mutual open loop inductances of the simplified circuit using the PMSR technique are listed in Table 2.7. After solving the reduced model using MNA, the input impedance was obtained by dividing the voltage difference at the port points by the value of the source current. Equivalent inductance can be extracted from the impedance curve using (25).

$$L = \left| \frac{Z}{j2\pi f} \right| \tag{25}$$

where Z is the input impedance in ohms at f frequency in Hz.

For equivalent circuit validation, the L_{above} for the circuit (Figure 2.17 b) can be analytically found using (26) and (27).

$$L_{ol,trace} = \frac{L_{ol11,trace} L_{ol22,trace} - L_{ol12,trace}^2}{L_{ol11,trace} + L_{ol22,trace} - 2L_{ol12,trace}^2} \tag{26}$$

$$L_{above} \approx L_{p11,via} + L_{p22,via} + 2L_{p12,via} + L_{ol,trace} + L_{ol11,plane} + L_{ol12,PlanetoTrace} \tag{27}$$

Commercial full wave simulation tools cannot generate equivalent circuit elements as shown in Figure 2.17 a. For validation purposes, the total equivalent inductance of the system was extracted from the input impedance and compared.

EMCoS EMC Studio was used for PMSR validation. EMC Studio is a powerful program package for EMC/EMI problem analysis. It is based on Method of Moments (MoM) approach [11].

The input impedance of the system obtained from the PEEC method, from EMC Studio, and from the PMSR circuit reduction are compared in Figure 2.19. The values of L_{above} inductance extracted from the impedance curves are listed in Table 2.8.

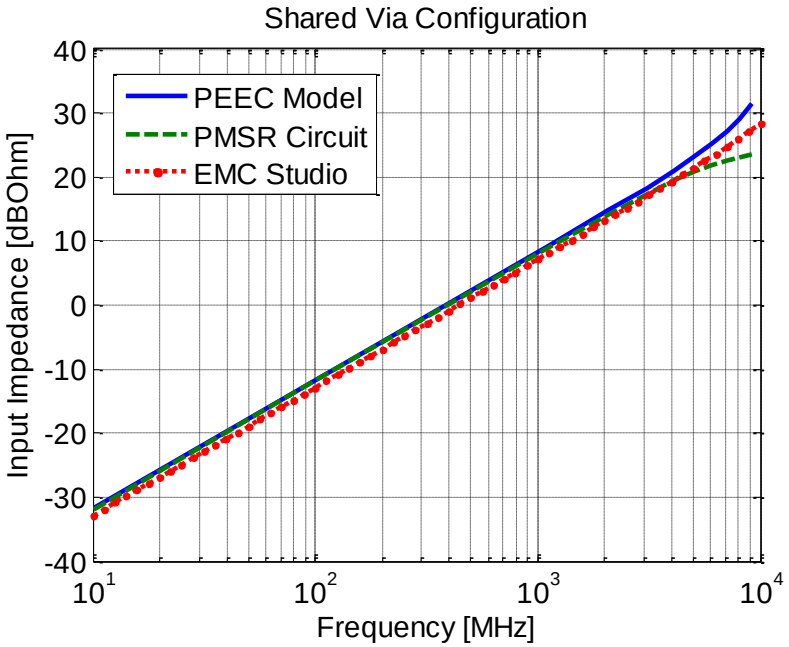


Figure 2.19. The input impedance vs. frequency for a shared via geometry

The difference between EMC Studio simulations and PEEC result is about 11%. In the PEEC model, the via is approximated as a wire and an analytical formula is applied. In case when vias are closed to each other, the current distribution over the surface is not uniform anymore. Thus approximating the vias as a wire results in this small discrepancy between the PEEC and EMC Studio results. Based on this assumption, this difference may be acceptable.

Table 2.7. Self and mutual open loop inductances of the simplified circuit obtained using PMSR method for a shared via geometry

$L_{p11,via}$	$L_{p22,via}$	$L_{p12,via}$	$L_{ol11,trace}$	$L_{ol22,trace}$	$L_{ol12,trace}$	$L_{ol11,plane}$	$L_{ol12,PlanetoTrace}$
20 pH	20 pH	2.9 pH	621 pH	621 pH	6.4 pH	85 pH	21 pH

Table 2.8. L_{above} equivalent inductance for a shared via design

PEEC Model	PMSR Circuit	Analytical Solution from Reduced Model	EMC Studio
411 pH	406 pH	403 pH	361 pH

2.4.2. Doublet Design. The doublet configuration for mounting decoupling capacitors with alternating power/ground-reference vias was proposed in [12]. The authors suggest using the alternating doublet design which has the lowest effective L_{below} inductance. Here, the L_{above} of the doublet configuration is investigated. To compare with other designs, the same dimensions are used for the doublet design as was used for the shared via. The distance between the vias is maintained at 1 mm. Top and side views for the alternating doublet configuration are shown in Figure 2.20 and Figure 2.21 respectively.

Using the PMSR technique, the PEEC model was reduced to an equivalent simplified circuit model as shown in Figure 2.22. In Figure 2.23 the circuit diagram of the equivalent model is presented in an intuitive way. The equivalent model is intuitively related to the geometry of the structure as shown in Figure 2.24.

The self and mutual open loop inductances generated using the PMSR technique on the simplified circuit are listed in Table 2.9.

To validate the equivalent circuit, L_{above} for the circuit (Figure 2.23) can be found analytically using (28), (29) and (30). For simplicity, plane inductances have been neglected in (28), (29) and (30).

$$L_{ol,PG1} \approx L_{ol11,via} + L_{ol22,via} + 2L_{ol12,via} + L_{ol11,trace} \tag{28}$$

$$L_{ol,PG2} \approx L_{ol33,via} + L_{ol44,via} + 2L_{ol34,via} + L_{ol22,trace} \tag{29}$$

$$L_{above} \approx \frac{L_{ol,PG1}L_{ol,PG2} - L_{ol12,trace}^2}{L_{ol,PG1} + L_{ol,PG2} - 2L_{ol12,trace}} \tag{30}$$

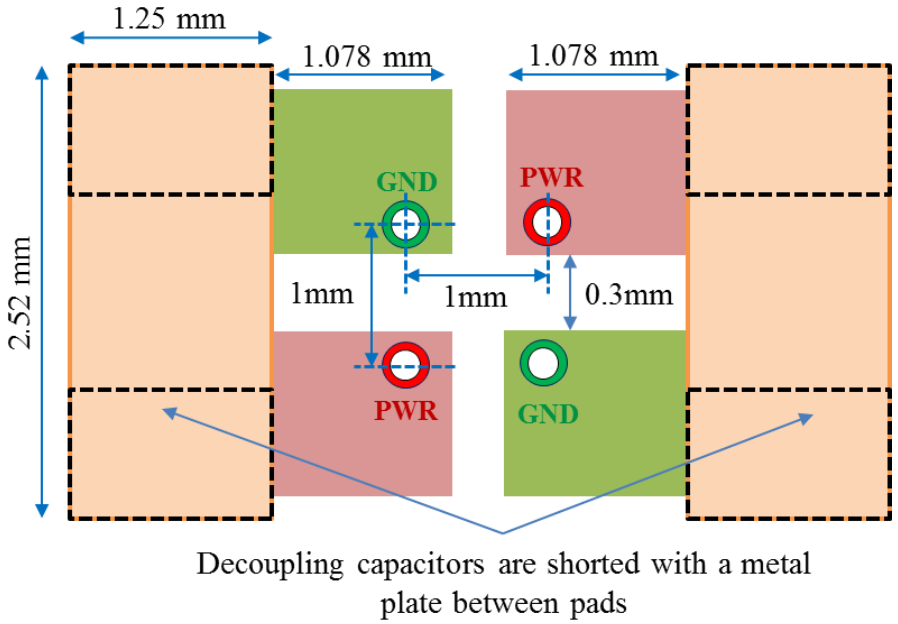


Figure 2.20. Top view of the doublet decoupling capacitors connection method. The capacitor was modeled as a metal plate

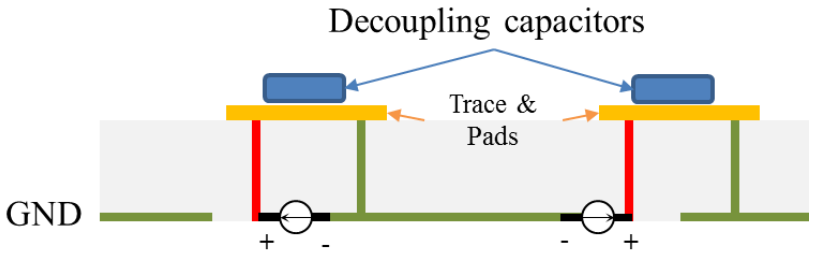


Figure 2.21. Side view of doublet decoupling capacitors connection method

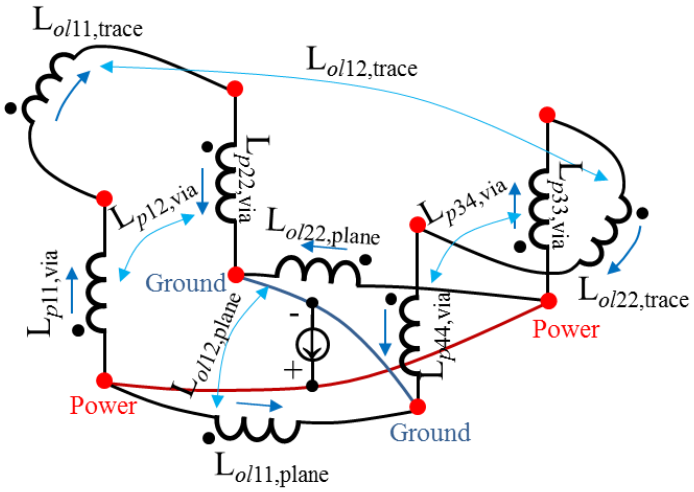


Figure 2.22. Reduced equivalent circuit for the doublet design

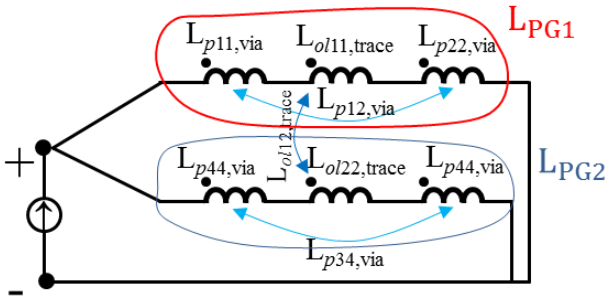


Figure 2.23. Circuit diagram for the doublet design

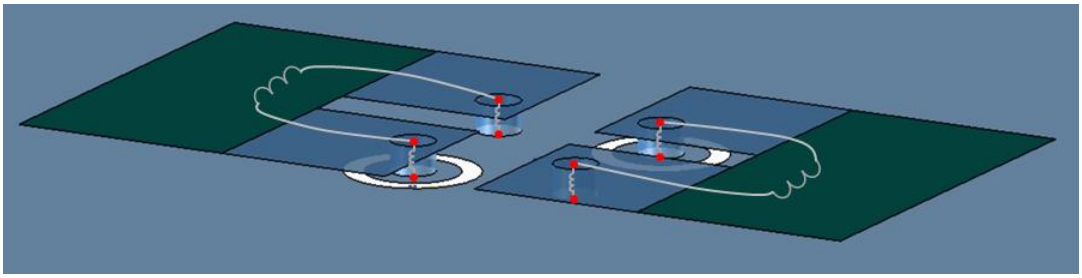


Figure 2.24. Equivalent model super imposed on the doublet geometry

L_{above} equivalent inductance of the system obtained from PEEC method, EMC Studio and PMSR circuit are listed in Table 2.10.

The values of L_{above} obtained from PEEC method, EMC Studio and PMSR are listed in Table 2.10. The difference between EMC Studio and PEEC is 12%. This difference is again related to the via model assumption and is within the acceptable range. Additional inductance is added in the EMC Studio model as lumped port is defined on a 1 mm long wire segment in order to excite both power vias at the same time. We cannot avoid wire inductance, but we can make it small as compared to the system inductance by increasing the wire diameter. Analytical solution for the reduced circuit using (28), (29) and (30) is 7% lower than the PMSR solution because plane inductances are neglected.

Table 2.9. Self and mutual open loop inductances of the simplified circuit obtained using PMSR method for the doublet design

$L_{p11,via}$	$L_{p22,via}$	$L_{p33,via}$	$L_{p44,via}$
20 pH	20 pH	20 pH	20 pH

$L_{p12,via}$	$L_{p13,via}$	$L_{p14,via}$	$L_{p23,via}$	$L_{p24,via}$	$L_{p34,via}$
2.9 pH	2.0 pH	2.9 pH	2.9 pH	2.0 pH	2.9 pH

$L_{ol11,trace}$	$L_{ol22,trace}$	$L_{ol12,trace}$
335pH	335 pH	28 pH

Table 2.10. L_{above} equivalent inductance for the doublet design

PEEC Model	PMSR Circuit	Analytical Solution from Reduced Model	EMC Studio
218 pH	218 pH	205 pH	244 pH

2.4.3. Shared Pad Design. The third proposed connection method for connecting two decoupling capacitors is when they are sharing big pads. The geometry of the two capacitors mounted on the shared pad is shown in Figure 2.25. For consistency with other designs, similar dimensions are used for this shared pad design.

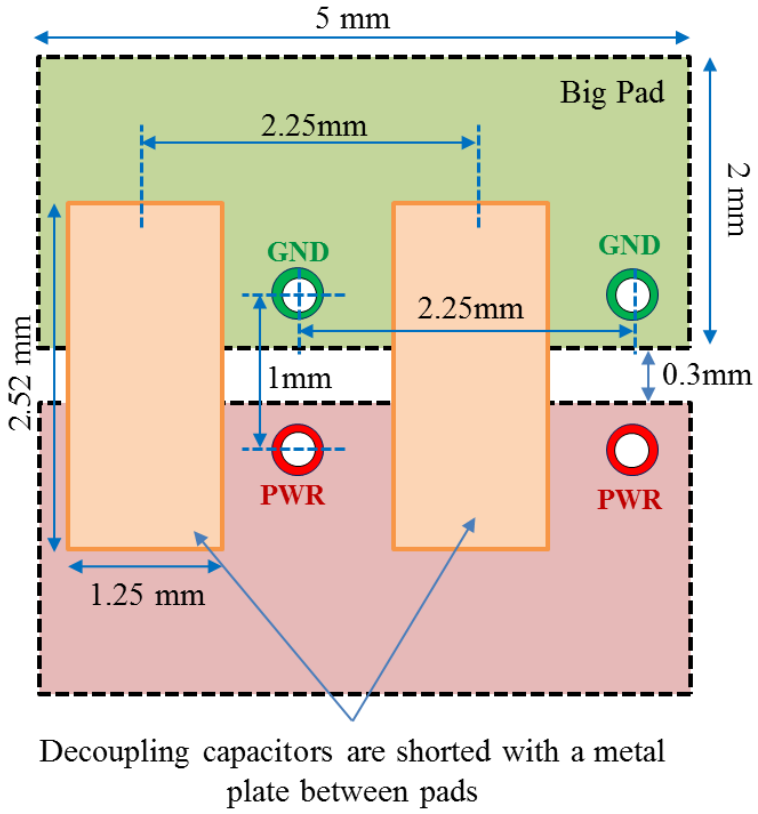


Figure 2.25. Top view of the shared pad decoupling capacitors connection method

Using the PMSR technique, the PEEC model was reduced to the equivalent simplified circuit model shown in Figure 2.26. In Figure 2.27 the circuit diagram of the equivalent model is presented in an intuitive way. The equivalent model is intuitively related to the geometry of the structure as shown in Figure 2.28.

The self and mutual open loop inductances of the simplified circuit using PMSR technique are listed in Table 2.11.

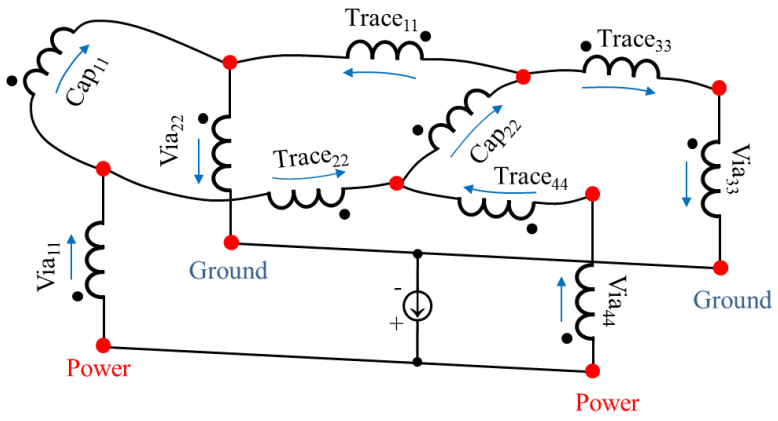


Figure 2.26. Reduced equivalent circuit for the shared pad design

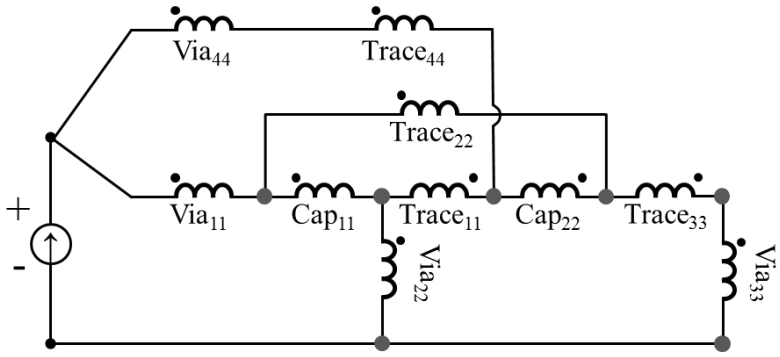


Figure 2.27. Circuit diagram for the shared pad design

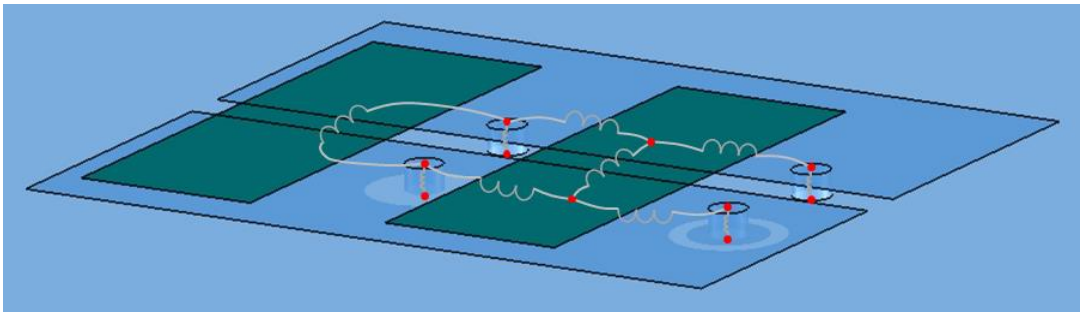


Figure 2.28. Equivalent model super imposed on the shared pad geometry

The L_{above} equivalent inductance of the system obtained from PEEC method, EMC Studio, and PMSR are listed in Table 2.12. The difference between the EMC Studio simulation and PEEC result is 9%.

Table 2.11. Self and mutual open loop inductances of the simplified circuit obtained using PMSR method for the shared pad design

$L_{p11,via}$	$L_{p22,via}$	$L_{p33,via}$	$L_{p44,via}$
20 pH	20 pH	20 pH	20 pH

$L_{p12,via}$	$L_{p13,via}$	$L_{p14,via}$	$L_{p23,via}$	$L_{p24,via}$	$L_{p34,via}$
2.9 pH	1.3 pH	1.2 pH	1.3 pH	1.2 pH	2.9 pH

$L_{ol11,cap}$	$L_{ol22,cap}$	$L_{ol11,trace}$	$L_{ol22,trace}$	$L_{ol33,trace}$	$L_{ol44,trace}$
248 pH	210 pH	246 pH	212 pH	314 pH	225 pH

Table 2.12. L_{above} equivalent inductance for the shared pad design

PEEC Model	PMSR Circuit	EMC Studio
178 pH	179 pH	197 pH

2.5. CONCLUSION

PMSR method enables one to create simple lumped element circuit models from complex PEEC models. These models reflect the physics of the system and hence have good correlation with the geometry of the structure. Generating physics based models which are tightly correlated to the geometry is the core idea of the PMSR method. The PMSR method was applied to three decoupling capacitor connection methods. According to the equivalent circuit model of the shared via design it can be observed that the total open loop inductance of the traces and pads, L_{trace}, is increased due to mutual inductance

as the current direction is the same through the $L_{11,trace}$ and $L_{22,trace}$. In the shared via design, the via and trace inductances are in series which add up resulting in a higher equivalent inductance. However, for the doublet design, two power/ground loops are summed up as a series inductance and then treated as a parallel loop inductance. Parallel connection here reduces the total equivalent inductance significantly as compared to the shared via design which is connected in series. Based on the derived partial inductance parameters, it was shown that the shared pad design was most effective at reducing the connection inductance. The shared pad design yields the least equivalent inductance as compared to the doublet or shared via design. Complex analytical solution for the shared pad design can be obtained using a Y to Δ or Δ to Y conversion for equivalent impedance calculations. Due to multiple such conversions, the intuitive representation of the physics is lost. However, once the simplified model is obtained, by using spice solvers one can arbitrarily change the partial element quantities and observe the impact on the input impedance. By identifying the partial elements which have the most significant impact on the input impedance, these can be related back to the dominant part of the geometry.

Based on the equivalent circuit of the doublet design, it can be noted that the mutual open loop inductance between two trace loops is small as compared to the self open loop inductance. Thus partial and open loop inductances of the via and trace do not have much effect on the equivalent inductance. It is expected that by increasing distance between the vias (with same trace length) will have no significant impact on the equivalent inductance. However, making this change effects the L_{below} equivalent inductance. As a design guideline for reducing equivalent inductance of the system, traces and pads should be as wide and as close to each other restricted only by the manufacturing process. In this way self inductance of the traces and pads will decrease with increasing current flowing area.

The PMSR technique can be applied to any complex design structure and would enable us to obtain its equivalent physics based circuit model. In this study, the internal inductance of the capacitors was not taken into consideration. As a future study, these internal inductances (self and mutual between the different decoupling capacitors) can be added to the designs which would result in a more complex circuit model but with increased accuracy for determining L_{above}.

3. ALIEN CROSSTALK

3.1. INTRODUCTION

BroadR-Reach® is a point-to-point Ethernet Physical Layer (PHY) standard, which is used in automotive applications [15]. This technology allows full-duplex communication between two devices over a single, unshielded twisted pair cable. Systems with a BroadR-Reach® Ethernet PHY should meet automotive Electromagnetic Compatibility (EMC) requirements.

The BroadR-Reach® protocol realizes simultaneous transmit and receive operations through an unshielded twisted pair cable at 100Mb/s. In test applications, there is a bundle of 6 UTPs, making this a problem of one victim pair with 5 aggressors [16]. Alien crosstalk is generally present when cables are bundled together. Alien crosstalk is defined between more than one link segments. Alien noise may also consist of unknown sources outside the cabling that couple into the link segment via electric and magnetic fields. The self-crosstalk noise from the nearby duplex channel in the pair can be cancelled using digital signal processing techniques, whereas alien crosstalk from an alien connection cannot be cancelled in the same fashion. The transmitted signal from an alien crosstalk noise source is not available to the PHY of the disturbed duplex channel.

There is a lot of ongoing research regarding crosstalk analysis. Statistical models for hand-assembled cable bundles are investigated in [18] and [19]. Statistical single wire bundle model with cross-sectional analysis of RLGC parameters was developed. Spice based models were developed for each cross-section and the radiated field was predicted and validated with experiments. In [20], a T-network model for estimating the statistical crosstalk variation in cable bundles was proposed. The T-network method approximates the cable as cascaded segments of multi-conductor transmission lines, which results in fast calculation times as compared to SPICE analysis. These above mentioned references deal with cable bundles but do not discuss on the connector effects.

In order to determine the near-end coupling parameters, an experimental methodology based on VNA measurements was developed in [21]. An equivalent circuit model was created to predict the single-ended and differential crosstalk below 400 MHz. Using a closed-form expression it was shown that the coupling mainly occurs inside the

connector shell, as predicted by [24]. Equivalent low-frequency models with strong dominating inductive or capacitive coupling at the near-end have been proposed in [22]. The worst-case coupling scenarios with the dominant type of coupling were identified. As mentioned in [22], the same methodology cannot be applied to far-end crosstalk estimate, because inductive and capacitive coupling are out of phase and equally dominant at the far end.

Power Sum Near End Crosstalk (NEXT) and Far End Crosstalk (FEXT) measured for a 26 AWG and a 24 AWG twisted pair cable bundle was analyzed in [23] based on T1.417 standard. NEXT and FEXT coupling levels are compared for different number of cable bundle pairs.

All the listed work relates to the development of statistical cable bundle models or equivalent circuits for the coupling model at the near end. In this work effects of different brands of cable bundles with different lengths of untwisted region on near-end and far-end coupling is analyzed. One of the objectives of the work is to determine which one of two brands of cables has the best performance. The communication channel in physical layer of the BroadR-Reach® protocol consists of two inline connectors connecting three 5 m cable bundle segments. Performance of the full channel (with inline connectors) should meet standard limits. Adding a connector in the UTP means that a certain length of untwisted region will be added in the channel. Coupling in the untwisted region may result in a signal degradation and increase in crosstalk. Investigation of the maximum acceptable untwisted region is necessary.

3.2. ALIEN CROSSTALK

Near-End Crosstalk (NEXT) and Far-End Crosstalk (FEXT) concepts are conceptually different from Alien Near-End Crosstalk (ANEXT) and Alien Far End Crosstalk (AFEXT) respectively. NEXT and FEXT are defined within the link segment, whereas ANEXT and AFEXT are defined between more than one link segment as shown in Figure 3.1. The word alien represents an unknown source coupling into the link segment.

According to IEEE standard definition for Ethernet, a link segment is an electrical connection between networking devices using a shared medium. A duplex channel is a communication system for connecting two devices that can communicate with each other in both directions at the same time.

In BroadR-Reach® communication 100BASE-T1, one pair of unshielded twisted pair is used. Thus, there is no Near-End Crosstalk (NEXT) or Far End Crosstalk (FEXT) in the link segment because it consists of only one pair.

The self-crosstalk noise from the nearby duplex channel in the link segment can be cancelled using digital signal processing techniques, whereas the alien crosstalk from an alien connection cannot be cancelled in the same fashion. The transmitted signal from an alien crosstalk noise source is not available to the physical layer (PHY) of the disturbed duplex channel.

Since the transmitted signal from the alien noise source in one cable is not visible on the other cable, cancellation cannot be performed. When there are multiple pairs of UTP cables bundled together, where each pair carries a 100 Mb/s link, then each duplex link is disturbed by the neighboring links, degrading the signal quality in the victim pair. In the test application, a bundle of 6 UTPs, creates a “one victim, 5 aggressor” scenario as shown in Figure 3.2.

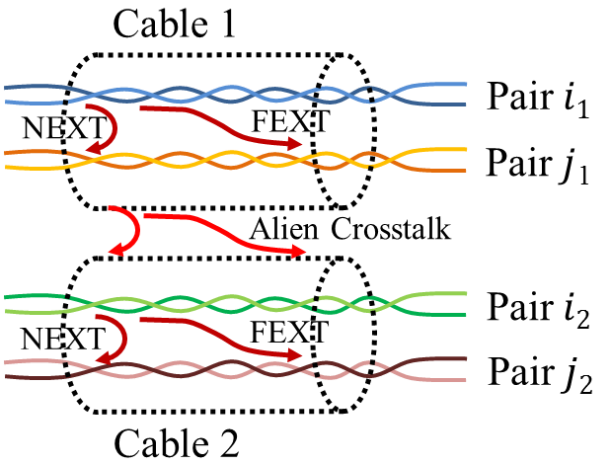


Figure 3.1. Crosstalk demonstration within and between link segments

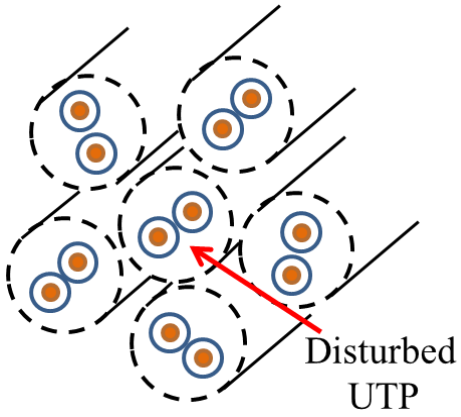


Figure 3.2. 5-around-1 UTP cable bundle

In order to limit the near end crosstalk noise for a 5-around-1 UTP cable bundle (up to 15 m cable length and two inline connectors, equally spaced at 5 meter and 10 meter distances), the Power Sum Alien Near-End Crosstalk (PSANEXT) loss should fulfil the condition (31) as defined in [15]:

$$PSANEXT_{dB} > 31.5 - 10\log_{10}\frac{f}{100} \tag{31}$$

where f is the frequency ranging from 1 MHz - 100 MHz.

Moreover, the Power Sum Alien Equal Level Far End (PSAELFEXT) for a 5-around-1 UTP cable bundle (up to 15 m length cable and two inline connectors, equally spaced at 5 meter and 10 meter distances) would follow equation (32) as defined in [15]:

$$PSAELFEXT_{dB} > 16.5 - 20\log_{10}\frac{f}{100} \tag{32}$$

where f is the frequency ranging from 1 MHz - 100 MHz.

The computation of PSAELFEXT is consistent with the computation of power sum alien attenuation to crosstalk ratio far end (PS AACR-F). The term PS AACR-F is

used in ISO/IEC TR 24750 and in the 1st amendment to the second edition of ISO/IEC 11801.

Power sum alien NEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT values. PSANEXT is defined between a link segments as in (33):

$$PSANEXT_n(f) = 10\log_{10}\sum_{j=1}^{m}\sum_{i=1}^{n}10^{\frac{-AN(f)i,j,N}{10}} \tag{33}$$

where $AN(f)i,j,N$ is the magnitude in dB of the alien NEXT loss at frequency f of the individual pair combination i (1 to n) of the disturbing link j (1 to m) for each disturbed pair N.

For calculating PSANEXT of one victim, the differential insertion loss, $S_{ij\mathbf{dd}}$, parameter between all aggressor pairs and victim pair between the link segments should be measured at the near-end.

Power sum alien ELFEXT is determined by summing the power of the individual pair-to-pair differential alien ELFEXT as shown in (34):

$$PSAELFEXT_n(f) = 10\log_{10}\sum_{j=1}^{m}\sum_{i=1}^{n}10^{\frac{-EL(f)i,j,N}{10}} \tag{34}$$

where $EL(f)i,j,N$ is determined using equation (35) as the magnitude in dB of the alien ELFEXT of the coupled length at frequency f of the individual pair combination i of the disturbing link j for each disturbed pair N corrected by subtracting the $10\log_{10}$ ratio of the disturbed length insertion loss to the coupled length insertion loss. The coupled length is the length of cabling over which the crosstalk coupling can occur.

$$EL(f)_{i,j,N} = AELFEXT(f)_{i,j,N} - 10\log_{10}\frac{DisturbedIL_N}{CoupledlengthIL(f)_{i,j,N}} \tag{35}$$

where $AELFEXT(f)_{i,j,N}$ is determined using equation (36) as the difference of the magnitude in dB of the Alien FEXT of the coupled length at frequency f of the individual pair combination i (1 to n) of the disturbing link j (1 to m) for each disturbed pair N and the insertion loss of the coupled length:

$$AELFEXT(f)_{i,j,N} = AFEXT(f)_{i,j,N} - CoupledlengthIL(f)_{i,j,N} \quad (36)$$

where $CoupledlengthIL(f)_{i,j,N}$ is determined as the minimum of the insertion loss of the disturbed pair N and the disturbing individual pair i (1 to n) of the disturbing link j (1 to m).

For calculating PSAELFEXT of one victim, the differential insertion loss, S_{ijdd}, parameter between all aggressor pairs and the victim pair in the link segments should be measured at the far-end.

3.3. MEASUREMENT PROCEDURE AND TESTING EUTS

In order to calculate PSANEXT for a 5-around-1 UTP configuration, (33) can be re-written as (37). This rewrite is possible because the number of duplex channels in the link segment equals to one ($m = 1$) and number of aggressor link segments, for pair 1 victim, is $n = 5$.

$$PSANEXT_1(f) = 10\log_{10}\sum_{i=1}^{5} 10^{\frac{-AN(f)i,1}{10}} \quad (37)$$

In the same way for PSAELFEXT, (34) will be changed to (38).

$$PSAELFEXT_1(f) = 10\log_{10}\sum_{i=1}^{5} 10^{\frac{-EL(f)i,1}{10}} \quad (38)$$

Equation (35) for Equal Level (EL) calculation will be simplified to (39) because lengths of all the pairs are the same (15 m).

$$EL(f)_{i,1} \approx AELFEXT(f)_{i,1} \tag{39}$$

Thus the insertion loss for each pair is nearly equal, which results on the $10\log_{10}$ ratio of insertion loss to be equal to 0. This simplification is described in Figure 3.3.

Two 5-around-1 cable bundles with Leoni Dacar 546 and 545 UTPs, with and without inline Circular Plastic Connector (CPC) are tested for meeting PSANEXT and PSAELFEXT standard requirements.

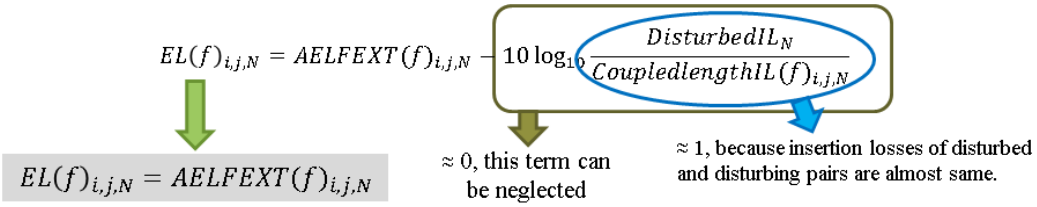


Figure 3.3. Simplification of Equal Level calculation

3.3.1. Alien Crosstalk for 5-around-1 Cable Bundle. Two EUTs were constructed for Leoni Dacar 546 and 545 UTPs bundle as shown in Figure 3.4 and Figure 3.5, respectively. Two 15m, 5-around-1 cable bundles are wound around the hollow cylindrical ground structures. Cable spacing varied between 6 mm to 9 mm. A 1 mm thick foam material was used all around the ground structure to maintain a uniform spacing of the cables over the ground structure as shown on Figure 3.6 a. Each wire was loaded with a single-ended 50 ohm SMA termination. Wire to SMA adapter PCB with 50 ohm microstrip traces were placed at the end of the bundles. PCB ground plane was connected to the global cylindrical reference structure with 90 degree aluminum angle brackets as shown in Figure 3.6 b.

Six UTPs create a 24 single-ended and/or 12 mixed mode port network system as presented in Figure 3.7. It is expected that the middle pair in the bundle will have the highest level of alien crosstalk, because power from all 5 aggressors are coupled from all directions with the smallest separation distance [16]. Thus, in the test application, the middle pair is assumed as a victim and the 5 pairs around it as aggressors.

Port 1 is an observation point for detecting coupling from other ports. ANEXT is defined between victim port 1 and aggressor ports 2, 3, 4, 5 and 6 at the near end. ANEXT is differential pair to pair coupling S_{ijdd} in dB, where $i = 1$ and $j = 2, 3, 4, 5$ and 6. Meanwhile, AFEXT exists between victim port 1 and aggressor ports 8, 9, 10, 11 and 12. AFEXT is differential pair to pair coupling S_{ijdd} in dB, where $i = 1$ and $j = 8, 9, 10,$ 11 and 12. Insertion loss between port 1 and port 7 is $CoupledlengthIL(f)_{i,j,N}$ from (36).

Figure 3.4. Measurement setup for Leoni Dacar 546 cable bundle

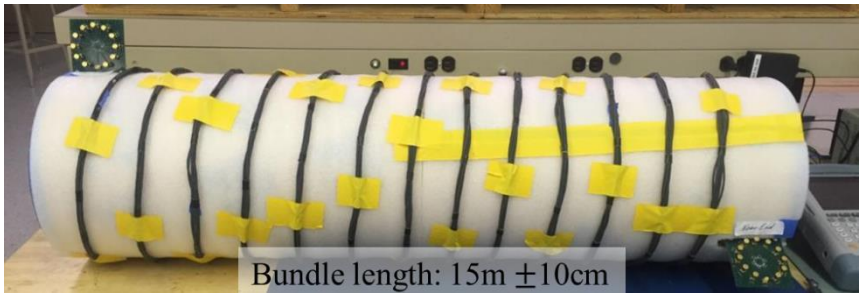
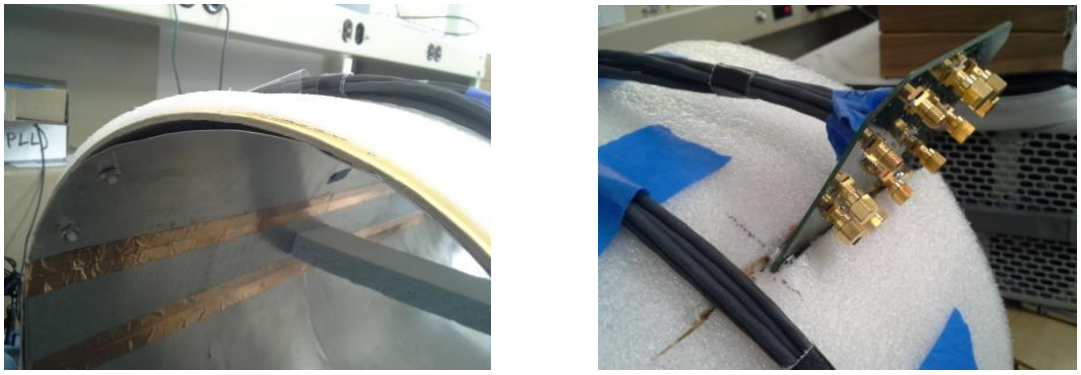


Figure 3.5. Measurement setup for Leoni Dacar 545 cable bundle



a) b)

Figure 3.6. a) A 1 mm thick foam material is placed between the cables and the ground structure, b) Wire to SMA adapter PCB with single-ended 50 ohm SMA terminations

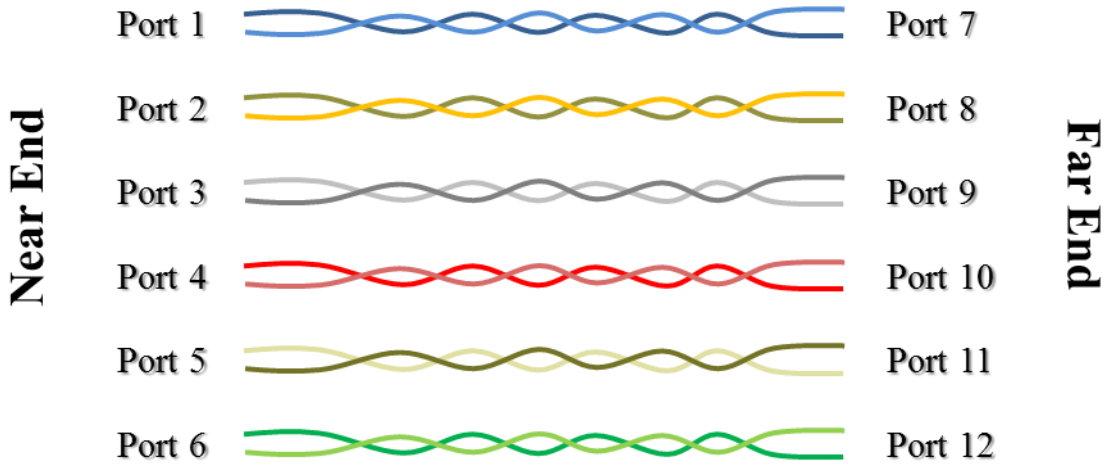
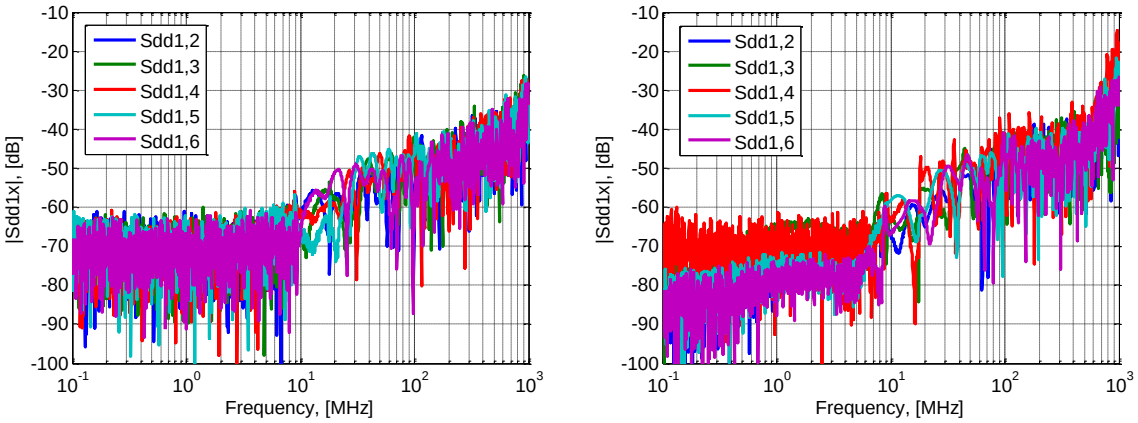


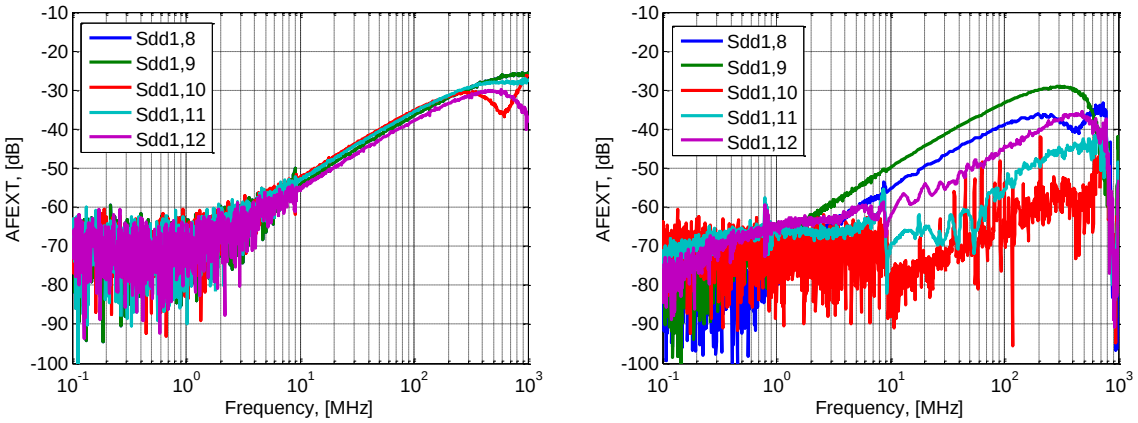
Figure 3.7. A 24 Single-ended and 12 mixed mode network system

Measured ANEXT at the near end and AFEXT at the far end for Leoni Dacar 546 and 545 cable bundles are shown in Figure 3.8 and Figure 3.9, respectively. Insertion loss for pair 1 is shown in Figure 3.10. For the differential S parameter measurement a Vector Network Analyzer was used with the settings as listed in Table 3.1.



a) b)

Figure 3.8. ANEXT for a) Leoni Dacar 546; b) Leoni Dacar 545 cable bundle

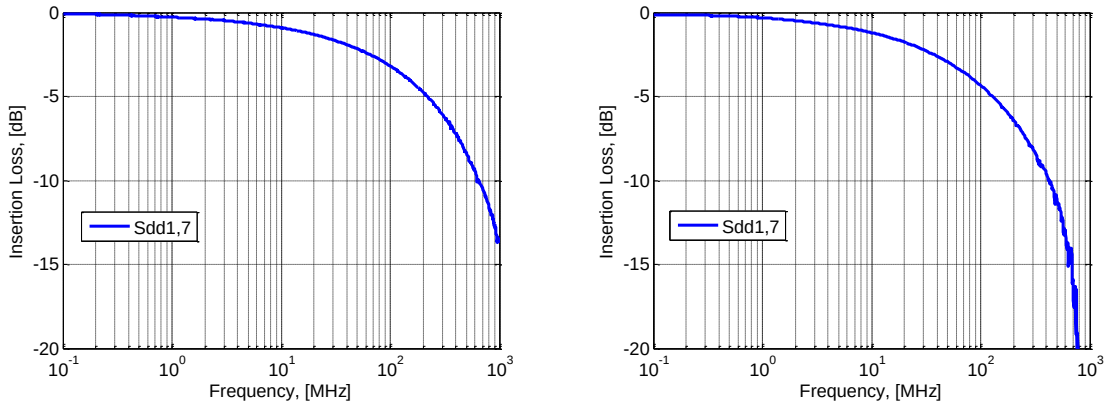


a) b)

Figure 3.9. AFEXT for a) Leoni Dacar 546; b) Leoni Dacar 545 cable bundle

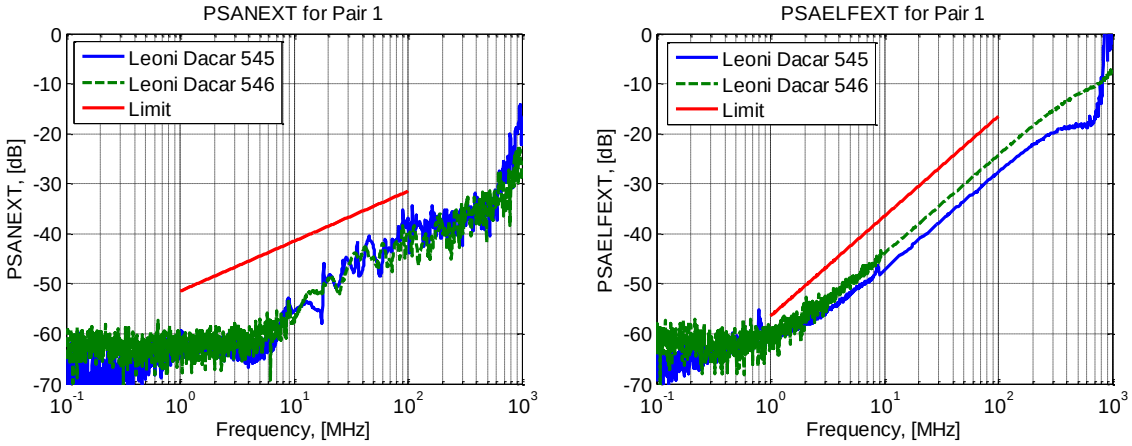
Using (37) PSANEXT for victim pair 1 can be calculated from measured ANEXTs. The two cable bundle results are compared in Figure 3.11 a. Both cable bundle pass the standard limitation, defined using (31), with 8 dB margin at 100 MHz. PSAELFEXT is calculated based on measured AFEXT and victim pair insertion loss according to (38). In Figure 3.11 b both Leoni cable bundle PSAELFEXT results are

compared. Dacar 546 and 545 cables pass the PSAELFEXT standard requirements with 8 dB and 10 dB margins at 100 MHz, respectively.



a) b)

Figure 3.10. Insertion loss for a) Leoni Dacar 546; b) Leoni Dacar 545 cable bundle



a) b)

Figure 3.11. a) PSANEXT and b) PSAELFEXT for Leoni Dacar 546 and 545 compared to standard limit over frequency range

Table 3.1. Vector Network Analyzer settings

Parameter	Value
f_{start}	100KHz
f_{stop}	1GHz
Sweep type	Logarithmic
Sweep points	1601
Output power	-10dBm
IF bandwidth	70 KHz
Data calibration kit	Mechanical calibration kit
Averaging function	Deactivated
Smoothing function	Deactivated

3.3.2. Alien Crosstalk for 5-around-1 Cable Bundle with Inline Connector. A physical layer is defined according to Figure 3.12 in the standard [15]. Two equally spaced inline connectors connect the 5 m cable bundle pieces. Link segment including inline connectors should meet standard limits as defined in (31) and (32). Circular Plastic Connectors (CPC) are widely used in automotive applications for low frequencies. Here, CPC suitability for BroadR-Reach® protocol is tested at higher frequency ranges. For placing twisted wire pairs inside the connector, the UTPs are untwisted and placed as parallel single wires. The untwisted region in the UTP results in differential to common mode conversion and signal degradation. Effect of the untwisted region may prevent meeting the standard limits.

Generally the CPC length is about 5 cm, thus at least a 5 cm untwisted segment is added to the cable bundle. Most often, wire placement in the CPC is manual, which results in an additional 1 cm untwisted region at both female and male sides. This makes the total untwisted region length at least 7 cm as shown in Figure 3.13 a. In real applications the CPC is placed inside an outer socket, which encases all the untwisted parallel wires. Approximately an 10 cm untwisted region is added on both sides of the

CPC, which makes the total untwisted length nearly 25 cm as shown in Figure 3.13 b. Considering the minimum and maximum untwisted regions, the CPC was added in the middle of the Leoni Dacar 546 cable bundle as shown in Figure 3.14 and Figure 3.15, respectively.

PSANEXT and PSAELFEXT measurements are performed in the same way as described in section 3.3.1. ANEXT, AFEXT and victim insertion loss for 7 cm and 25 cm untwisted segments are shown in Figure 3.16, Figure 3.17 and Figure 3.18, respectively.

Based on the ANEXT and AFEXT measurements, power sum alien crosstalk were calculated for minimum and maximum untwisted lengths for the Leoni Dacar 546 UTPs cable bundle. As shown in Figure 3.19, the CPC connector passes PSAELFEXT requirements with a maximum untwisted segment of 25 cm whereas it fails PSANEXT limits.

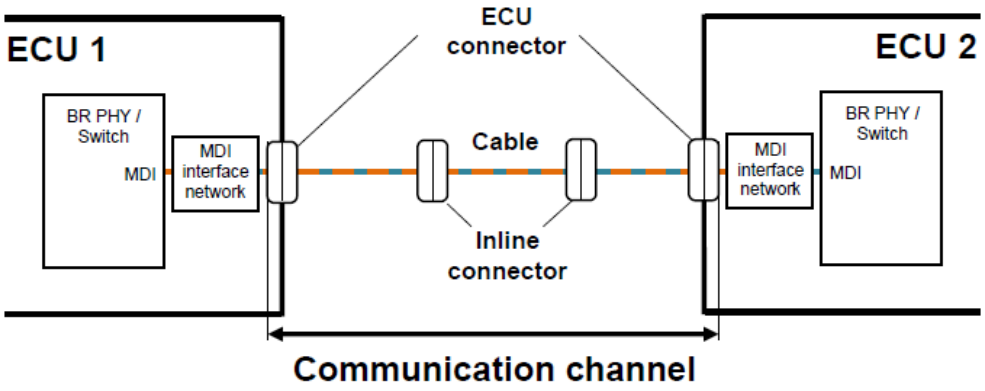
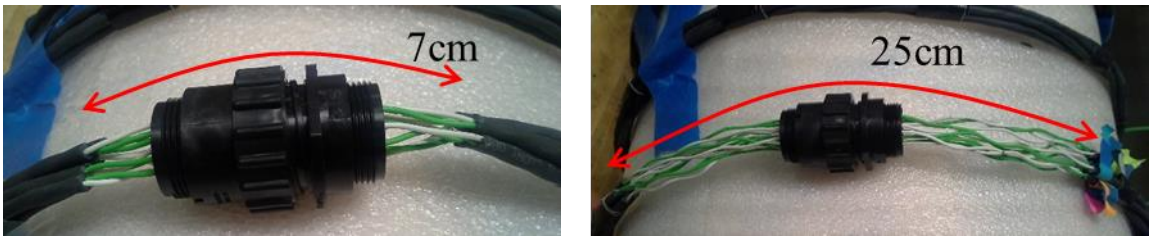


Figure 3.12. BroadR-Reach® link segment definition

Alien crosstalk analysis shows that the untwisted region in the bundle has significant undesirable effects on the coupling. Reducing the length of this untwisted segment is necessary, which cannot be achieved with the CPC connector plus socket configuration in BroadR-Reach® protocol.

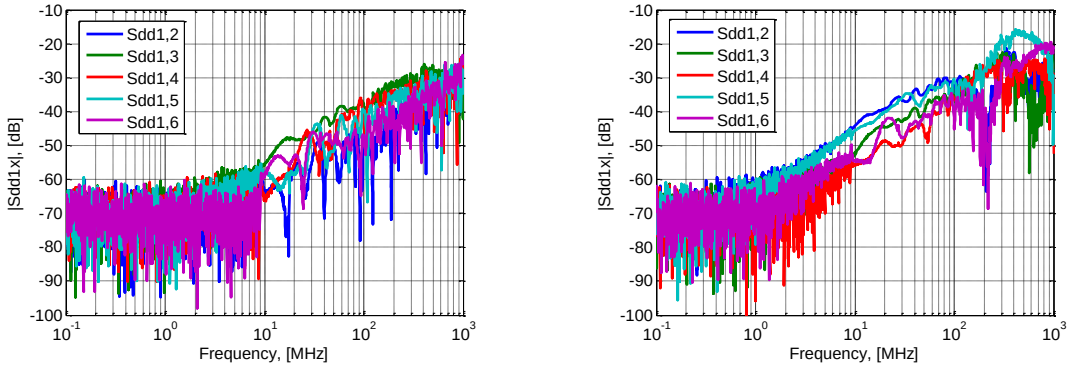


a) b)

Figure 3.13. Due to CPC configuration a) minimum 7 cm and b) maximum 25 cm untwisted segment is added in the bundle

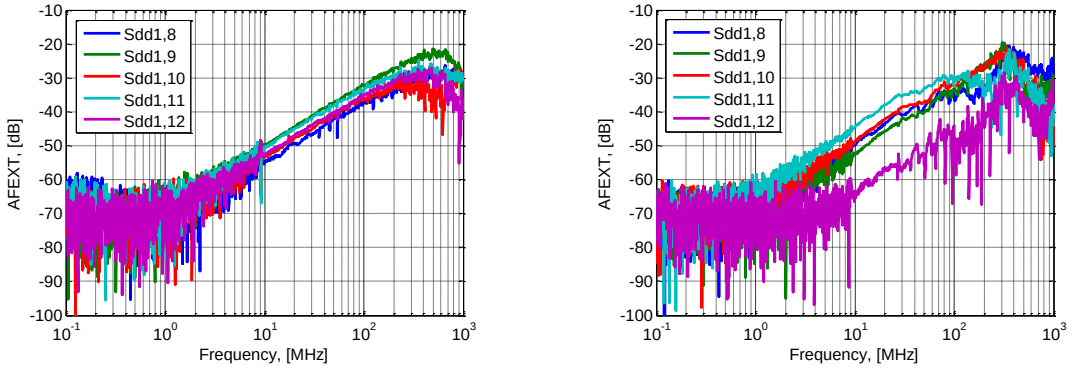
Figure 3.14. Measurement setup for Leoni Dacar 546 cable bundle with an inline CPC with minimum 7 cm untwisted segment

Figure 3.15. Measurement setup for Leoni Dacar 546 cable bundle with an inline CPC with maximum 25 cm untwisted segment



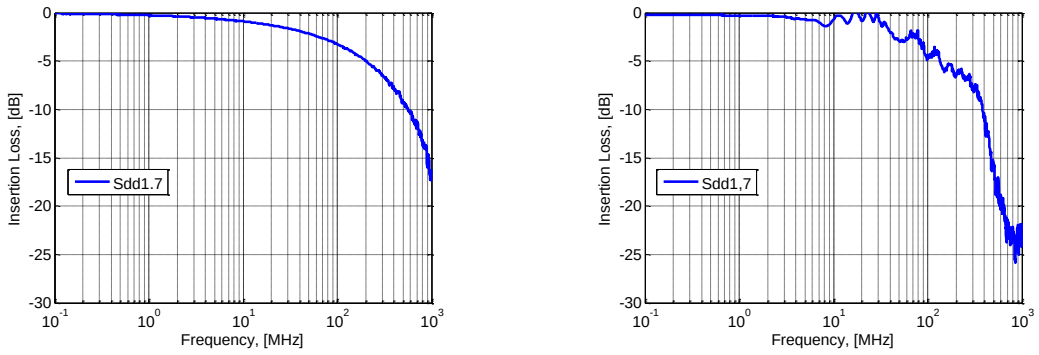
a) b)

Figure 3.16. ANEXT for a) 7 mm; b) 25 mm untwisted region



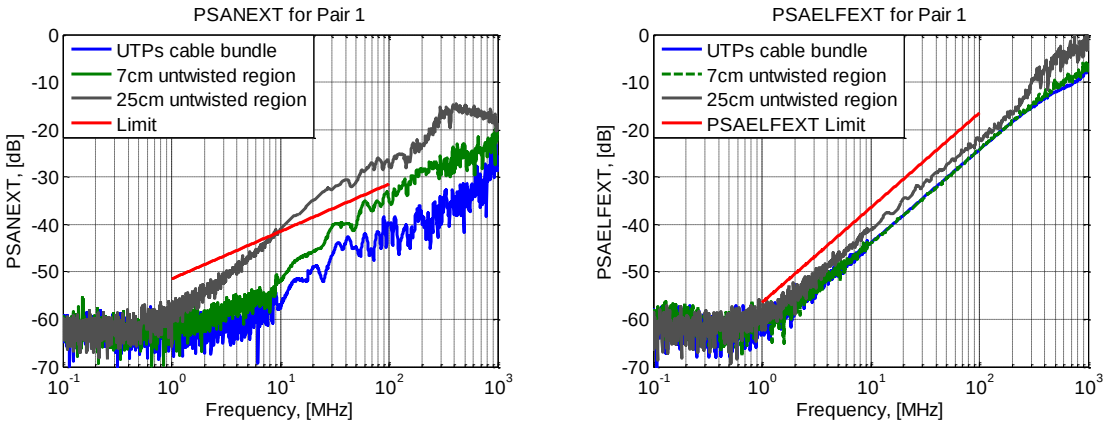
a) b)

Figure 3.17. AFEXT for a) 7 mm; b) 25 mm untwisted region



a) b)

Figure 3.18. Insertion loss for a) 7 mm; b) 25 mm untwisted region



a) b)

Figure 3.19. a) PSANEXT and b) PSAELFEXT for Leoni Dacar 546 with CPC is compared to the standard limit

3.3.3. Effect of an Inline Connector on Alien Crosstalk. The test setup shown in Figure 3.20 was built in order to determine the effect of the untwisted region of the cable around the connector. The setup uses a 36 cm long Leoni Dacar 546 UTPs cable bundle and is tested with and without the CPC connector for different untwisted lengths as shown in Figure 3.21. In Figure 3.22 a and b PSANEXT and PSAELFEXT for the untwisted regions are compared.

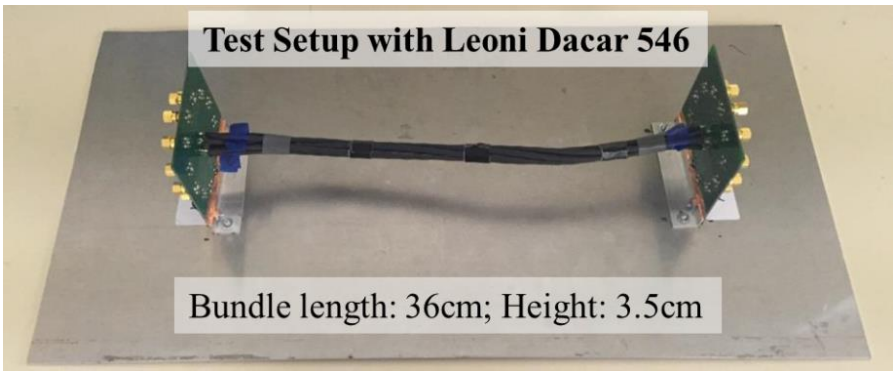
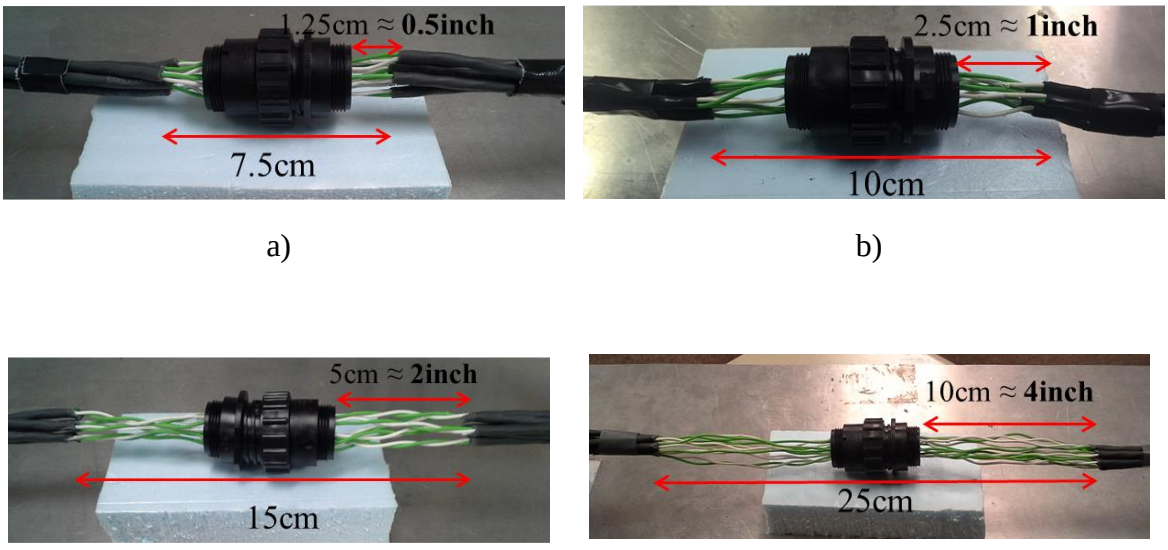


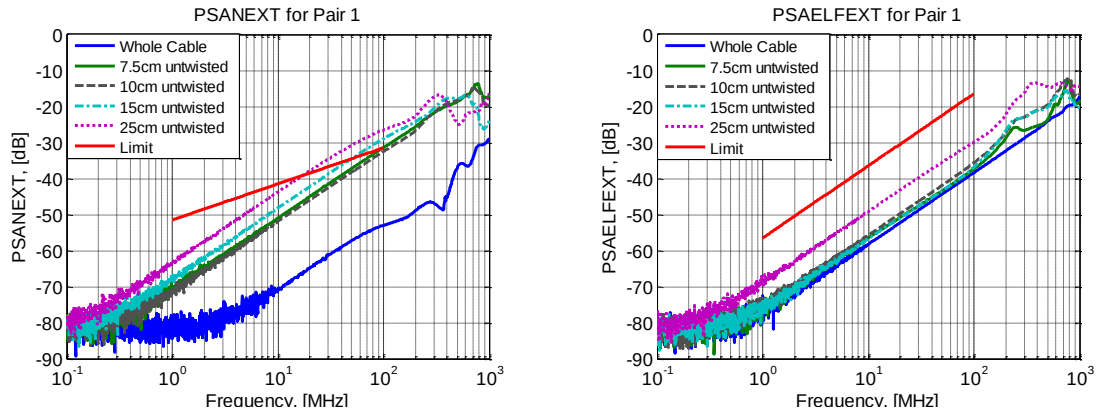
Figure 3.20. Test setup with twisted UTPs



a) b)

c) d)

Figure 3.21. CPC connector with a) 7.5 cm; b) 10 cm; c) 15 cm and d) 25 cm unshielded regions

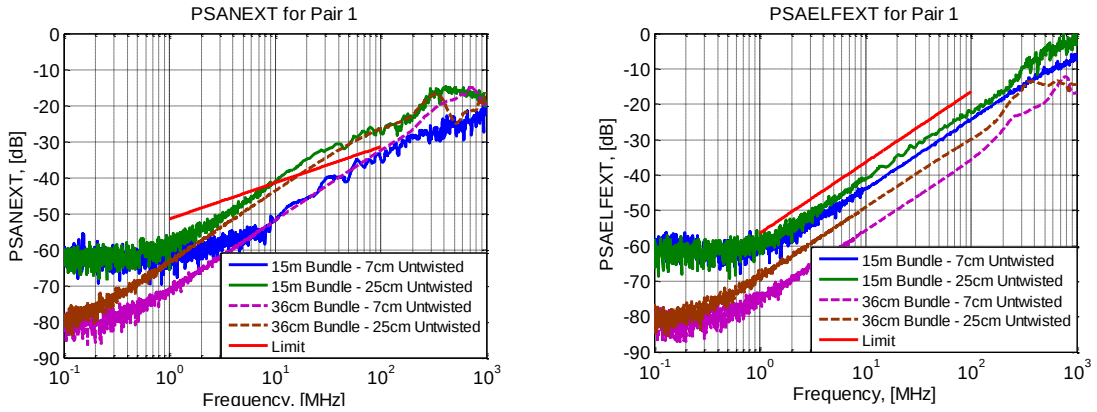


a) b)

Figure 3.22. a) PSANEXT and b) PSAELFEXT for test setup with different lengths of untwisted regions

Based on measurement results shown in Figure 3.22 a, the power sum at the victim pair increases by over 20 dB with a 7 cm untwisted length compared to a cable bundle with no untwisted length. A 10 dB change is observed in the far-end, by increasing the untwisted segment length from zero to 25 cm.

PSANEXT and PSAELFEXT for a 15 m Leoni Dacar 546 cable bundle tested in 3.3.2 is compared to the test setup in Figure 3.23 a and b respectively. PSANEXT is dominated by the untwisted length and is independent of the total cable length. At the near-end, there is no significant effect of the twisted pair. At the far end, the power sum ELFEXT increases gradually by increasing the length of the untwisted region. This can be attributed to the combined effect of inductive and capacitive coupling at the near and far end.



a) b)

Figure 3.23. a) PSANEXT and b) PSAELFEXT for test setup comparing two cable lengths – 15 m and 36 cm having two untwisted lengths – 7 cm and 25 cm

3.4. CONCLUSION

Power sum alien near-end and equal level far-end crosstalk measurement procedure has been described. Power sum alien crosstalk was characterized at the near and far end for a Leoni Dacar 546 and 545 having 6 UTPs bundled as a cable. As far as both cables are well twisted, coupling between them is low, thus standard limits are met. PSAELFEXT of Leoni Dacar 545 is 2 dB lower than for Dacar 546 cable bundle. However, this variation is caused by statistical cable bundle alignment.

Effect of the untwisted region length in the cable bundle was analyzed. As expected, an untwisted region increases the coupling between the bundles. According to

measurement results, an inline connector in the middle of a 15 m 6 UTP cable bundle with a 25 cm long untwisted region fails the PSANEXT standard limitation by 4 dB at 100 MHz, while the same bundle without it passes the standard by a margin of 8 dB at 100 MHz. Base on the measurement result analysis, the total untwisted region length should not exceed 7 mm for meeting standard limits. Thus a CPC connector cannot be used for Broad-Reach® protocol applications.

In a future study, approximate equivalent circuit models for capacitive and inductive coupling should be developed for near-end and far-end crosstalk analysis. Approximate statistical description for crosstalk as a function of connector length should be developed. Study of other types of connector (other than CPC) and their effects on alien crosstalk in a communication channel is necessary.

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VITA

Tamar Makharashvili was born in Gori, Georgia on January 6, 1991. She received her Bachelor's degree (with highest honors) in Electrical and Electronics Engineering from Tbilisi State University, Tbilisi, Georgia in 2013. She completed her M.S. degree in electrical engineering at Missouri University of Science and Technology, Rolla, MO, USA in December 2015.

She was working in EMCoS, Ltd. from 2011 to 2013, in the support group related to numerical solutions of electromagnetic compatibility problems.

She was a Graduate Research Assistant in the Electromagnetic Compatibility Laboratory at Missouri University of Science and Technology from 2014 to 2015. Her research areas included numerical electromagnetic analysis and electromagnetic compatibility in power electronic systems.